ESE370: Circuit-Level Modeling, Design, and Optimization for Digital Systems

Lec 26: November 10, 2021

Dynamic Logic Pt 2, Memory Overview

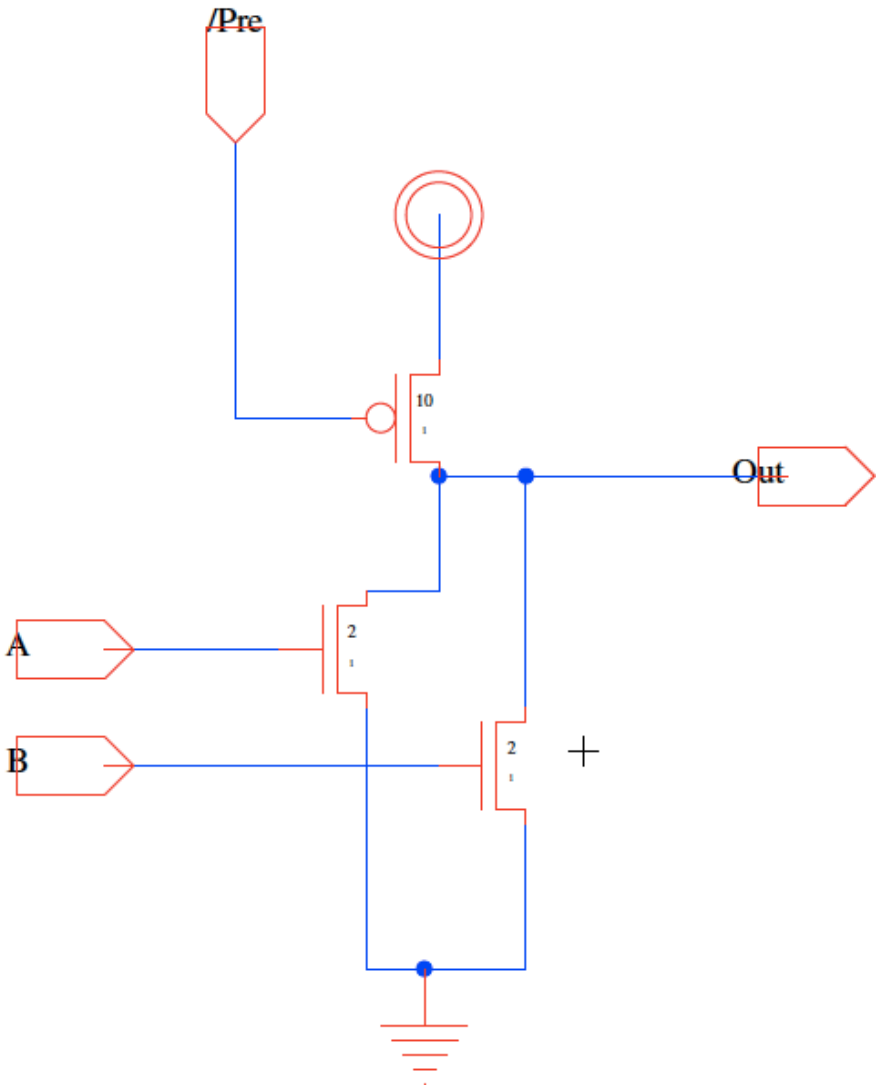
Today

- Dynamic (Clocked) Logic
  - Domino Logic
  - Compare CMOS
- Memory Overview

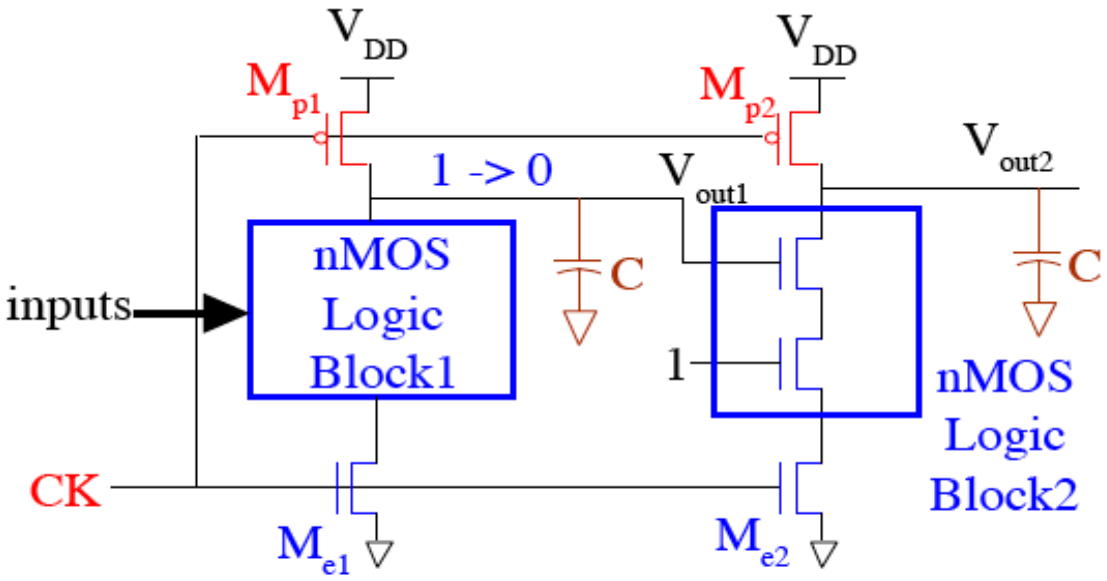
Dynamic Logic

Idea

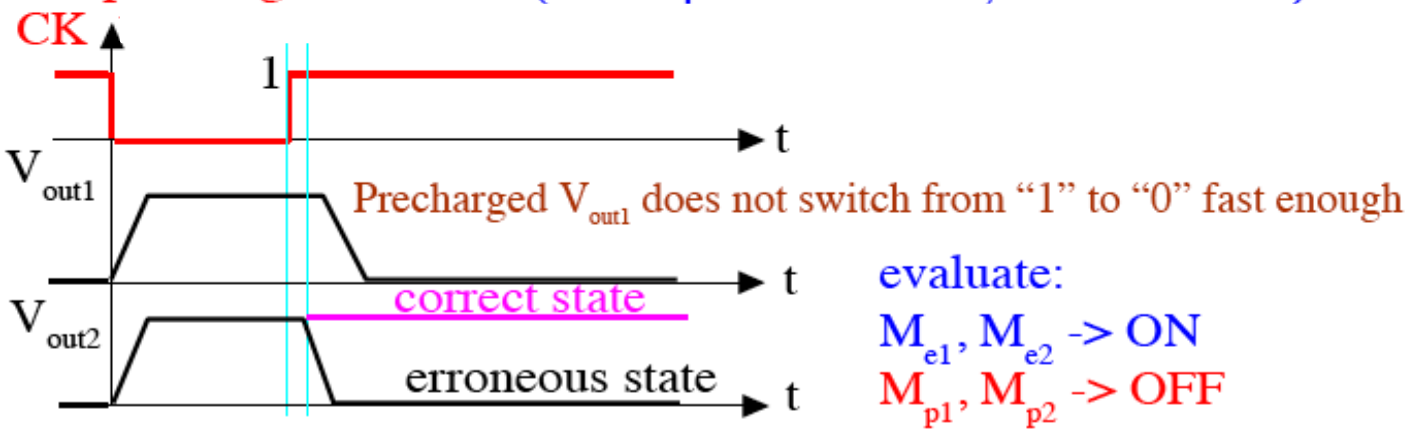
- Use clock to disable pullup network during logic evaluation
- Define two phases
  - Pre-charge
    - Output pre-charged
  - Evaluation
    - Pulldown network evaluates gate logic



Cascaded Dynamic Logic

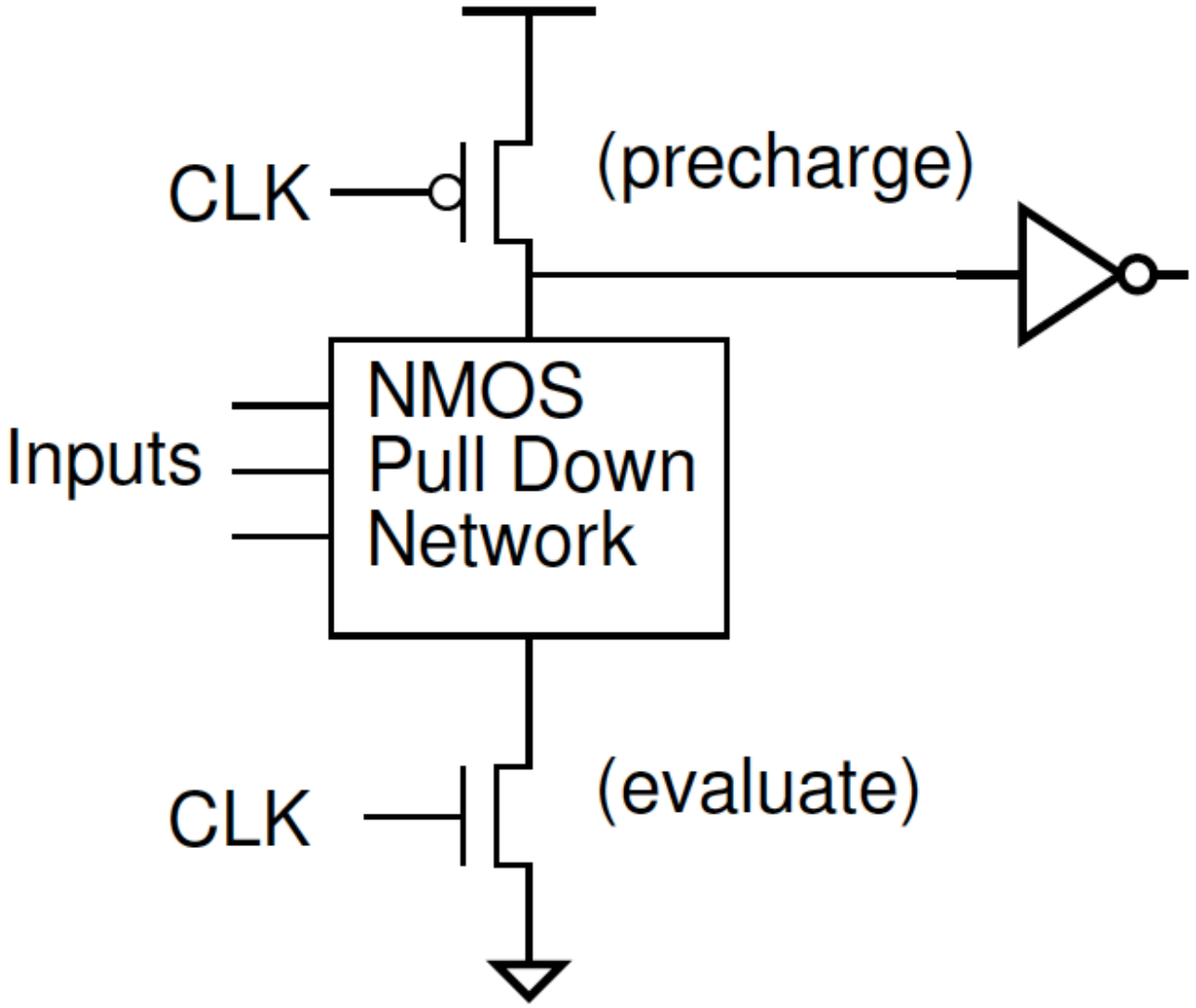


precharge evaluate (all outputs selectively switch 1 -> 0)



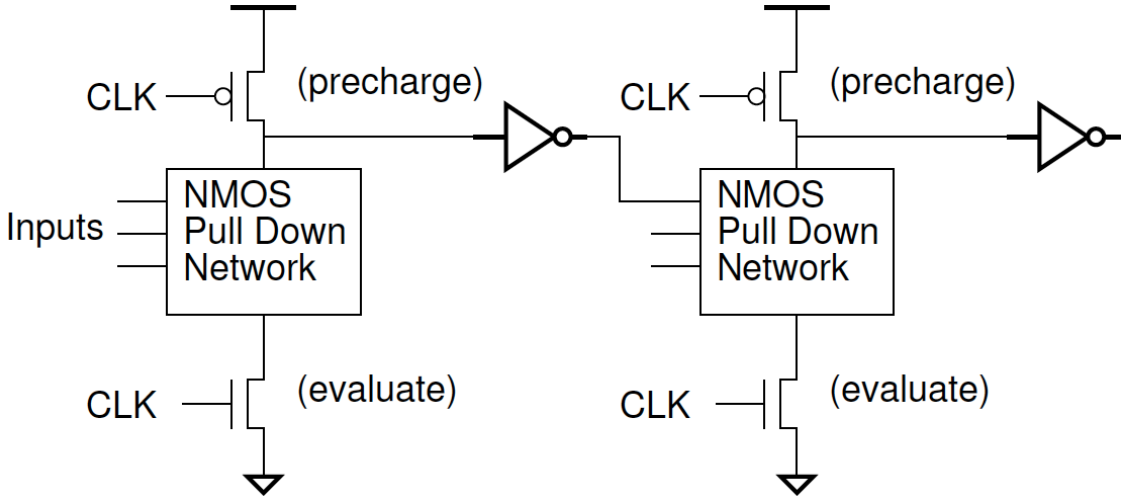
PROBLEM: ALL STAGES MUST EVALUATE SIMULTANEOUSLY
SINGLE CLOCK DOES NOT PERMIT PIPELINING OF STAGES

Domino Logic

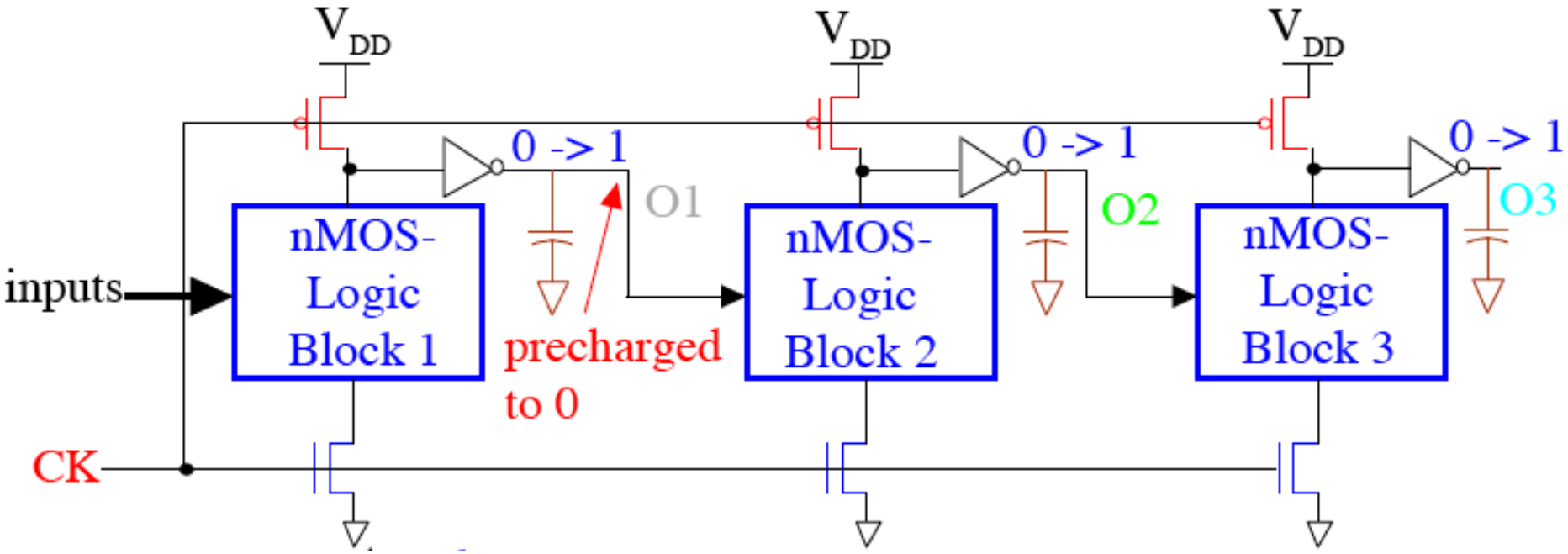


Requirements

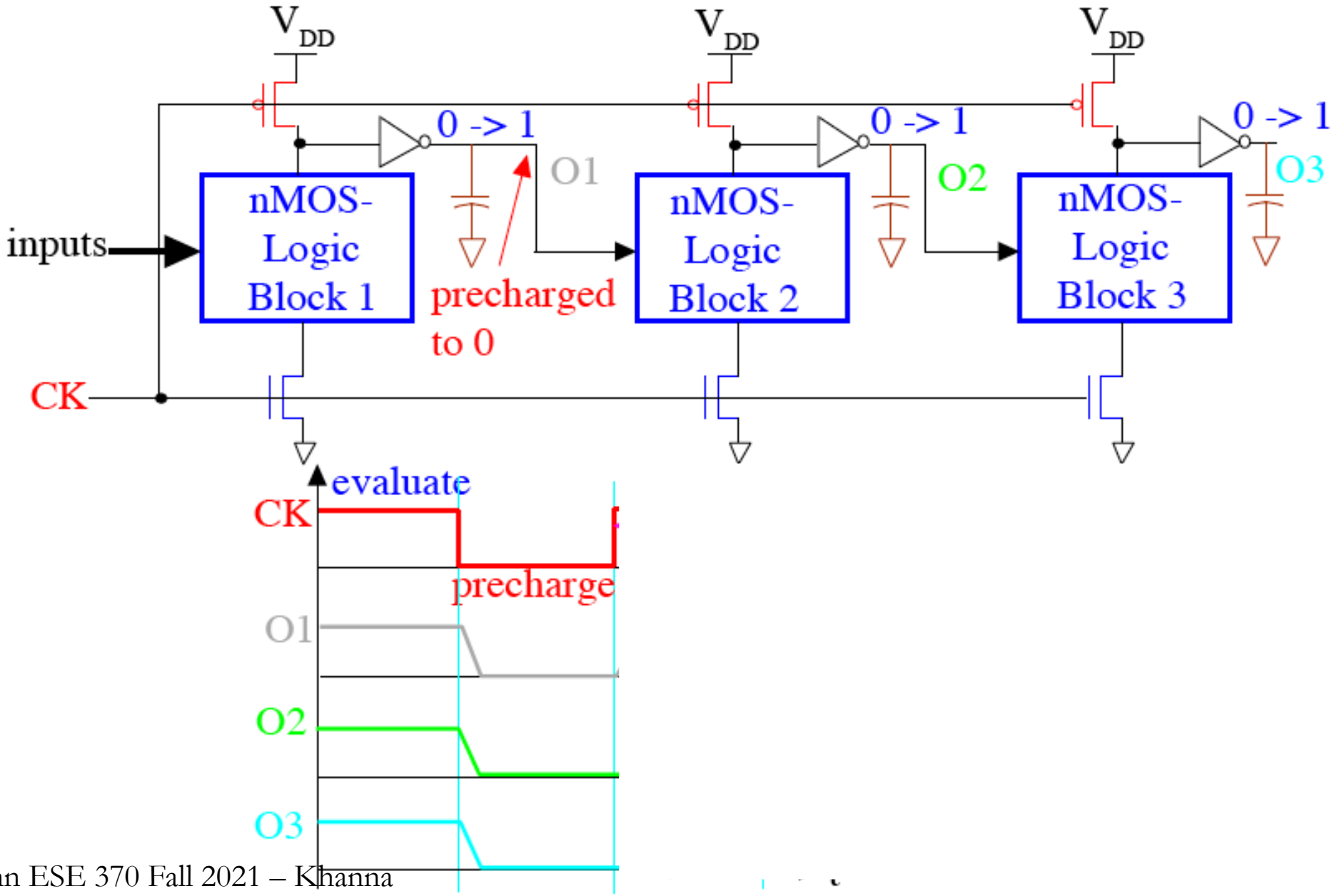
- Single transition
  - Once transitioned, it is done → like domino falling
- All inputs at 0 during precharge
  - "Outputs" pre-charged to 1 then inverted to 0
- Non-inverting gates fundamental gate



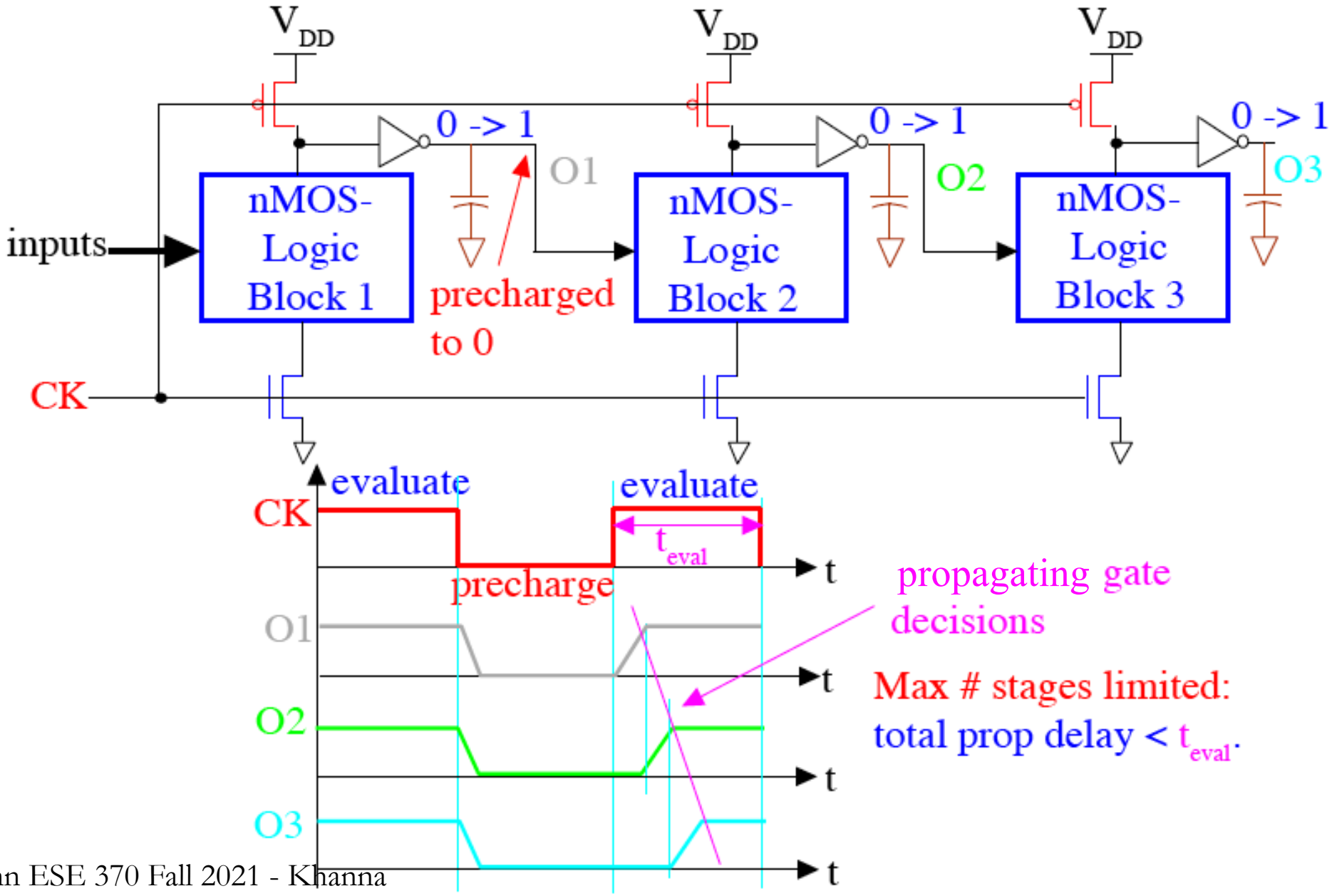
Cascaded Domino CMOS Logic Gates



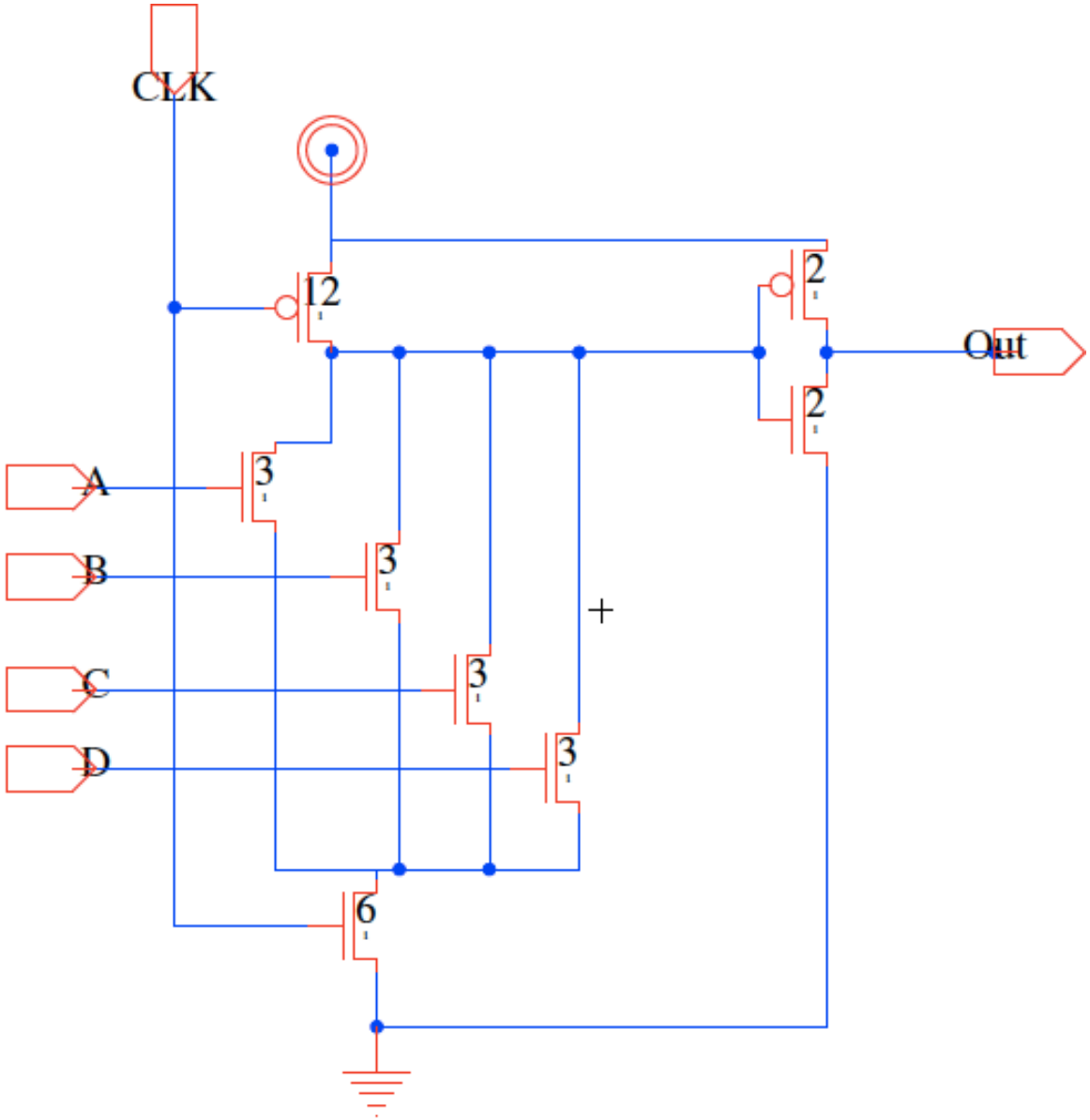
Cascaded Domino CMOS Logic Gates



Cascaded Domino CMOS Logic Gates

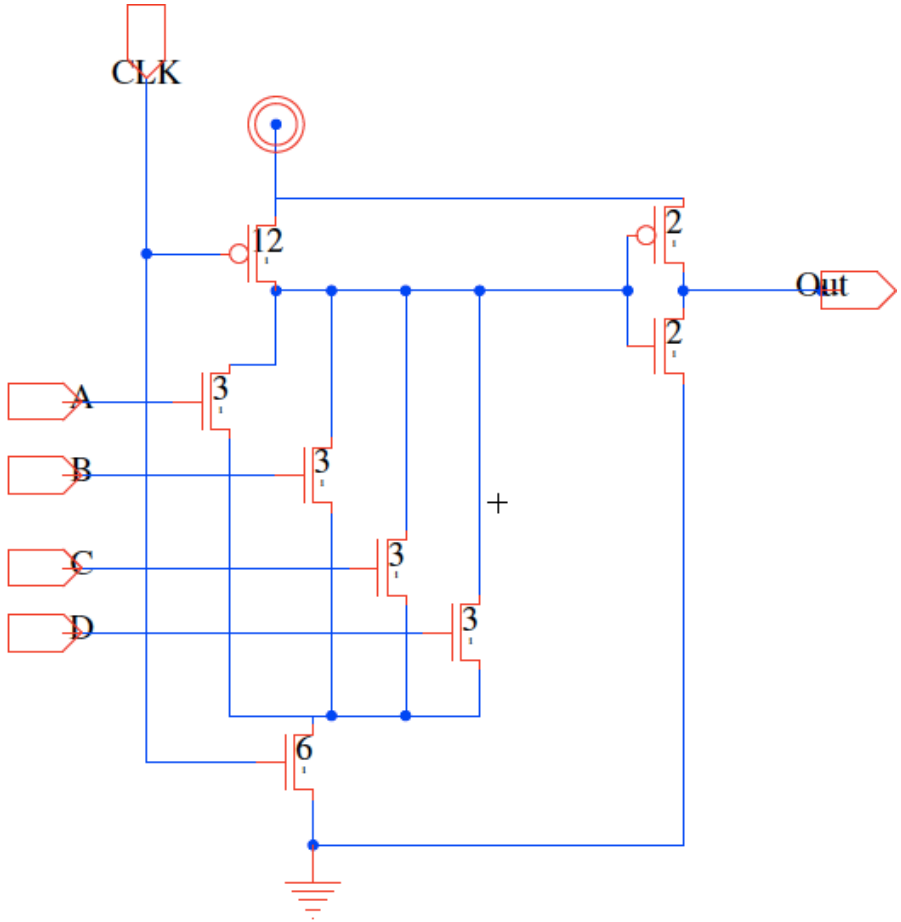


Domino or4 (Preclass 3)



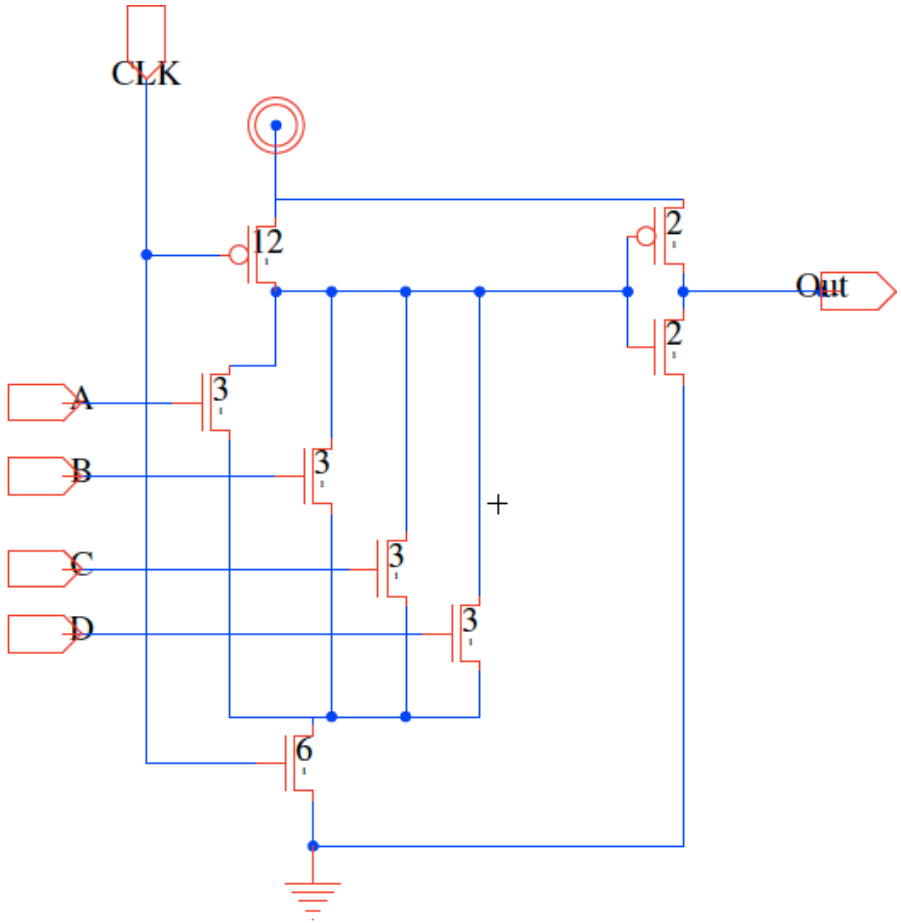
Domino Logic (Preclass 3)

- Performance
  - $R_0/2$ input
- Compare to CMOS cases?
  - nor4
  - or4
  - nand4



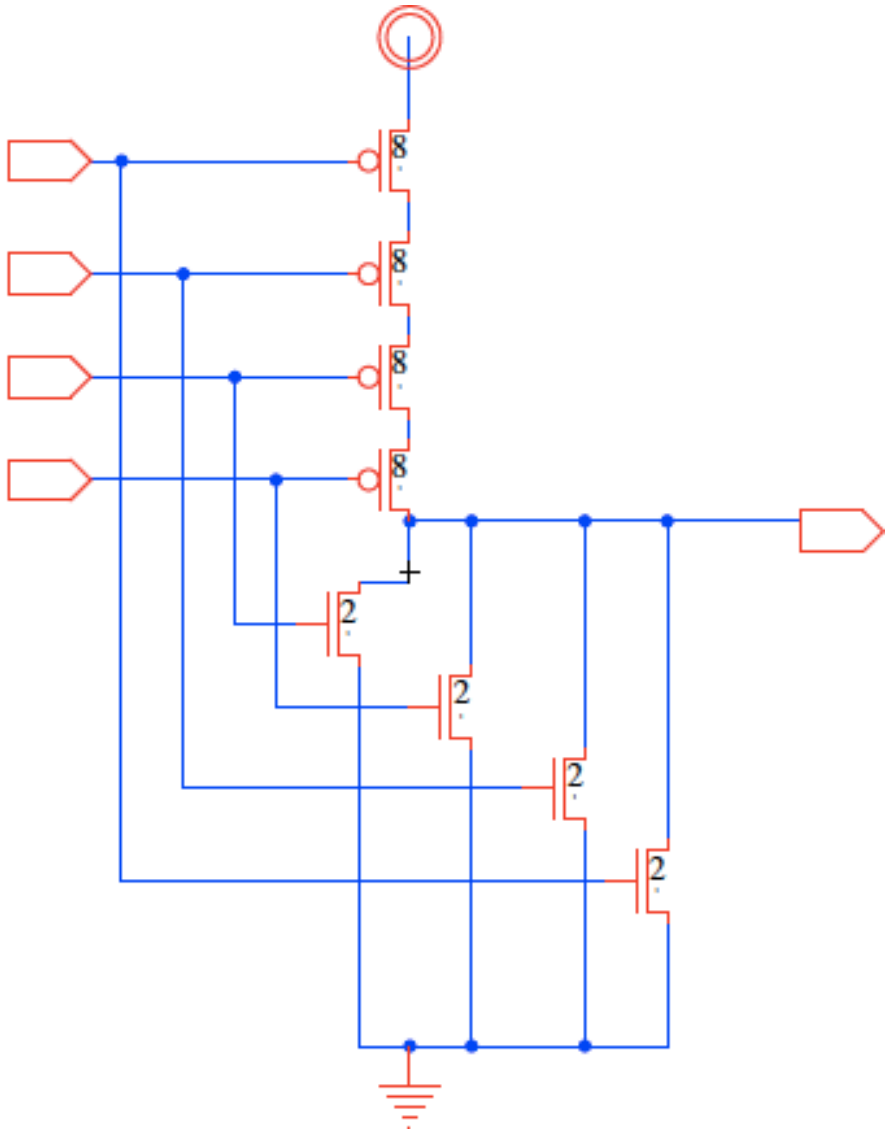
Dynamic OR4 (Preclass 3)

- Precharge time?
- Driving input
  - With $R_0/2$ inverter
- Driving inverter?
- Self output Delay?



CMOS NOR4 (Preclass 3)

- Driving input
  - With $R_0/2$ inverter
- Self output Delay?



Dynamic Logic Issues

- Noise sensitive
  - During evaluation phase, when output is high it's floating and therefore more susceptible to noise
- Power
  - Eliminates static current
  - Higher activity factor—always a 0→1 transition, large pre-charge device dissipates extra switching power

Observe

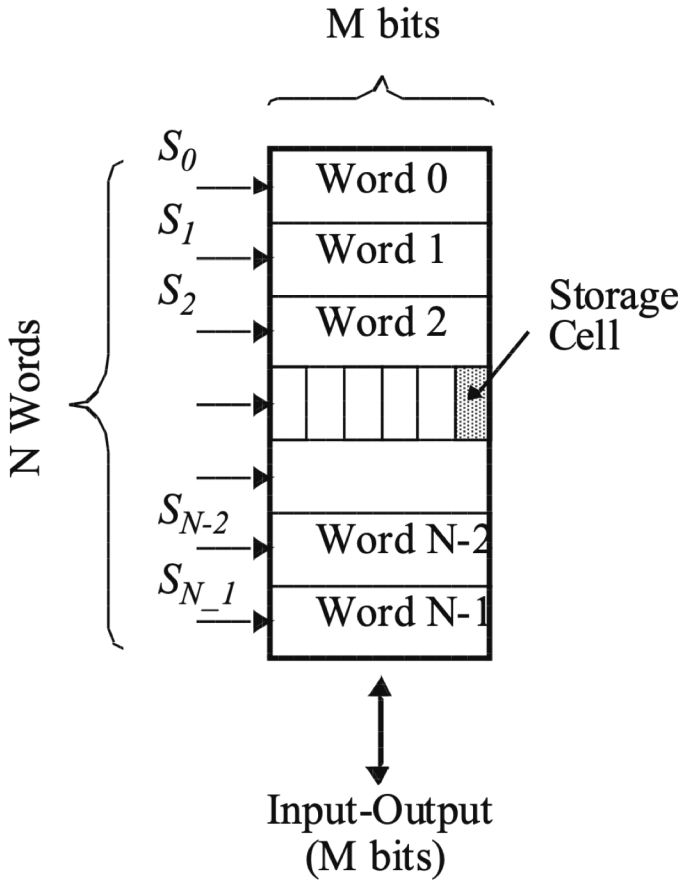
- Better (lower) ratio of input capacitance to drive strength
- Particularly good for
  - Driving large loads
  - Large fanin gates
- Harder to design with
  - Timing and polarity restrictions
  - Avoiding noise
    - Especially with today's high variation tech
- Can consume more energy

Memory Overview

Semiconductor Memory Classification

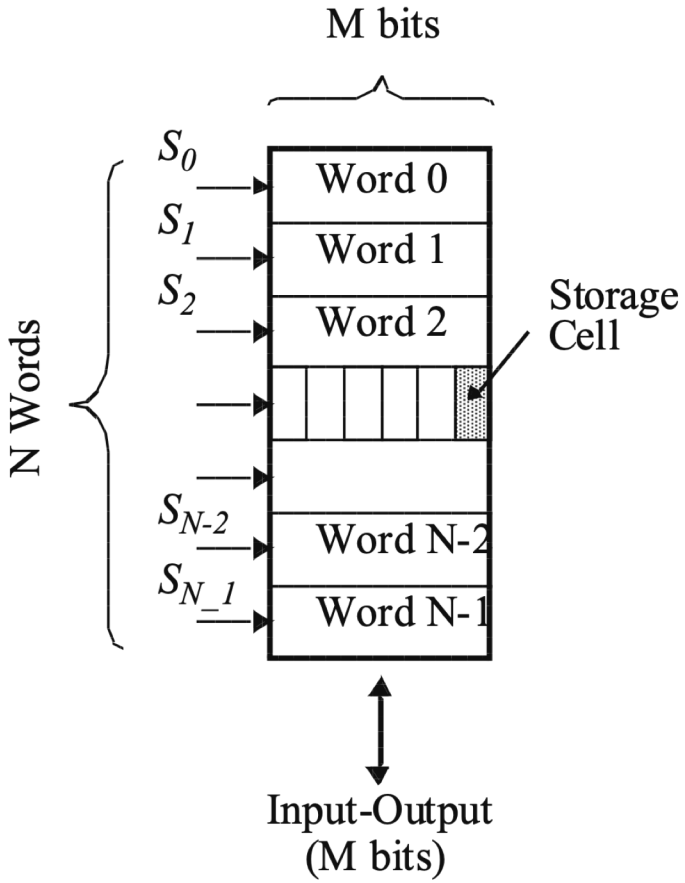
RWM		NVRWM	ROM
Random Access	**Non-Random Access**	EPROM E^2PROM FLASH	Mask-Programmed Programmable (PROM)
SRAM DRAM	FIFO LIFO Shift Register CAM		

Memory Architecture: Core



N words => N select signals
Too many select signals

Memory Architecture: Decoders



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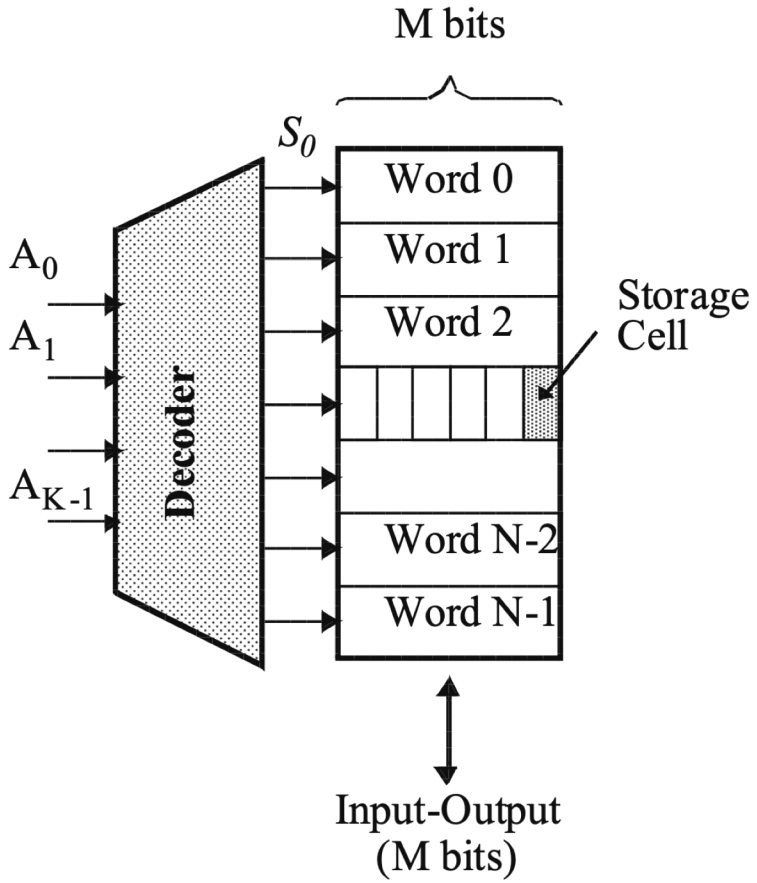
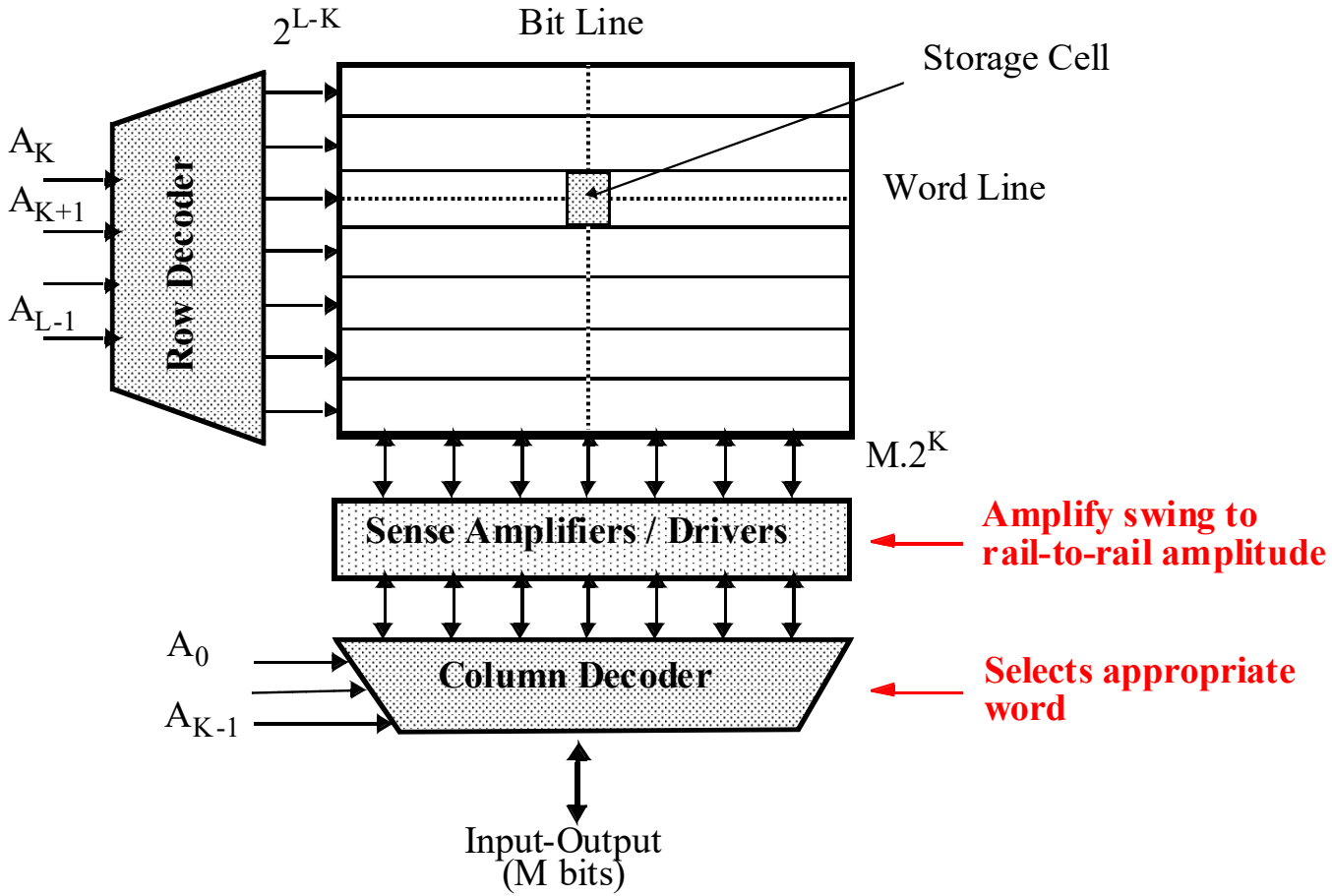


Decoder reduces # of select signals
$K = log_2 N$

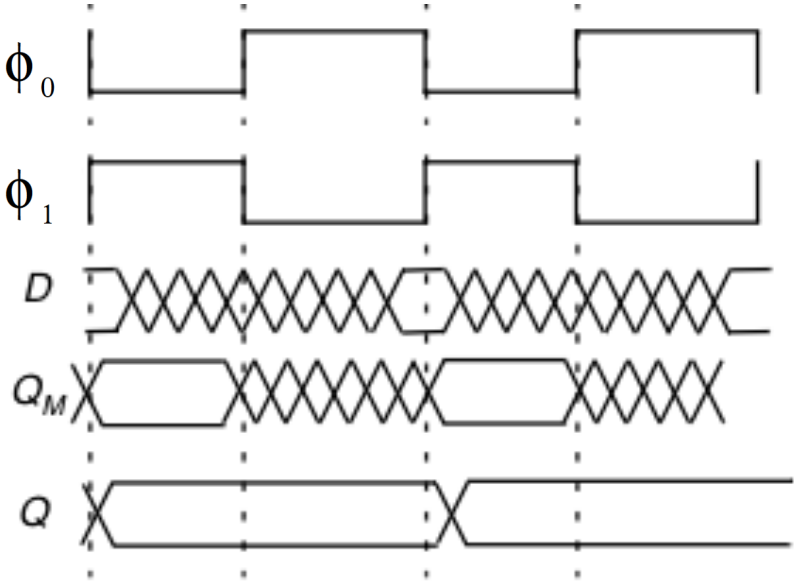
Array-Structured Memory Architecture

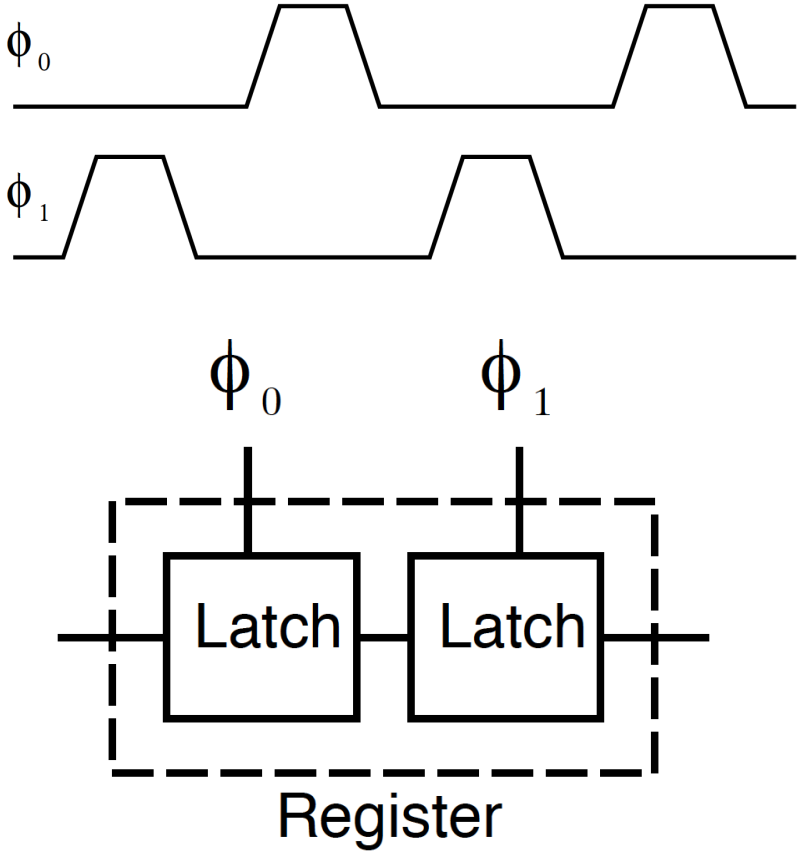
Problem: ASPECT RATIO or HEIGHT >> WIDTH



Latches/Register – Can Store a State

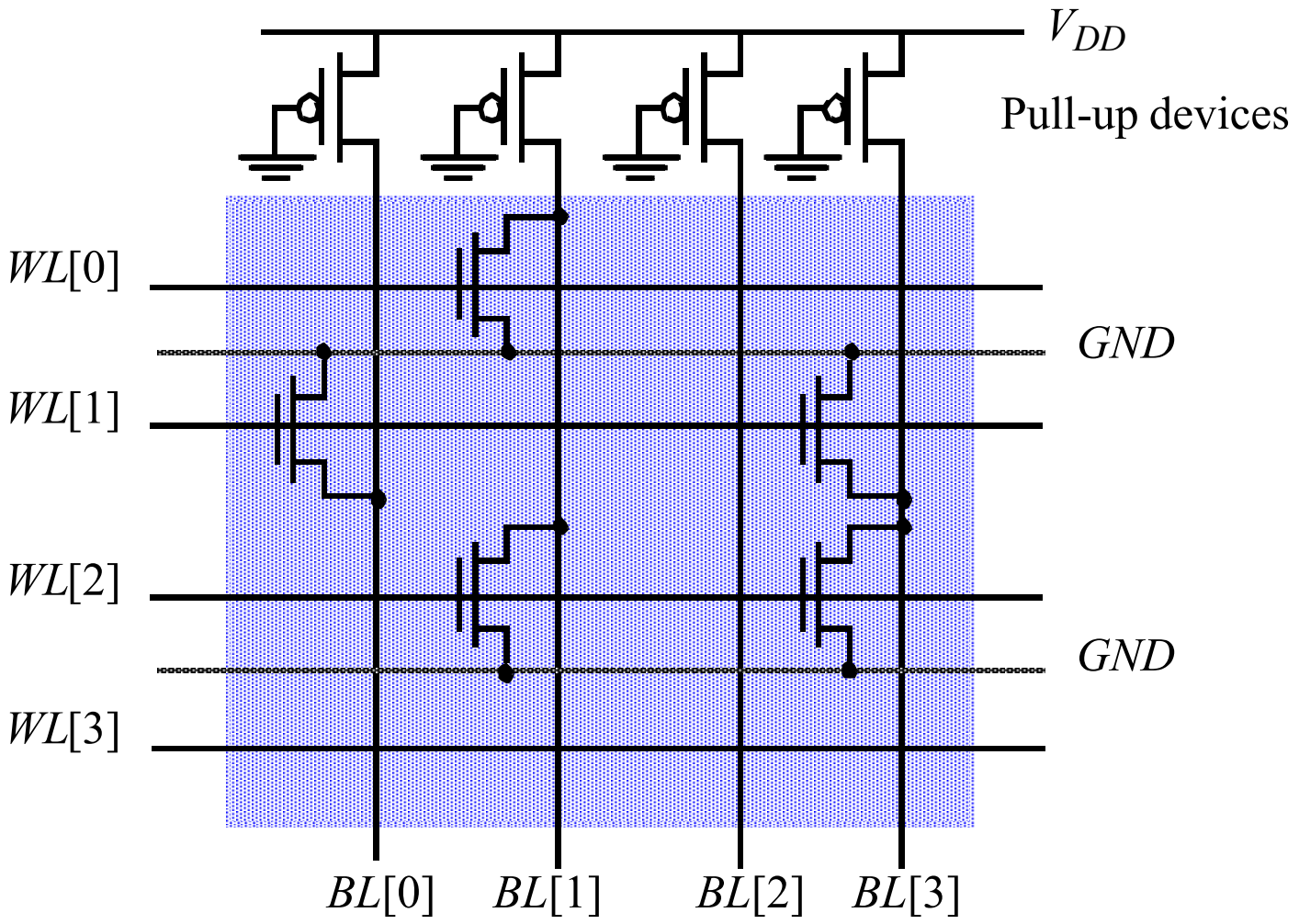
- Build register from pair of latches
- Control with non-overlapping clocks





ROM Memories

MOS NOR ROM



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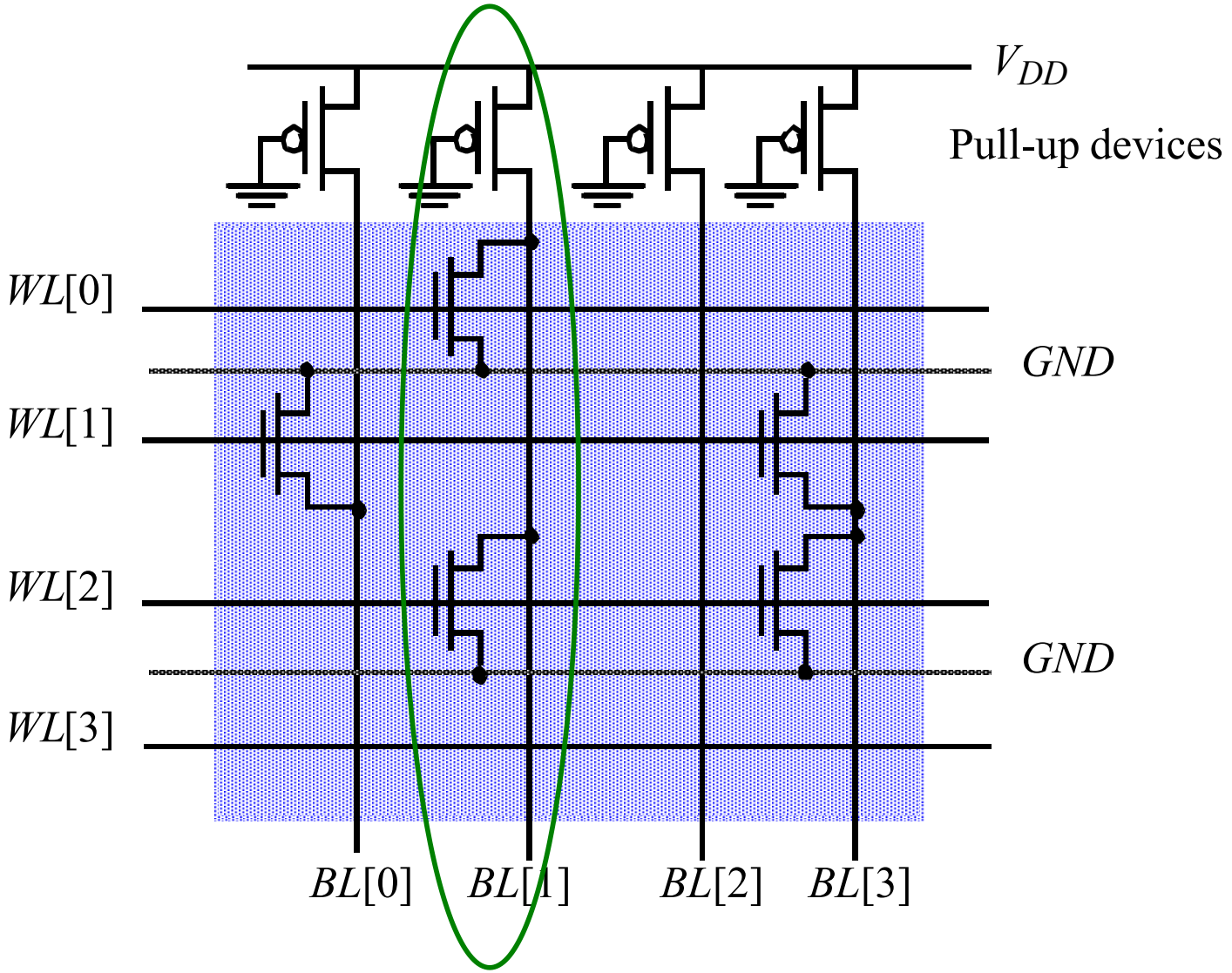

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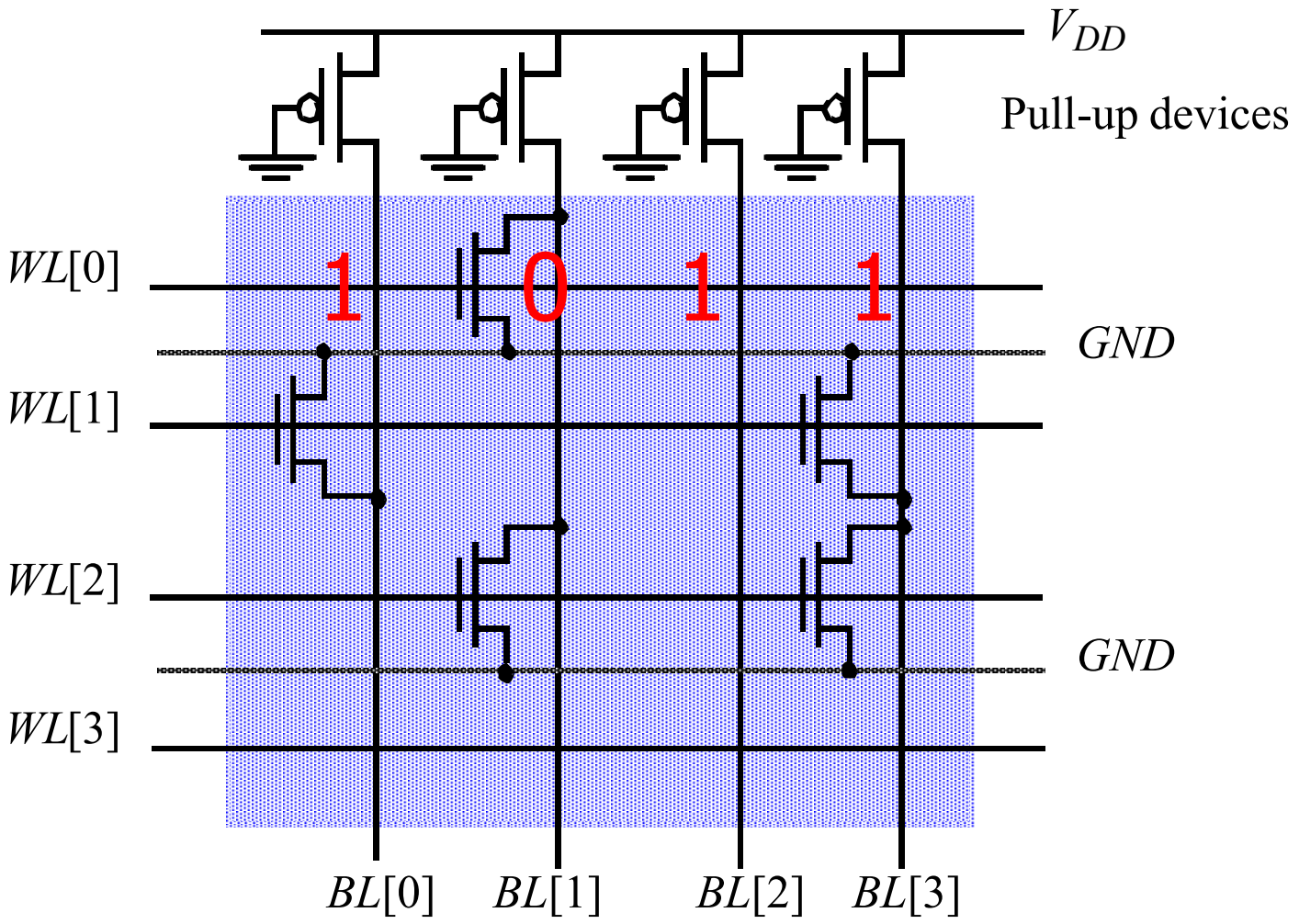
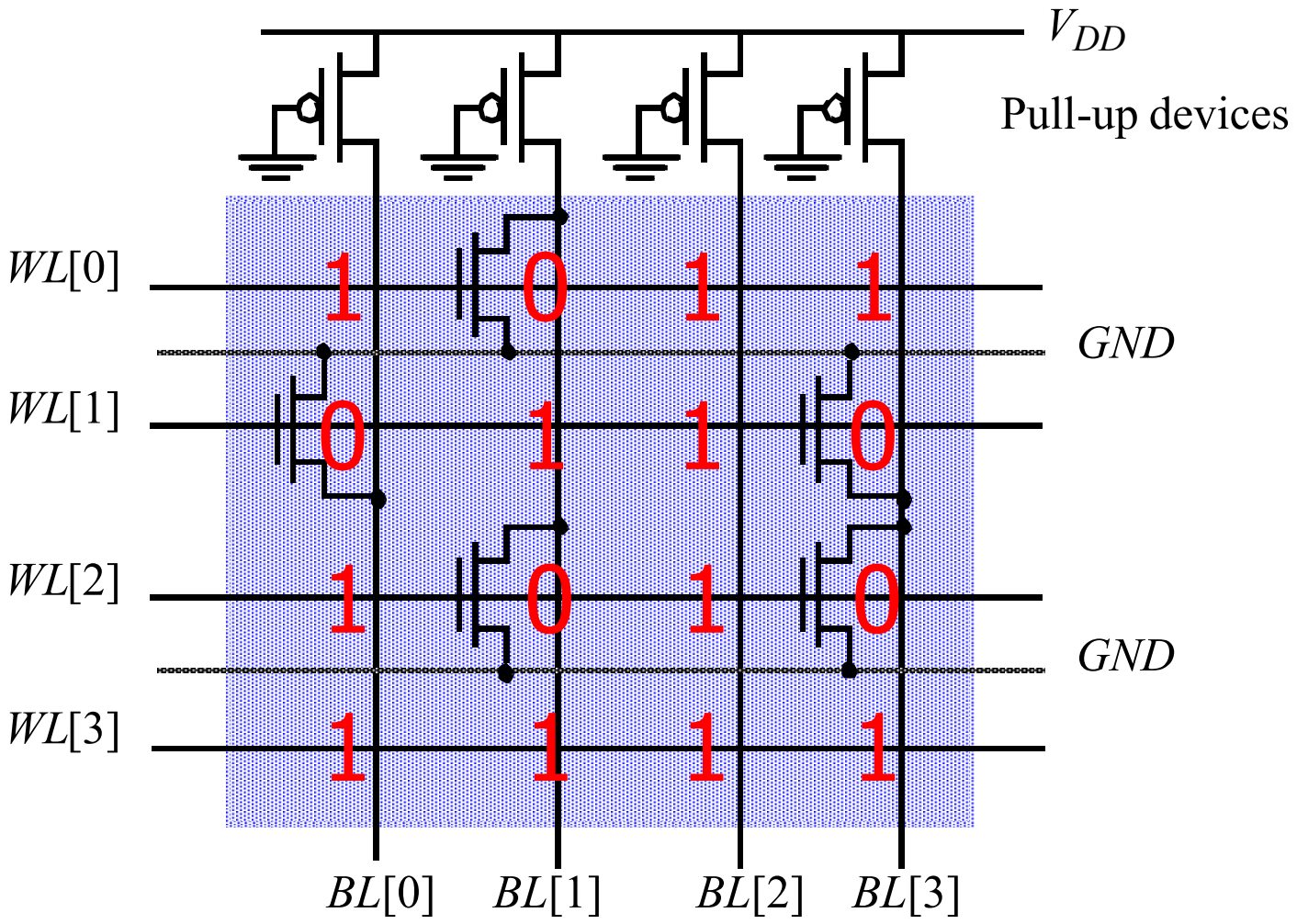

V_{DD}
Pull-up devices
WL[0]
WL[1]
WL[2]
WL[3]
1
0
1
1
GND
GND
BL[0]
BL[1]
BL[2]
BL[3]

MOS NOR ROM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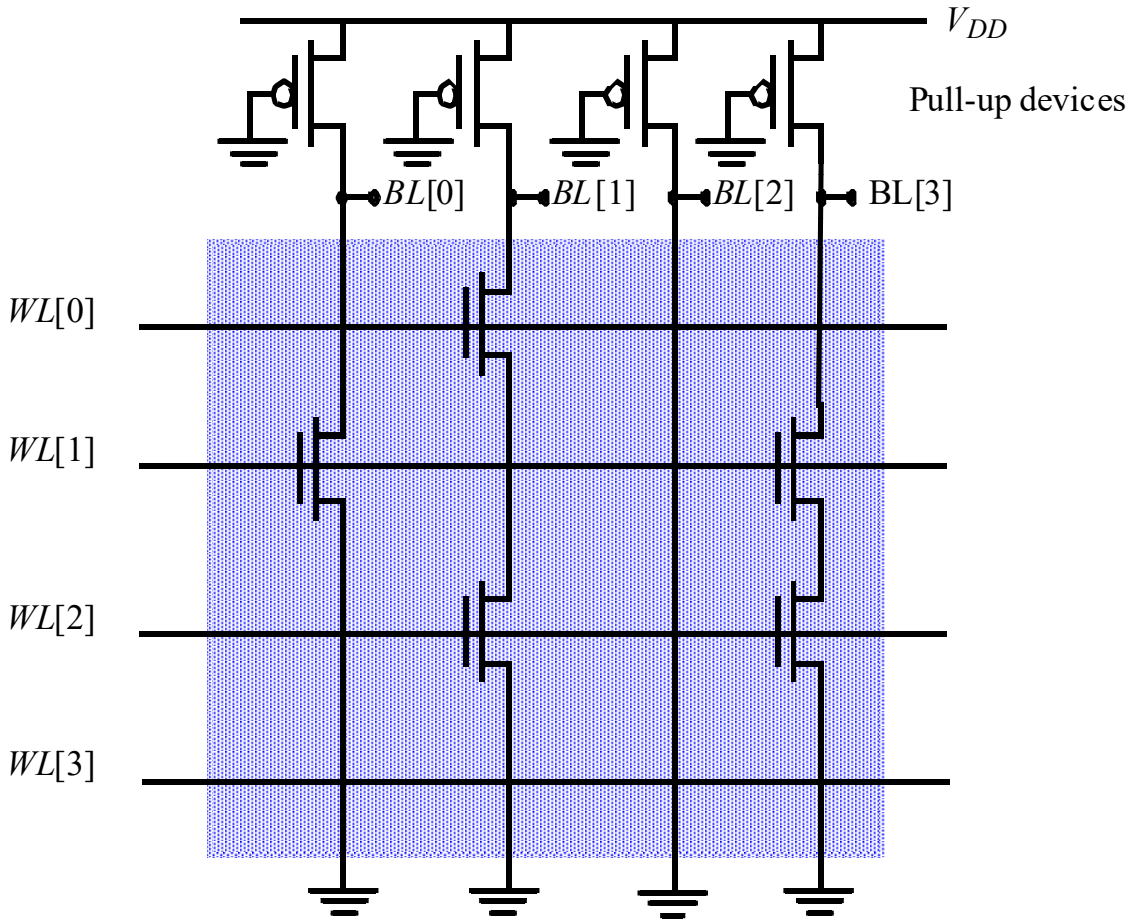

All word lines high by default with exception of selected row

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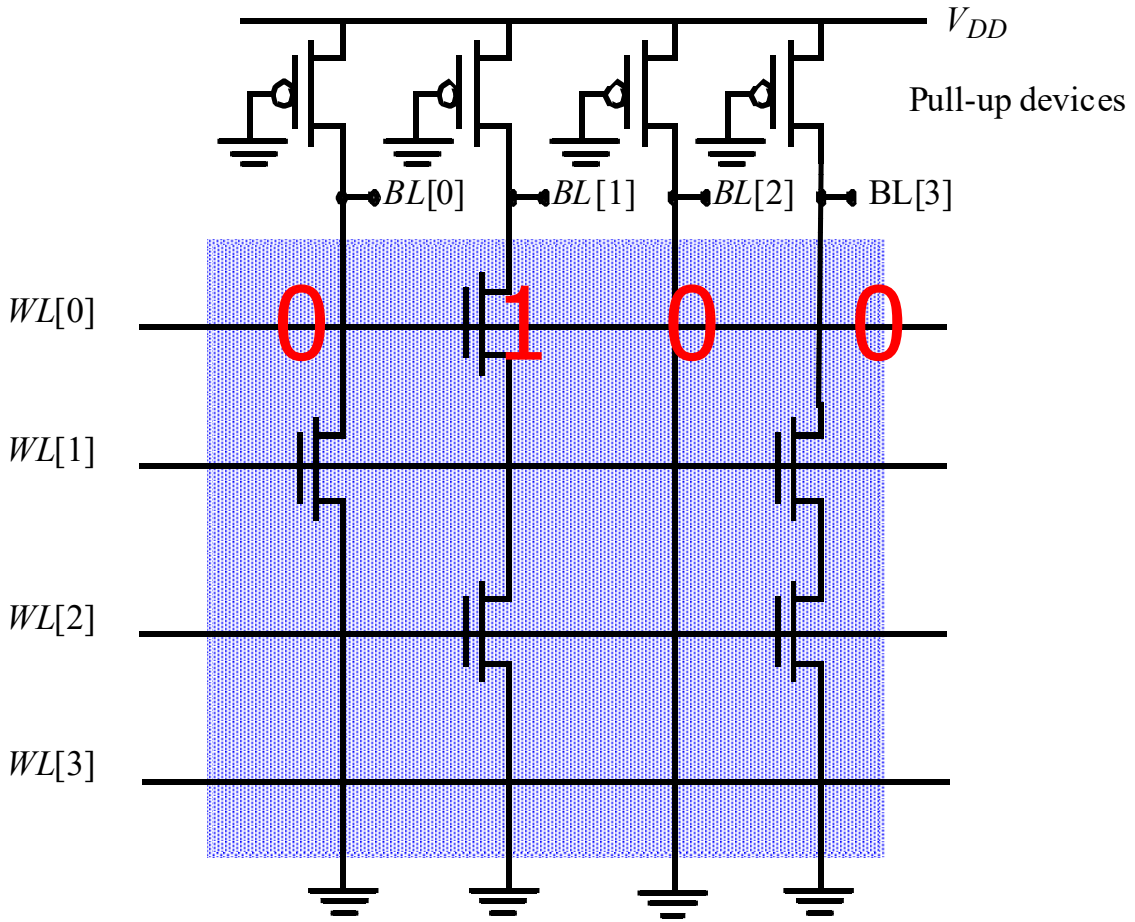

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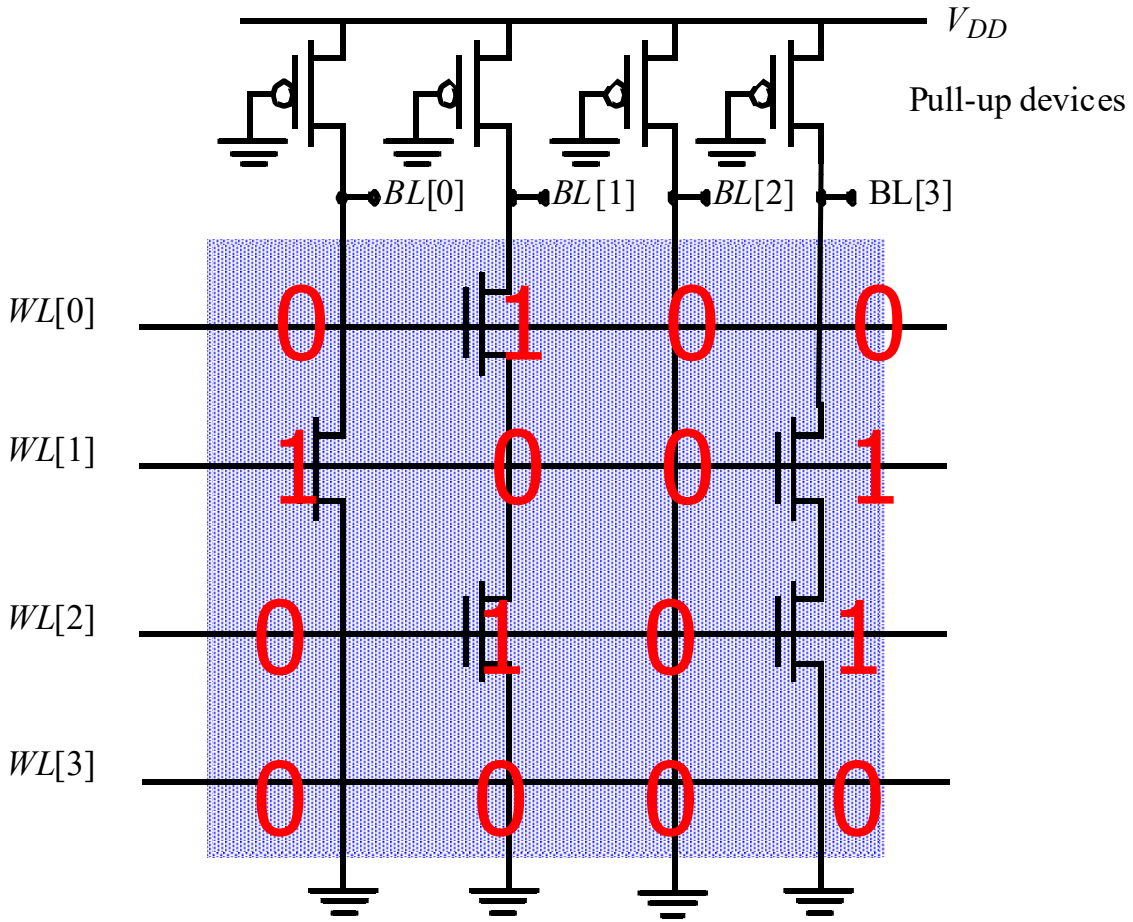

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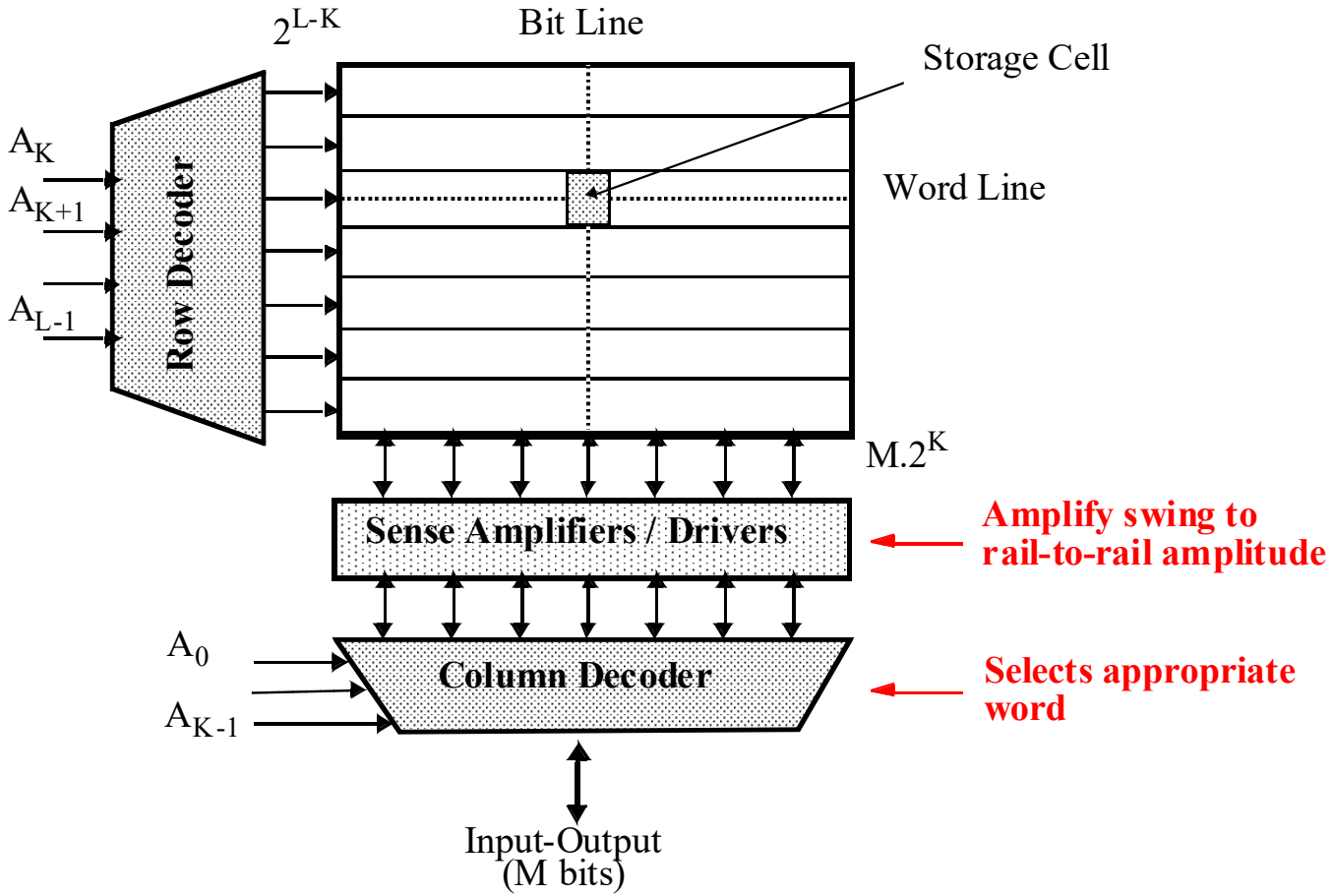

Idea

- Dynamic/clocked logic
  - Only build/drive one pulldown network
    - Domino Logic
  - Fast transition propagation
  - Spend delay (capacitance) on pullup of critical path of logic
  - More complicated design, power dissipation
    - Reserve for when most needed
- Memory for compact state storage
  - Minimize area per bit → maximize density

Admin

- Homework 6
  - Due Friday 11/12