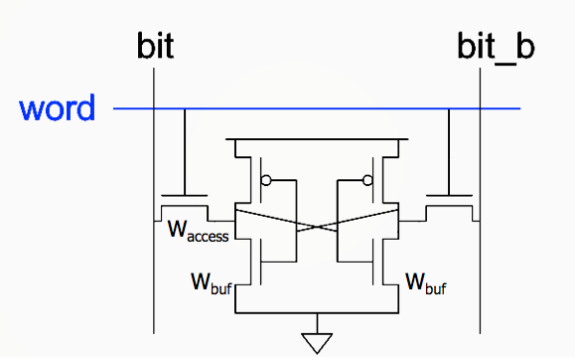

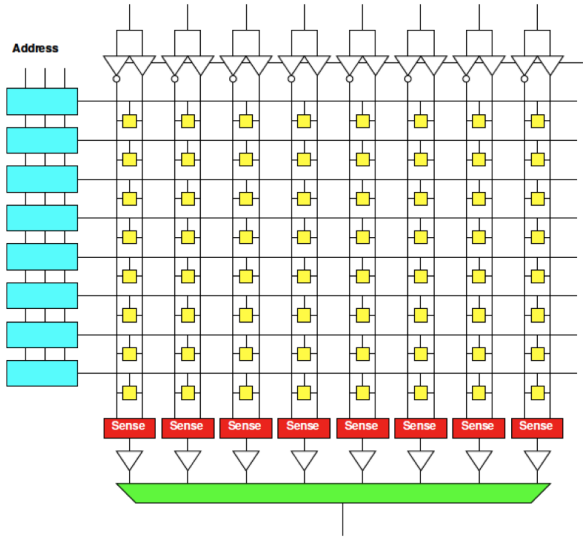

1. What is capacitance of the bit line?
   In terms of access transistor width W_{access}, number of words on bit line, d, γ, and C_0.

2. Delay of memory cell driving bit line? (Read operation)
   In terms of variables above plus buffer size, W_{buf}, and R_0.

3. Concrete delay for $W_{access} = W_{buf} = 1$, $\gamma = 0.5$?
   In terms of $\tau = R_0 C_0$.

Unit	Delay in τ
d=32 (register file)	
d=512 (BRAM or small L1 Cache)	

4. What is the capacitance of the word line? In terms of access transistor width W_{access}, number of bits on the word line, w, γ, and C_0.

5. Delay driving word line, assuming driven by a driver with equivalent drive strength to $W_{wldrive}$ inverter? (other parameters as above)