ESE370: Circuit-Level Modeling, Design, and Optimization for Digital Systems

Lec 29: November 17, 2021

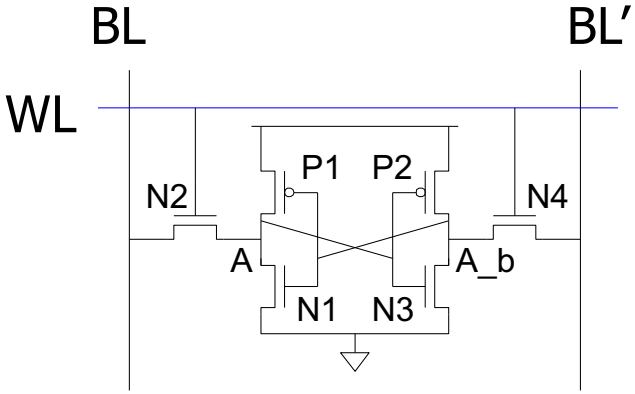
RAM Core Part 2

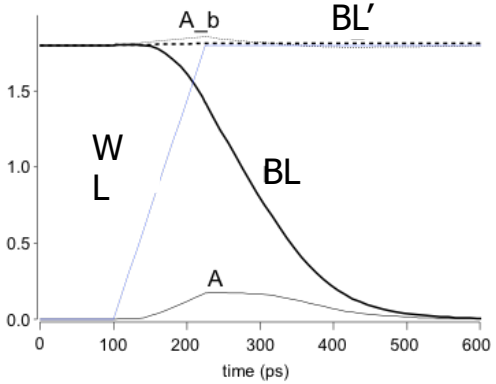
Today

- 6T SRAM
- 5T SRAM
- Multiported SRAM
- DRAM

SRAM Read

- Precharge both bitlines high
- Then turn on wordline, WL
- One of the two bitlines will be pulled down by the cell
- Ex: A = 0, A_b = 1
  - BL discharges, BL' stays high
  - But A bumps up slightly
- *Read stability*
  - A must not flip
  - N1 > N2



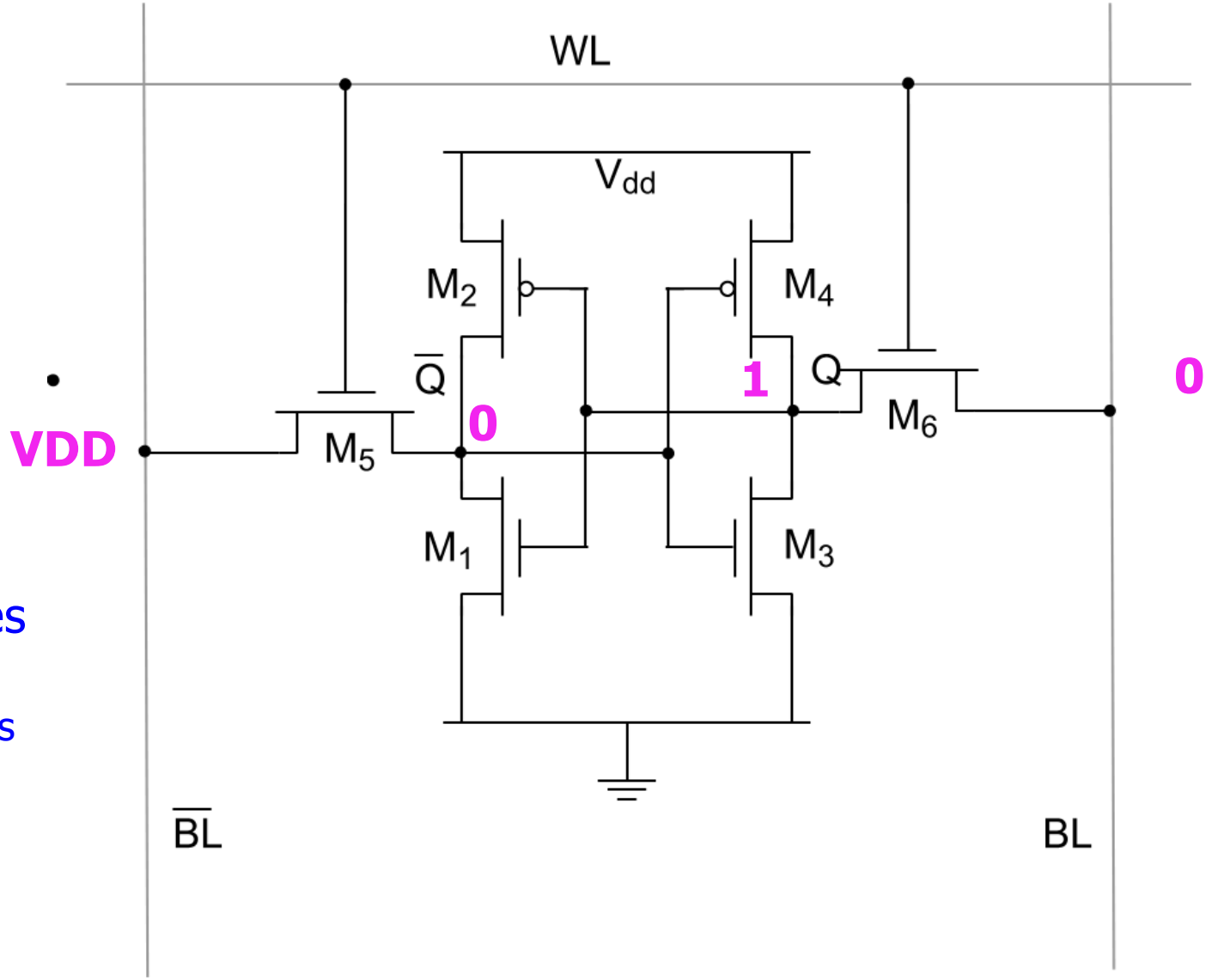


6-transistor CMOS SRAM Cell

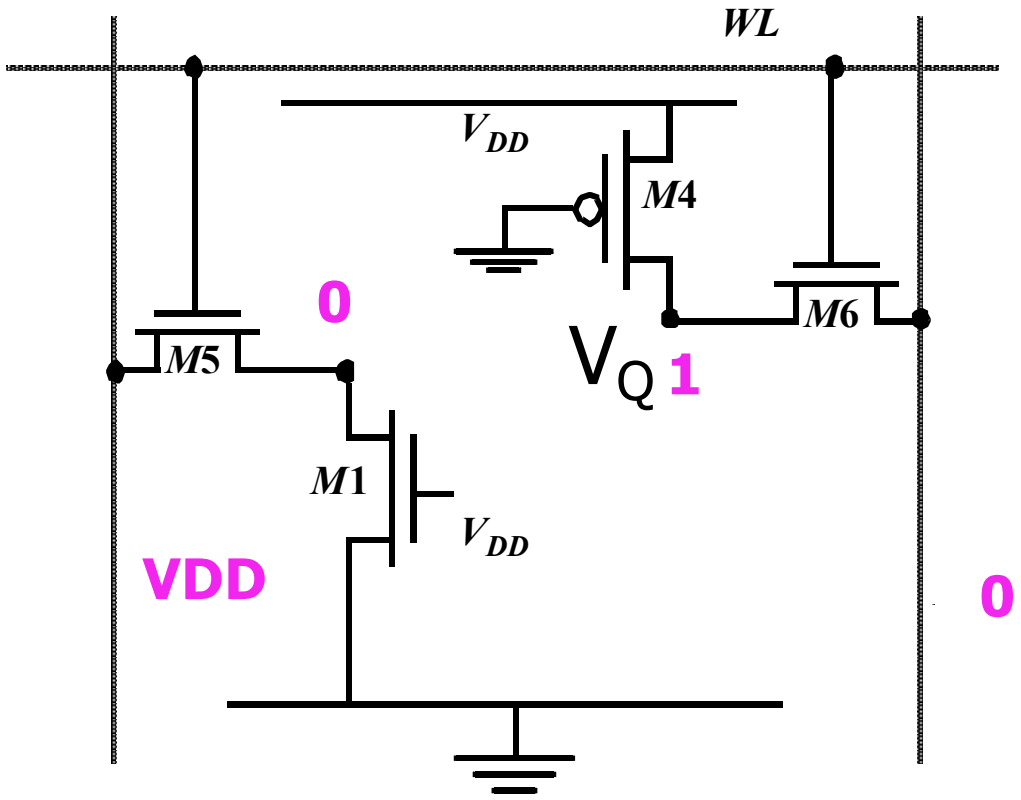
Assume 1 is stored (Q=1)

Write Operation:

- Want to write a 0
- First drive bitlines with input data
- Then wordline goes high (Vdd)
  - Still driving bitlines

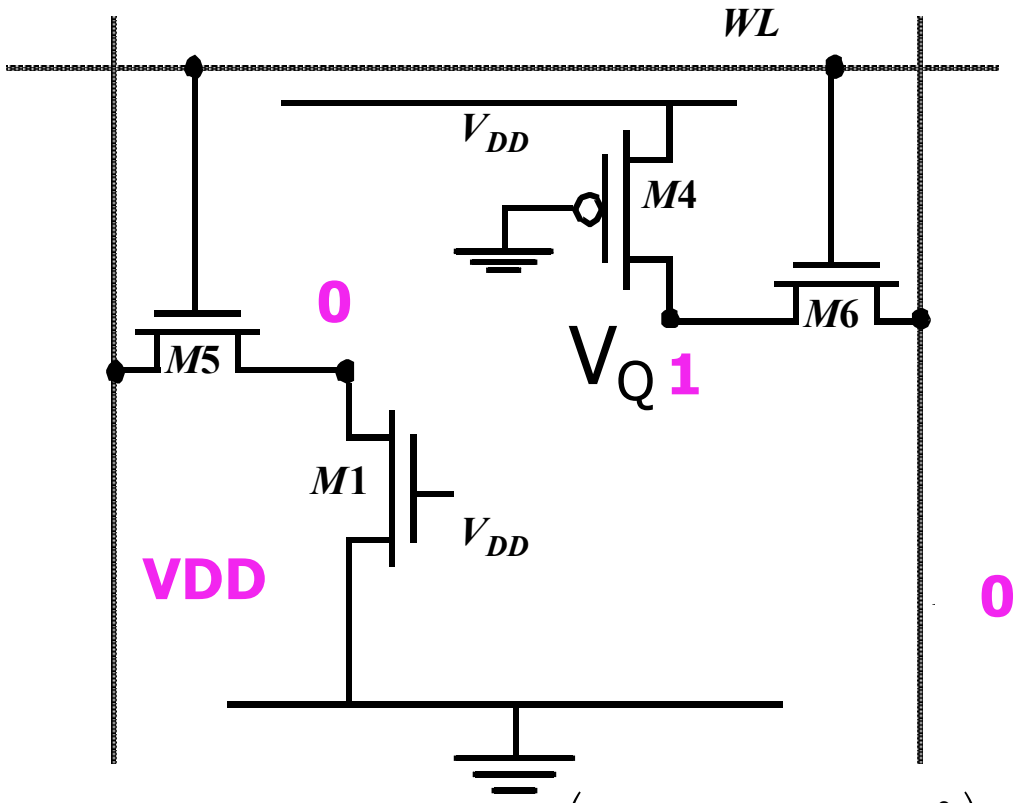


CMOS SRAM Analysis (Write)



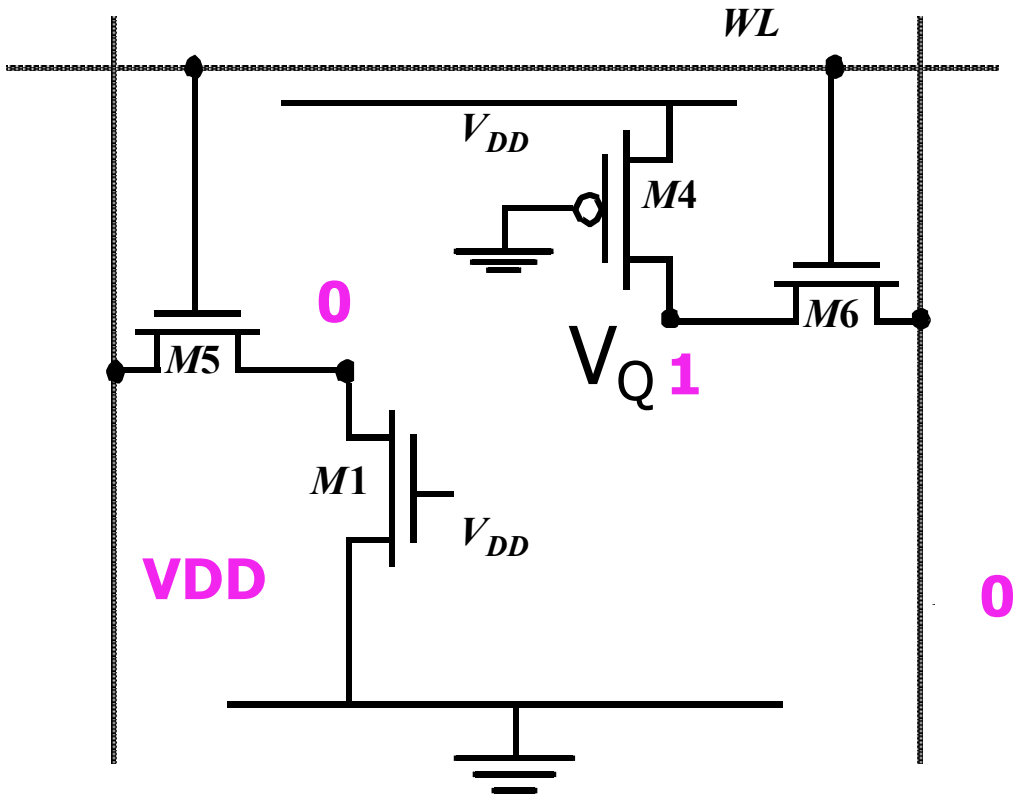
Which transistor discharges Q to Gnd?
Which transistor must it overpower?
What regions of operation are the transistors in?
Write the KCL equation for the two transistors

CMOS SRAM Analysis (Write)



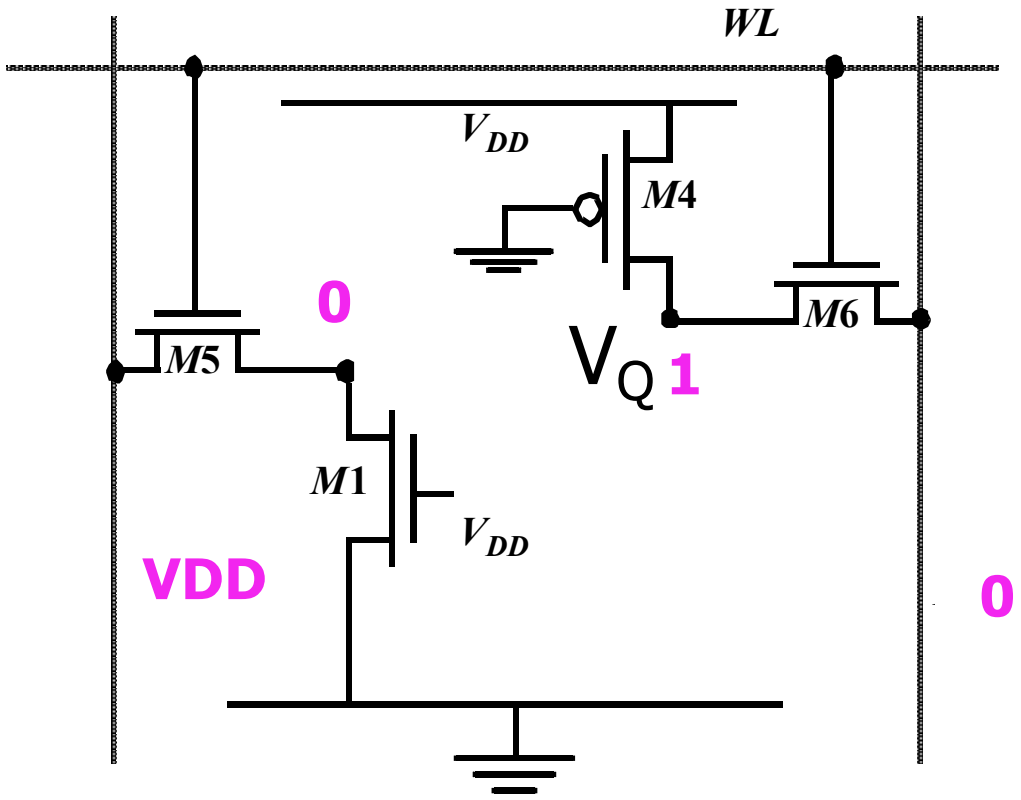
$$k_{p,M4}\left(V_{DD}-\left|V_{Tp}\right|\right)^2 = k_{n,M6}\left((V_{DD}-V_{Tn})V_Q-\frac{V_Q^2}{2}\right)$$

CMOS SRAM Analysis (Write)



$$\frac{k_{p,M4}}{k_{n,M6}} = \frac{(V_{DD} - V_{Tn})V_Q - \frac{V_Q^2}{2}}{\left(V_{DD} - |V_{Tp}|\right)^2}$$

CMOS SRAM Analysis (Write)



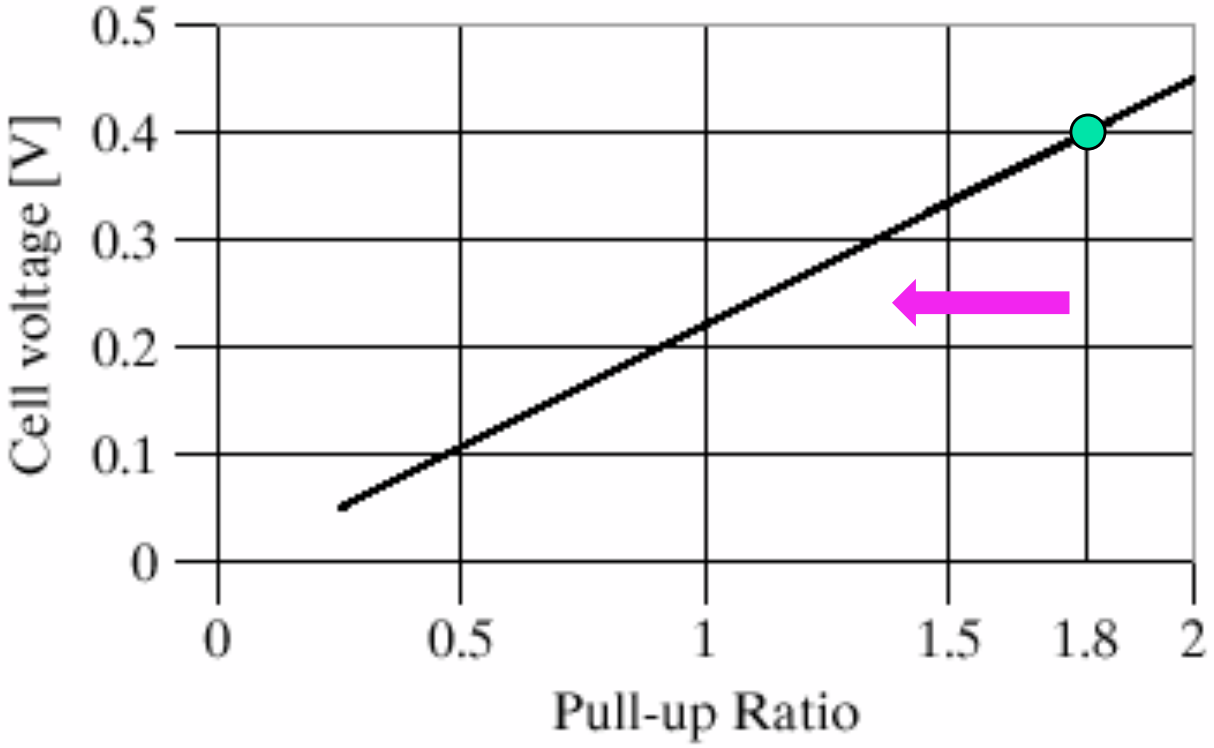
$$PR = \frac{W_4/L_4}{W_6/L_6}$$

$$\frac{k_{p,M4}}{k_{n,M6}} = \frac{(V_{DD} - V_{Tn})V_Q - \frac{V_Q^2}{2}}{\left(V_{DD} - |V_{Tp}|\right)^2}$$

$V_Q = V_{Tn}$

$$\frac{k_{p,M4}}{k_{n,M6}} = \frac{(V_{DD} - V_{Tn})V_{Tn} - \frac{V_{Tn}^2}{2}}{\left(V_{DD} - |V_{Tp}|\right)^2}$$

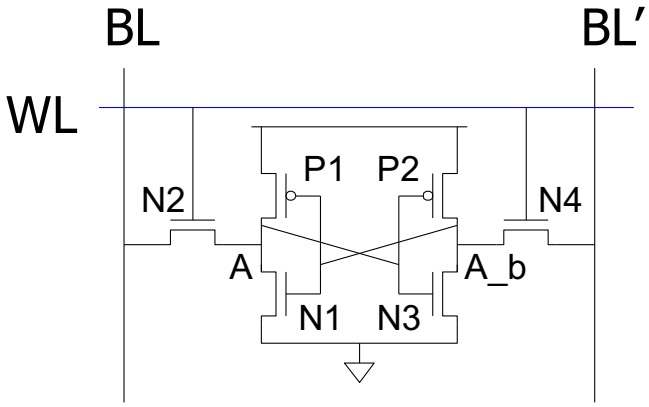
CMOS SRAM Analysis (Write)

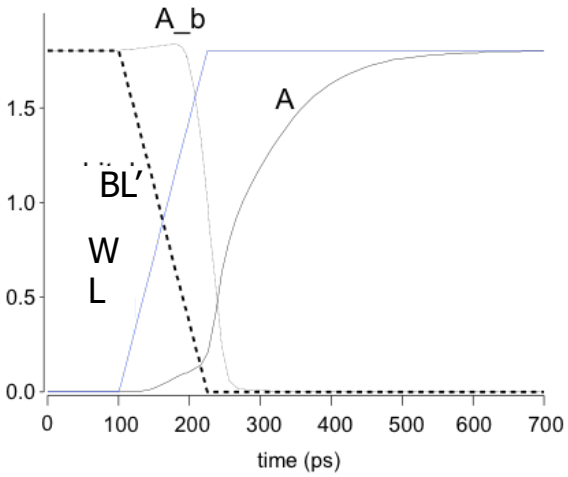


$$PR = \frac{W_4/L_4}{W_6/L_6}$$

SRAM Write

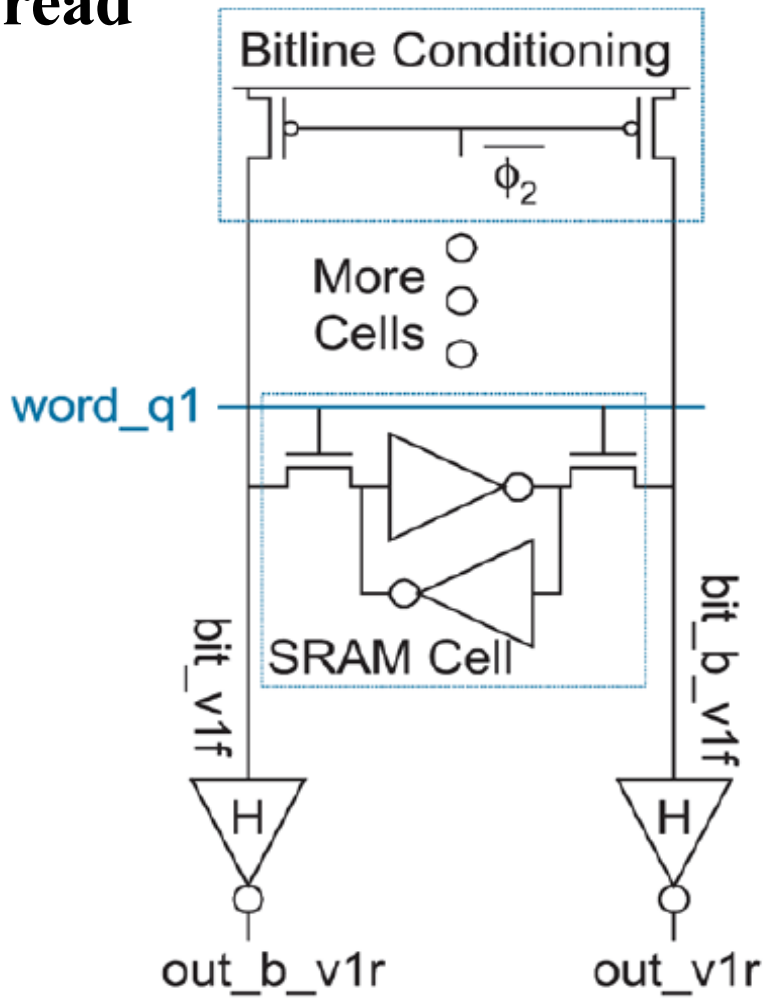
- Drive one bitline high, the other low
  - Depending on write data
- Then turn on wordline, WL
- Bitlines overpower cell with new value
- Ex: A = 0, A_b = 1, BL = 1, BL' = 0
  - Force A_b low, then A charges high
- *Writability*
  - Must overpower feedback inverter
  - N4 >> P2



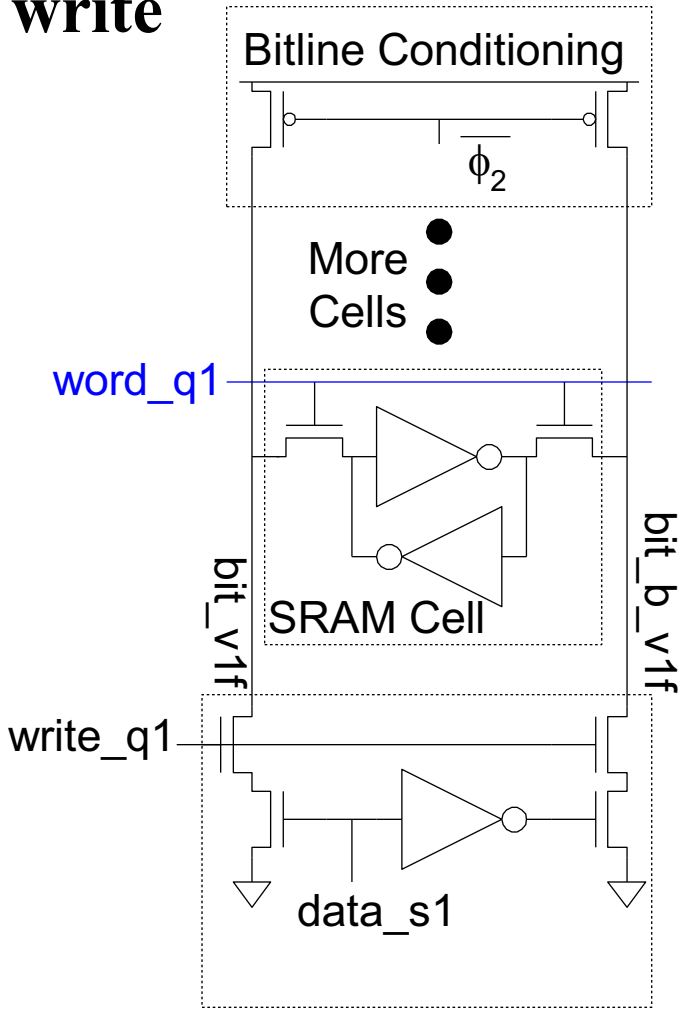


SRAM Column Example

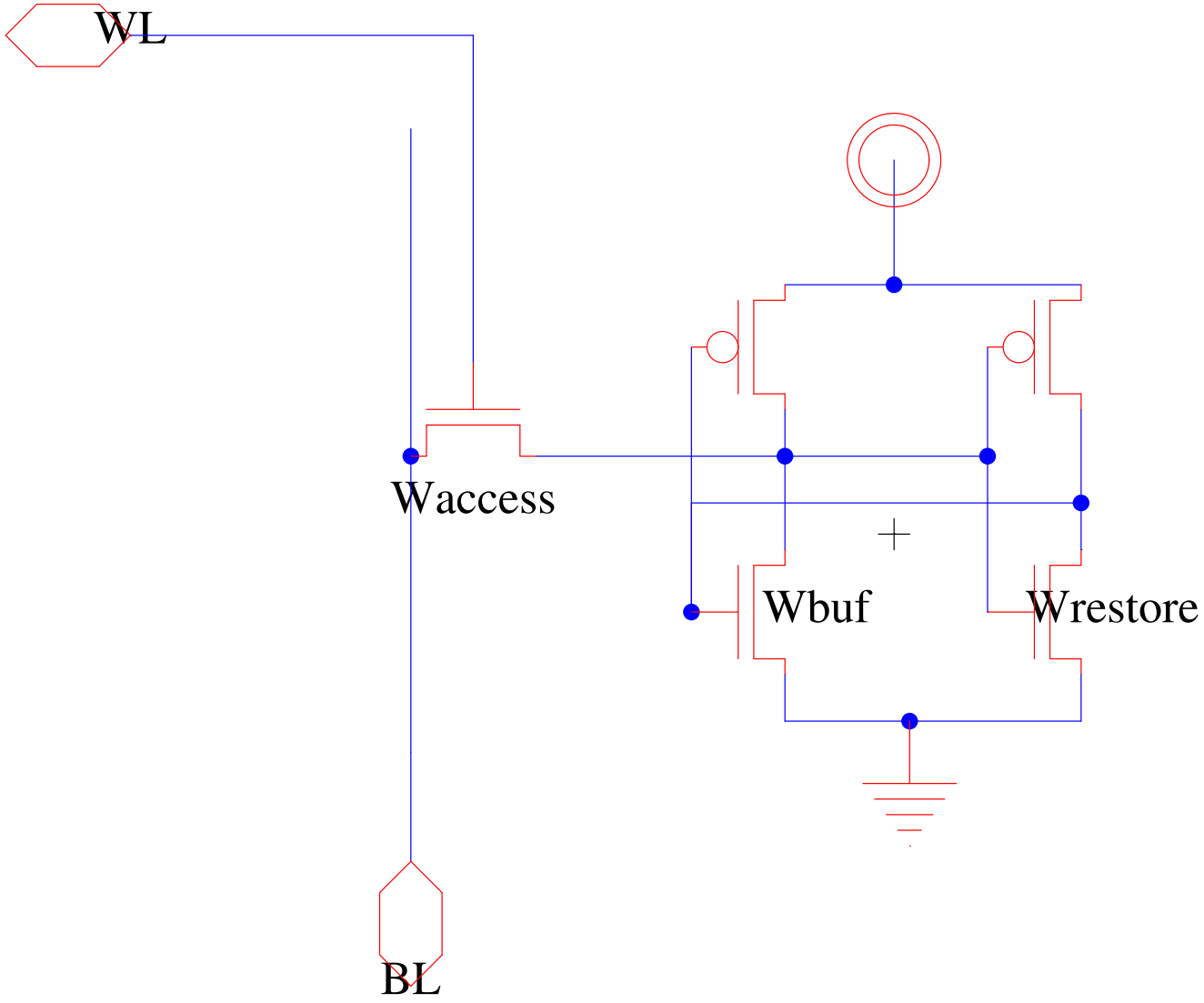
read



write



5T SRAM

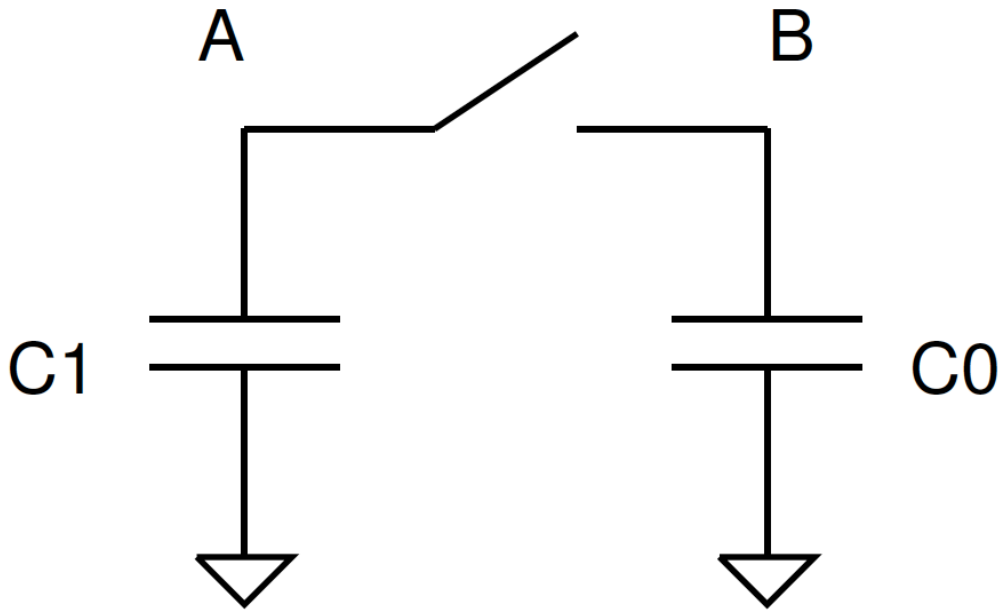


Charge Sharing (Preclass 1)

Initially

- A @ 1V
- B @ 0V

- Q_A=1V*C1=C1



Charge Sharing (Preclass 1)

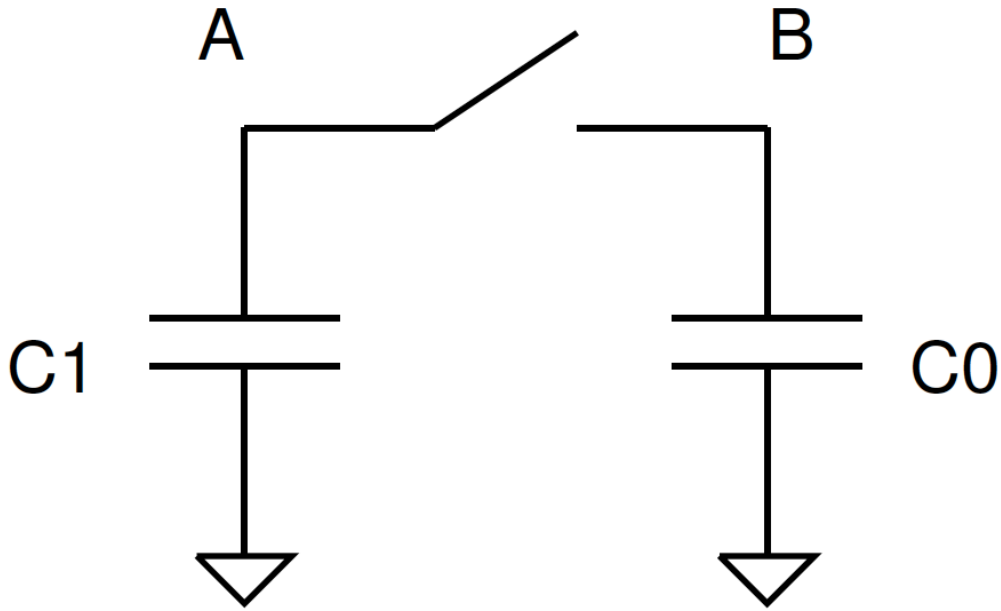
Initially

- A @ 1V
- B @ 0V

- Q_A=1V*C1=C1

Close switch

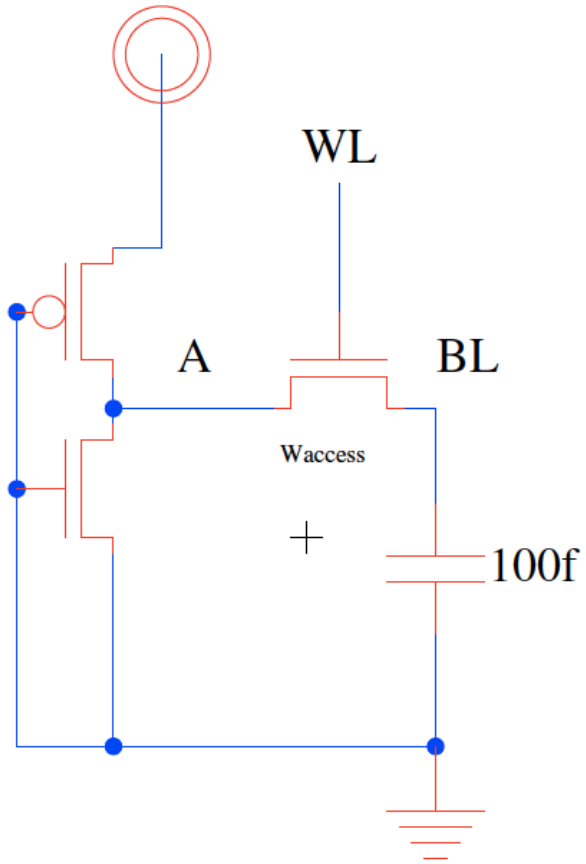
- $Q_{tot}=V_{final}*(C1+C0)$
- Charge conservation
  - $Q_A=Q_{tot}$
- $C1=V_{final}*(C1+C0)$



$$V_{final} = \frac{C1}{C1 + C0}$$

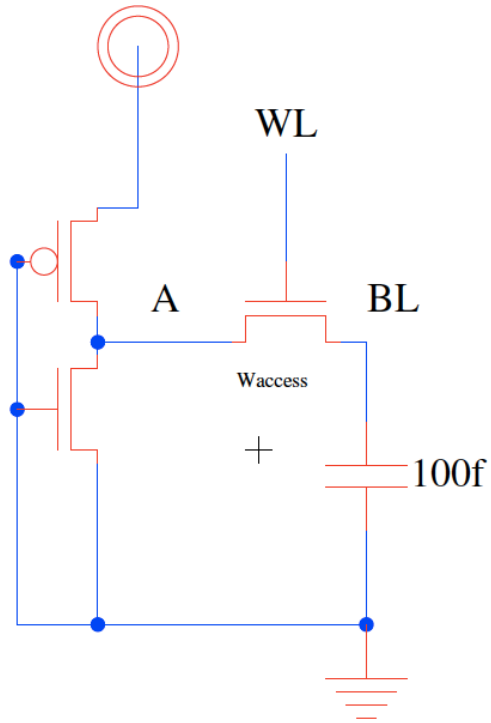
Consider (preclass 2)

- Read: What happens to voltage at A when WL turns from 0→1?
  - Assume W_{access} large
  - $W_{access} >> W_{pu}=1$
  - BL initially 0



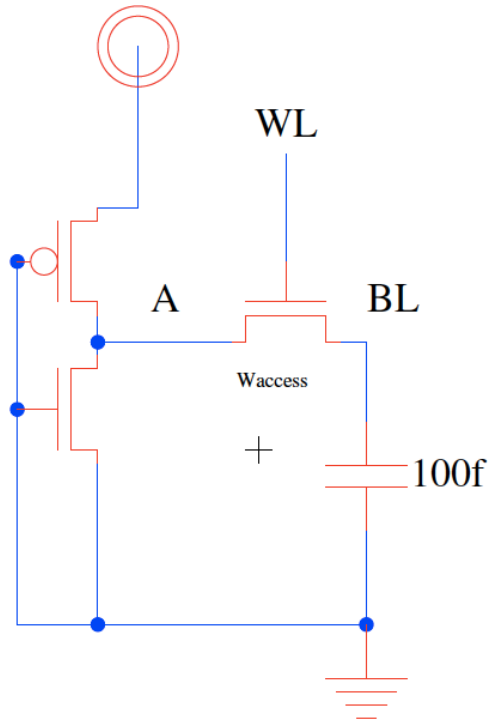
Voltage After enable Word Line

- $Q_{BL} = 0$
- $Q_A = (1V)(\gamma 2C_0 + \gamma W_{access} C_0)$

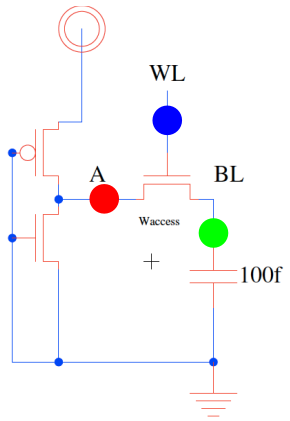


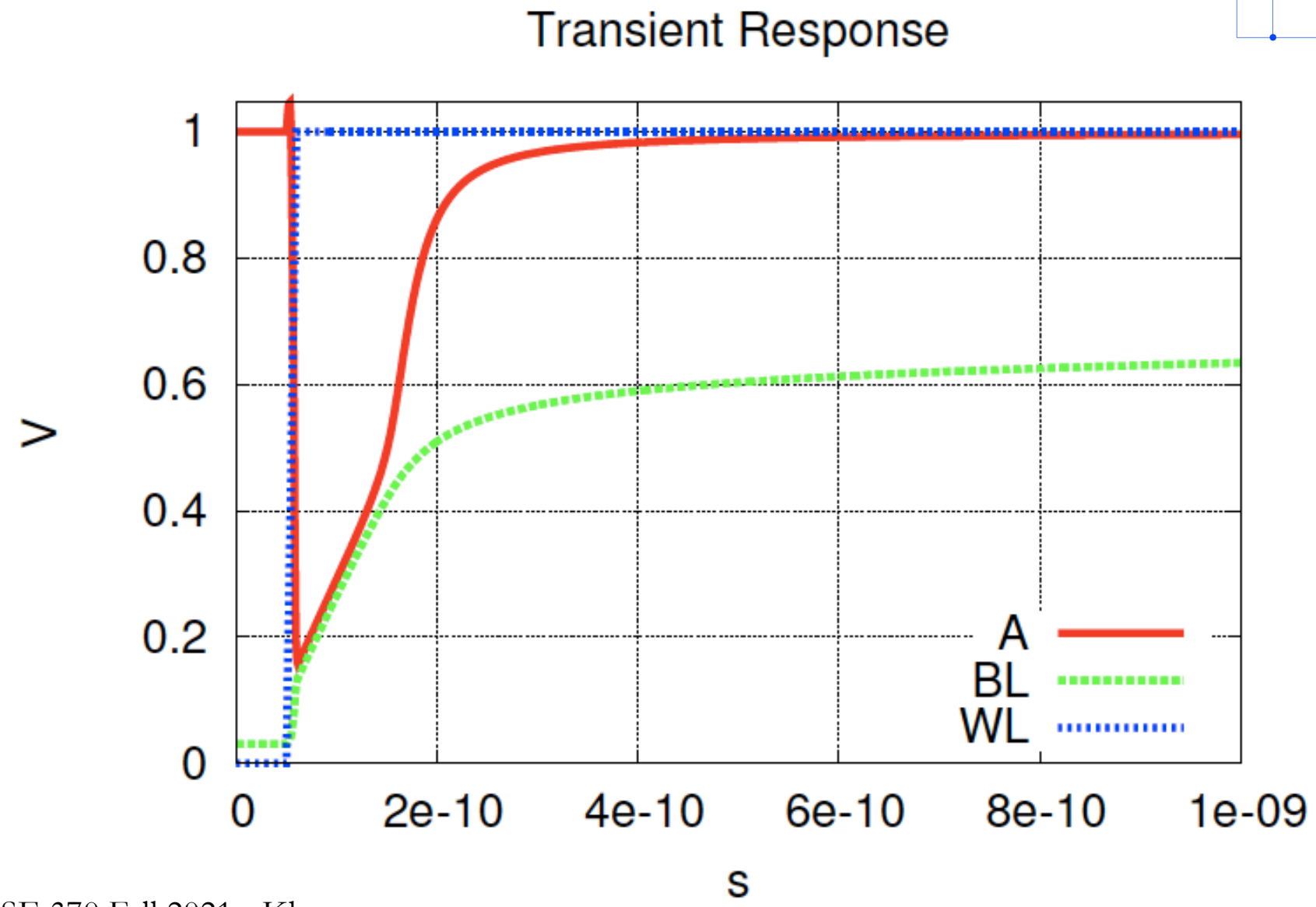
Voltage After enable Word Line

- $Q_{BL} = 0$
- $Q_A = (1V)(\gamma 2C_0 + \gamma W_{access} C_0)$
- $100fF = C_{BL} >> C_A = (\gamma(2 + W_{access})C_0)$
- After enable W_{access} (W_{access} large)
  - Total charge $Q_{BL} + Q_A$ unchanged
    - Charge conservation
  - Distributed over larger capacitance~=C_{BL}
  - $V_A = V_{BL} \sim = C_A / C_{BL}$



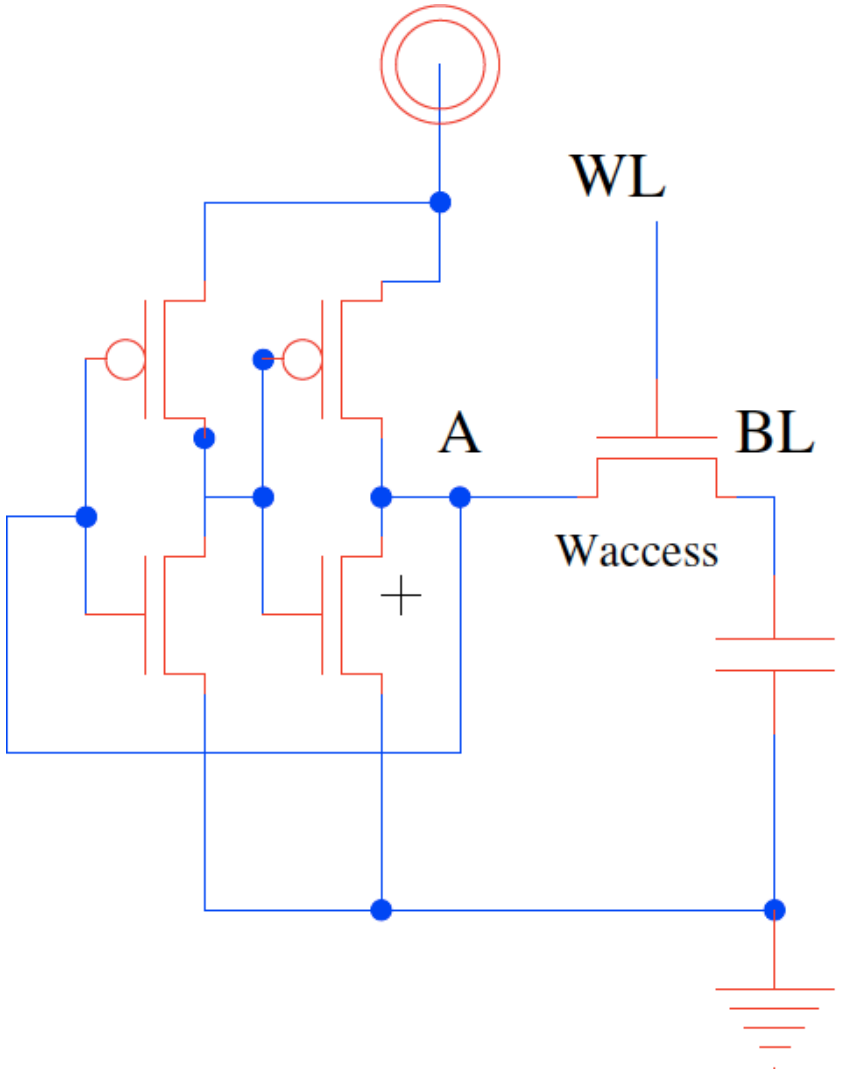
Simulation: W_{access}=100



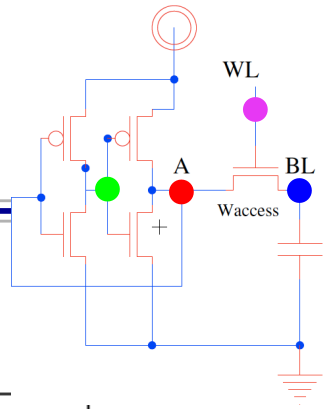


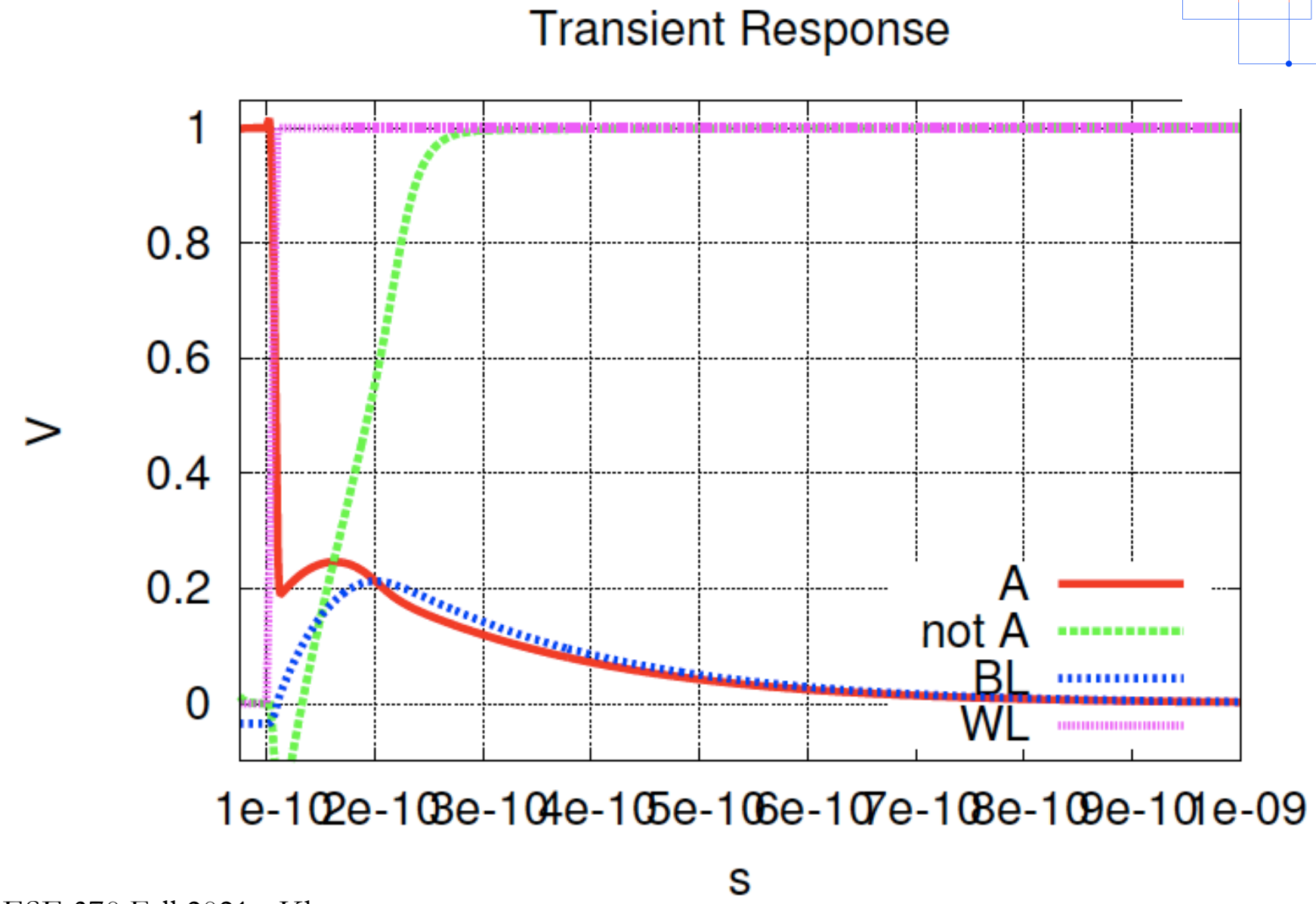
Consider (5T SRAM) (preclass 3)

- What happens to voltage at A when WL turns from 0→1?
  - Assume W_{access} large
  - A initially 1
  - BL initially 0

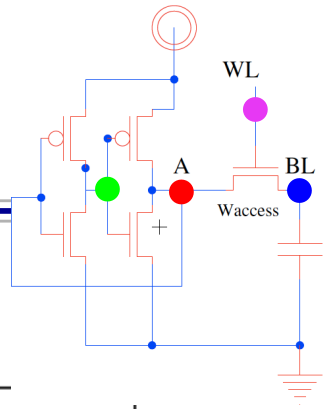


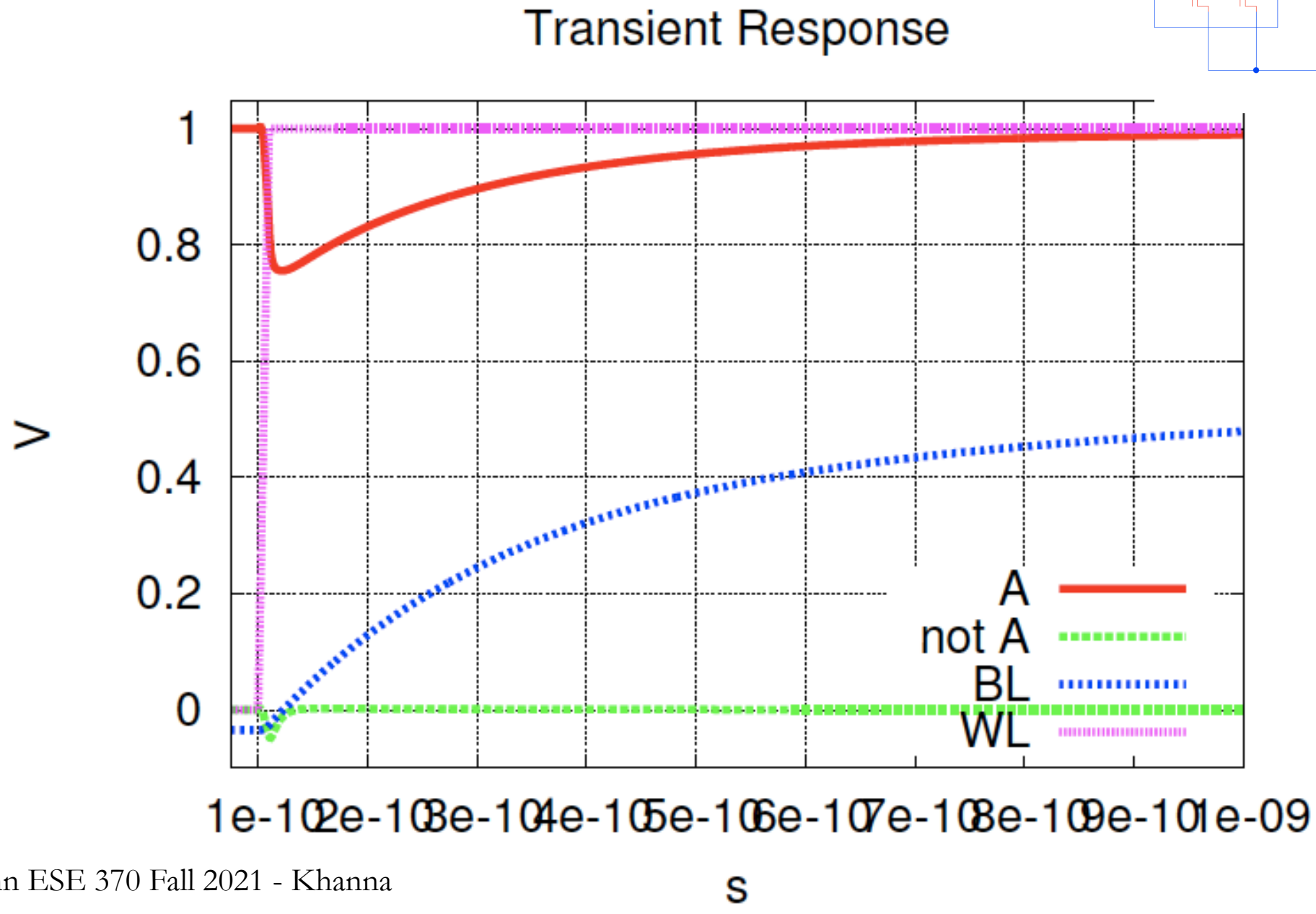
Simulation W_{access}=20





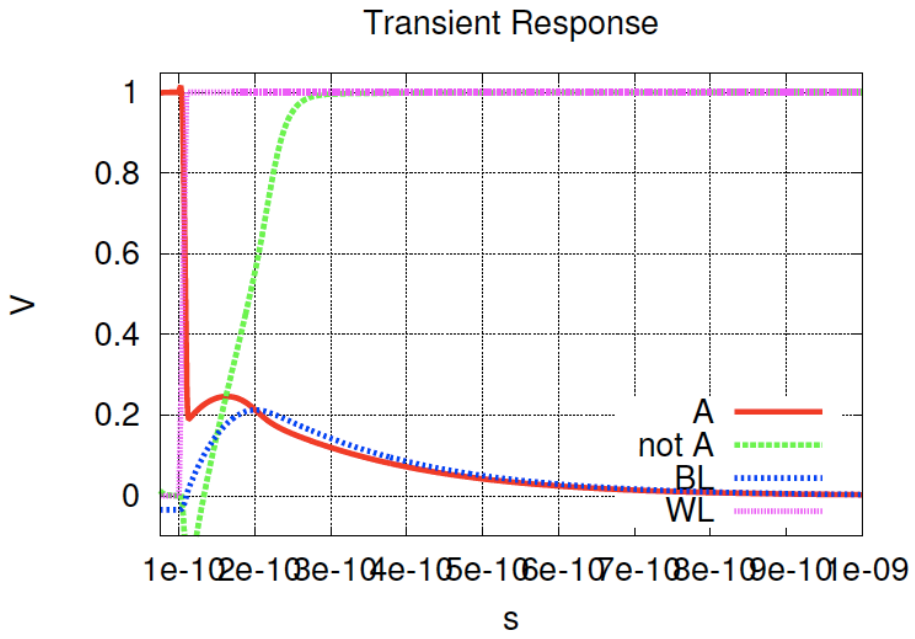
Simulation W_{access}=4



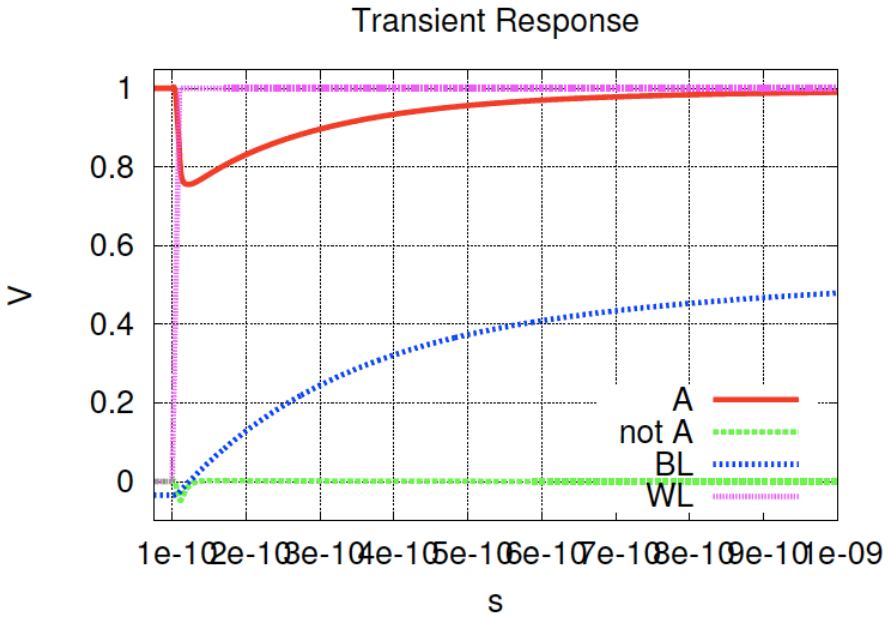


Charge Sharing

- **Conclude:** charge sharing can lead to read upset
  - Charge redistribution/sharing adequate to flip state of bit



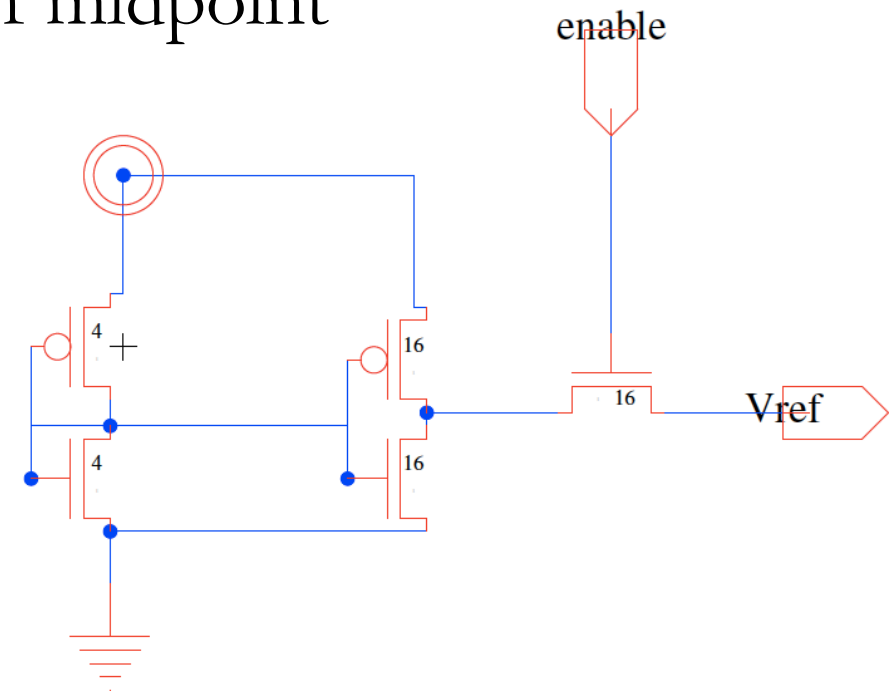
W_{access}=20

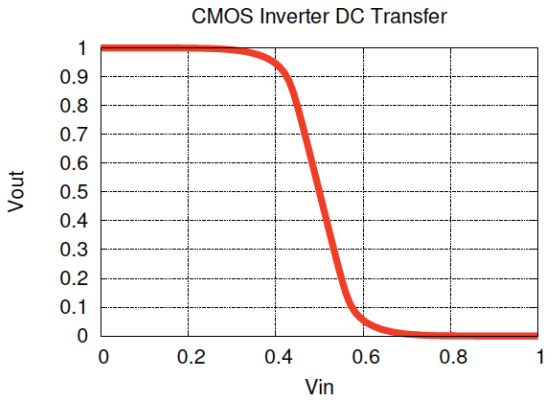


W_{access}=4

Charge to middle Voltage

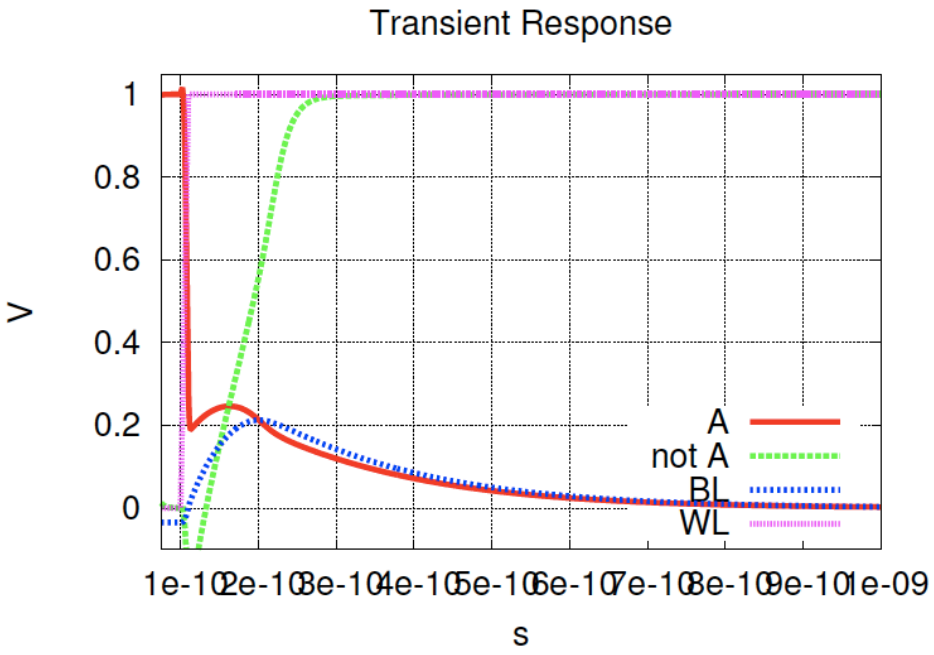
- Pre-charge bitlines to $V_{dd}/2$ before begin read operation
- Now charge sharing doesn't swing to opposite side of midpoint



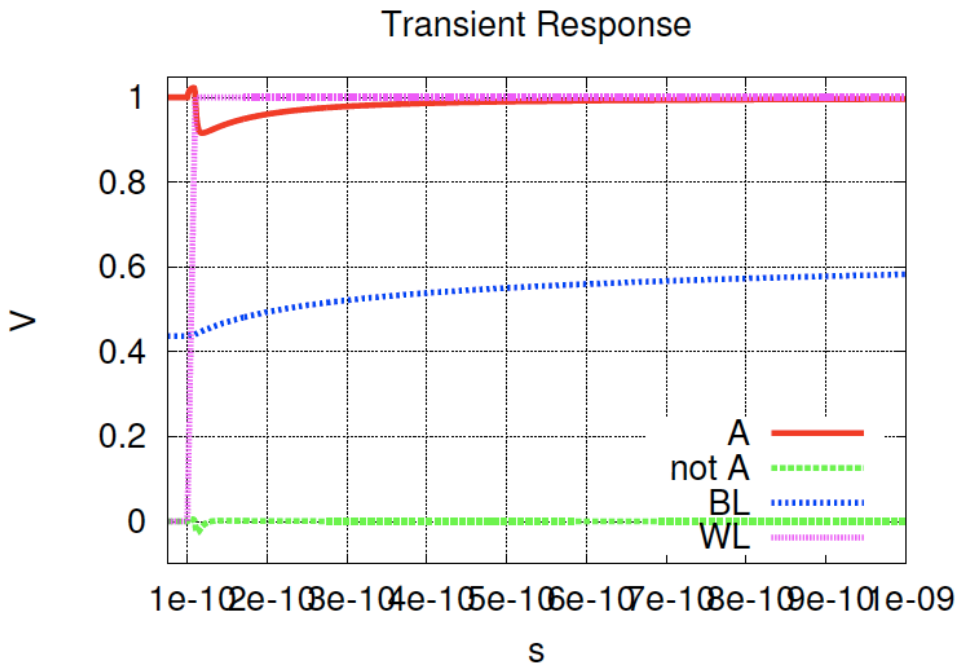


Compare

- Both W_{access}=20; vary BL precharge voltage

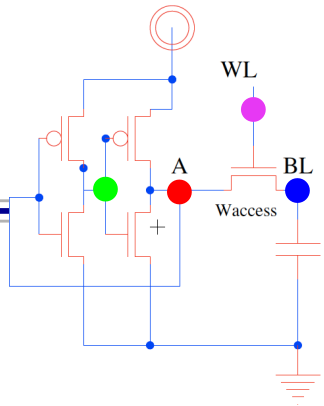


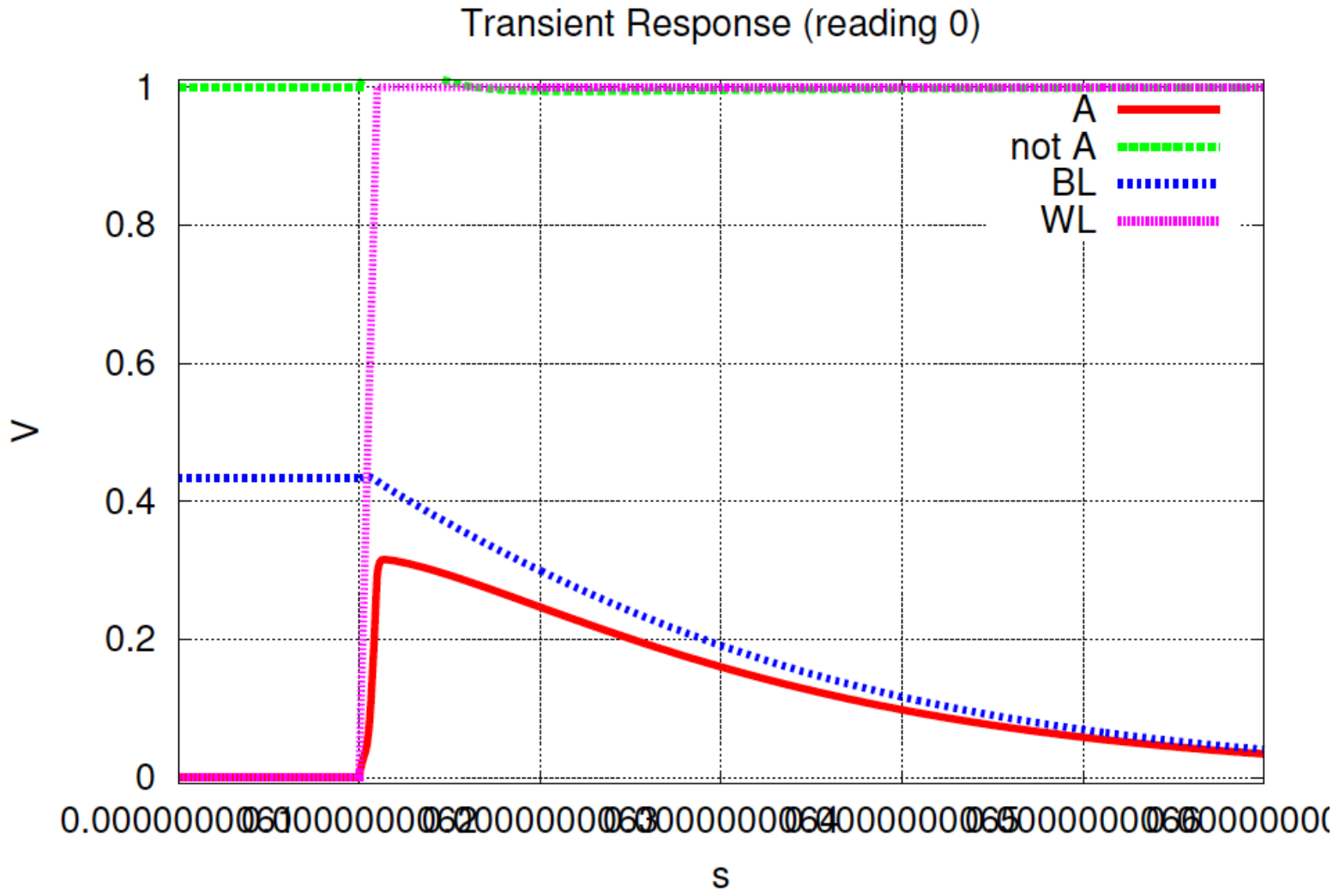
0 precharge



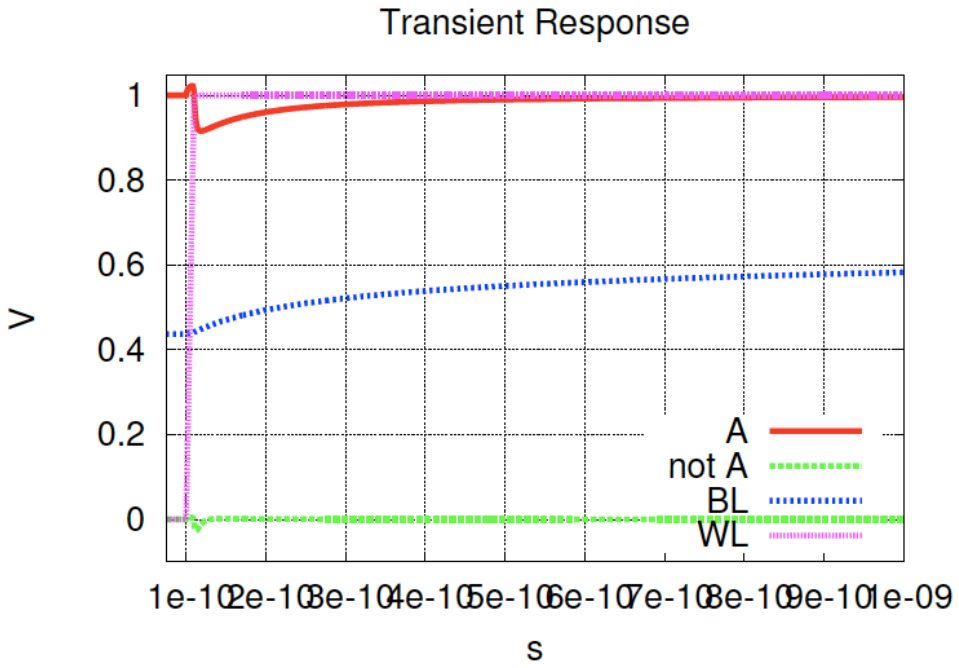
$V_{dd}/2$ precharge

Simulation W_{access}=20 (precharge Vdd/2, reading 0)

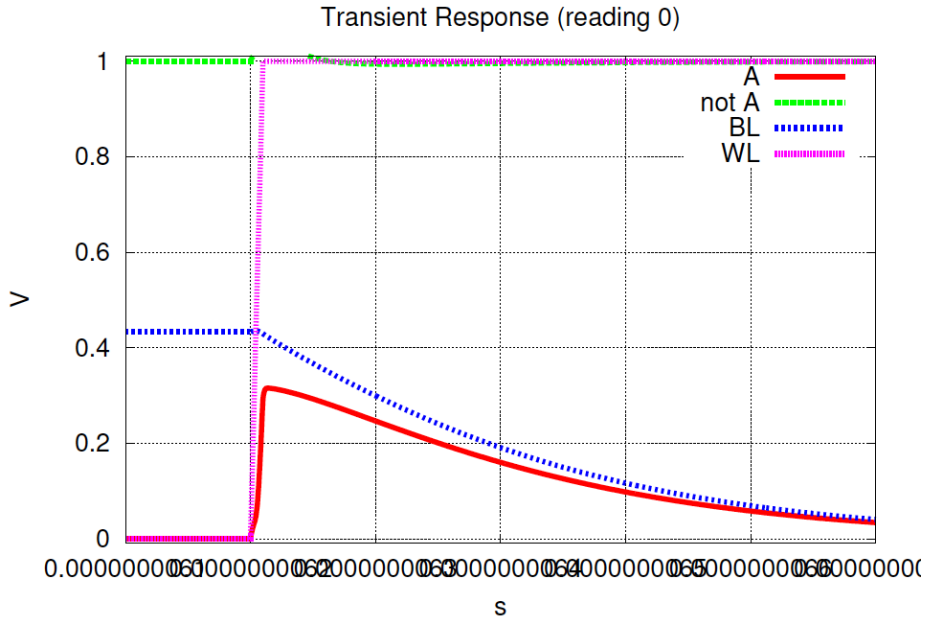




Simulation W_{access}=20 (with precharge Vdd/2)



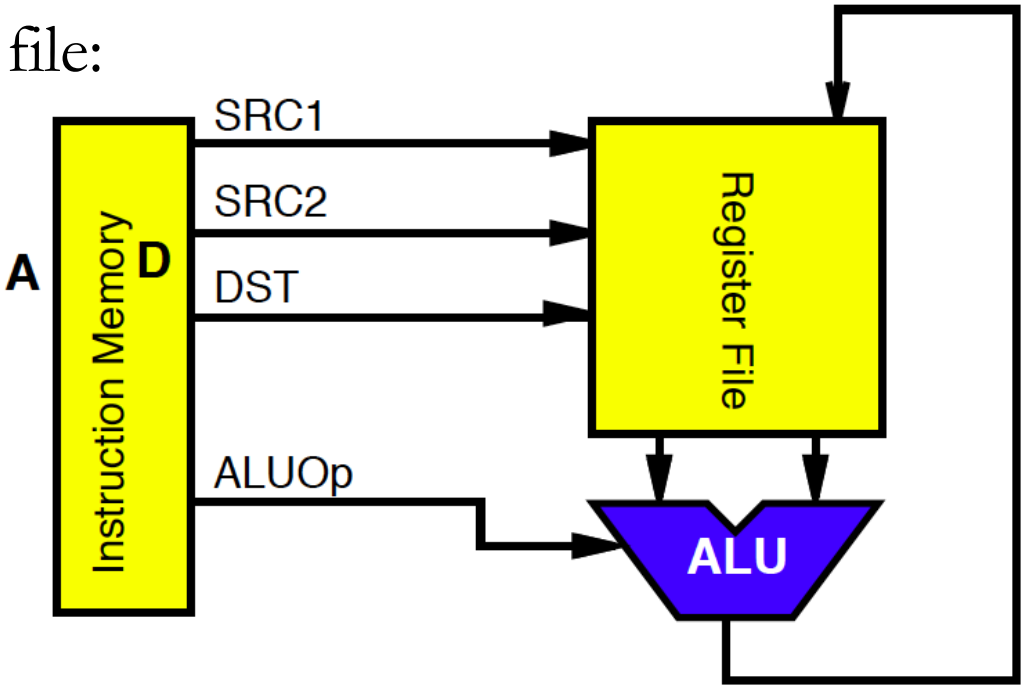
Read 1



Read 0

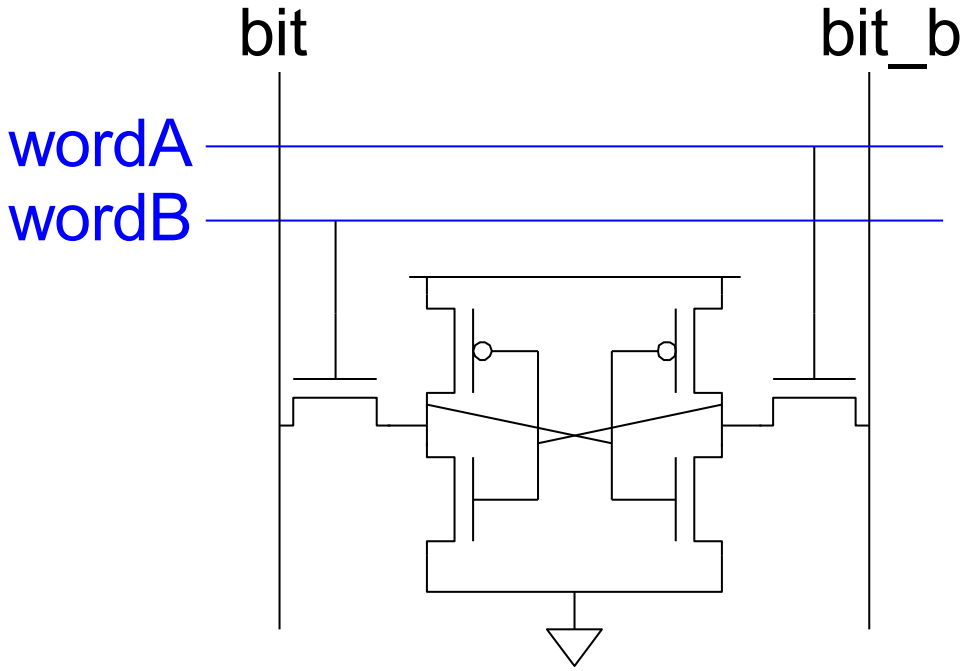
Multiple Ports

- We have considered single-ported SRAM
  - One read or one write on each cycle
- *Multiported* SRAM are needed for register files
- Examples:
  - Pipelined ALU register file:
    - add r1,r2,r3
    - R3←R1+R2
    - Requires two reads and one write



Dual-Ported SRAM

- Simple dual-ported SRAM
  - Two independent single-ended reads
  - Or one differential write



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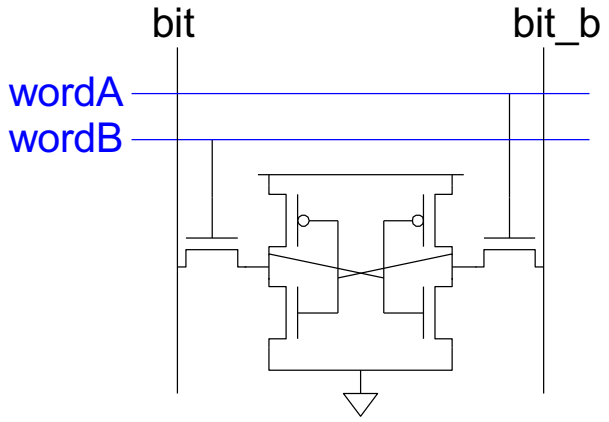
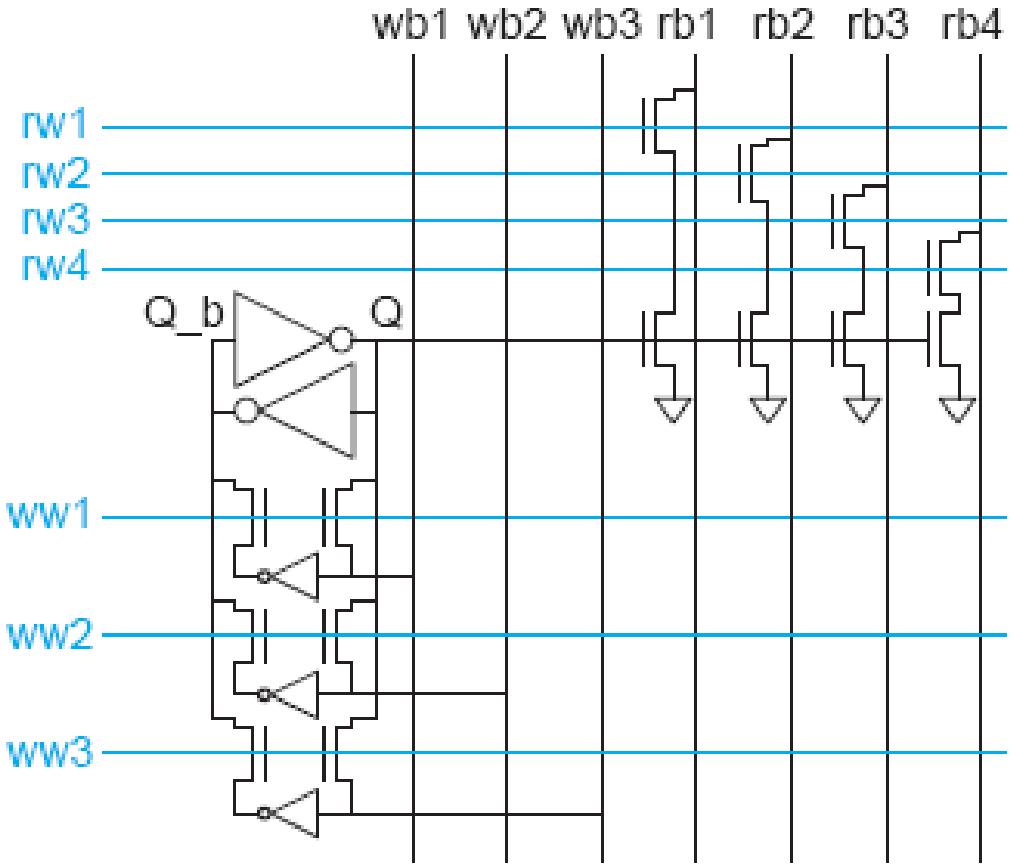


- Do two reads and one write by time multiplexing
  - Read during ph1, write during ph2

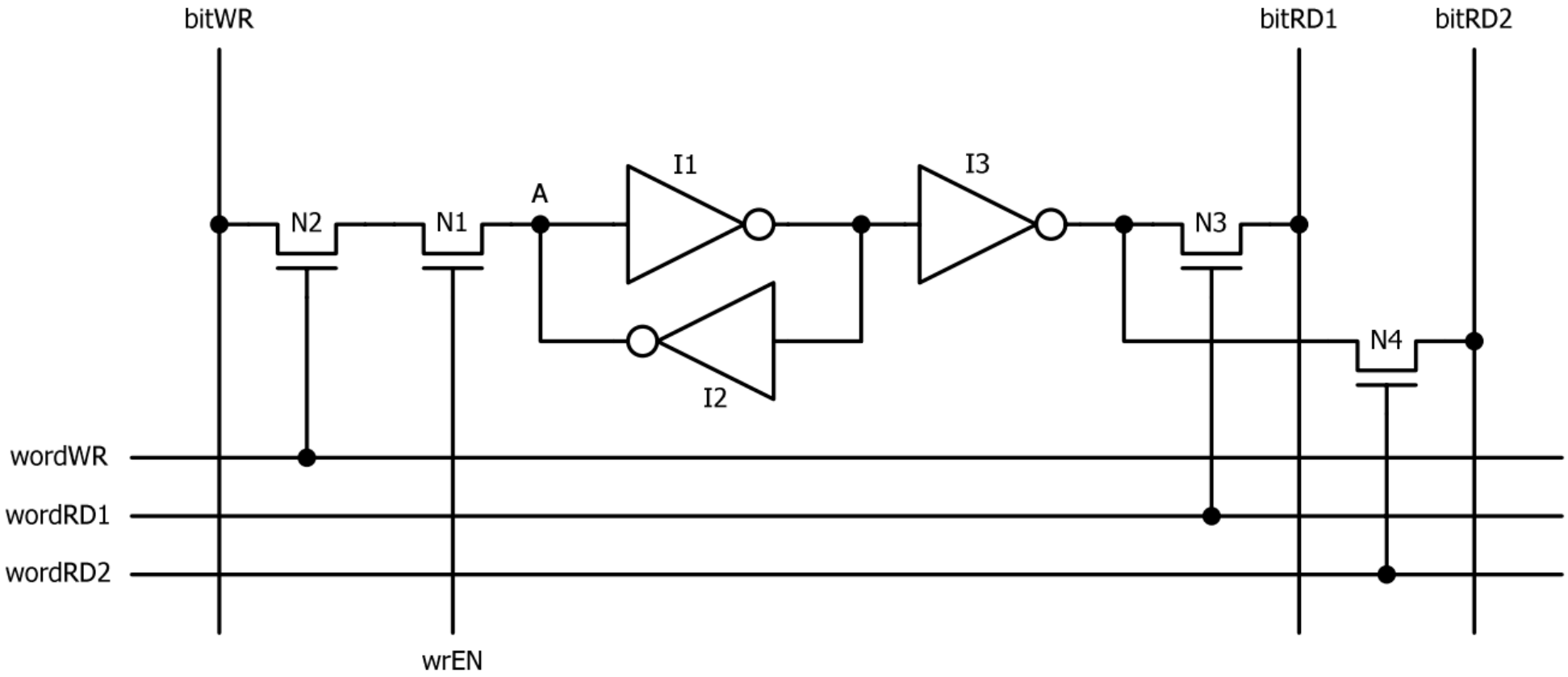
Multi-Ported SRAM

- Adding more access transistors hurts read stability
- Multiported SRAM isolates reads from state node
- Single-ended bitlines save area



Register File Cell

- Single-ended 2-read/1-write ports (Slow-write)

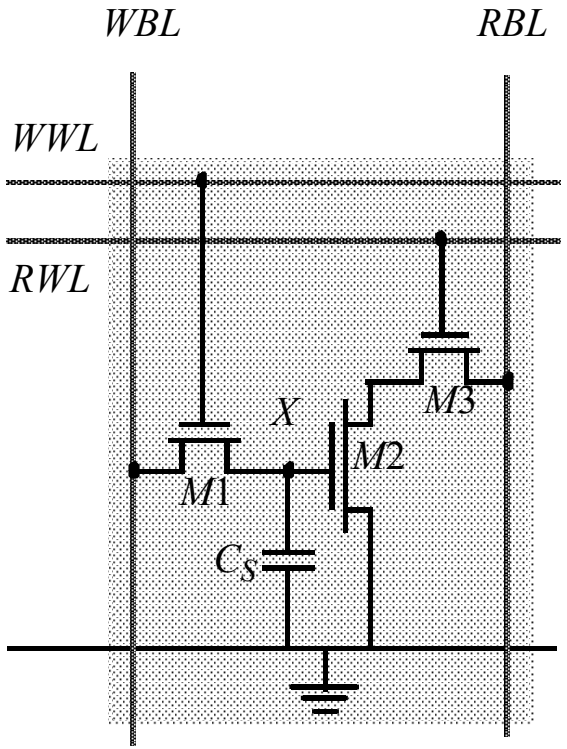


DRAM

- Smaller than SRAM
- Require data refresh to compensate for leakage

3-Transistor DRAM Cell (preclass 4)

- Cell is inverting on read operation



3-Transistor DRAM Cell

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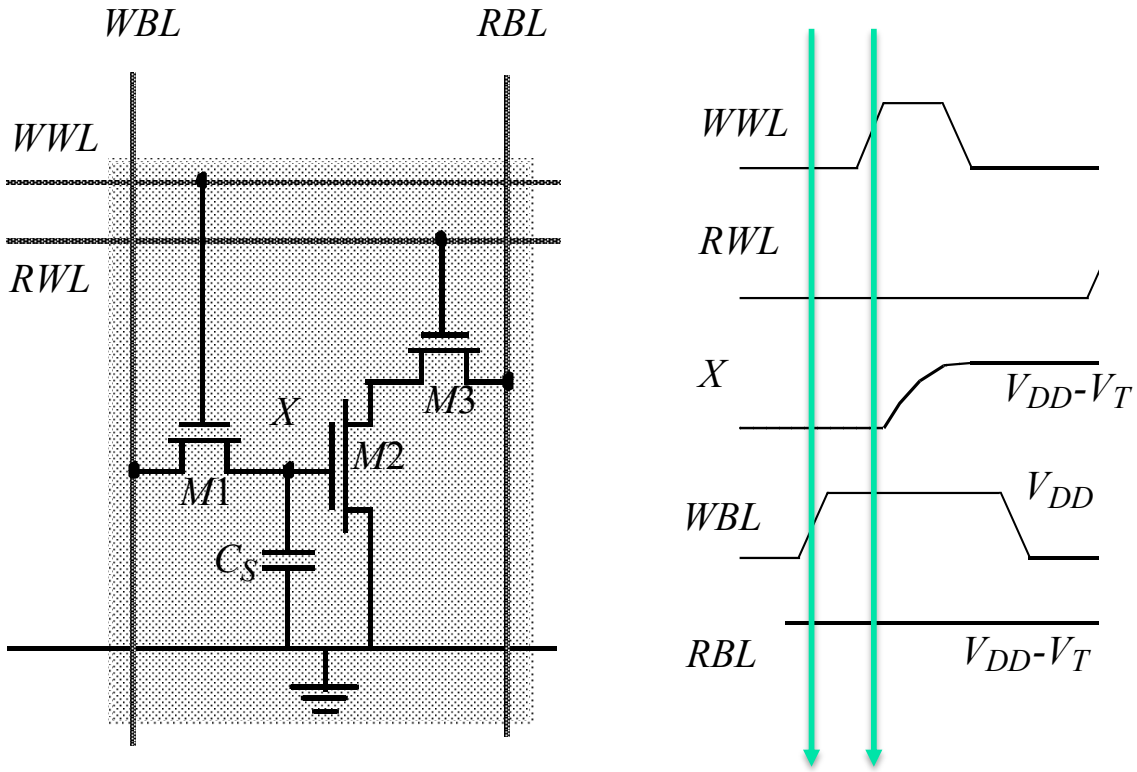

3-Transistor DRAM Cell

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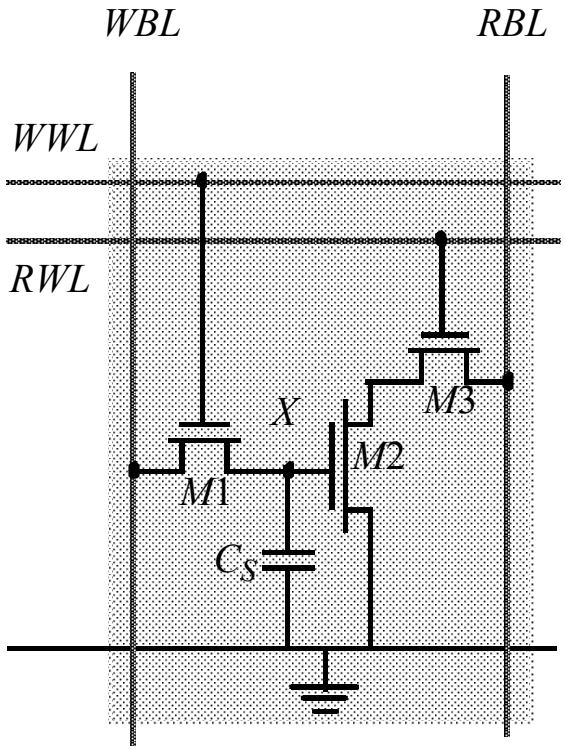
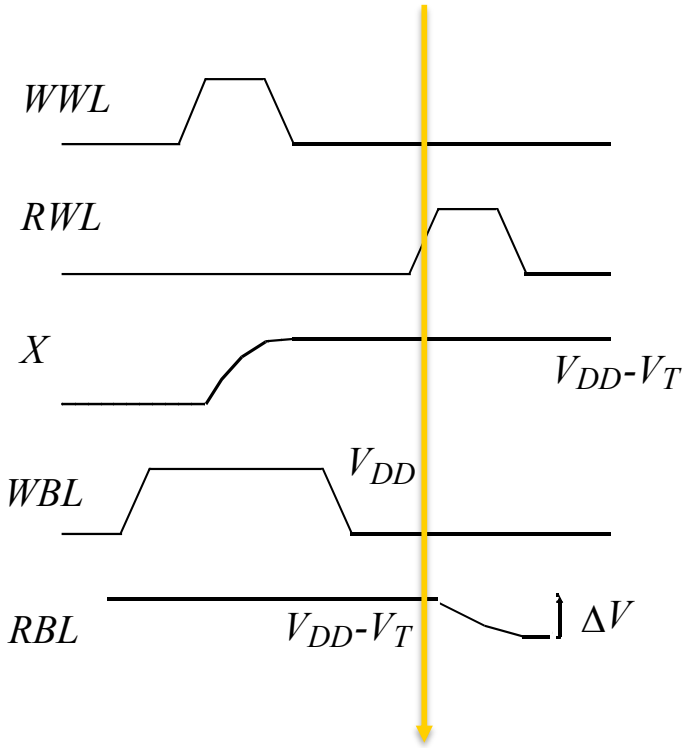
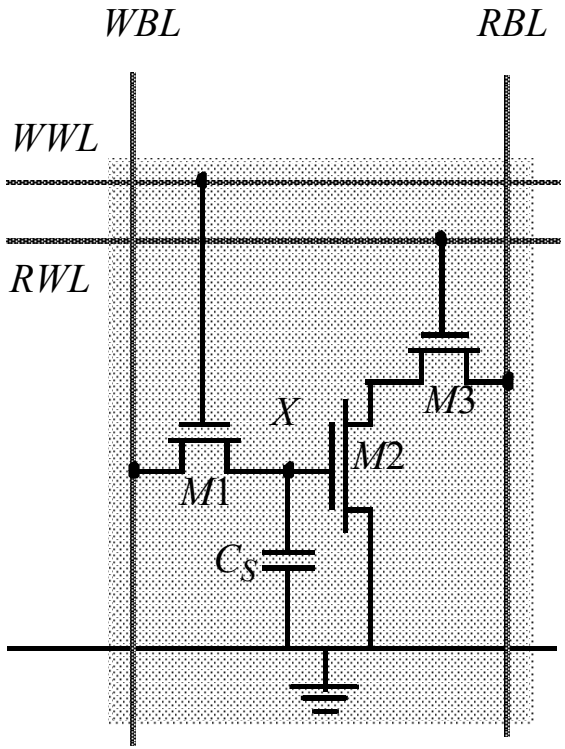
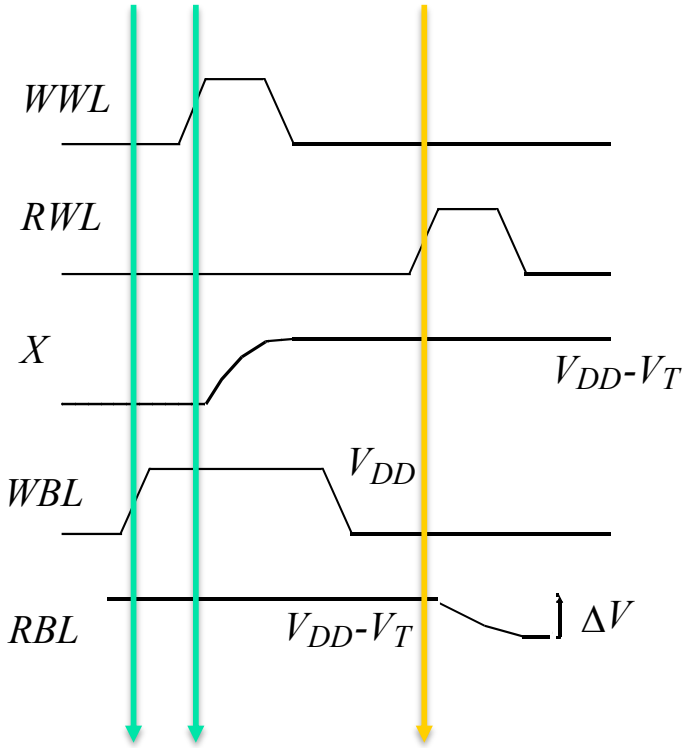




3-Transistor DRAM Cell

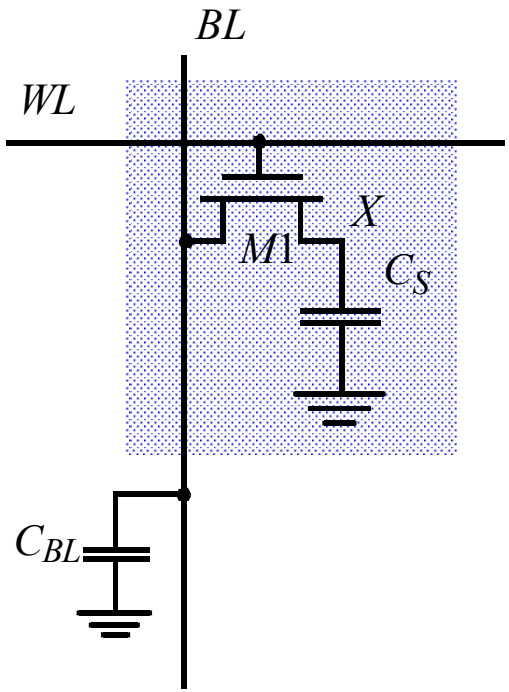
- Cell is inverting on read operation



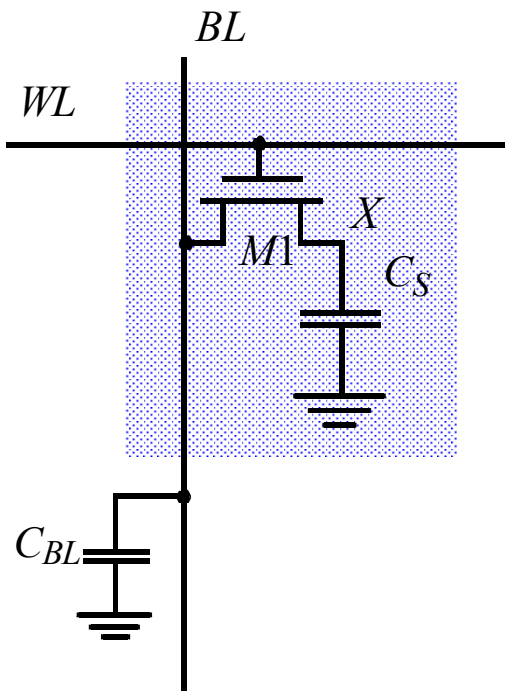


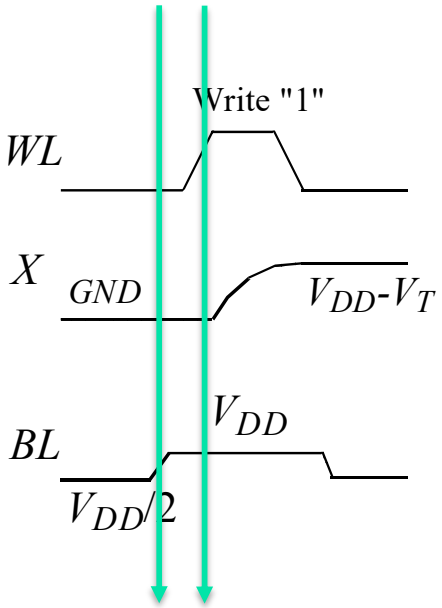
- No constraints on device ratios
- Reads are non-destructive
- Data stored has a V_T drop
  - When storing a 1, value at X = V_{WWL}-V_{Tn}

1-Transistor DRAM Cell (preclass 5)



1-Transistor DRAM Cell





Write: C_S is charged or discharged by asserting WL and BL.

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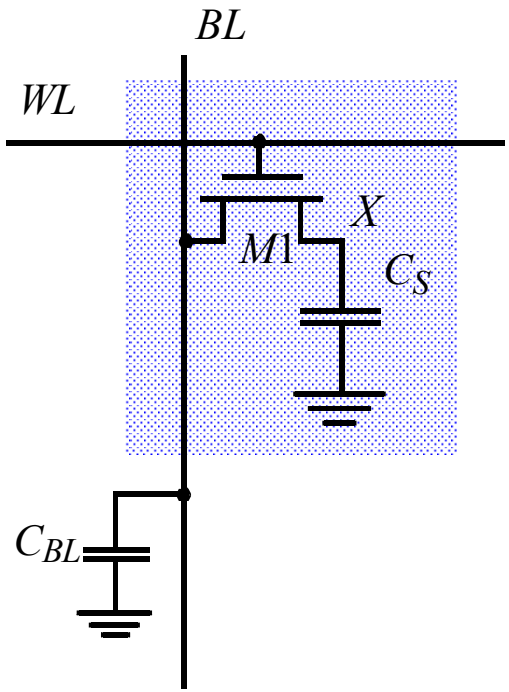

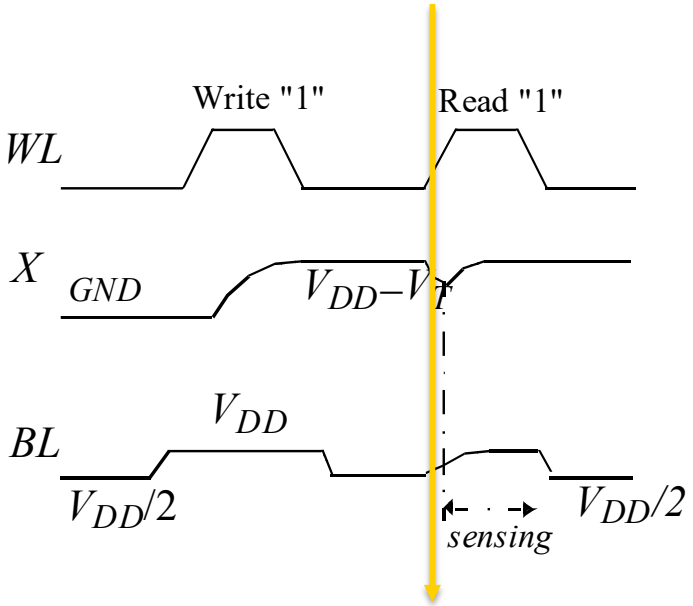

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Read: Charge redistribution takes places between bit line and storage capacitance

$$\Delta V = V_{BL} - V_{PRE} = (V_{BIT} - V_{PRE})\frac{C_S}{C_S + C_{BL}}$$

Voltage swing is small; typically around 250 mV.

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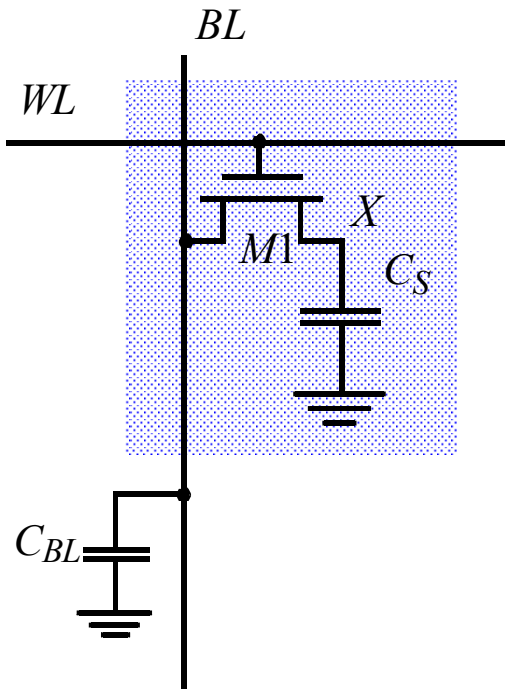

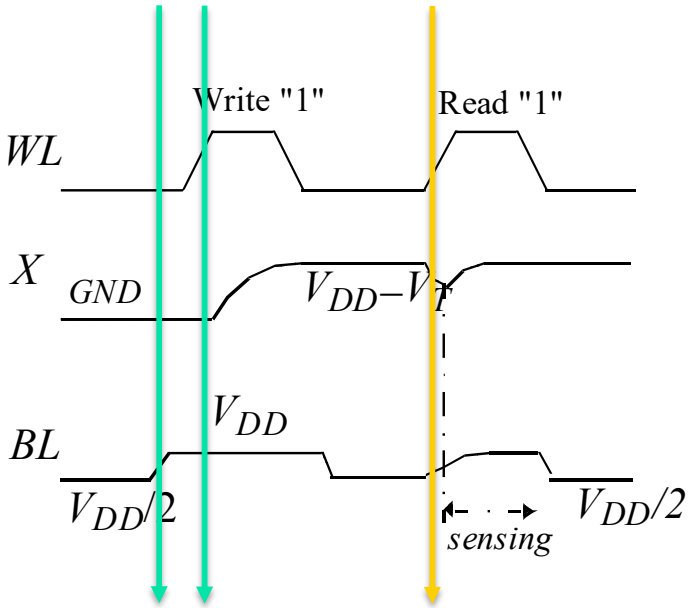

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DRAM Cell Observations

- 1T DRAM requires a sense amplifier for each bit line, due to charge redistribution read-out
- DRAM memory cells are single ended in contrast to SRAM cells
- The read-out of the 1T DRAM cell is destructive; read and refresh operation are necessary for correct operation
- Unlike 3T cell, 1T cell requires presence of an extra capacitance that must be explicitly included in the design
- When writing a "1" into a DRAM cell, a threshold voltage is lost. This loss can be circumvented by bootstrapping the word lines to a higher value than V_{DD}.

Idea

- Minimize area of repeated cell
  - 6T/5T SRAM
  - Mulitport trade off area for function
  - 1T/3T DRAM helps but slower
- Compensate with periphery
  - Decoders
  - Bitline (column) drivers
  - Sensing/Amplification (regeneration/restoration)

Admin

- Project 2 out
  - Milestone due Monday 11/22
    - I will give feedback by Wed (night) 11/24
  - Final report due 12/3