

ESE370: Circuit-Level Modeling, Design, and Optimization for Digital Systems

Lec 2: September 3, 2021
Transistor Introduction and
Gates from Transistors



Today

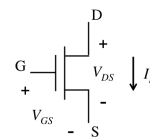
- Transistors – MOSFET
 - Model
- Zero-th order transistor model
 - Good enough for [what?]
- How to construct static CMOS gates
 - Gate function identification (preclass)
 - CMOS gate structure
 - Pullup/pulldown networks

Transistor

- Electrical switch to conduct electricity
 - Instead of physically connecting conducting materials to conduct electricity, apply a voltage to conduct



MOSFET



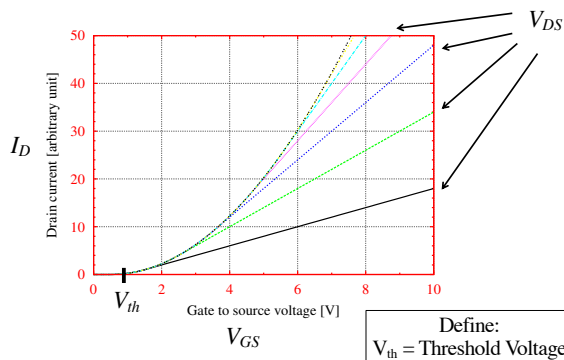
$$V_{GS} = V_G - V_S$$

$$V_{DS} = V_D - V_S$$

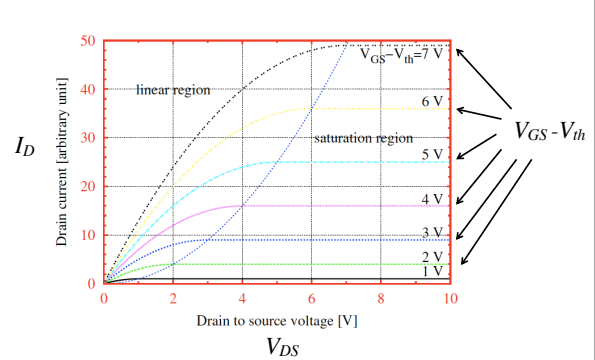
$$I_D = f(V_{DS}, V_{GS})$$

- Metal Oxide Semiconductor Field Effect Transistor
 - Primary **active** component for the term
 - Three terminal device
 - Voltage at gate controls conduction between two other terminals (source, drain)

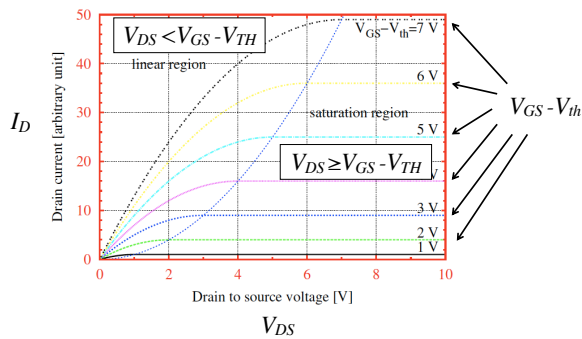
MOSFET – IV Characteristics



MOSFET – IV Characteristics



MOSFET – IV Characteristics

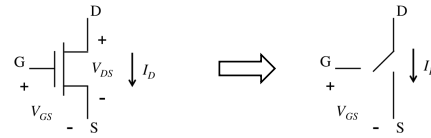


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MOSFET – Zeroeth Order Model



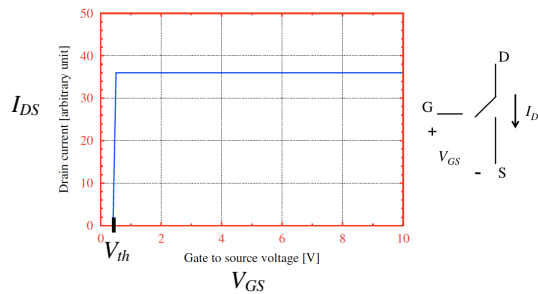
- Ideal Switch
 - $V_{GS} > V_{th} \rightarrow$ switch is closed, conducts
 - $V_{GS} < V_{th} \rightarrow$ switch is open, does not conduct
- Gate draws no current from input
 - Loads input capacitively (gate capacitance)

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MOSFET – Zeroeth Order Model



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MOSFET - Symmetric

- Switch turned on for positive V_{GS}
 - Which side is drain or source?



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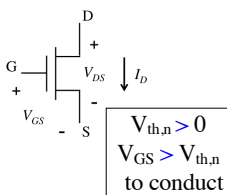
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MOSFET – N-Type

- Switch turned on for positive V_{GS}

$$V_D > V_S$$



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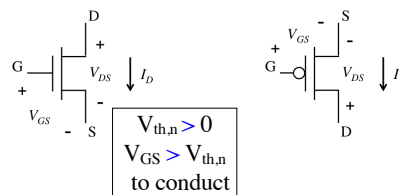
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MOSFET – N-Type, P-Type

- Switch turned on for positive V_{GS}
- Switch turned on for negative V_{GS}

$$V_D > V_S$$

$$V_S > V_D$$



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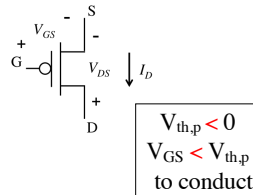
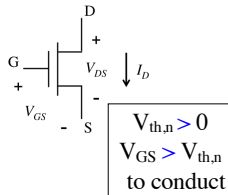
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MOSFET – N-Type, P-Type

- Switch turned on for positive V_{GS}
- Switch turned on for negative V_{GS}

$$V_D > V_S$$

$$V_S > V_D$$



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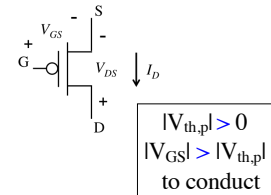
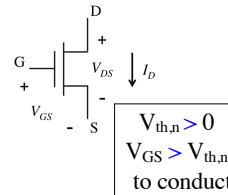
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MOSFET – N-Type, P-Type

- Switch turned on for positive V_{GS}
- Switch turned on for negative V_{GS}

$$V_D > V_S$$

$$V_S > V_D$$



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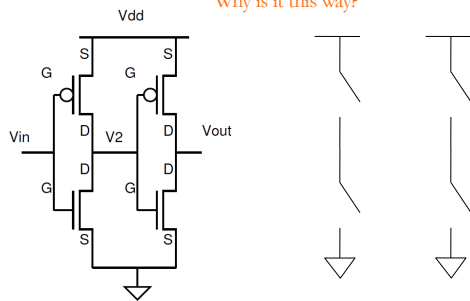
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Apply zero-order model

Note S, D annotation on this slide (won't be labeled in future)

Why is it this way?



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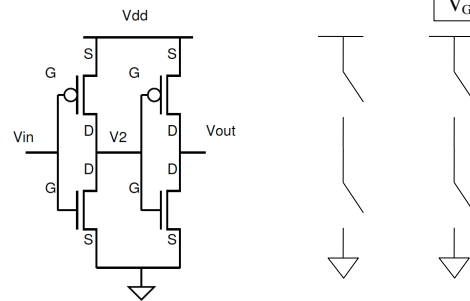
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Apply zero-order model?

What happens when $V_{in} = V_{dd} > V_{thn}$?

$$V_{th,p} = -V_{th,n}$$

$$V_{GS} = V_G - V_S$$



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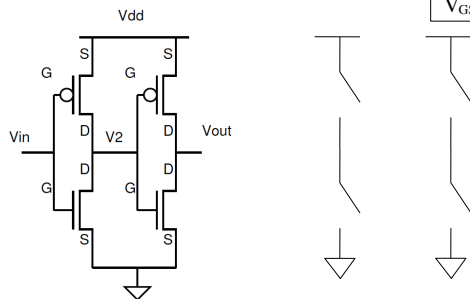
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Apply zero-order model?

What happens when $V_{in} = 0$?

$$V_{th,p} = -V_{th,n}$$

$$V_{GS} = V_G - V_S$$



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Convince yourself that $V_{out} = 0$.

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Zeroeth Order Model

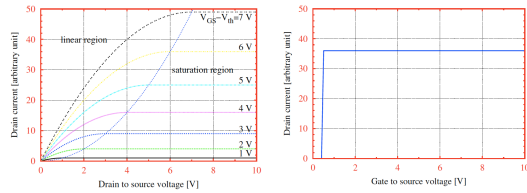
- Allows us to reason (mostly) at logic level about steady-state functionality of typical gate circuits before worrying about performance (speed, power, etc.) details

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What is missing in Zeroeth Order Model?



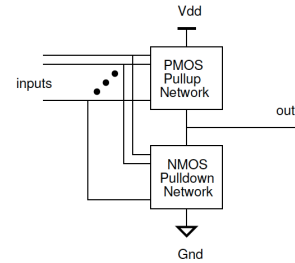
- Delay
 - Parasitic capacitances and resistances
- Dynamics
- Zeroeth Order captures behaviour if our circuit is **not**:
 - Capacitively loaded, acyclic (if there are Loops), rail-to-rail drive

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How to construct static CMOS gates



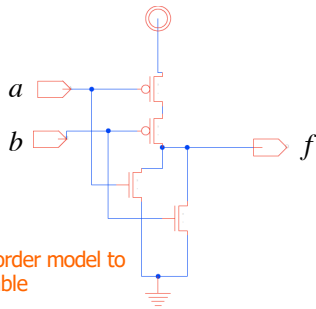
- Complementary Metal Oxide Semiconductor

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What gate is this? Preclass 1



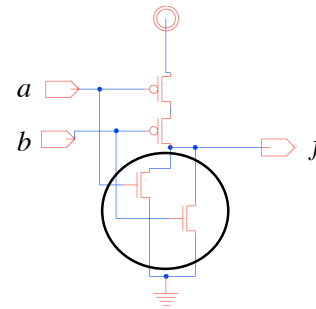
Hint: use zero order model to make a truth table

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What gate is this?

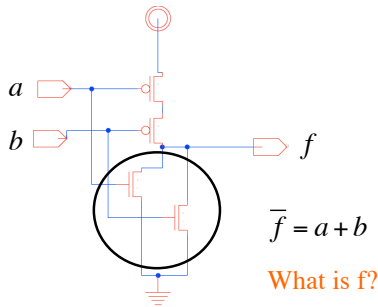


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What gate is this? Preclass 2



$$\bar{f} = a + b$$

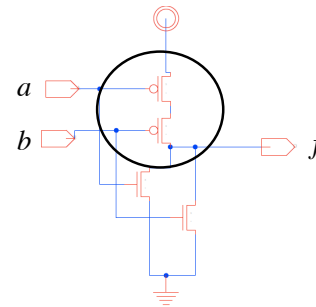
What is f?

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What gate is this?

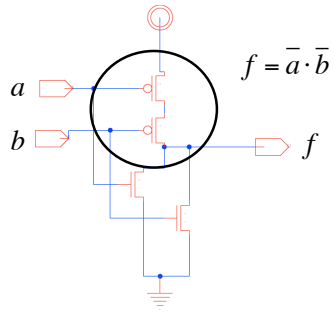


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What gate is this?

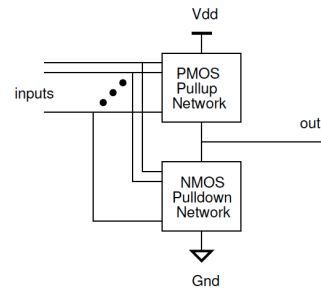


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Static CMOS Gate Structure

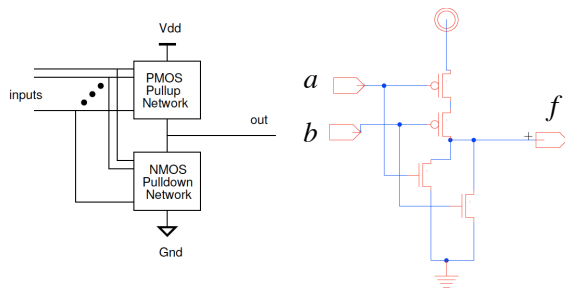


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Static CMOS Gate Structure



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CMOS

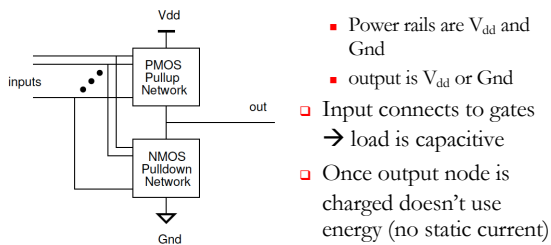
- Complementary Metal Oxide Semiconductor
- Uses *complementary* transistors
 - NMOS, PMOS
- Pull-down and pull-up networks are *complements* of each other
 - Only one network active (on) at a time to charge or discharge output to V_{dd} or Gnd respectively

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Static CMOS Gate Structure



- Drives rail-to-rail
 - Power rails are V_{dd} and Gnd
 - output is V_{dd} or Gnd
- Input connects to gates
 - load is capacitive
- Once output node is charged doesn't use energy (no static current)
- Output actively driven

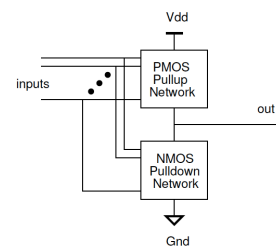
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Gate Design Example Preclass 3

- Design gate to perform: $f = (\bar{a} + \bar{b}) \cdot \bar{c}$
- Strategy:
 1. Use static CMOS structure
 2. Design PMOS pullup for f
 3. Use DeMorgan's Law to determine f'
 4. Design NMOS pulldown for f'



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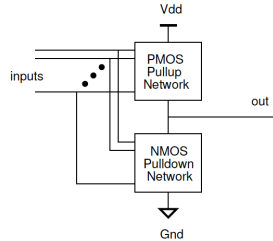
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Gate Design Example

□ Design gate to perform: $f = (\bar{a} + \bar{b}) \cdot \bar{c}$

□ PMOS Pullup for f '



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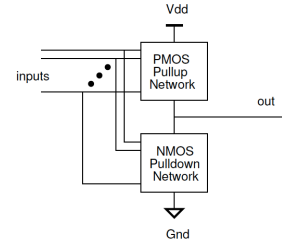
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Gate Design Example

□ Design gate to perform: $f = (\bar{a} + \bar{b}) \cdot \bar{c}$

□ What is f' ?

■ DeMorgan's Law



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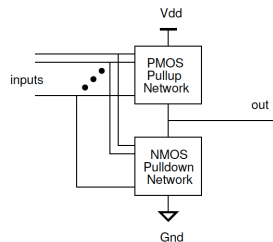
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Gate Design Example

□ Design gate to perform: $f = (\bar{a} + \bar{b}) \cdot \bar{c}$

□ Design NMOS pulldown for f'



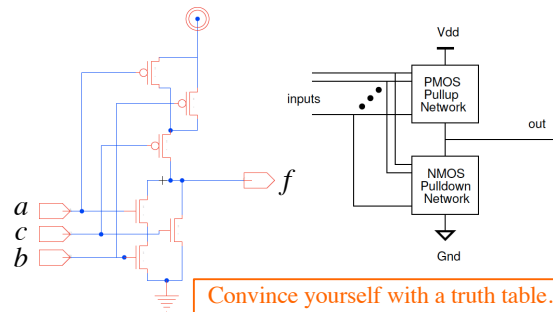
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Gate Design Example

□ Design gate to perform: $f = (\bar{a} + \bar{b}) \cdot \bar{c}$



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Big Idea

- MOSFET Transistor as switch
- Functionality-driven simplified modeling (Zero order)
 - Aid reasoning
 - Sanity check
 - Simplify design

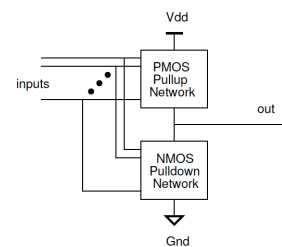
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Big Idea

- Systematic construction of any gate from transistors
 1. Use static CMOS structure
 2. Design PMOS pullup for f
 3. Use DeMorgan's Law to determine f'
 4. Design NMOS pulldown for f'



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Admin

- ❑ Access Survey – due tomorrow night for credit
- ❑ Diagnostic – due Tuesday
- ❑ HW 1 out – due 9/14
 - Will take time to learn Electric CAD tool, start early
- ❑ No class on Monday
- ❑ Wednesday – no lecture, Lab in Ketterer
- ❑ Friday regular lecture in Towne 307