ESE370: Circuit-Level Modeling, Design, and Optimization for Digital Systems

Lec 3: September 10, 2021

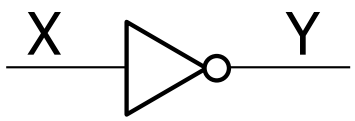
Transistor Introduction (first order)

Today

- Basic Digital Gates
- Boolean Logic
  - Basic Algebra
    - DeMorgan's Law
  - Minimum Sum of Products/K-maps
- Cascading Gates
- Transistor first order model
  - For performance estimates (i.e propagation delay!)
  - There are always Rs and Cs!

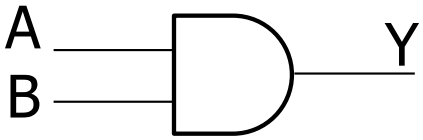
Basic Digital Gates

NOT
$Y = \overline{X}$



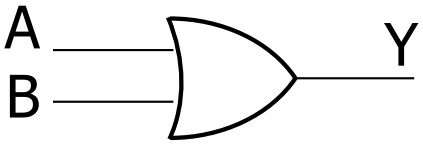
X	Y
0	1
1	0

AND
$Y = A \bullet B$



A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

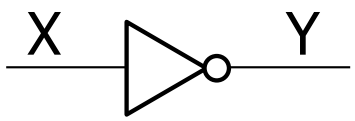
OR
$Y = A + B$



A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

Basic Digital Gates

NOT
$Y = \overline{X}$



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1	0

AND
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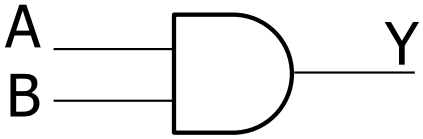
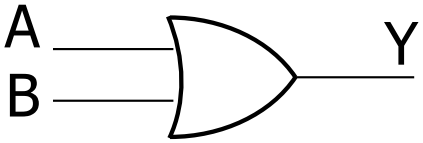


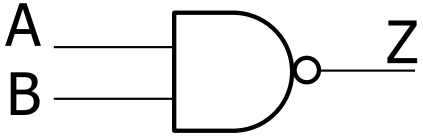
A	B	Y	Z
0	0	0	1
0	1	0	1
1	0	0	1
1	1	1	0

OR
$Y = A + B$

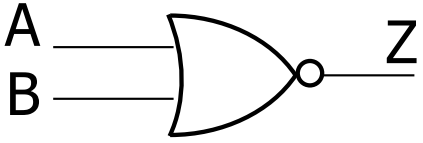


A	B	Y	Z
0	0	0	1
0	1	1	0
1	0	1	0
1	1	1	0

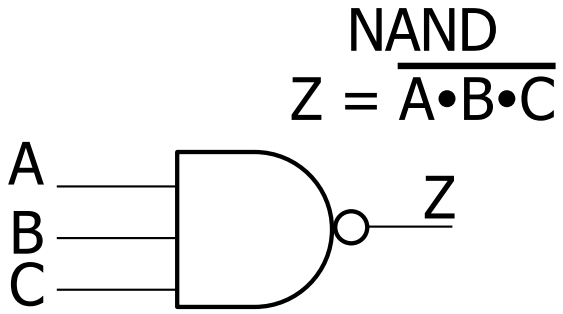
NAND
$Z = \overline{A \bullet B}$



NOR
$Z = \overline{A + B}$



Basic Digital Gates



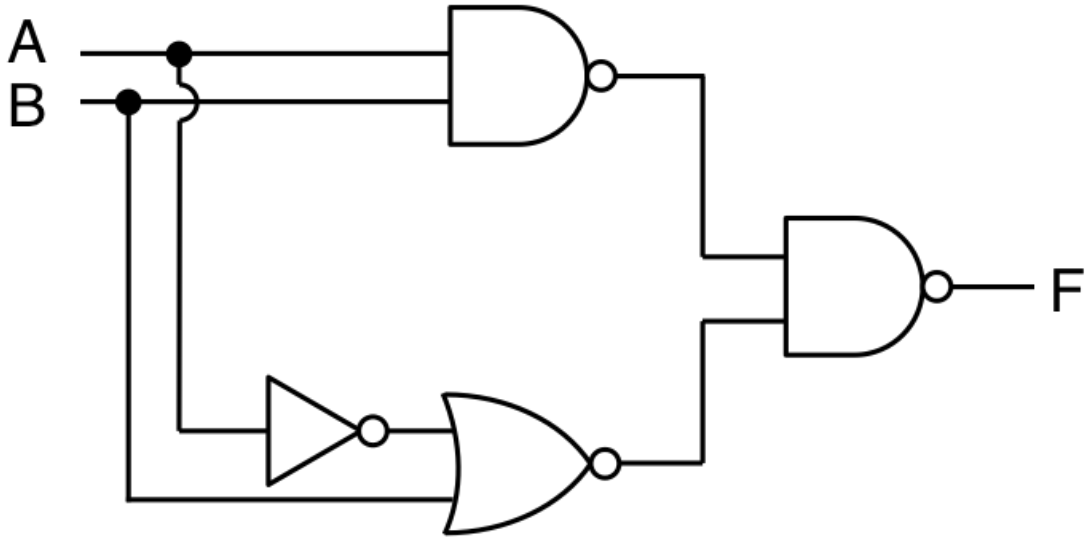
A	B	C	Z
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

Boolean Algebra

TABLE 2-3
Basic Identities of Boolean Algebra

1.	$X+0=X$	2.	$X\cdot 1=X$	
3.	$X+1=1$	4.	$X\cdot 0=0$	
5.	$X+X=X$	6.	$X\cdot X=X$	
7.	$X+\overline{X}=1$	8.	$X\cdot\overline{X}=0$	
9.	$\overline{\overline{X}}=X$			
10.	$X+Y=Y+X$	11.	$XY=YX$	Commutative
12.	$X+(Y+Z)=(X+Y)+Z$	13.	$X(YZ)=(XY)Z$	Associative
14.	$X(Y+Z)=XY+XZ$	15.	$X+YZ=(X+Y)(X+Z)$	Distributive
16.	$\overline{X+Y}=\overline{X}\cdot\overline{Y}$	17.	$\overline{X\cdot Y}=\overline{X}+\overline{Y}$	DeMorgan's

Combination



Boolean Expressions

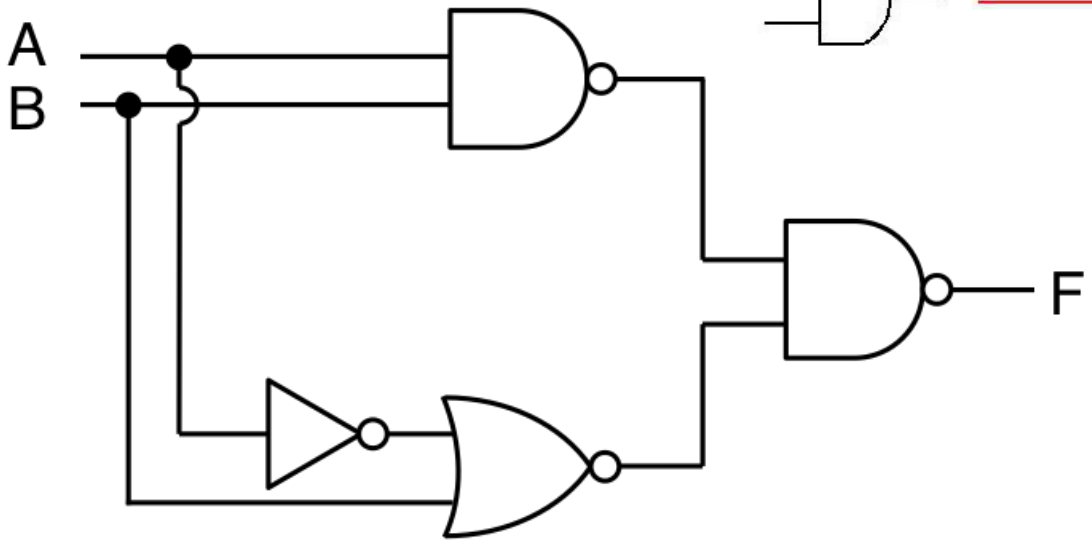
- Sum-of-products form (SOP)
  - Eg. ABC+DEF+GHI
- Product-of-sums form (POS)
  - Eg. (A+B+C)(D+E+F)(G+H+I)

- Convert between the two with Boolean algebra
  - DeMorgan's Law

$$A + B = \overline{\overline{A} \cdot \overline{B}}$$

$$A \cdot B = \overline{\overline{A} + \overline{B}}$$

Combination



Canonical Form

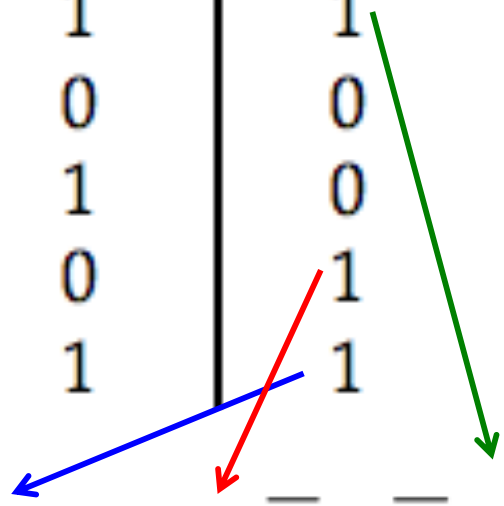
- Every minterm in your expression has every variable

Row Number	A	B	C	f
0	0	0	0	0
1	0	0	1	0
2	0	1	0	0
3	0	1	1	1
4	1	0	0	0
5	1	0	1	0
6	1	1	0	1
7	1	1	1	1

Canonical Form

- Every minterm in your expression has every variable

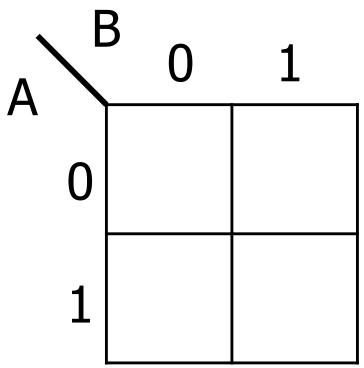
Row Number	A	B	C	f
0	0	0	0	0
1	0	0	1	0
2	0	1	0	0
3	0	1	1	1
4	1	0	0	0
5	1	0	1	0
6	1	1	0	1
7	1	1	1	1

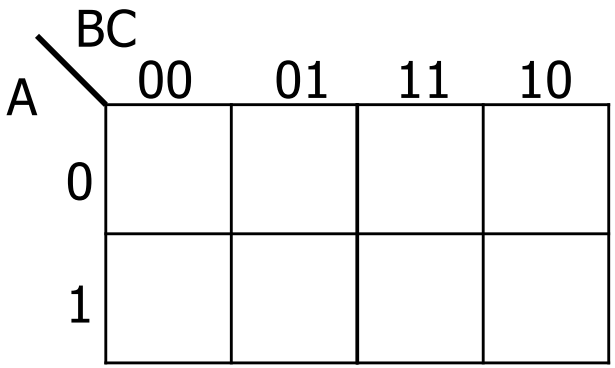


$$f(A,B,C) = A\bar{B}C + AB\bar{C} + \bar{A}BC$$

What is a K(arnaugh)-map?

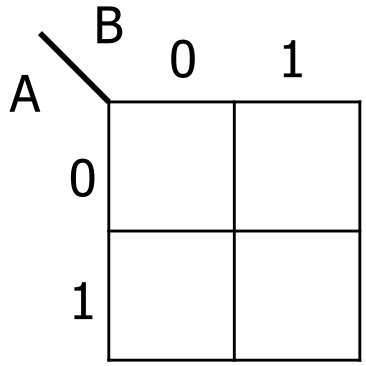
- A grid of squares (representing truth table)
- Each square represents one minterm
- The minterms are ordered according to Gray code
  - Only one variable changes between adjacent squares
- Squares on edges are considered adjacent to squares on opposite edges
  - I.e Table wraps around
- K-maps are clumsy with more than 4 variables





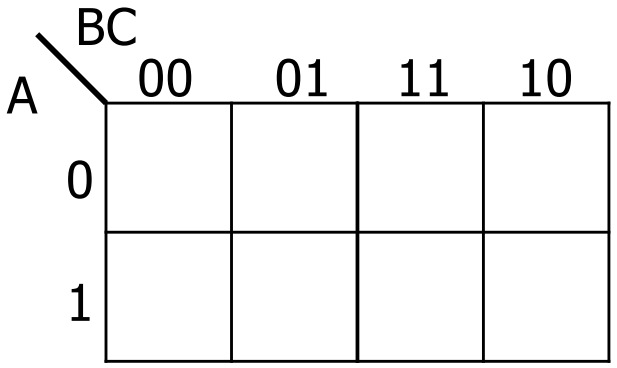
K-map Examples (Preclass 1)

- 2-variable



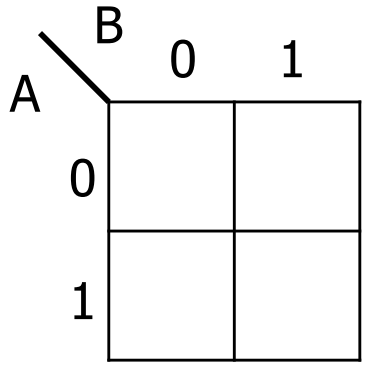
Eg: Z = A′B′ + AB′ + A′B

- 3-variable



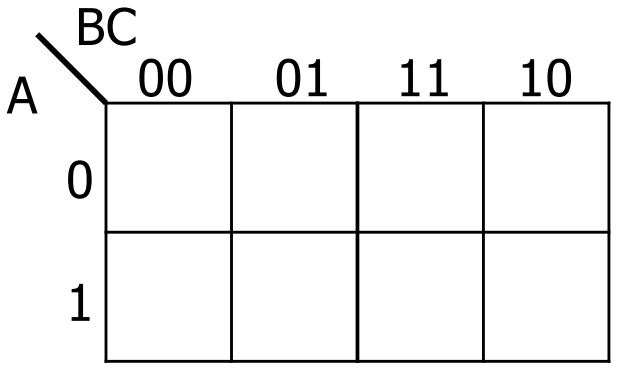
K-map Examples (Preclass 2)

- 2-variable



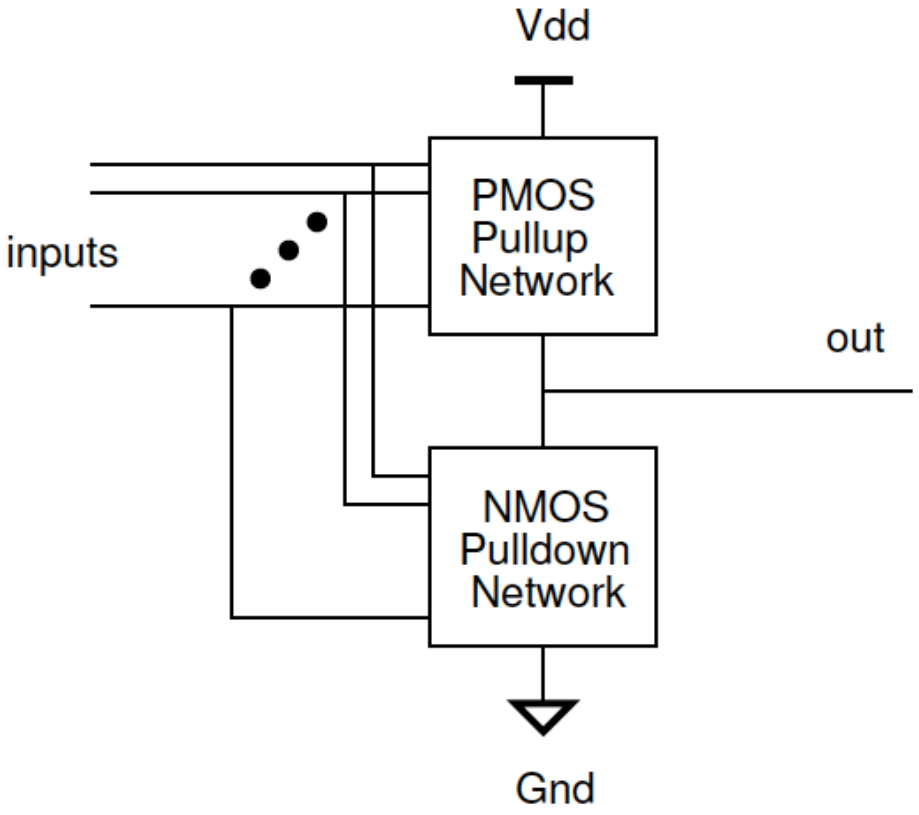
Eg: Z = A′B′ + AB′ + A′B

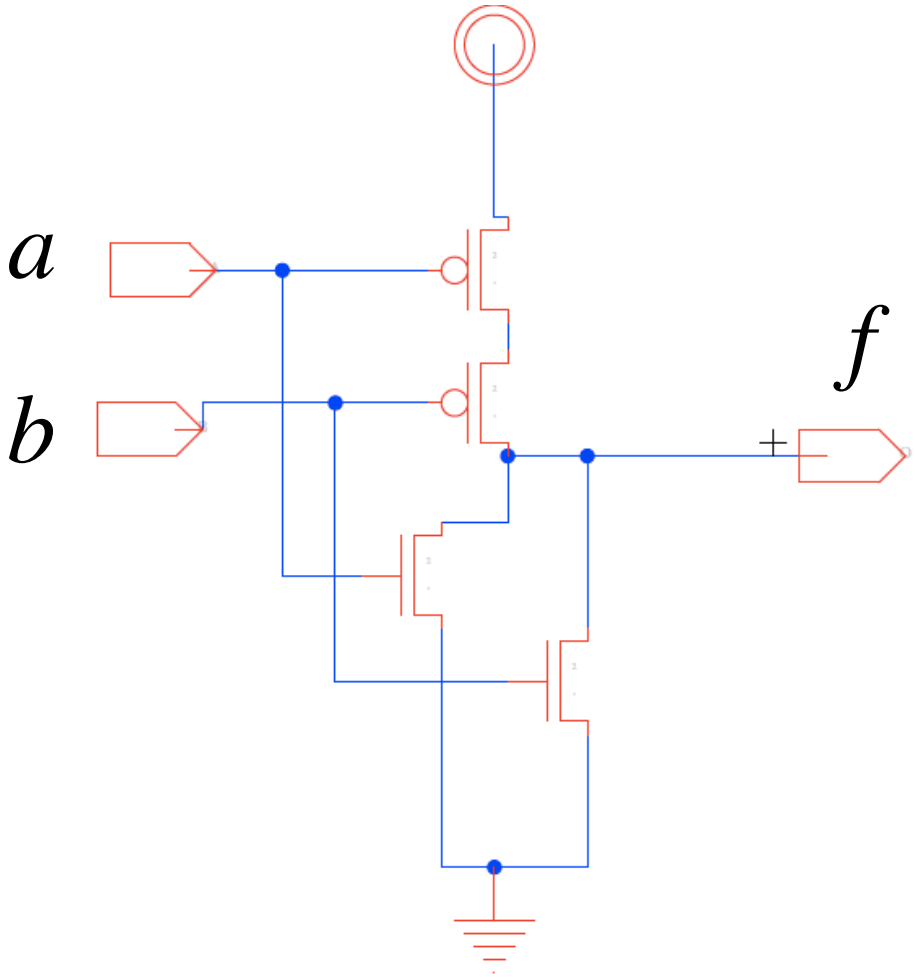
- 3-variable



Eg: Z = A′B′C′ + A′B + ABC′ + AC

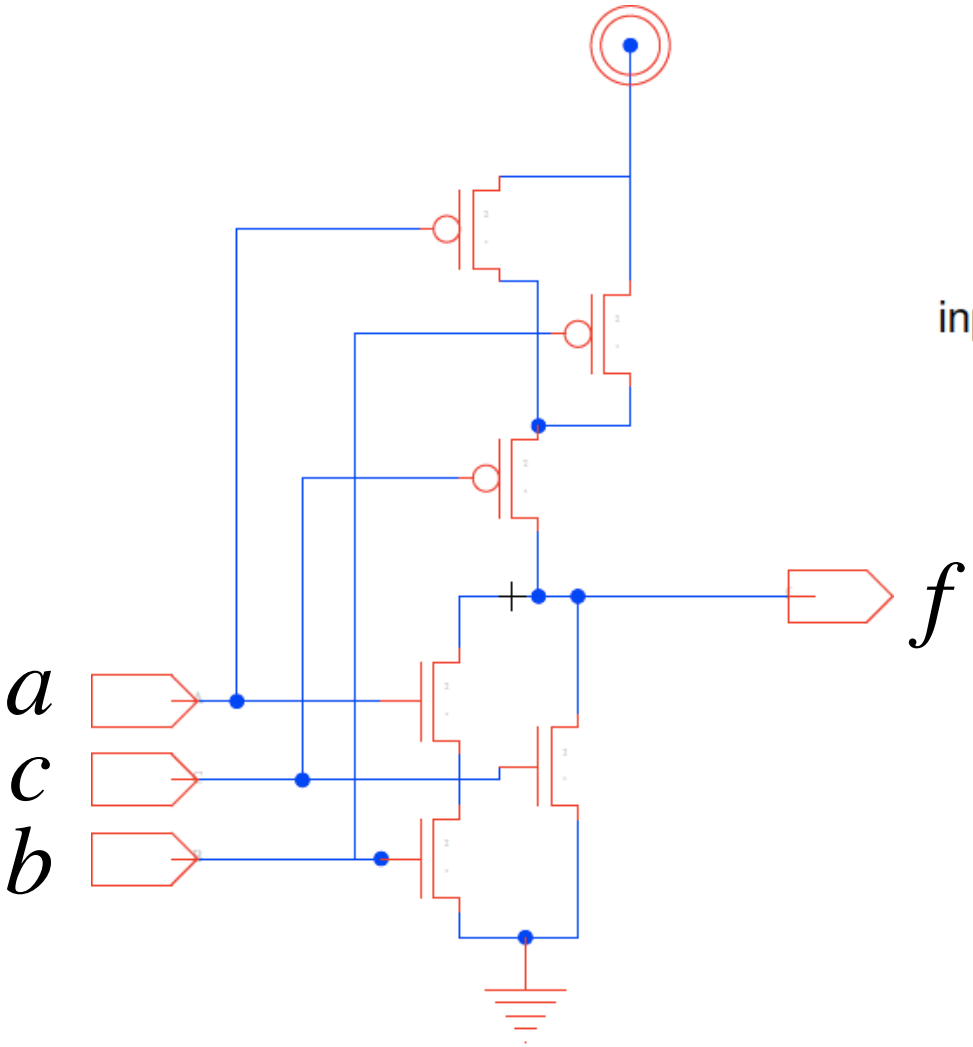
Static CMOS Gate Structure

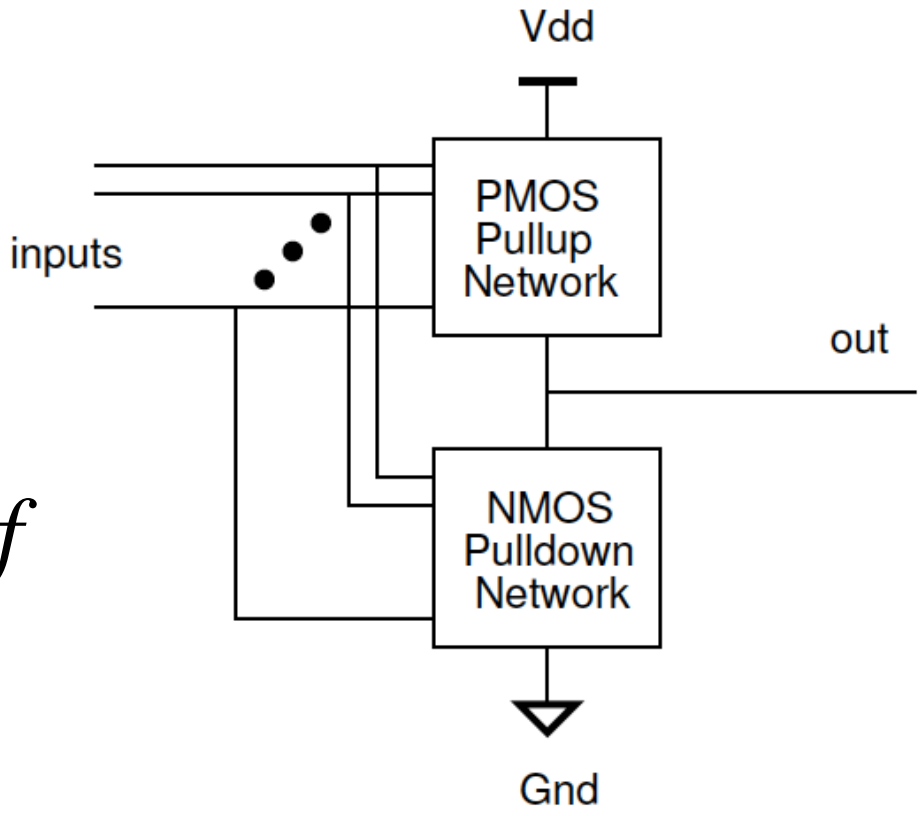




Gate Design Example

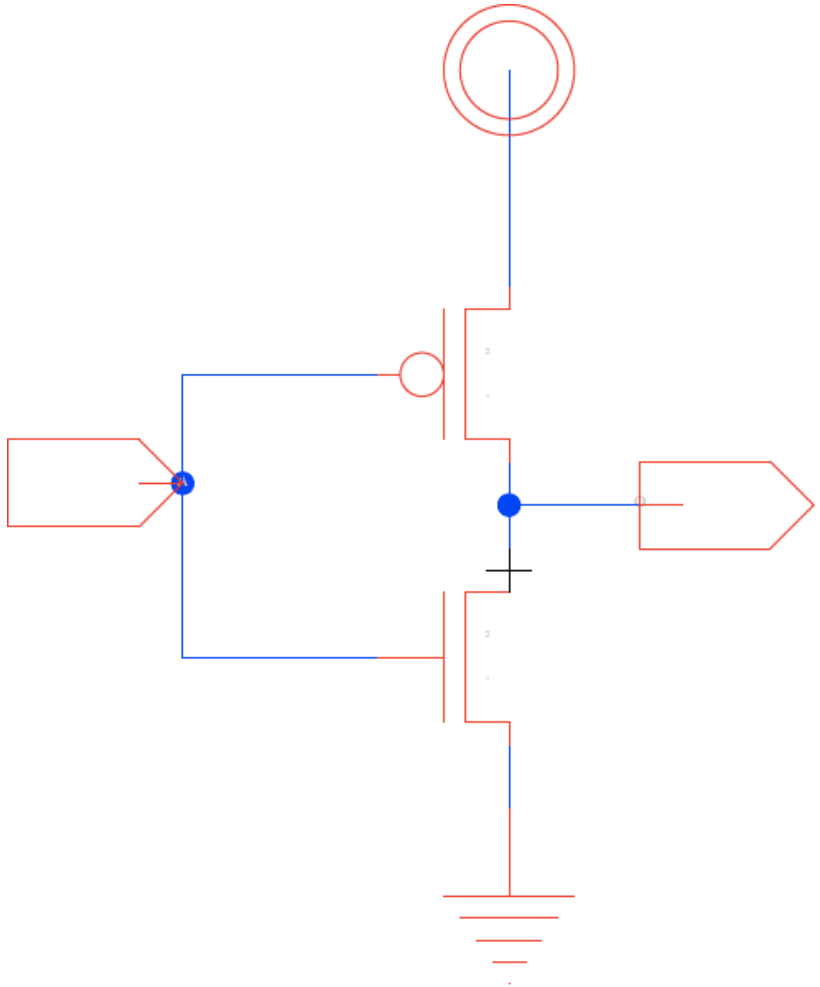
- Design gate to perform: $f = (\overline{a} + \overline{b}) \cdot \overline{c}$



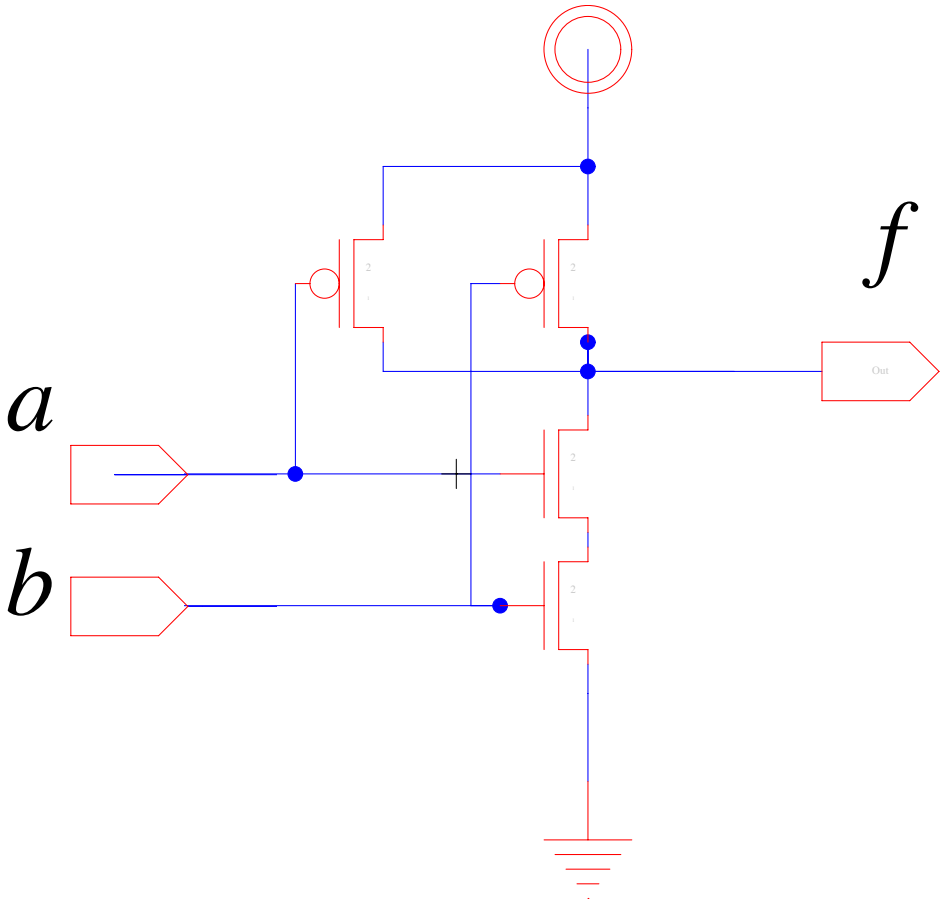


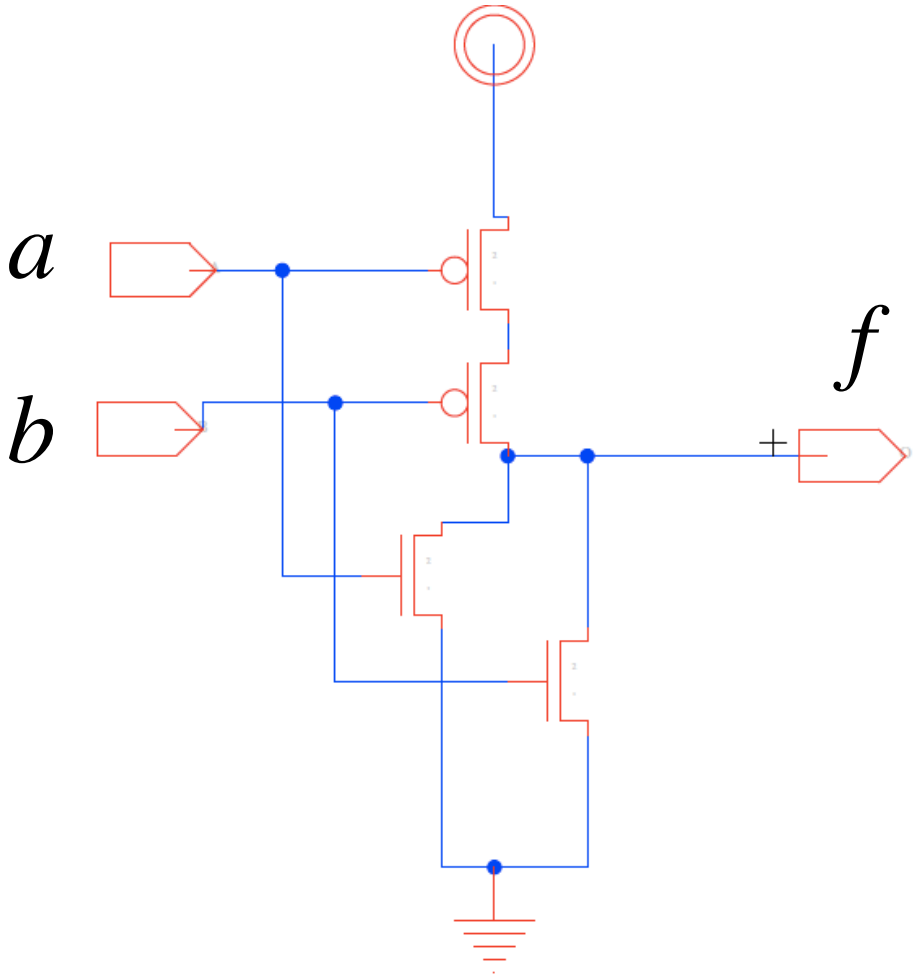
Inverting Stage

- Each stage of Static CMOS gate is inherently inverting



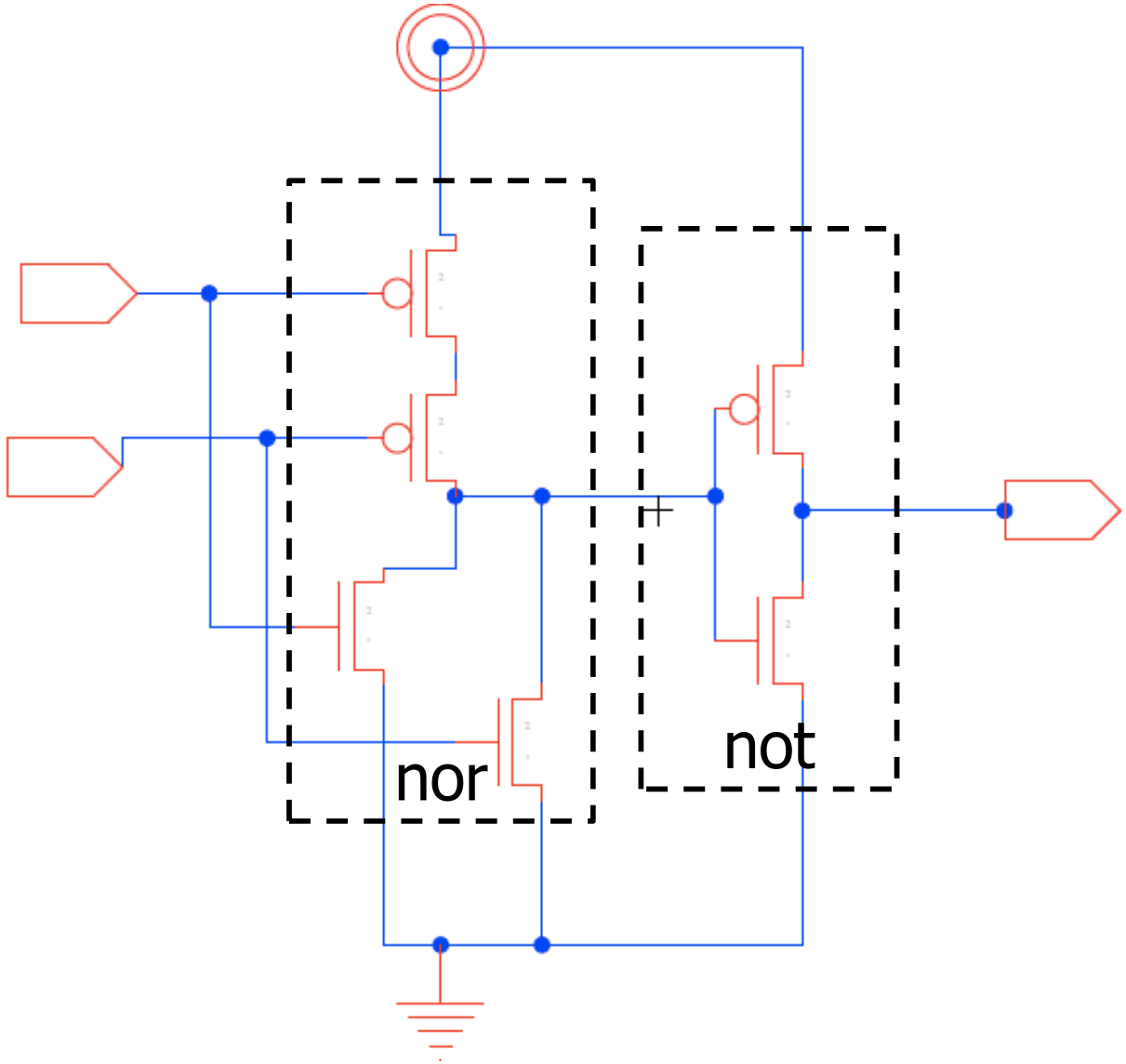
NAND/NOR Fundamental Gates





How implement OR?

How implement OR?



Cascading Stages

- Can always cascade "stages" to build more complex gates
- Could simply build nor2 or nand2 at circuit level and assemble arbitrary logic by combining – universality
  - but may not be smallest/fastest/least power

Implement: $f = a \cdot \bar{b}$

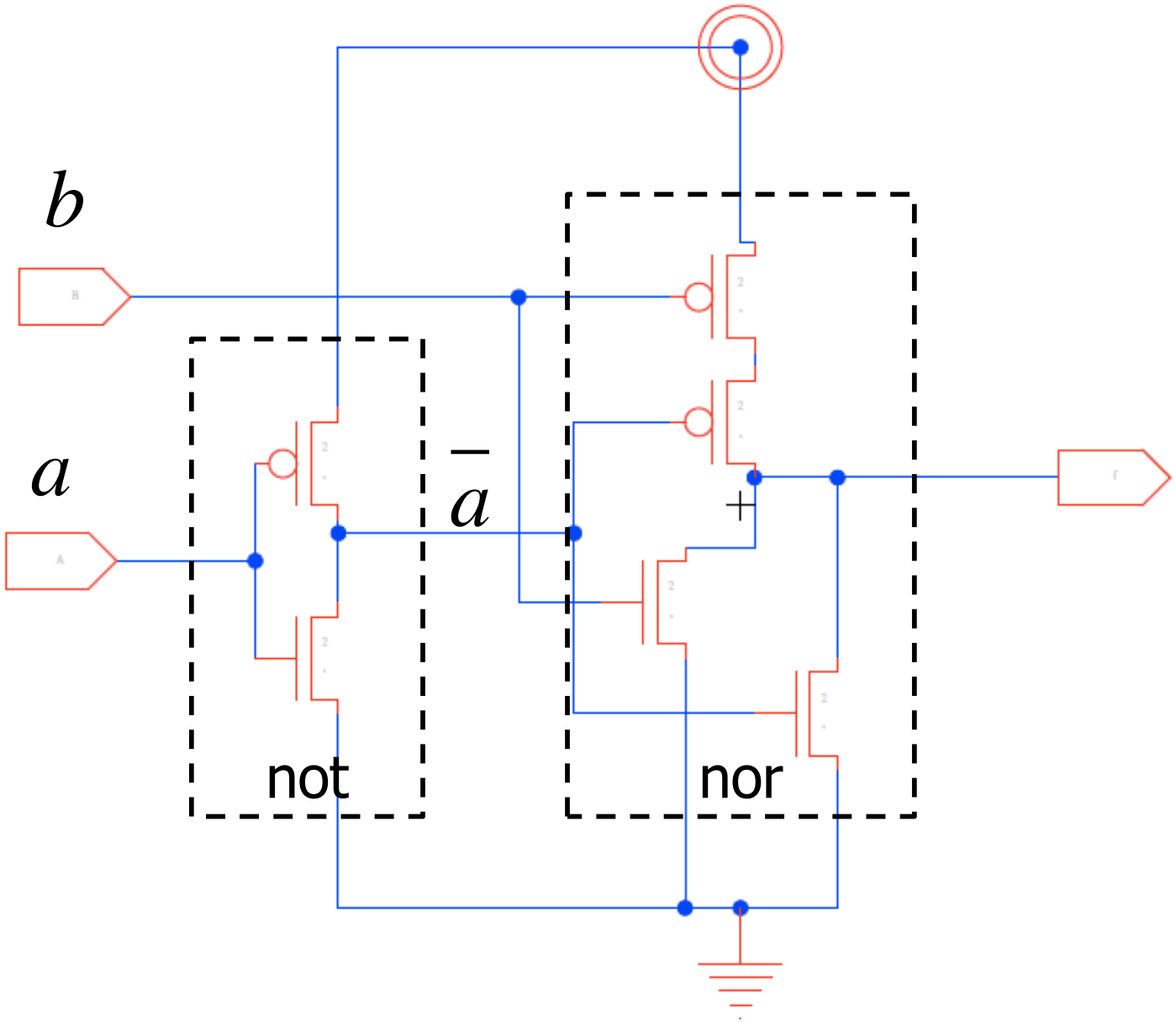
- Pullup?

- Pulldown?

Hint: use cascading stages

Implement: $f = a \cdot \bar{b}$

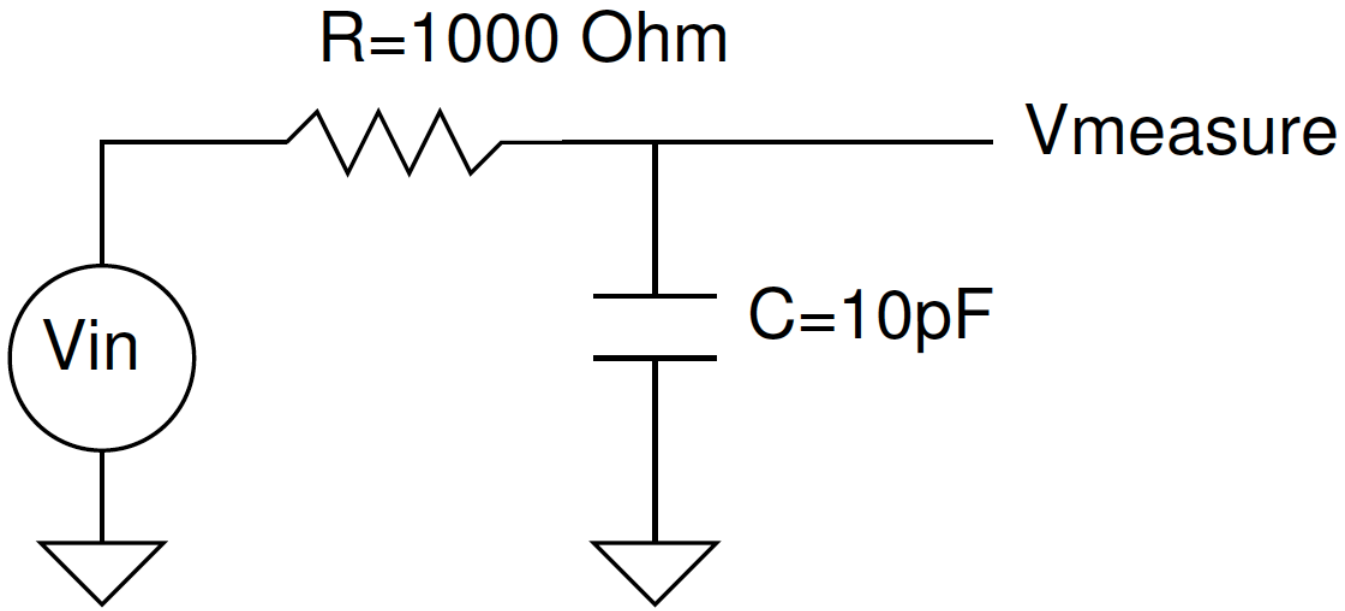
- Pullup?
- Pulldown?



Final Voltage? (Preclass 4)

Assume V_{in} is 0 for $t < 0$ and steps to 1V at $t = 0$.

What value does $V_{measure}$ take on as $t \to \infty$?



Final Voltage?

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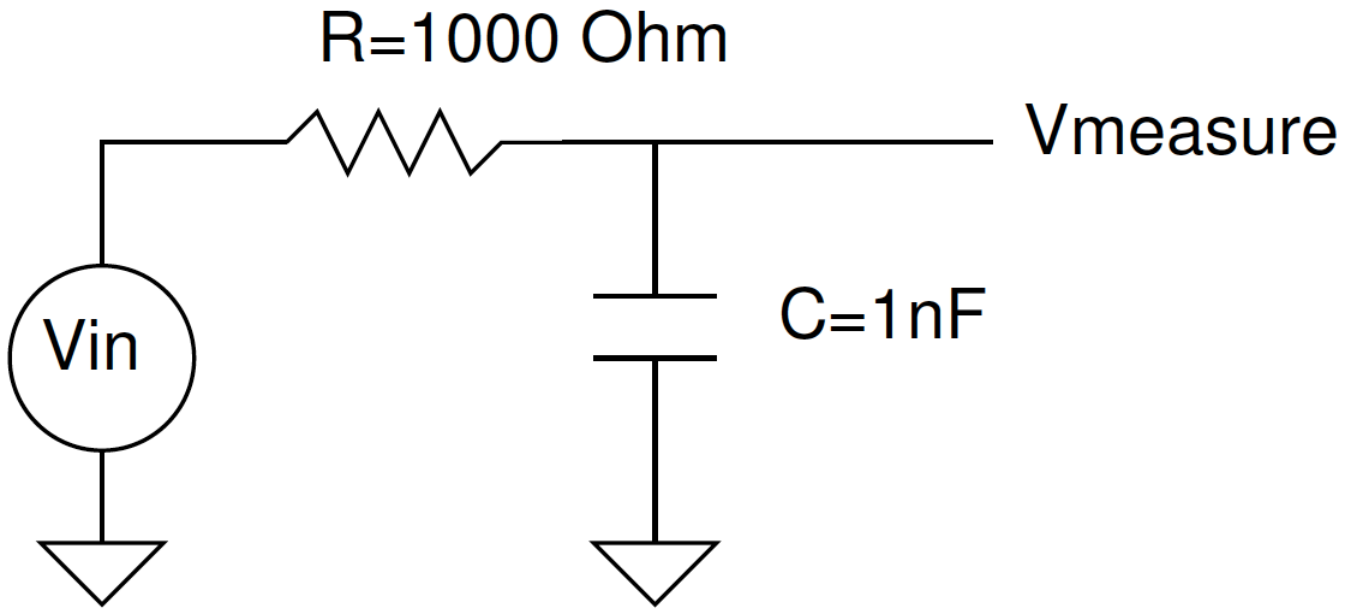
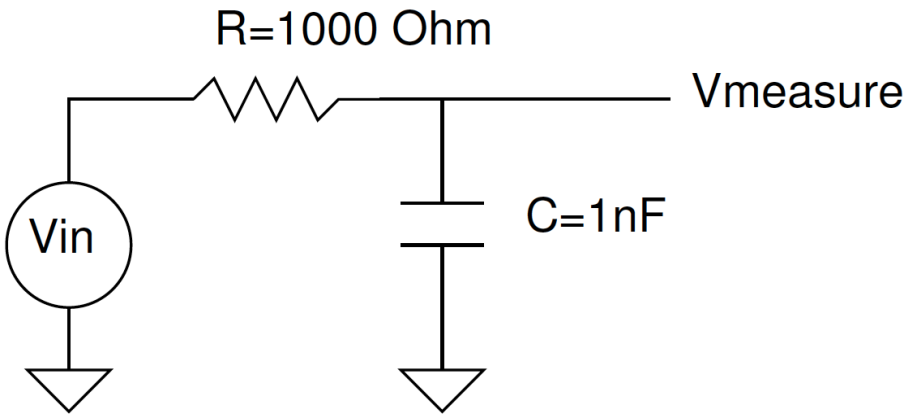
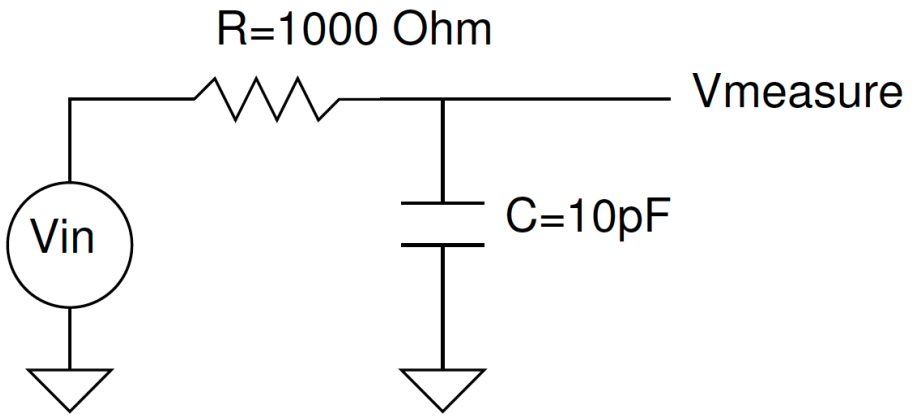


Final Voltage?

- Bonus question: Which one will settle faster?





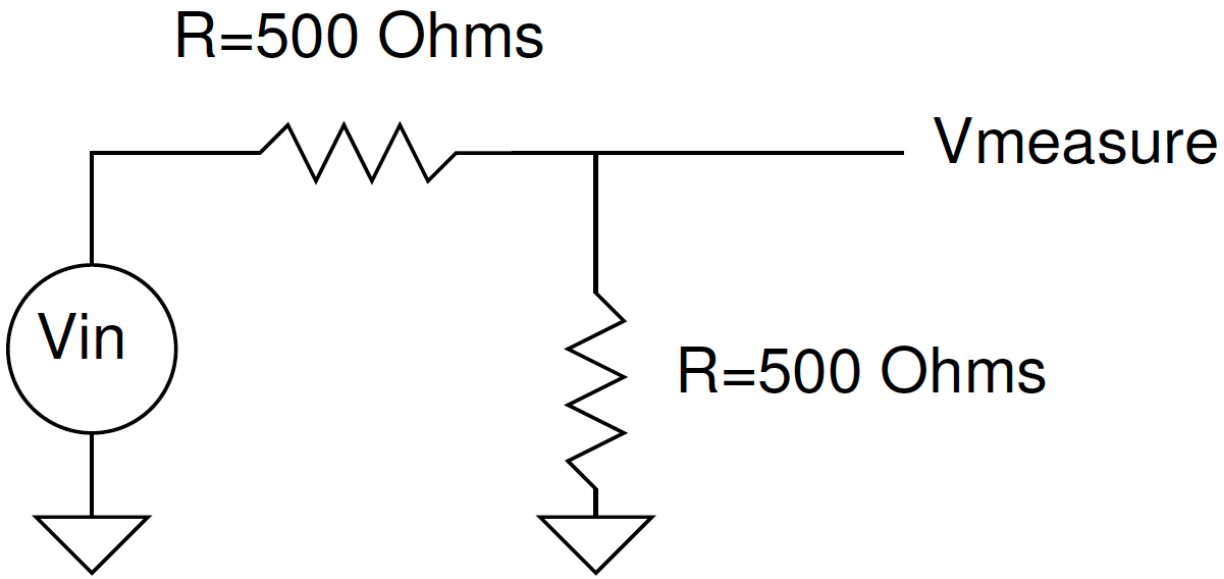
A

B

Final Voltage?

Assume V_{in} is 0 for $t < 0$ and steps to 1V at $t = 0$.

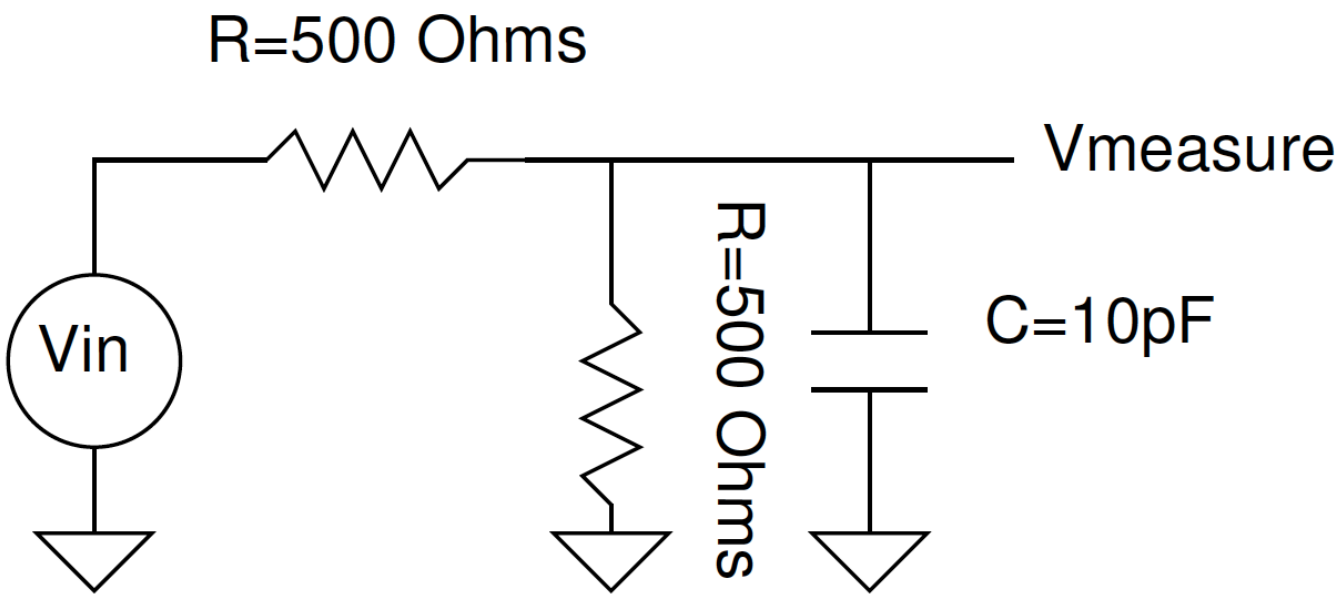
What value does $V_{measure}$ take on as $t \rightarrow \infty$?



Final Voltage?

Assume V_{in} is 0 for $t < 0$ and steps to 1V at $t = 0$.

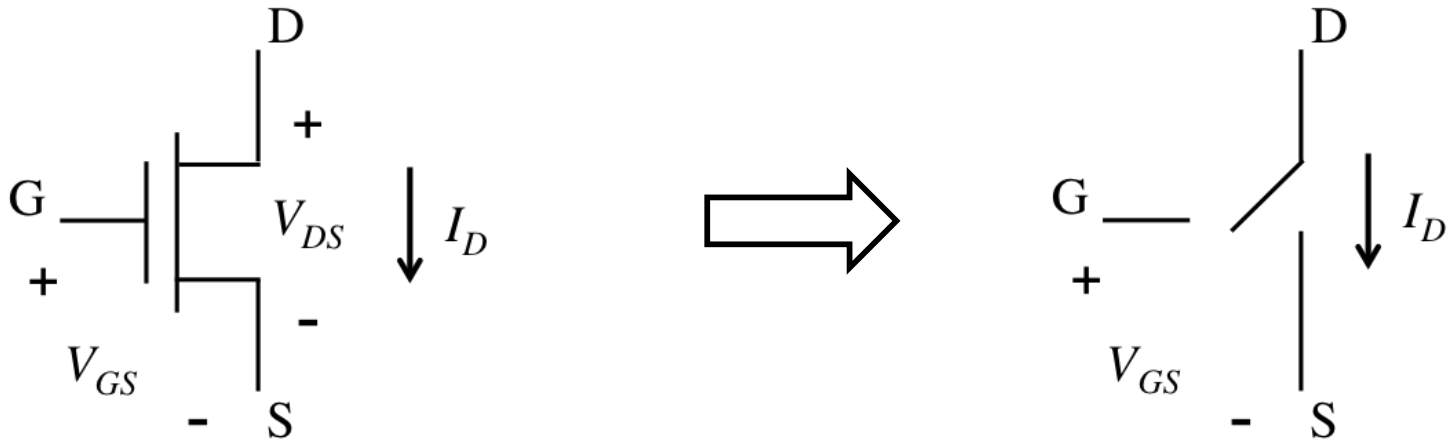
What value does $V_{measure}$ take on as $t \rightarrow \infty$?



Conclude?

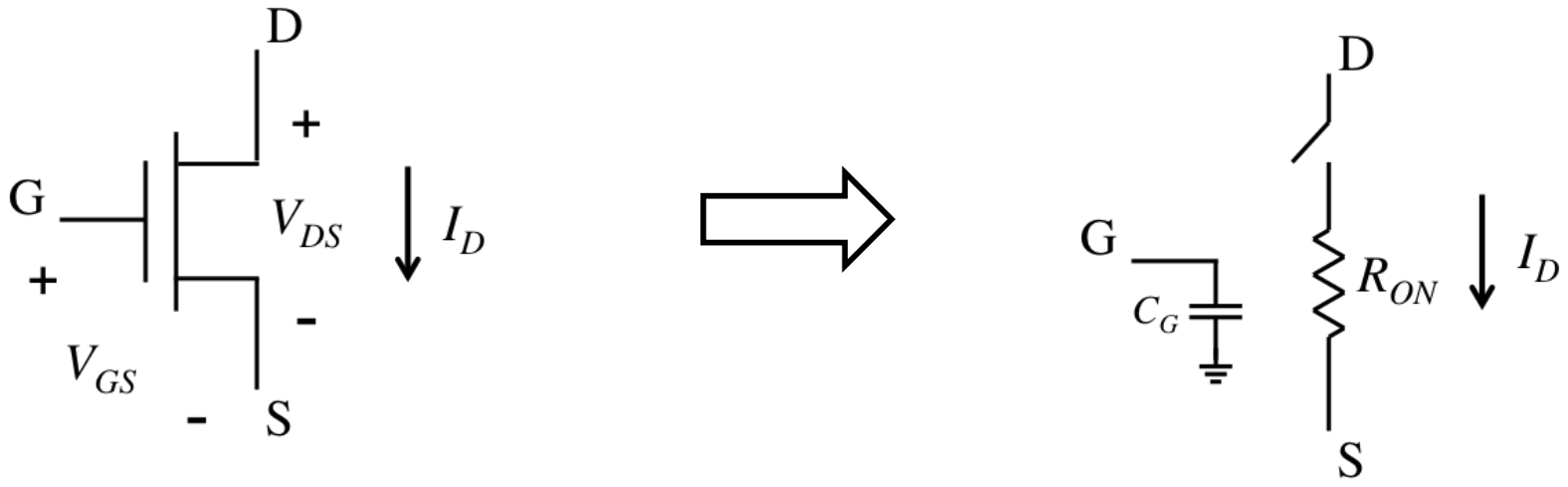
- DC/Steady-State
  - Ignore the capacitors
  - Look like "open circuit"

MOSFET – Zeroeth Order Model



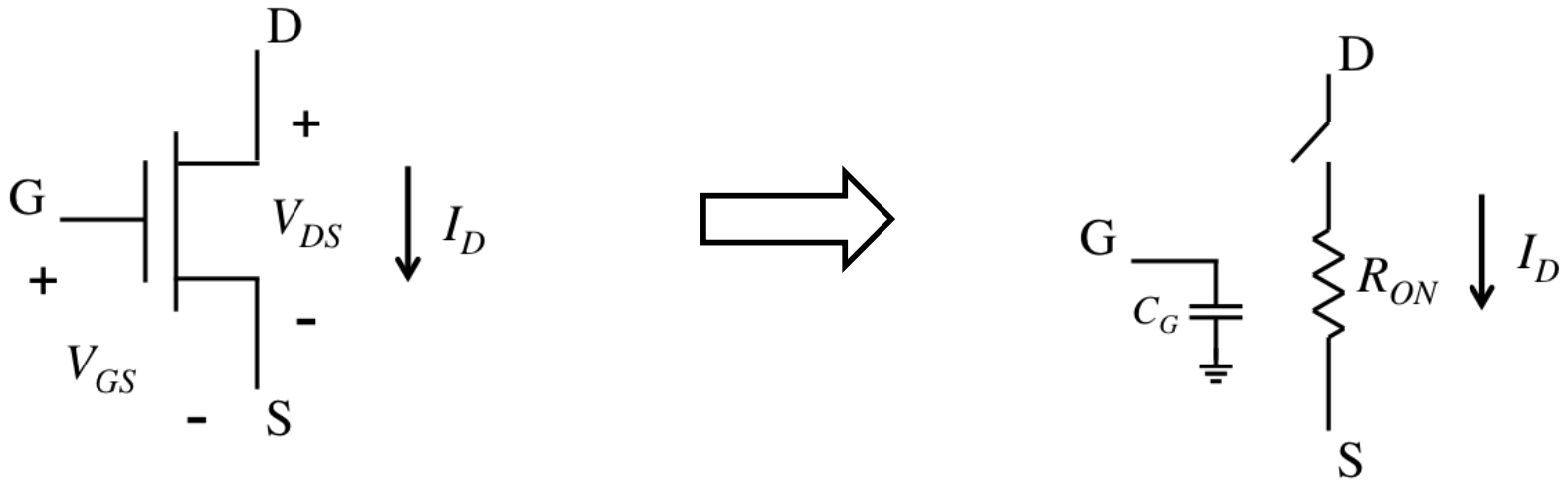
- Ideal Switch
  - $V_{GS} > V_{th}$ → switch is closed, conducts
  - $V_{GS} < V_{th}$ → switch is open, does not conduct
- Gate draws no current from input
  - Loads input capacitively (gate capacitance)

First Order Model



- Switch
  - Loads gate input capacitively
    - C_g
  - Has finite drive strength
    - R_{on}

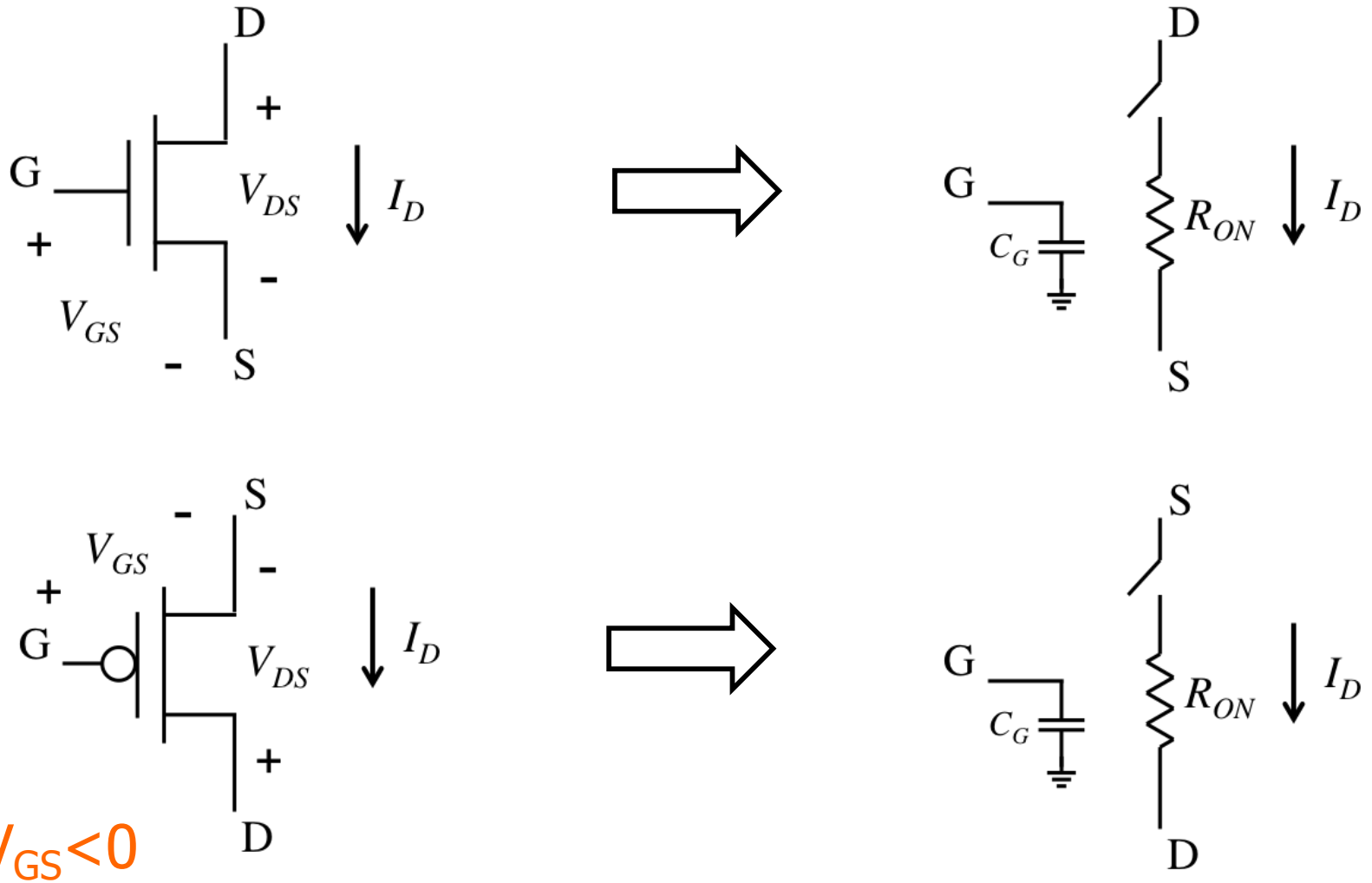
First Order Model



- Switch
  - Loads gate input capacitively
    - C_g
  - Has finite drive strength
    - R_{on}

What do drive and load mean?

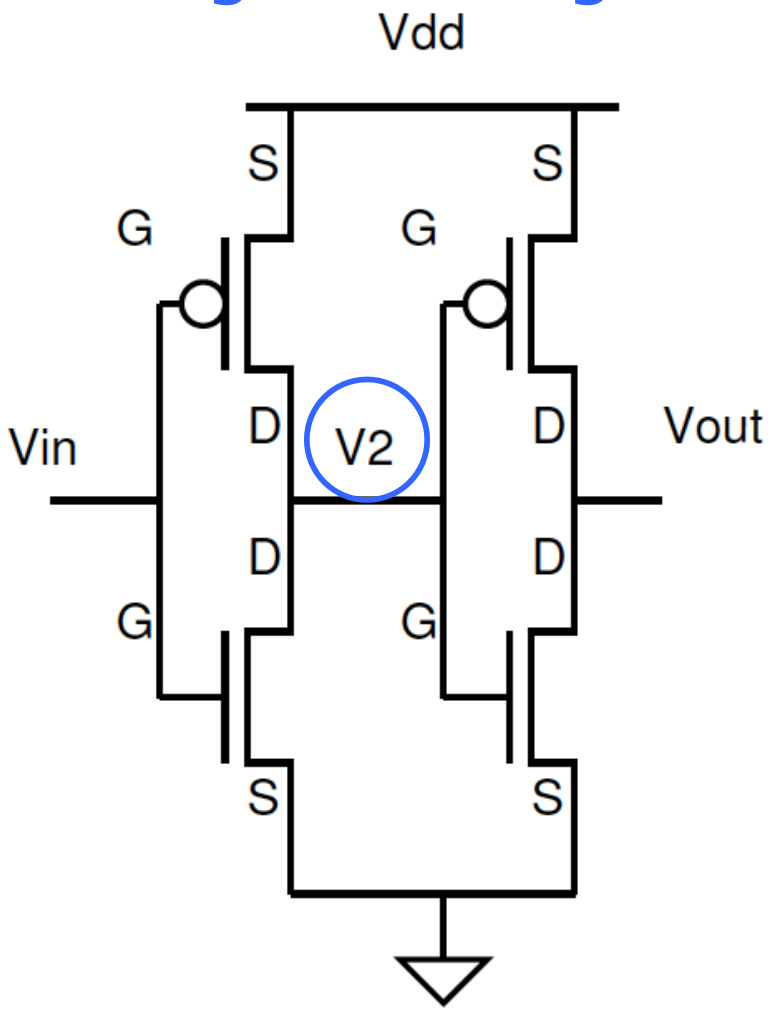
First Order Model - PMOS



$V_{DS}, V_{GS} < 0$

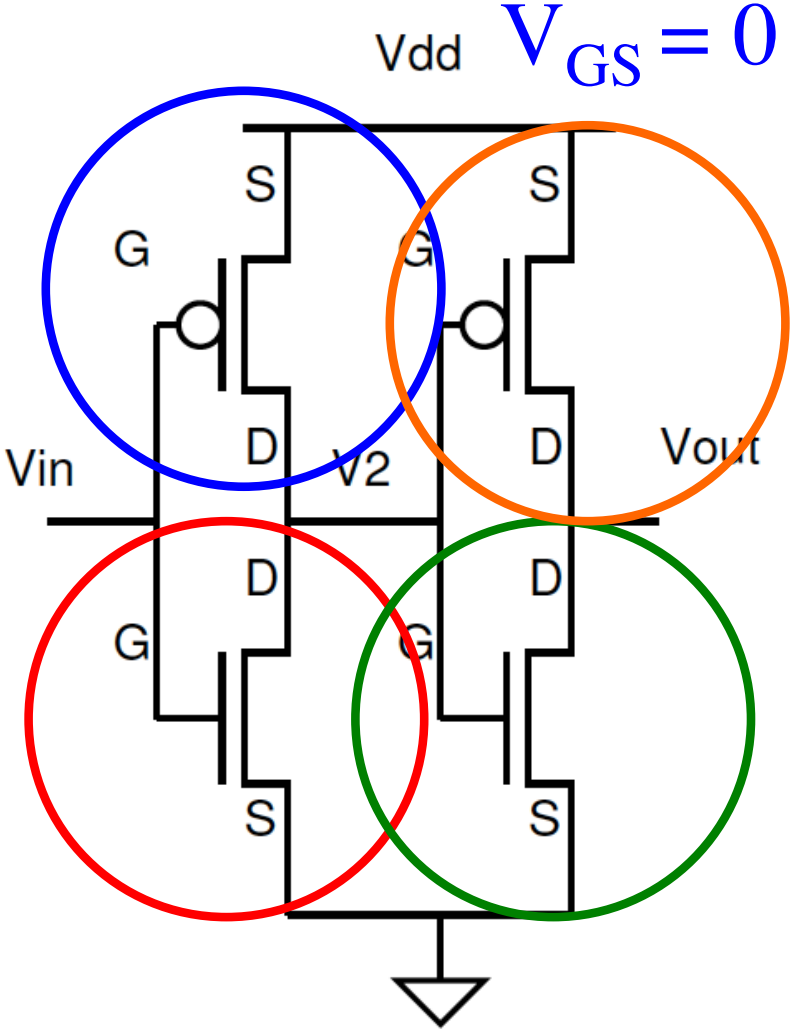
CMOS Buffer Gate

Stage 1 Stage 2



Reminder: Zero-Order Model?

What happens when $V_{in} = V_{dd} > V_{thn}$?



$V_{GS} = 0 > V_{th,p}$

$V_{th,p} = -V_{th,n}$

$V_{GS} = V_G - V_S$

$V_{GS} = -V_{dd} < V_{th,p}$

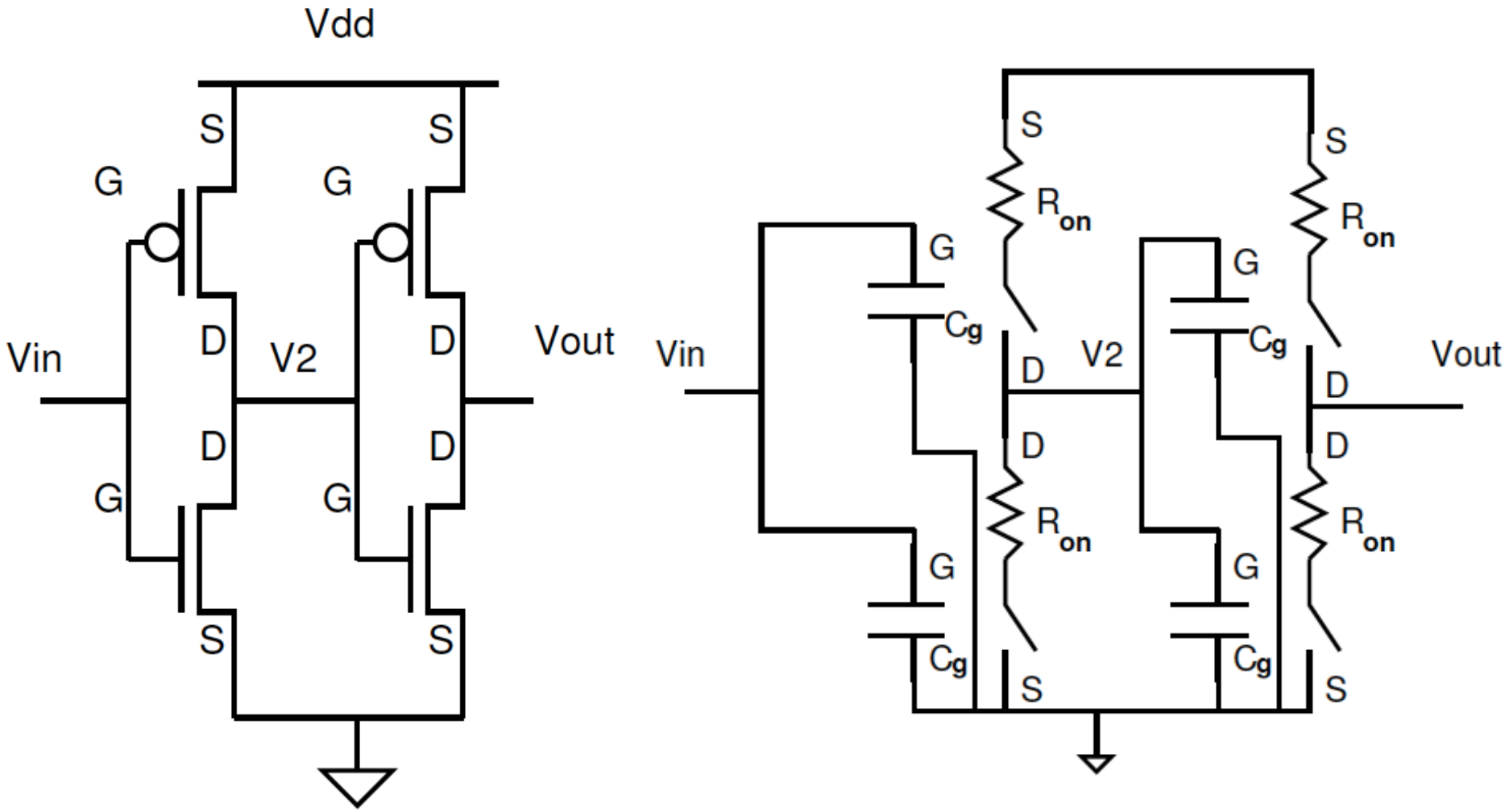
V_2=Gnd=0

$V_{out} = V_{dd}$

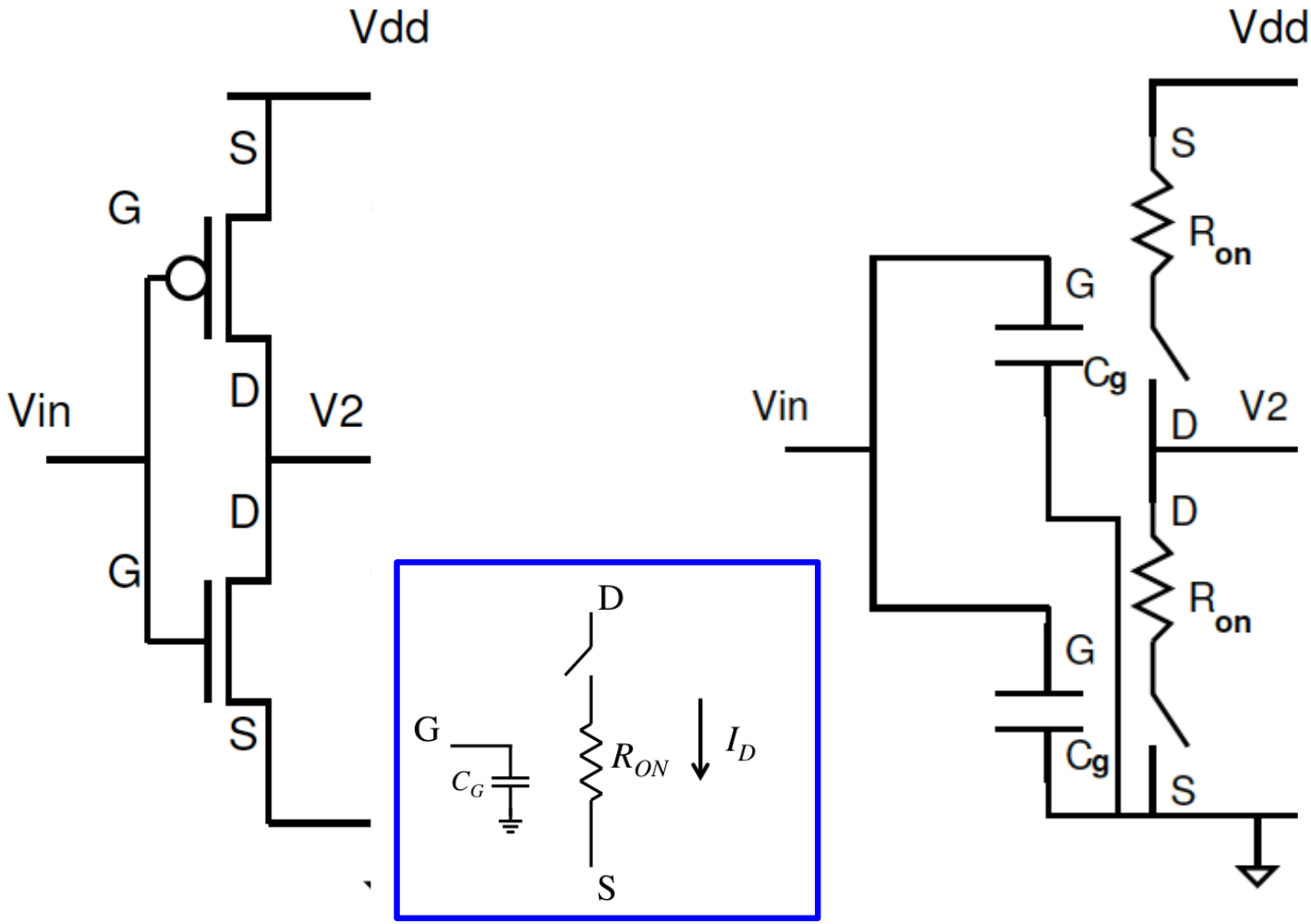
$V_{GS} = 0 < V_{th,n}$

$V_{GS} = V_G - V_S = V_{dd} > V_{th,n}$

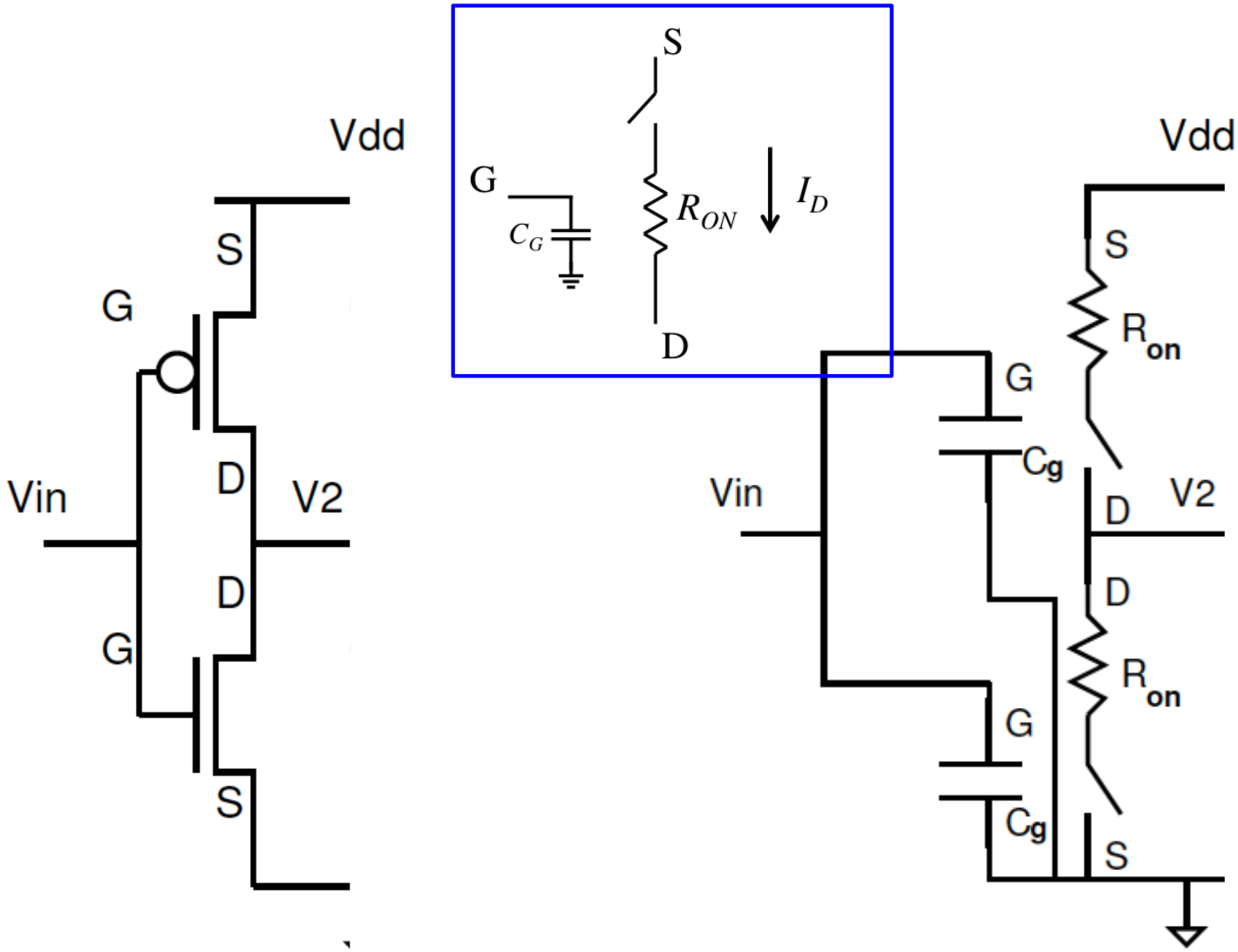
CMOS Buffer Gate - First Order



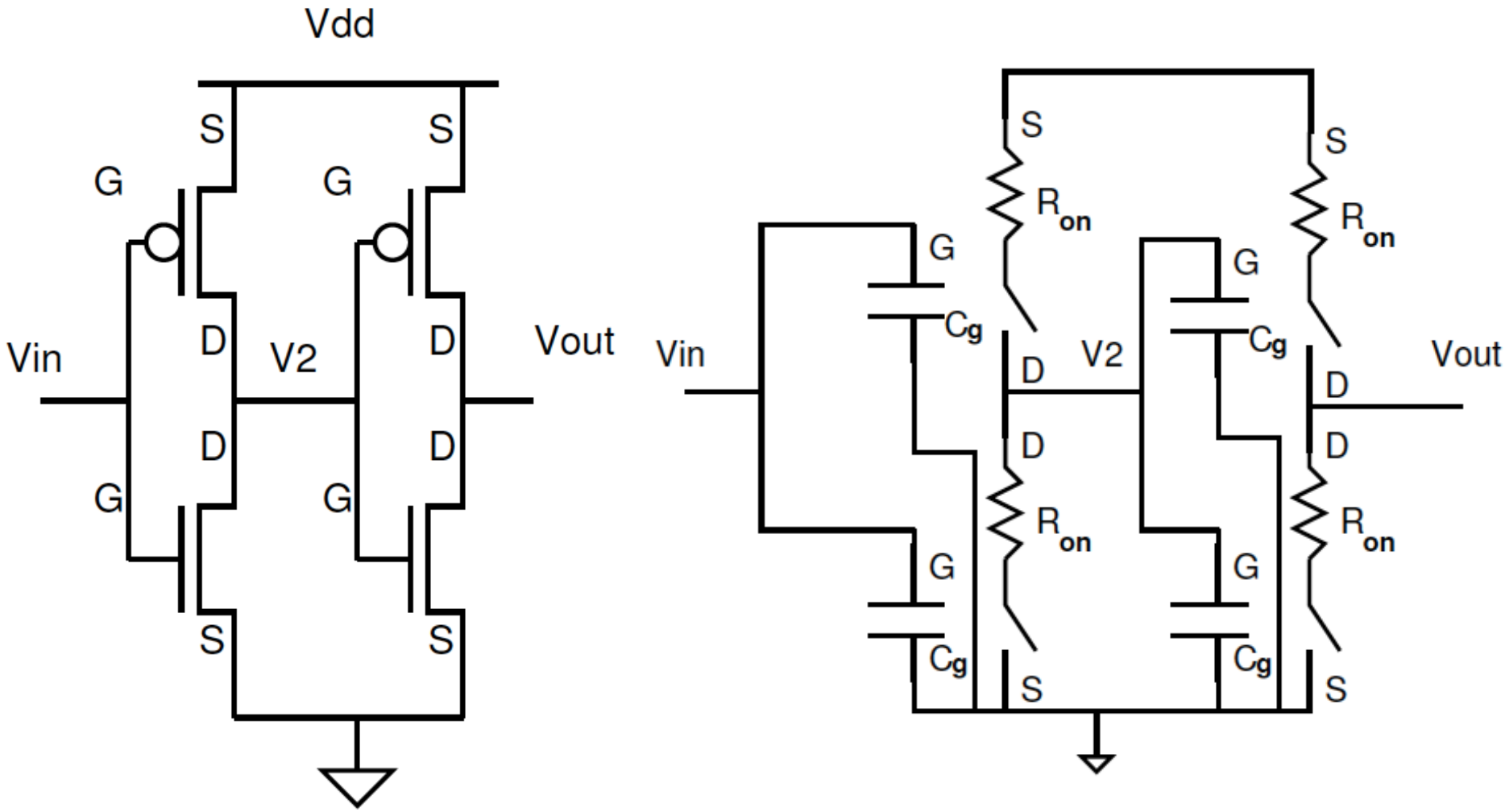
CMOS Buffer Gate - First Order



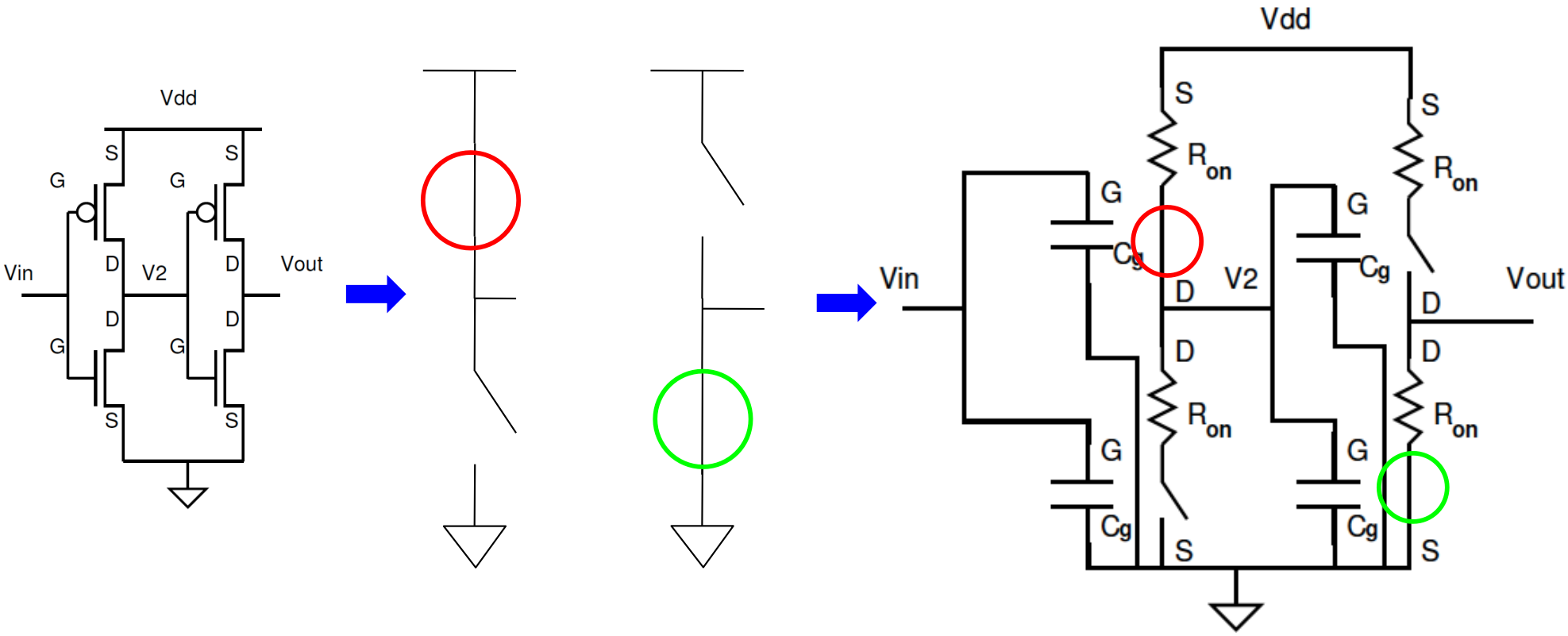
CMOS Buffer Gate - First Order



CMOS Buffer Gate - First Order

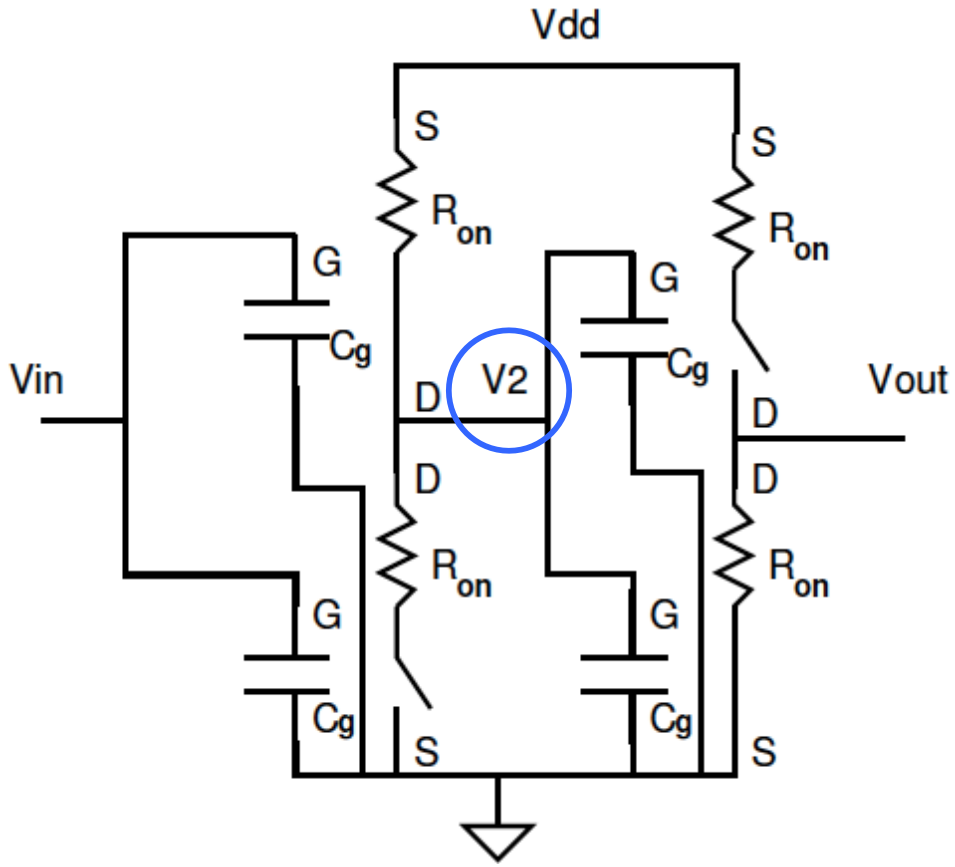


Zero-Order Model to Set Switches



- What is V_{IN} for this switch pattern?

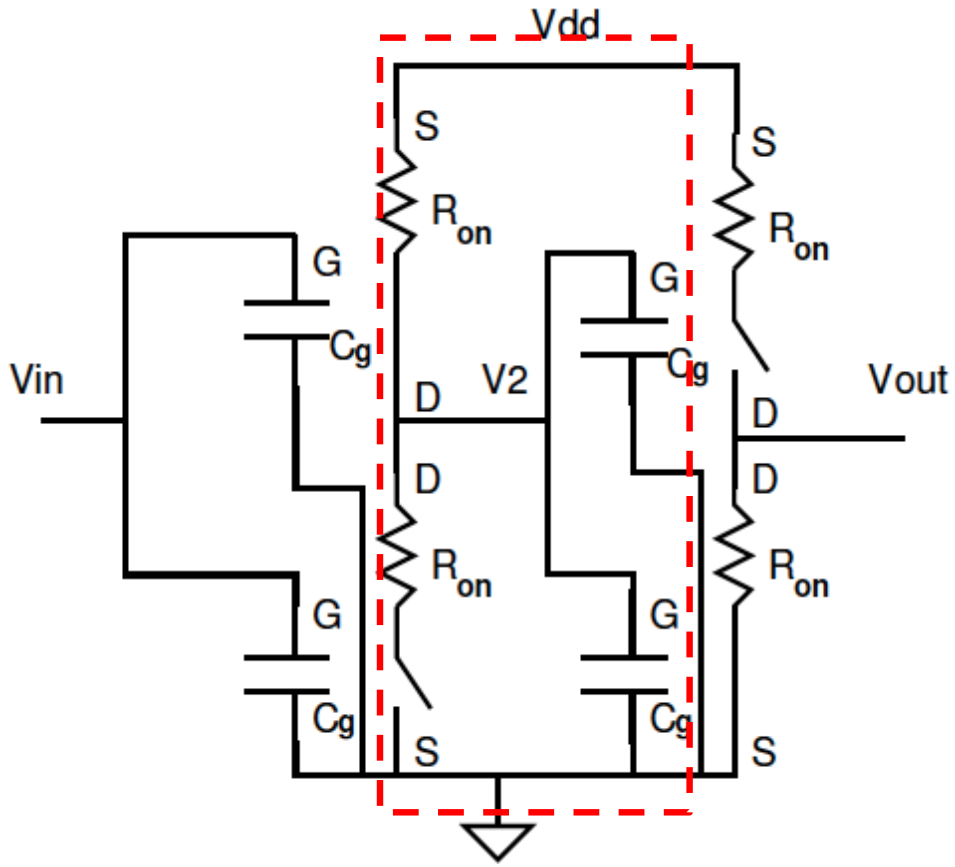
CMOS Buffer Gate - First Order



ESE215 problem

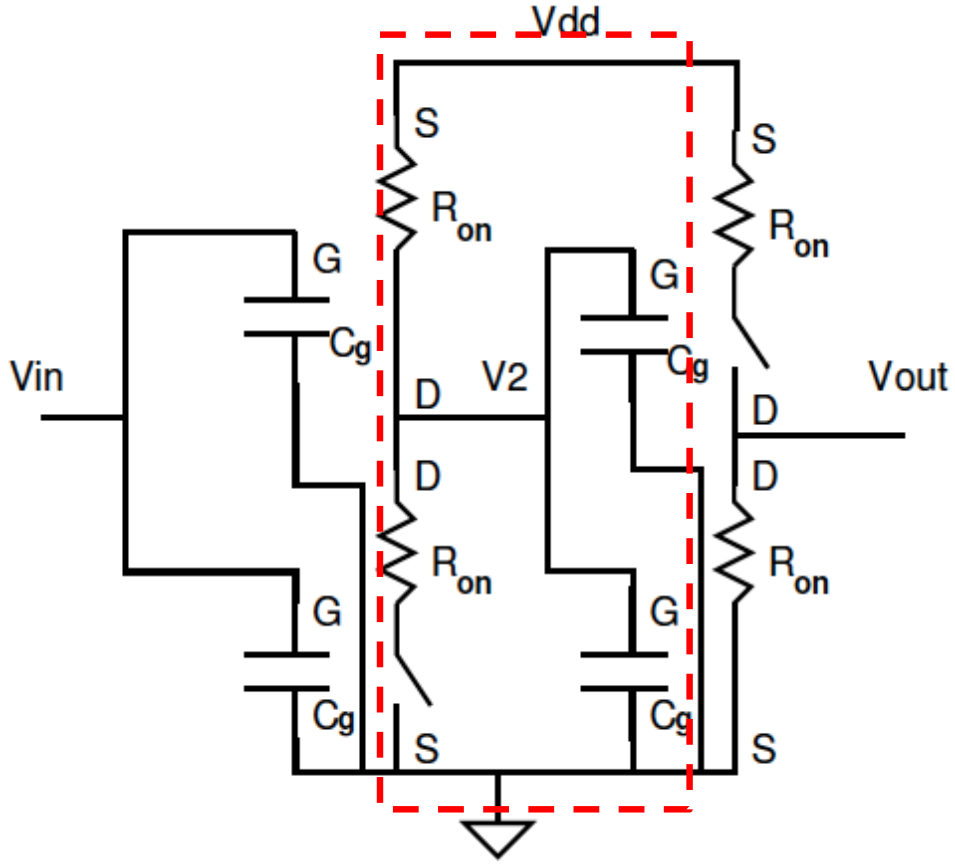
- Leaves an RC Circuit we can analyze

CMOS Buffer Gate - First Order



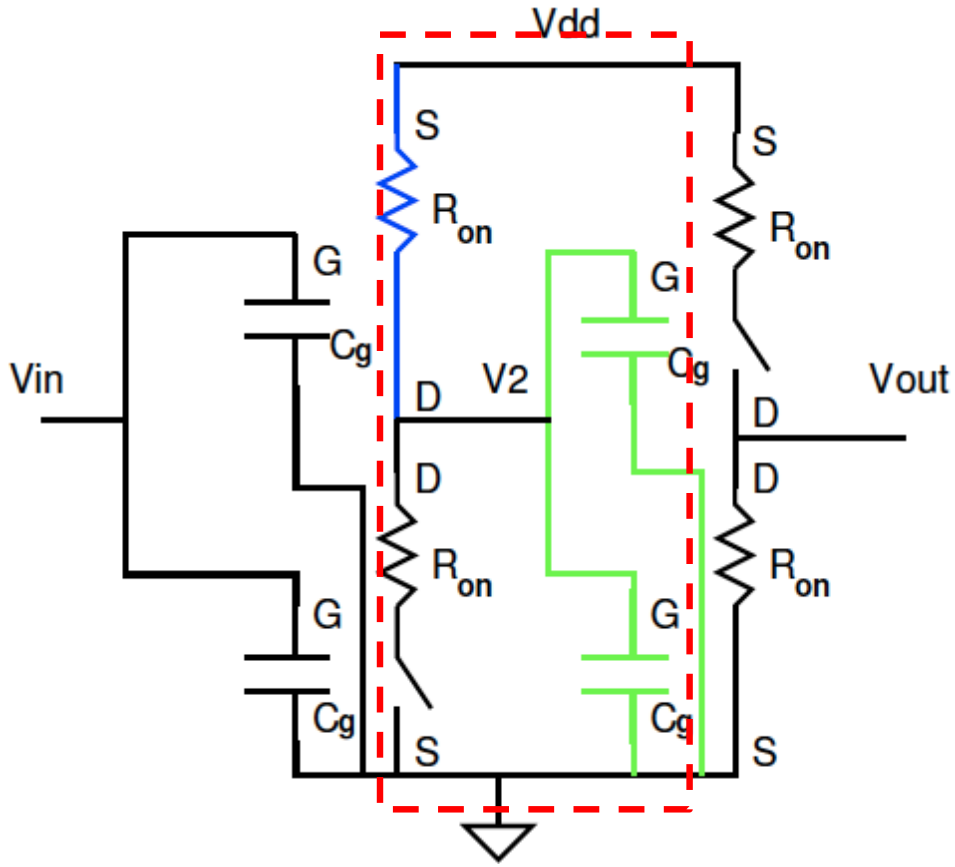
- Look at intermediary node V_2
  - Connected to output of stage 1 and input of stage 2

CMOS Buffer Gate - First Order



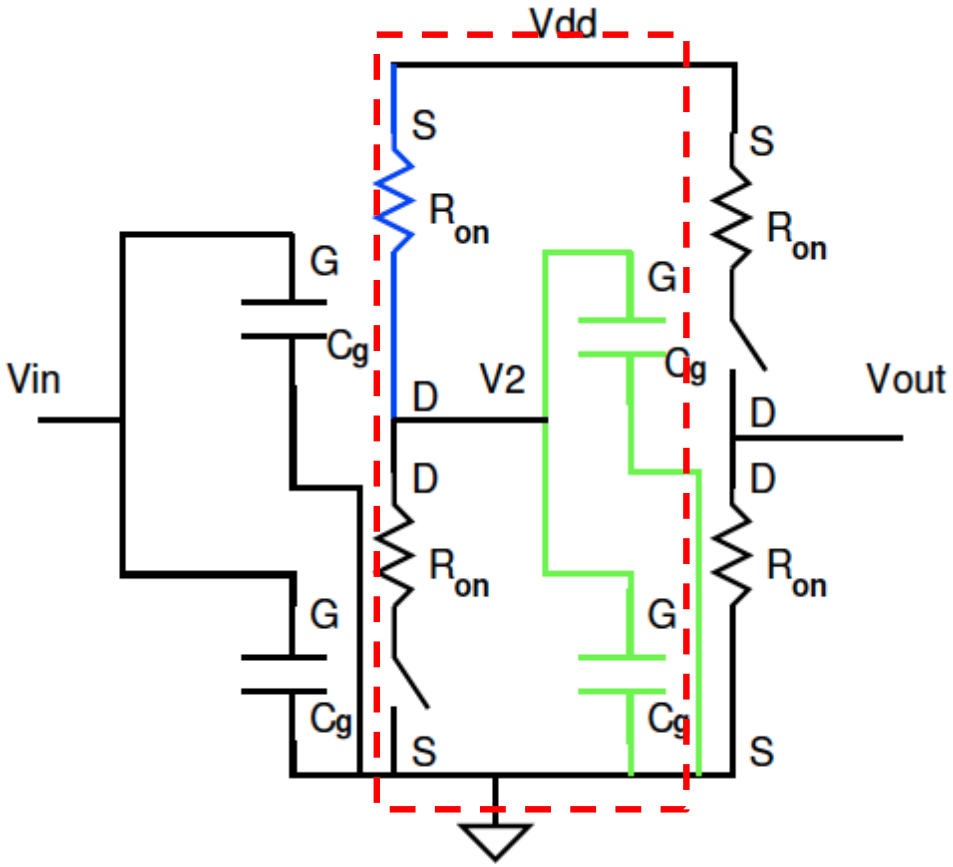
- What is equivalent circuit for the gate output of stage 1 driving V_2? What is load on the output of stage 1?

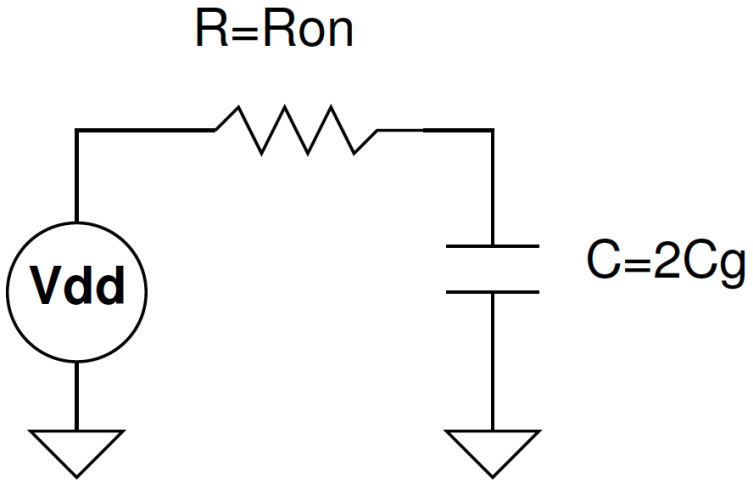
CMOS Buffer Gate - First Order



- Stage 1 equivalent circuit for the gate output
- Load on V_2
  - Capacitive, input of stage 2

CMOS Buffer Gate - First Order





- Stage 1 equivalent circuit for the gate output
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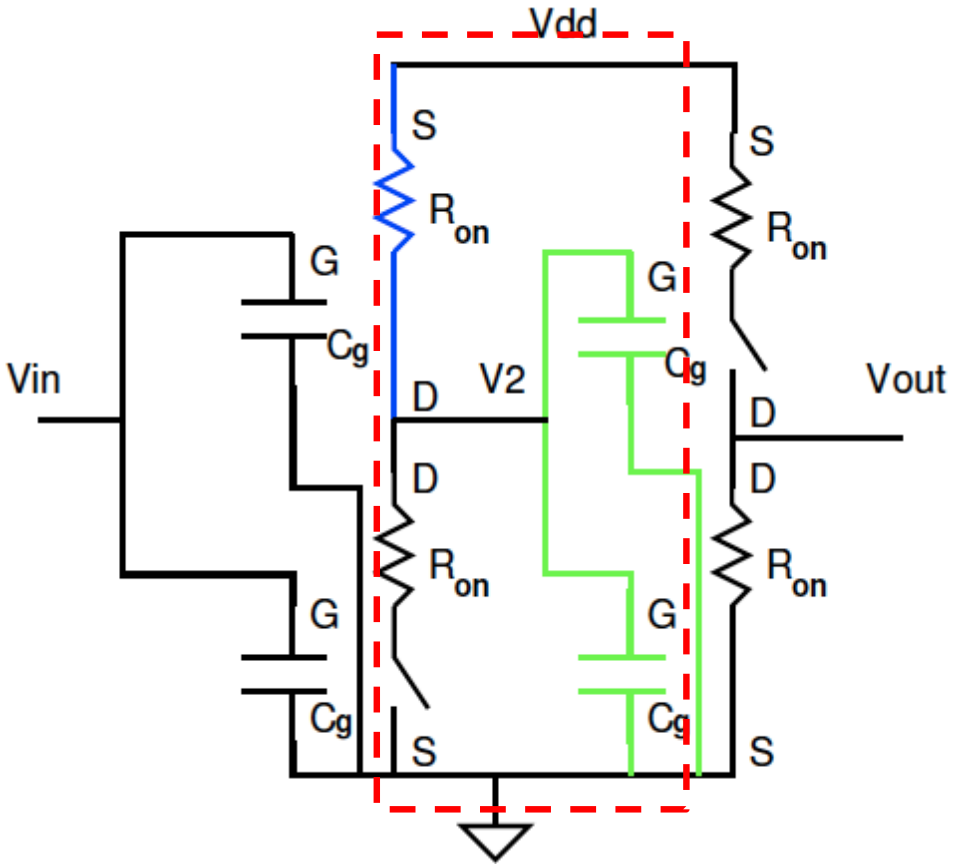
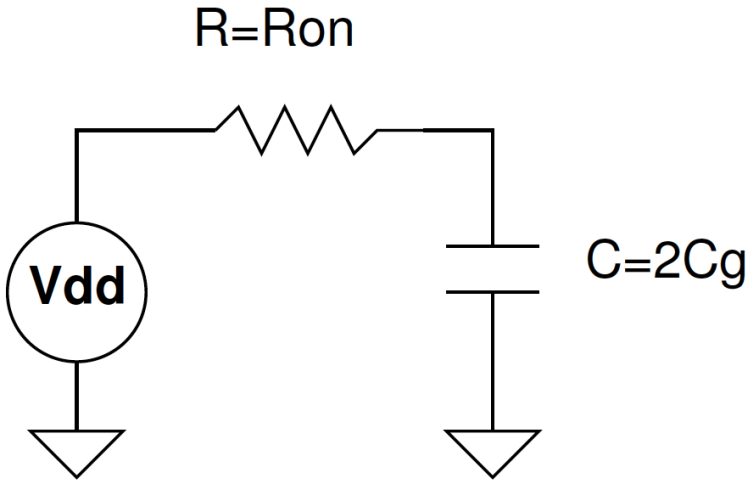
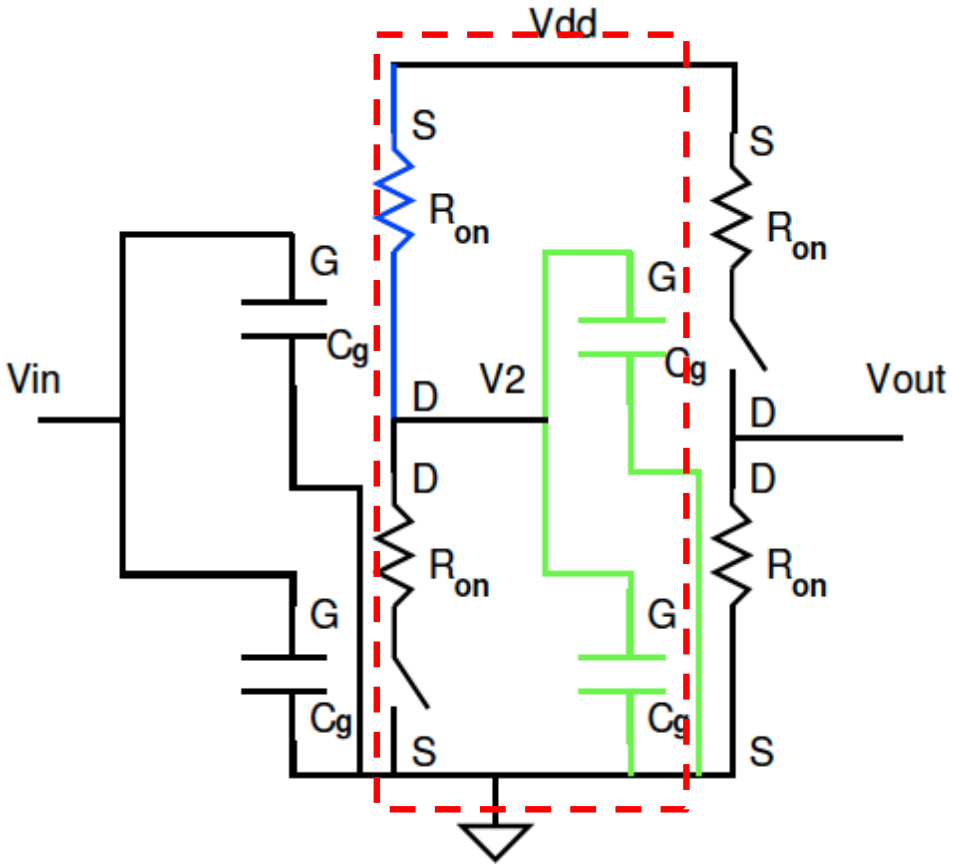
CMOS Buffer Gate - First Order

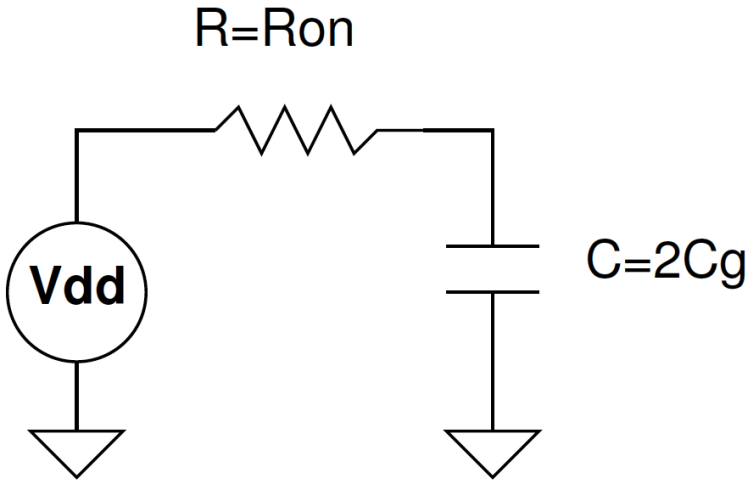




- What is time constant of V_2 when V_{in} switches from V_{DD} to 0?

CMOS Buffer Gate - First Order





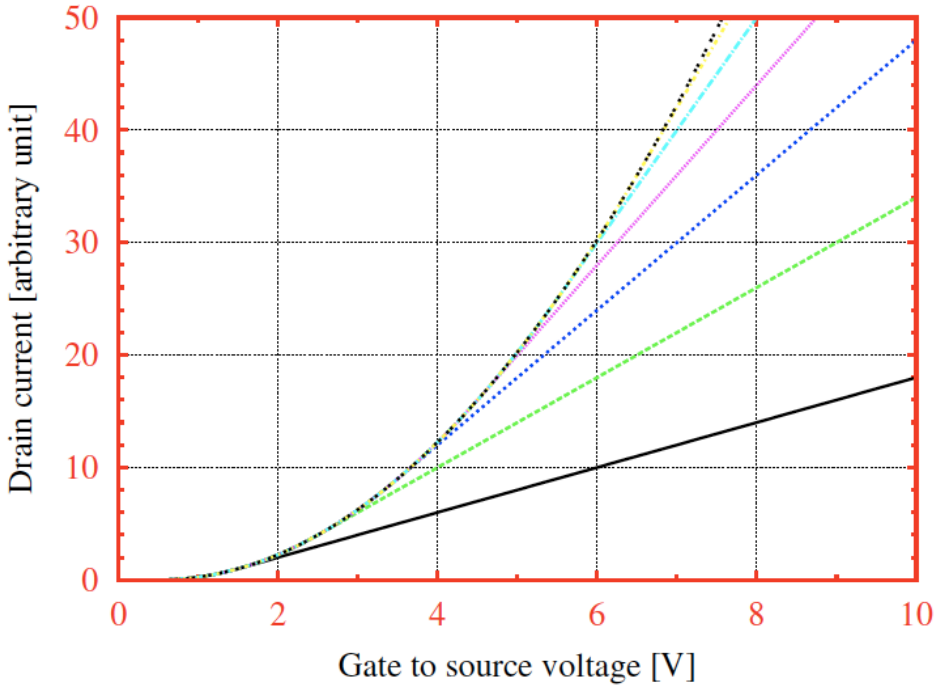
- What is time constant of V_2 when V_{in} switches from V_{DD} to 0?
  - $\tau = 2R_{on}C_g$

First-Order Model

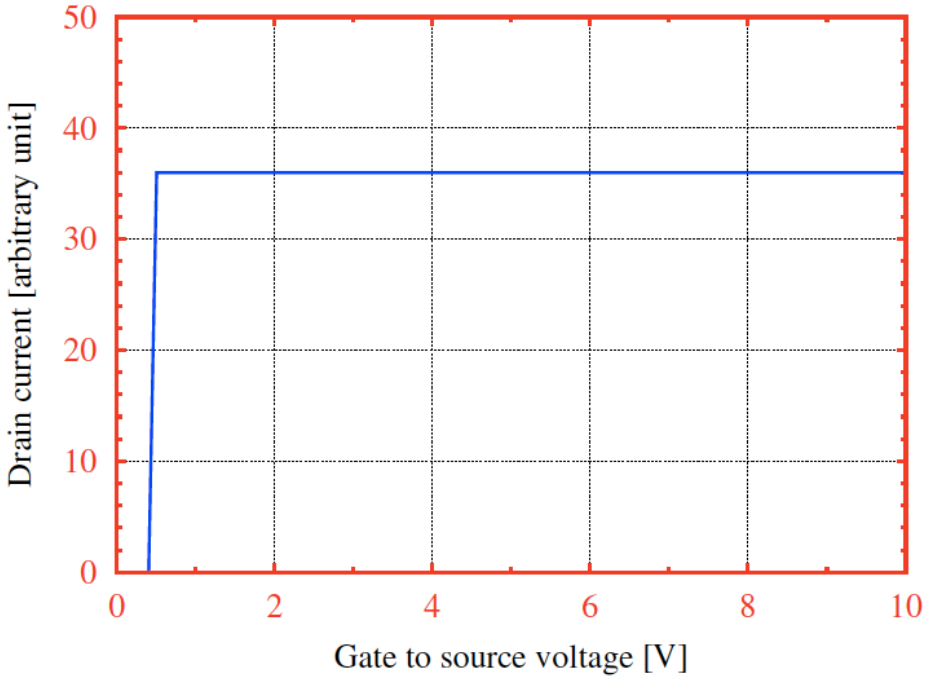
- Includes settling times/delay
- Voltage settling with capacitive loads
  - At least some basis for reasoning about delay

What is still missing?

IV curve



1st Order



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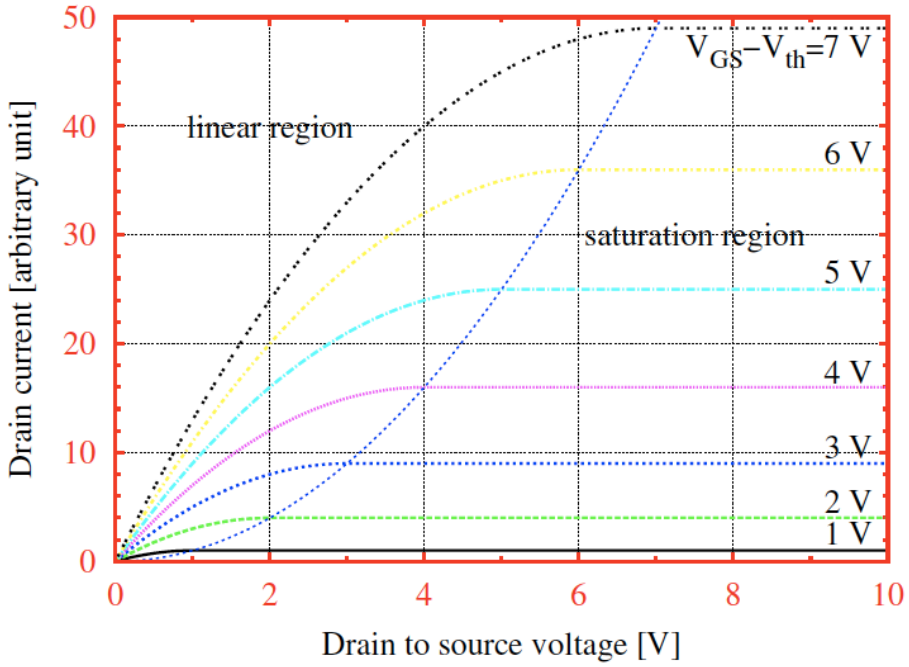
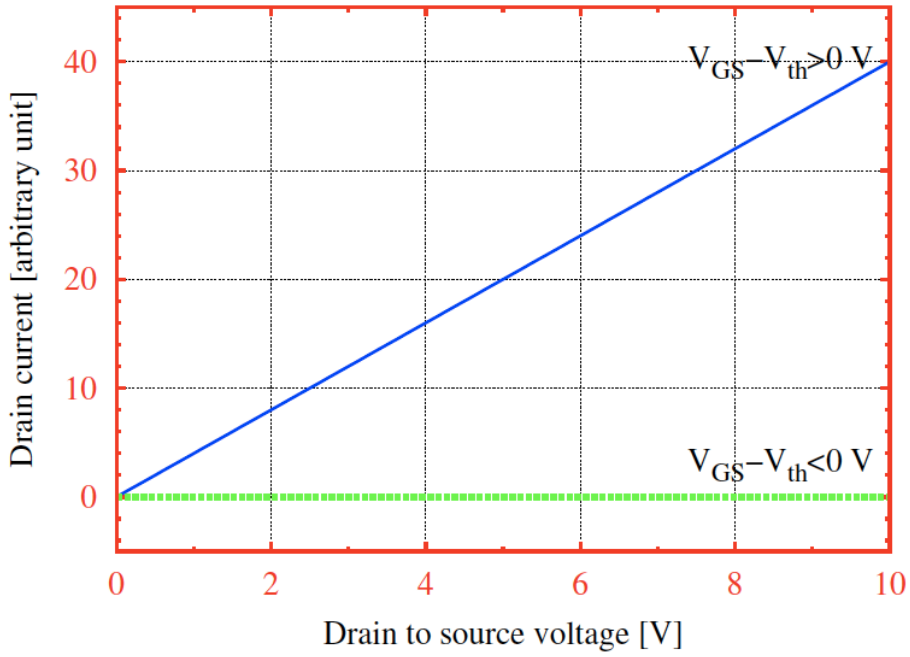
IV curve



1st Order



What is still missing?

- What happens at intermediate voltages?
  - When the input is not rail-to-rail (not just gnd or V_{dd} inputs)
- Details of dynamics, including…
  - Input transition is not an ideal step
  - Intermediate drive strengths change with V_{GS}
    - Drain resistance changes
- Sub-threshold operation
  - When $V_{gs}<V_{th}$

Design: Engineering Control

- V_{th}
  - Process engineer
- Drive strength (R_{on})
  - Circuit engineer
  - Control with sizing transistors
- Supply voltages (V_{dd})
  - Range set by process engineer
  - Detail use by circuit engineer

Big Ideas

- MOSFET Transistor as switch
  - With limited drive
- Purpose-driven simplified modeling
  - Aid reasoning, sanity check, simplify design
- Analysis methodology
  - Zero order to understand switch state (logic)
  - First-order to get equivalent RC circuit (delay)

Admin

- Diagnostic grades recorded
  - Solutions posted online (pdf in Canvas)
  - Make sure you understand
  - Diagnose what you need to review and study
    - Karnaugh maps (minimum sum of products), RC capacitive settling (time constant), and wire resistive and capacitive properties
- HW 1 due Tuesday 9/14 next week
  - Because you need Monday lecture for noise margins
    - Can look at last year's lecture slides if you want to look ahead
  - HW due following Monday 9/20