ESE370: Circuit-Level Modeling, Design, and Optimization for Digital Systems

Lec 31: November 24, 2021

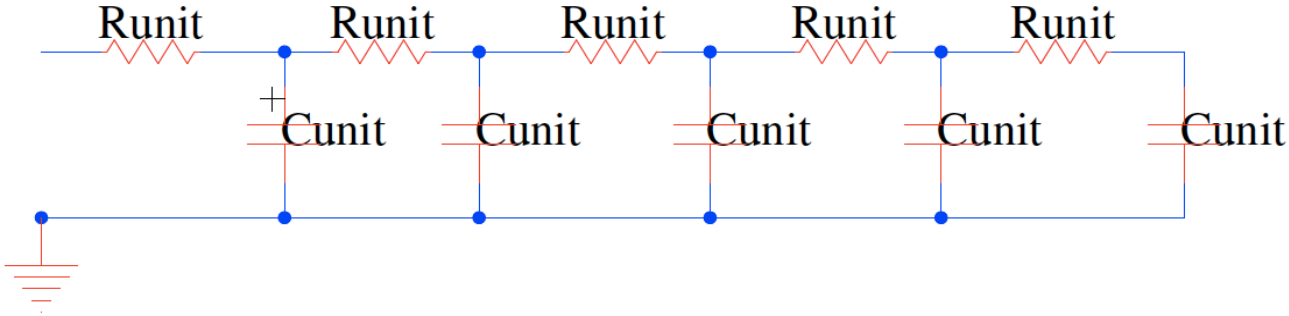
Crosstalk

Today

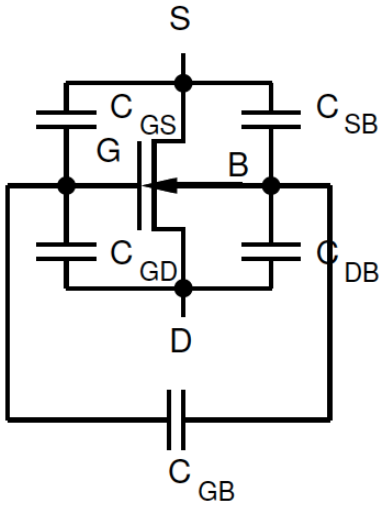
- Crosstalk
  - Characterization
    - Magnitude
  - Avoiding
    - Design practices

Capacitance

- There are capacitors everywhere
- Already talked about
  - Wires modeled as a distributed RC network



  - Parasitic capacitances between terminals on transistor



Capacitance Everywhere

- Potentially a capacitor between any two conductors
  - On the chip
  - On the package
  - On the board
- All wires
  - Package pins
  - PCB traces
  - Cable wires
  - Bit/word lines

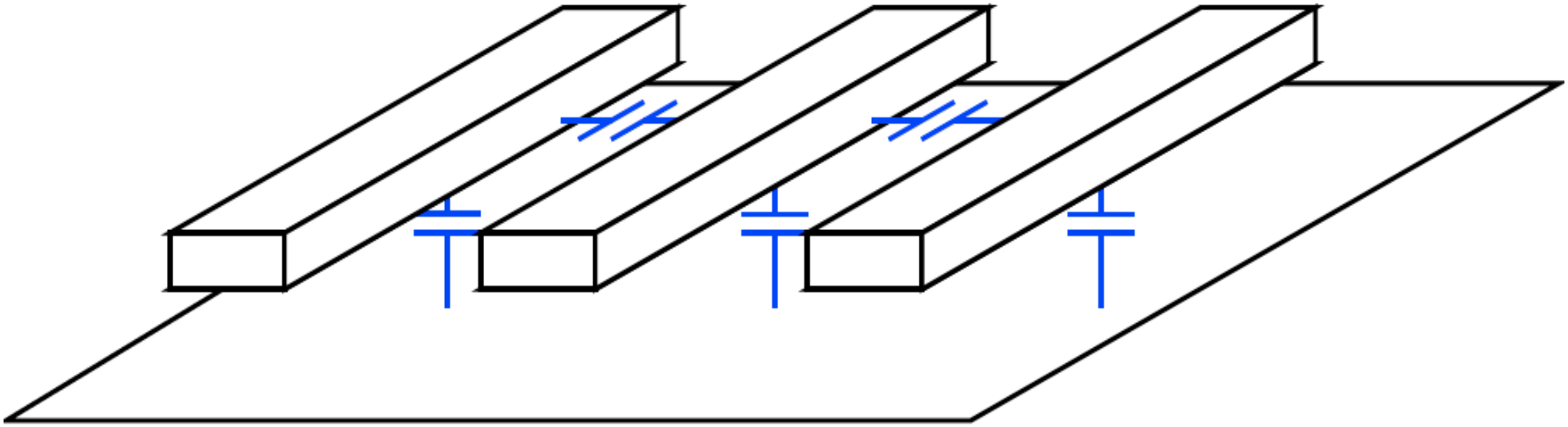
Capacitance…

- …decreases with conductor separation
- …increases with size
- …depends on dielectric

$$C = \varepsilon_r \varepsilon_0 \frac{A}{d}$$

Wire Capacitance

- Changes in voltage on one wire may couple through parasitic capacitance to an adjacent wire



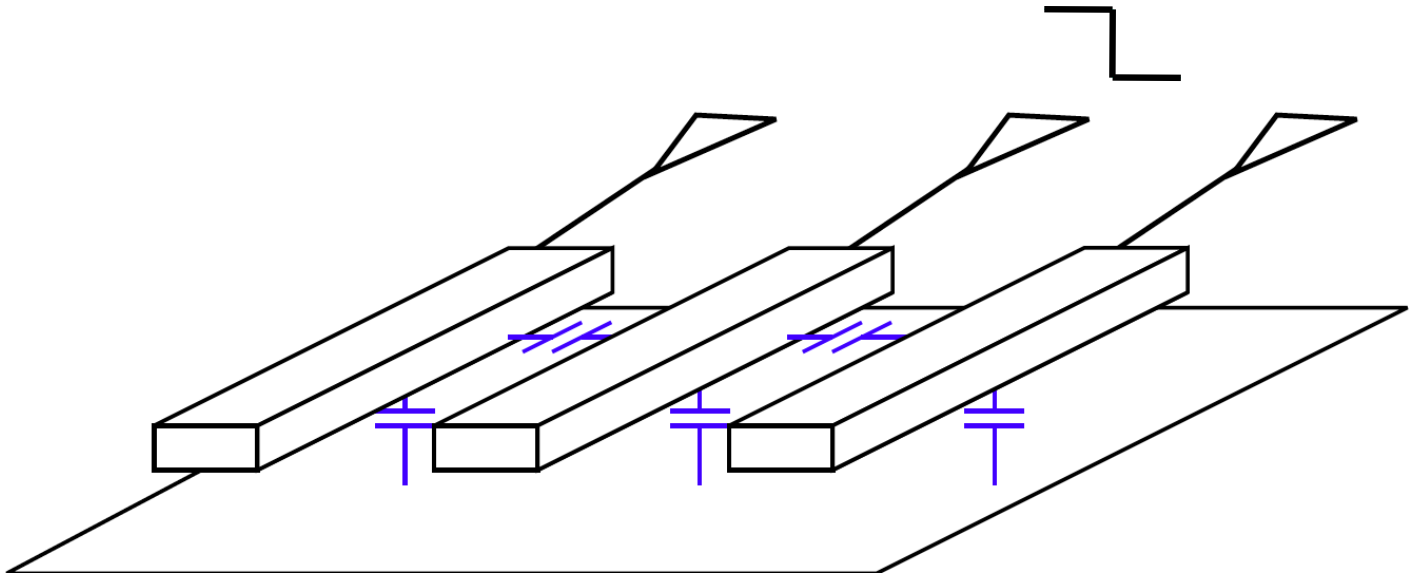
Crosstalk

- A capacitor does not like to change its voltage instantaneously
- A wire has high capacitance to its neighbor.
  - When the neighbor switches from 1-> 0 or 0->1, the wire tends to switch too.
  - Called capacitive *coupling* or *crosstalk*.
- Crosstalk effects
  - Noise on non-switching wires
  - Increased delay on switching wires

Qualitative

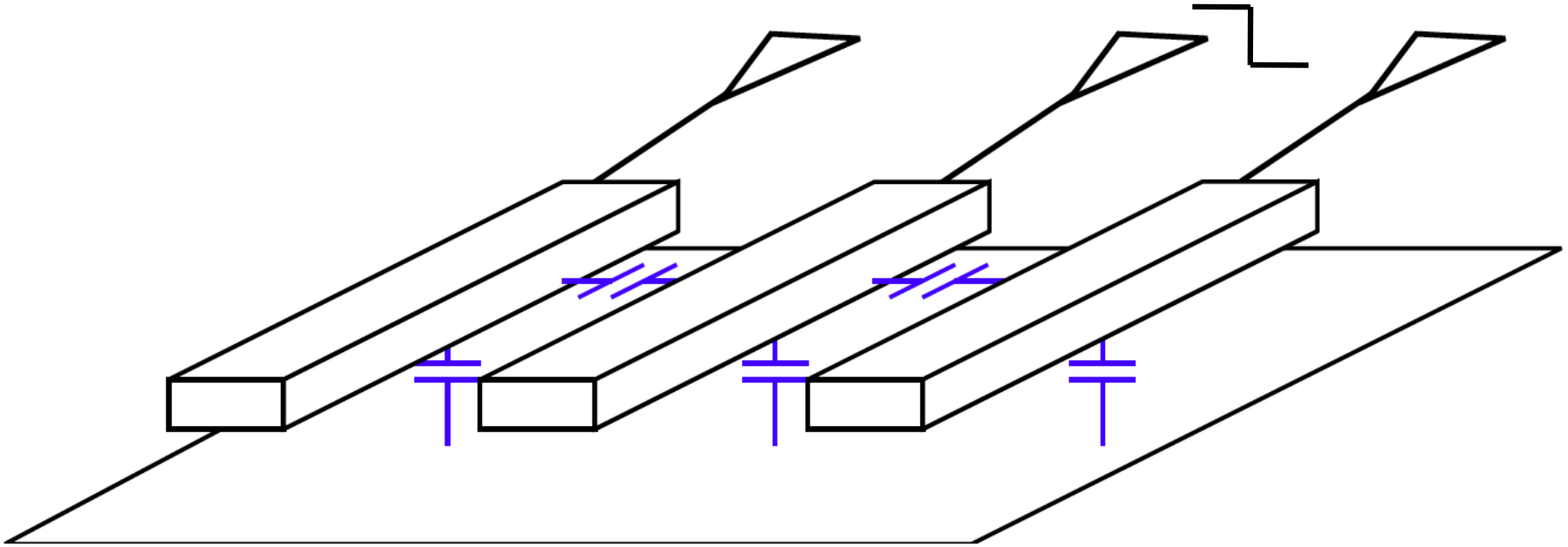
Undriven Wire

- What happens to undriven wire?
- Where do we have undriven wires?



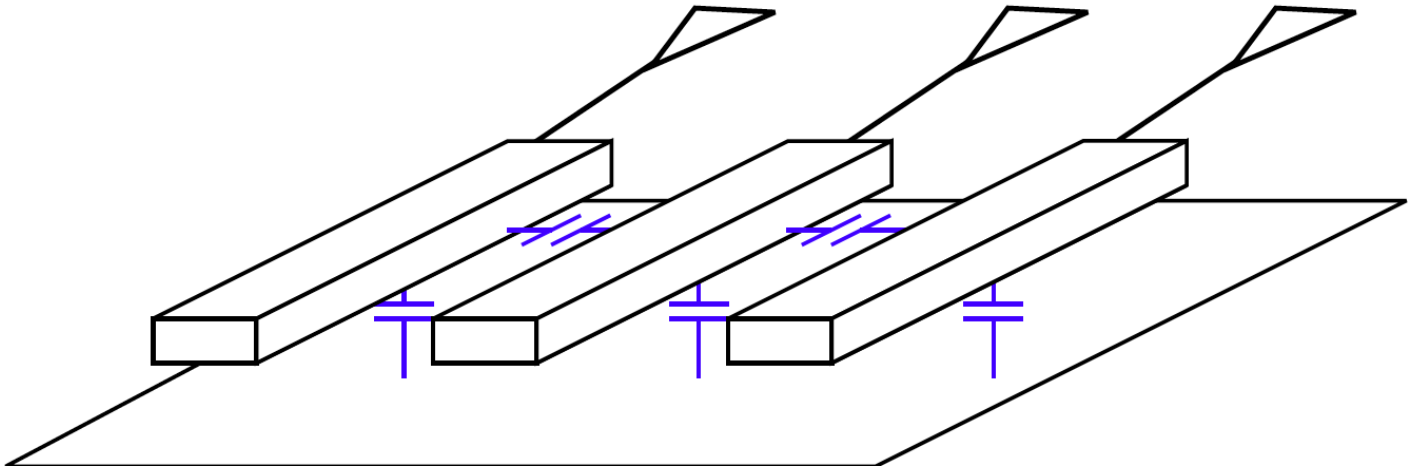
Driven Wire

- What happens to a driven "neighbor" wire?
  - One wire switches
  - Neighbors driven but not switch
  - What happens to neighbors?



Driven Wire

- Can this be a problem?
- What if switching neighbor is:
  - Clock line
  - Non-clock signal used in synchronous system
  - Asynchronous control



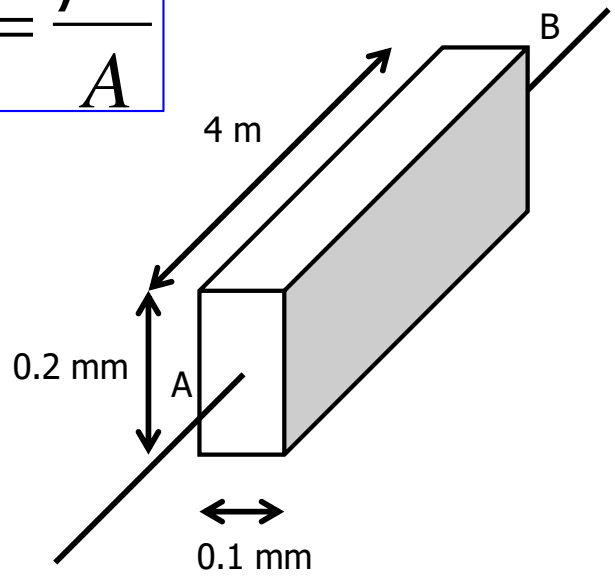
Clocked Logic

- CMOS driven lines
- Clocked logic
  - Willing to wait to settle/evaluate
- Impact is on delay
  - May increase delay of transitions

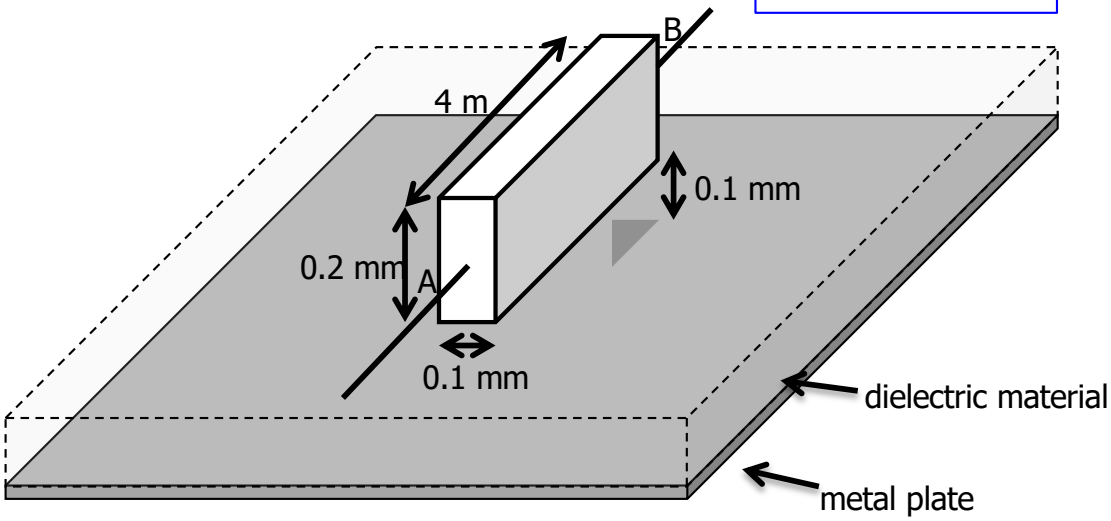
Quantitative

Isolated Wire RC

$$R = \frac{\rho L}{A}$$



$$C = \varepsilon_d \frac{A}{d}$$



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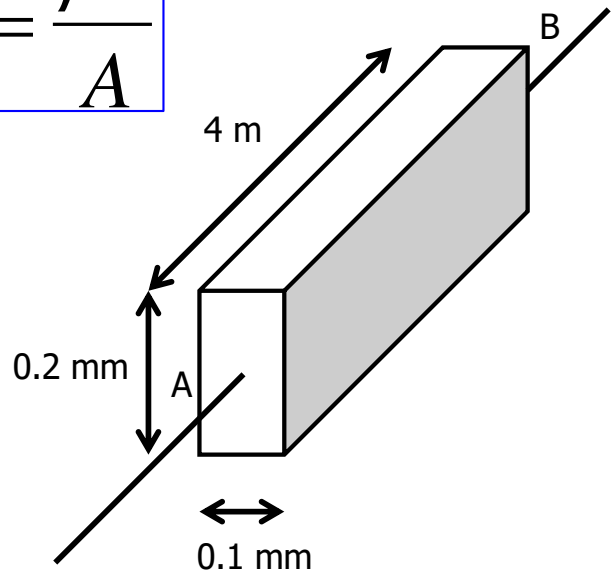

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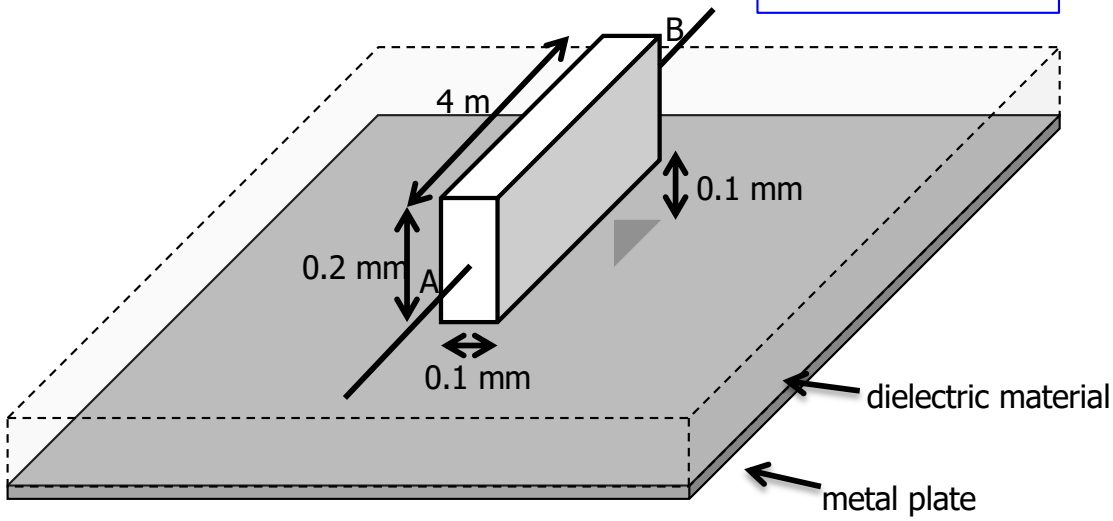
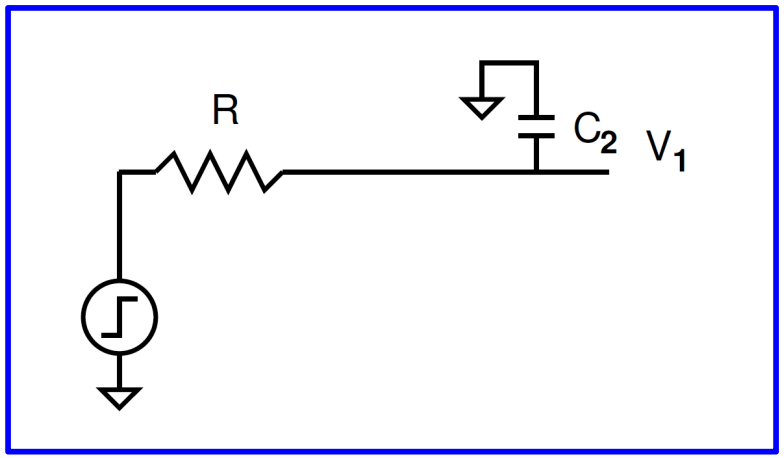
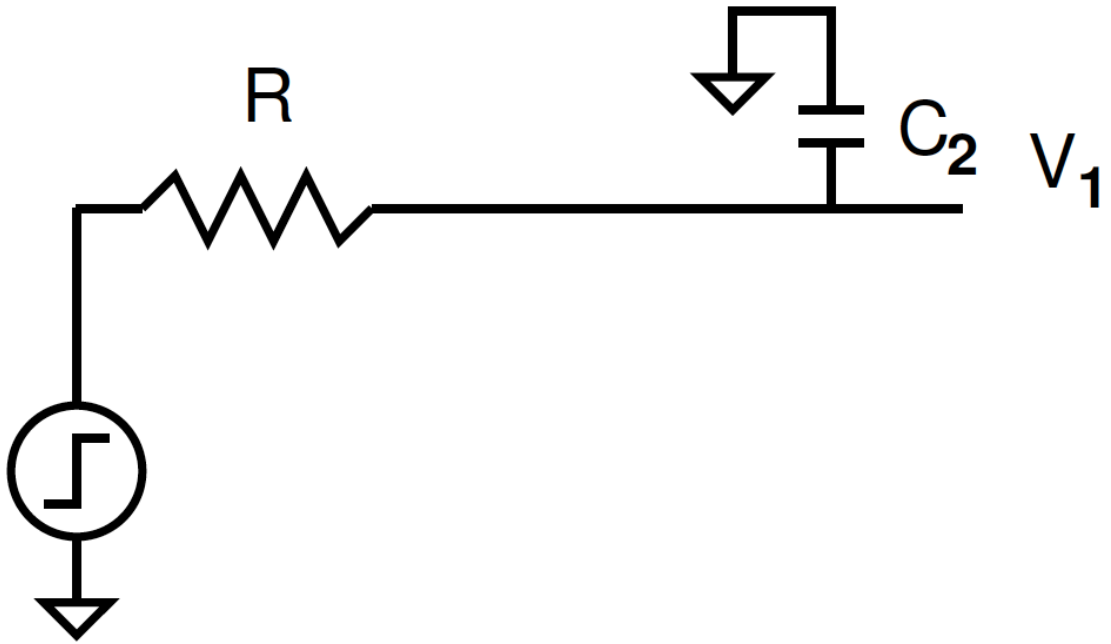




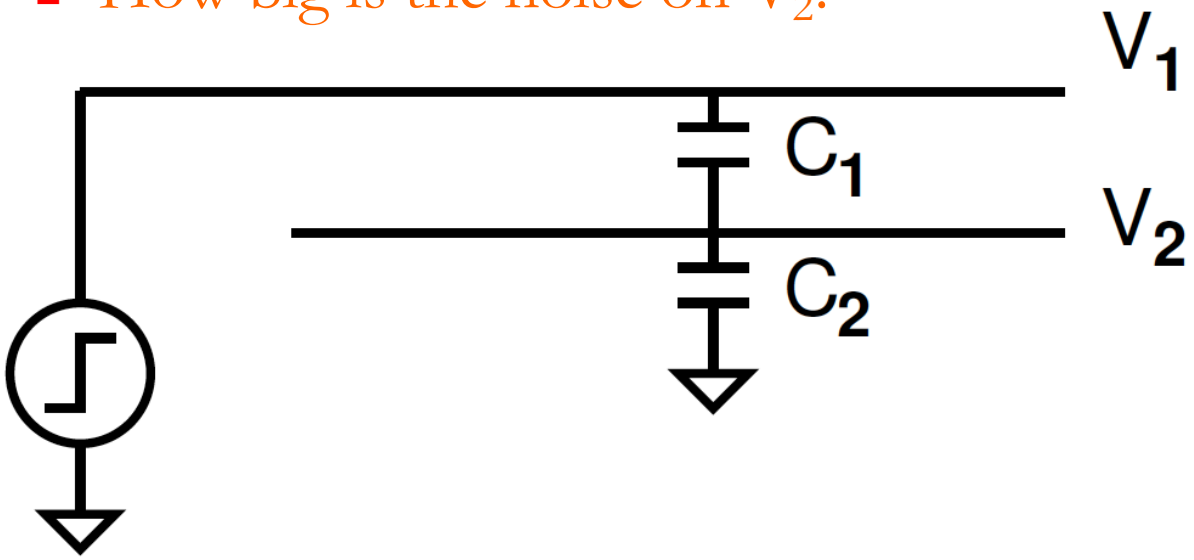
Wire step response (preclass 1)

- Step response for isolated wire?



Undriven Adjacent Wire (preclass 2)

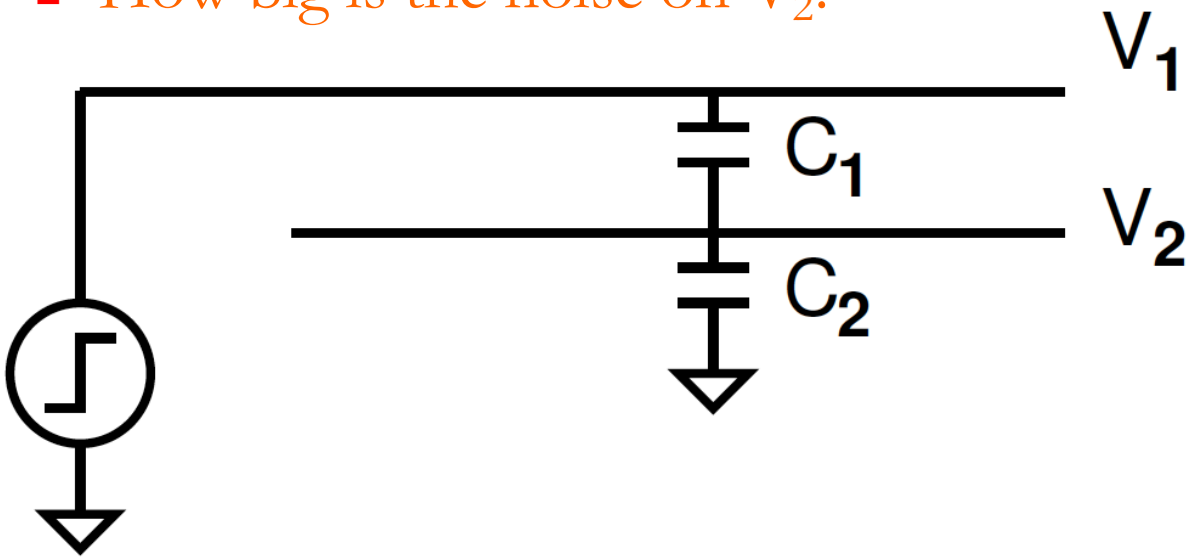
- V_1 transitions from 0 to V
  - How big is the noise on V_2?



Undriven Adjacent Wire

- V_1 transitions from 0 to V
  - How big is the noise on V_2?

$$I(t) = C\frac{dV(t)}{dt}$$



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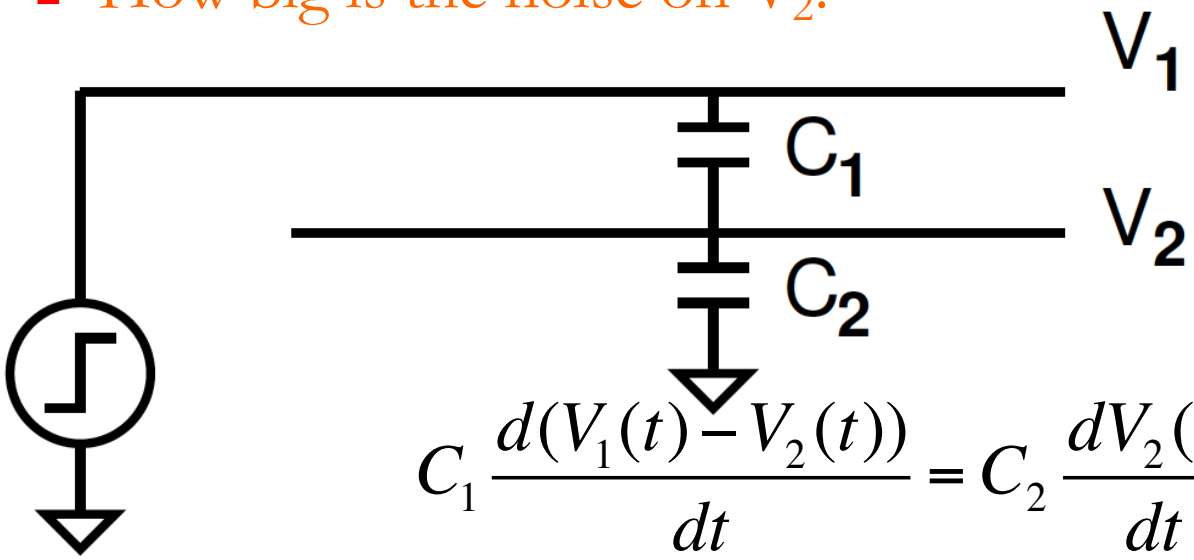


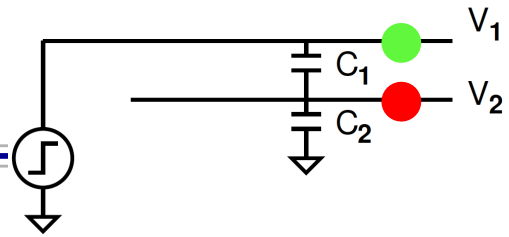
$$C_1\frac{d(V_1(t)-V_2(t))}{dt} = C_2\frac{dV_2(t)}{dt}$$

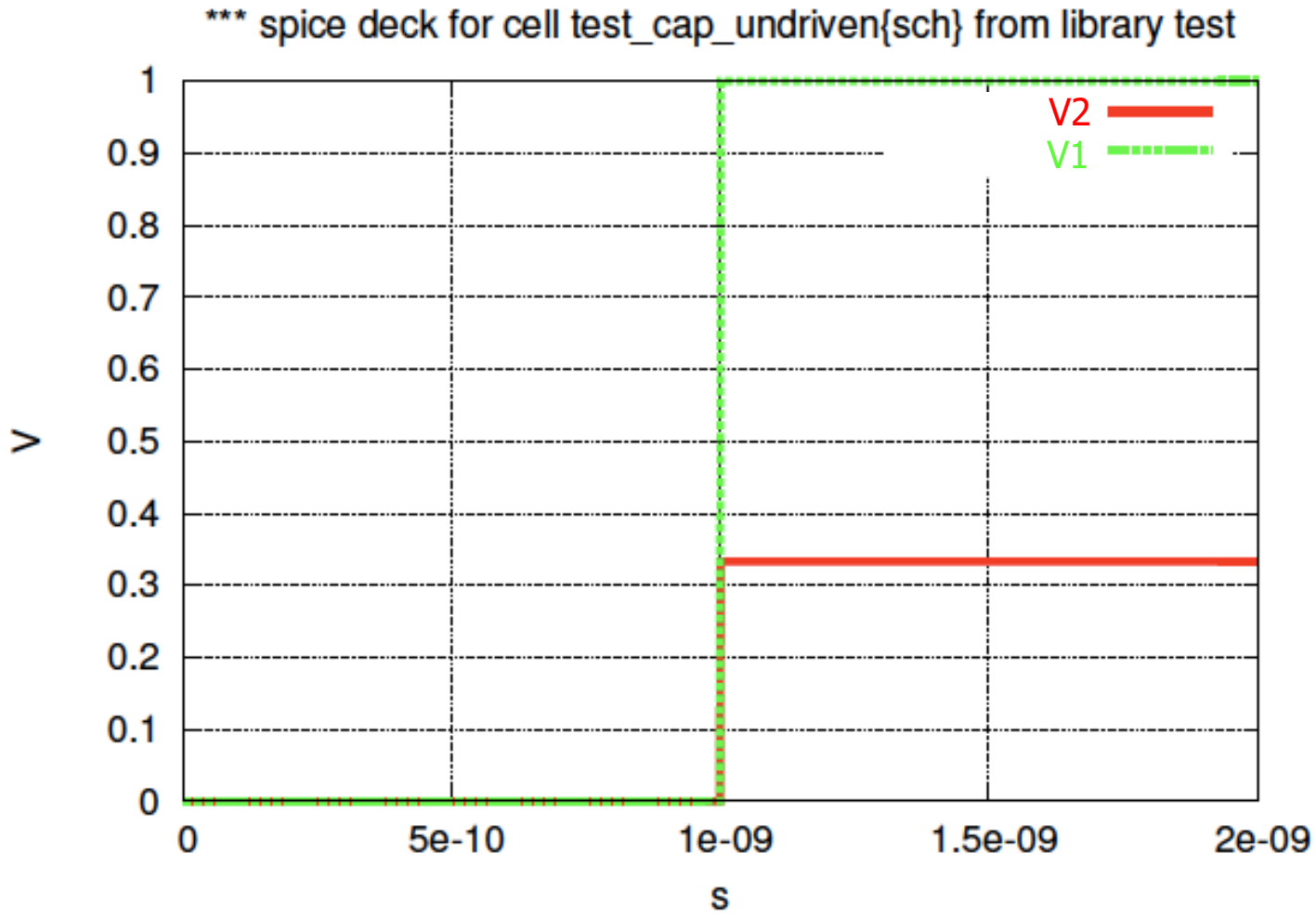
$$C_1\frac{dV_1(t)}{dt} = (C_1+C_2)\frac{dV_2(t)}{dt}$$

$$C_1V_1(t) = (C_1+C_2)V_2(t)$$

$$V_2(t) = \frac{C_1}{C_1+C_2}V_1(t)$$

SPICE C_1=10pF, C_2=20pF





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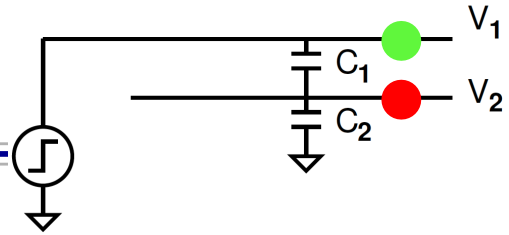
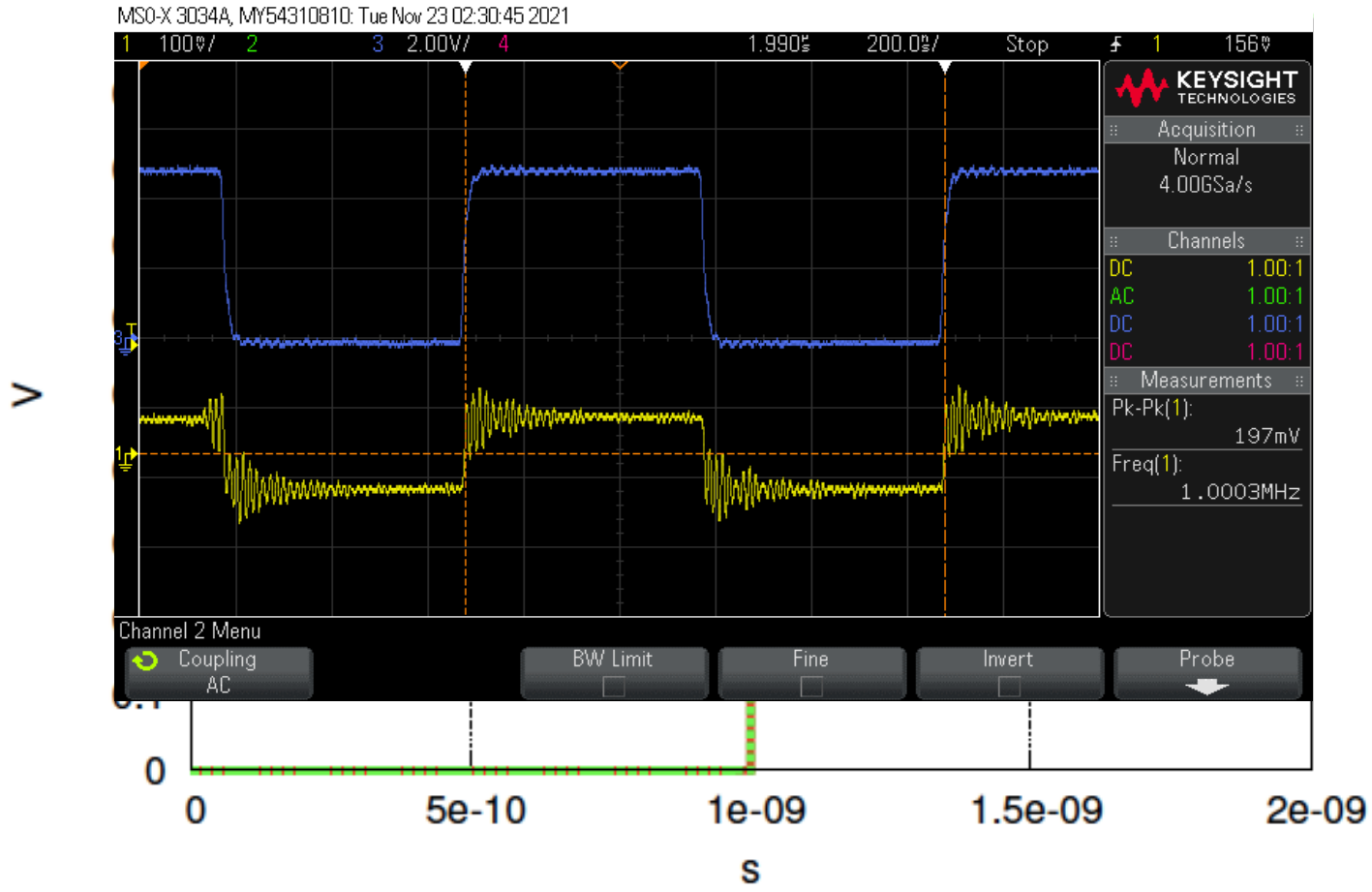
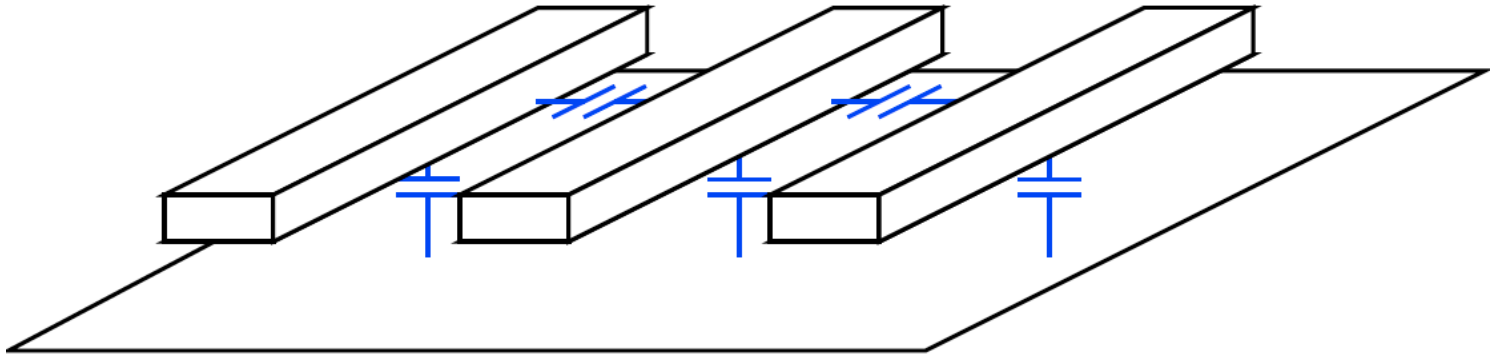


*** spice deck for cell test_cap_undriven{sch} from library test



Good (?) Capacitance

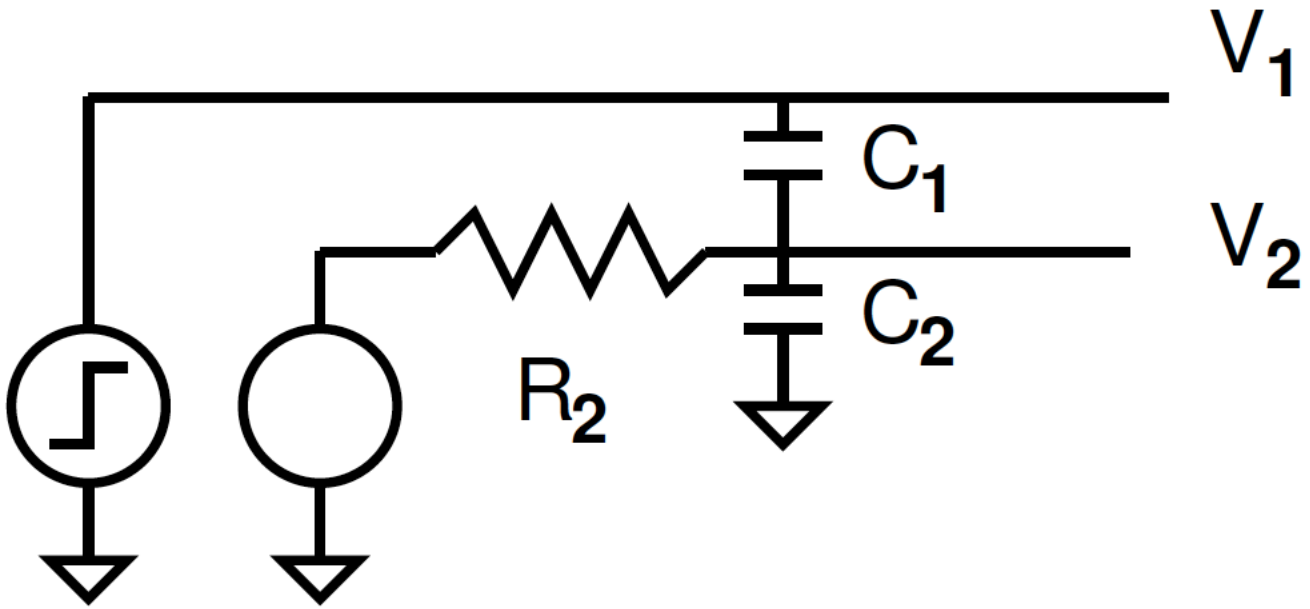
- High capacitance to ground plane (C_2)
  - Limits node swing from adjacent conductors



$$V_2 = \left(\frac{C_1}{C_1 + C_2} \right) V_1$$

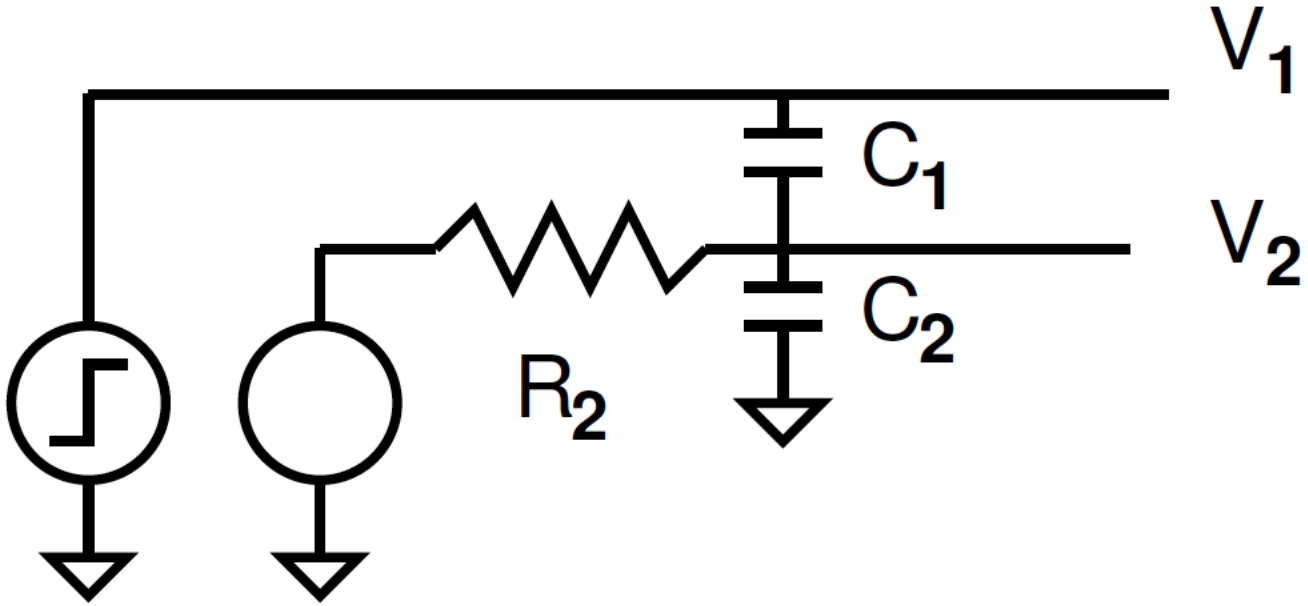
Driven Adjacent Wire (preclass 2)

- What happens when neighbor line is driven?

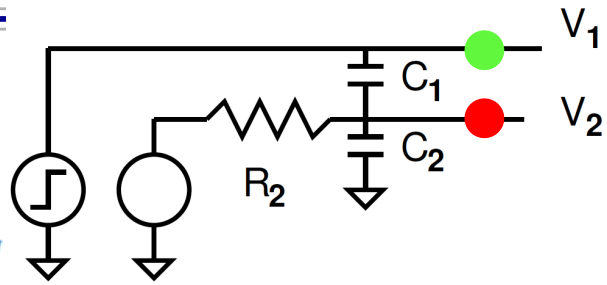


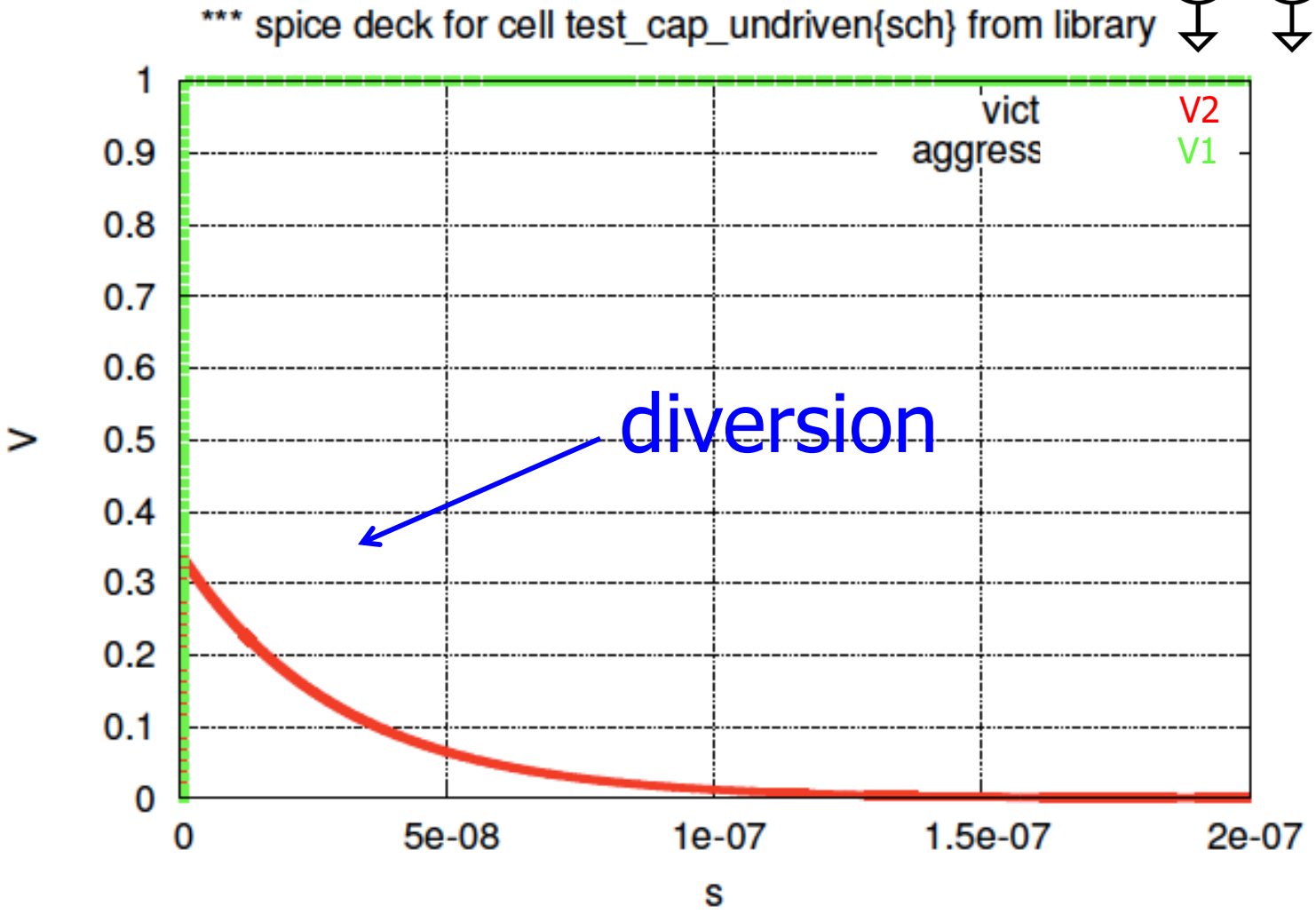
Driven Adjacent Wire

- What happens when neighbor line is driven?
  - Recovers with time constant: $R_2(C_1+C_2)$



Spice: R_2=1K, C_1=10pF, C_2=20pF





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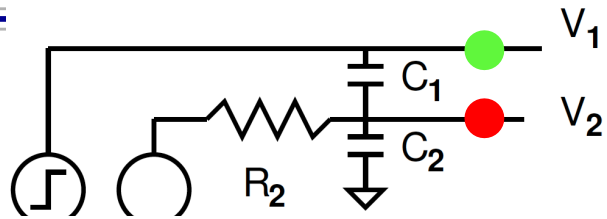
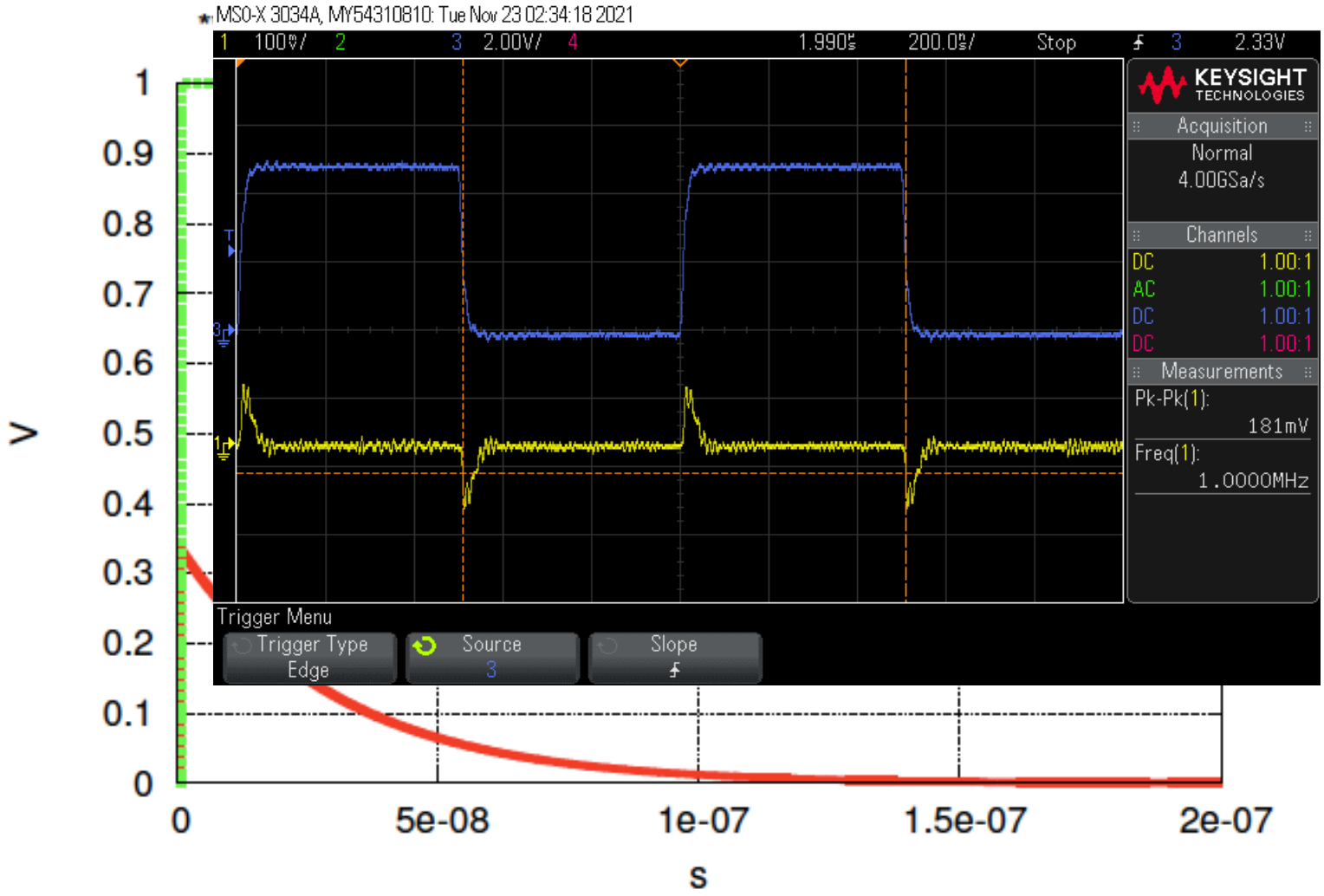
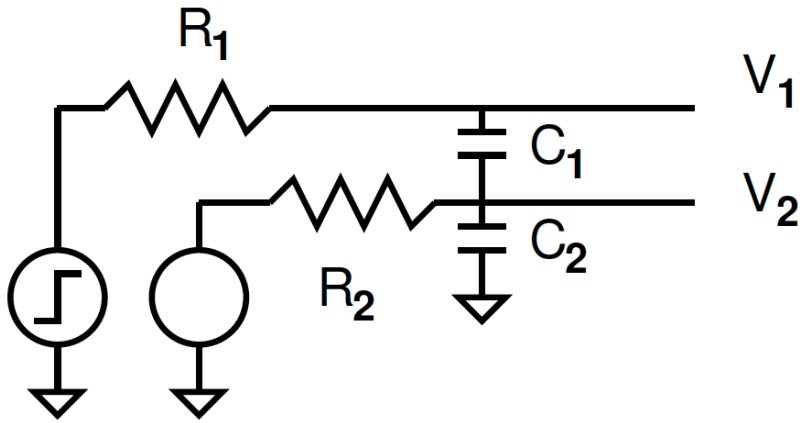




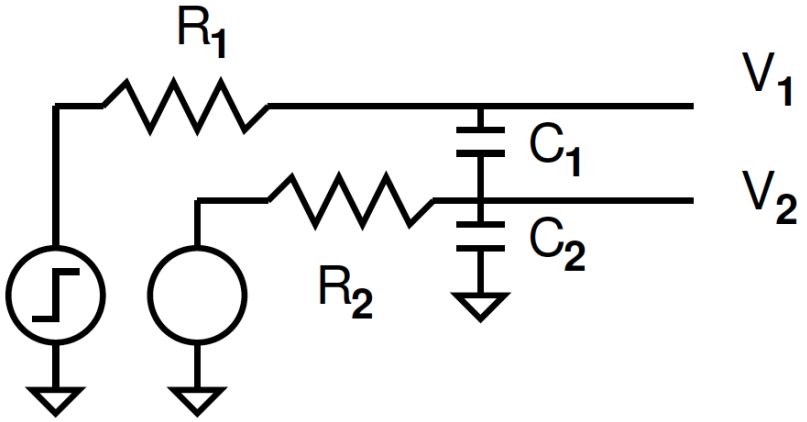
Magnitude of Noise on Driven Line (preclass 3)

- Magnitude of diversion depends on relative time constants
  - $\tau_1 << \tau_2$
  - $\tau_1 >> \tau_2$
  - $\tau_1 \sim = \tau_2$

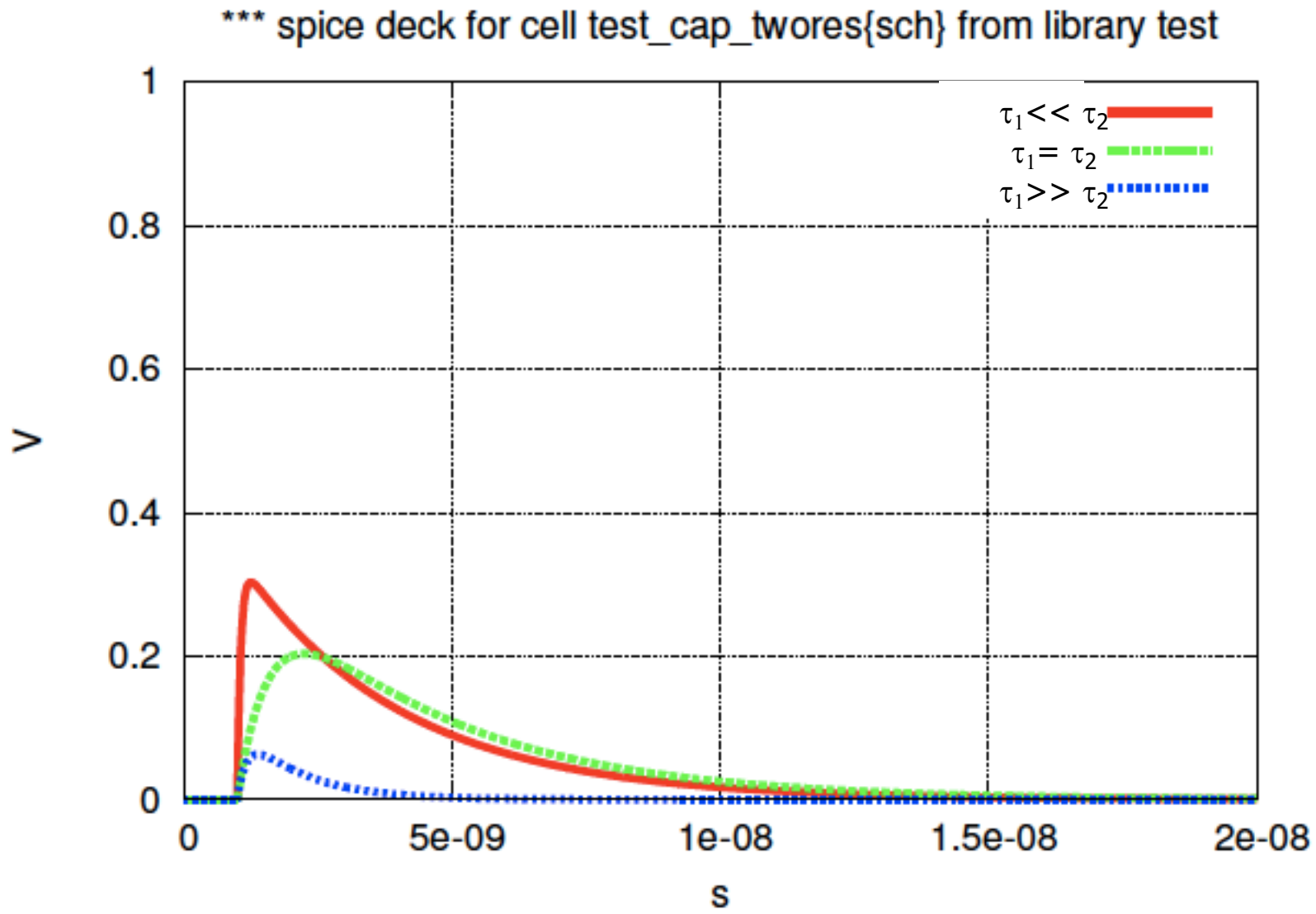


Magnitude of Noise on Driven Line

- Magnitude of diversion depends on relative time constants
  - $\tau_1 << \tau_2$
    - full diversion, then recover
  - $\tau_1 >> \tau_2$
    - Drive capacitor (C_2) faster than line 1 can change
      - little noise
  - $\tau_1 \sim= \tau_2$
    - Somewhere in between

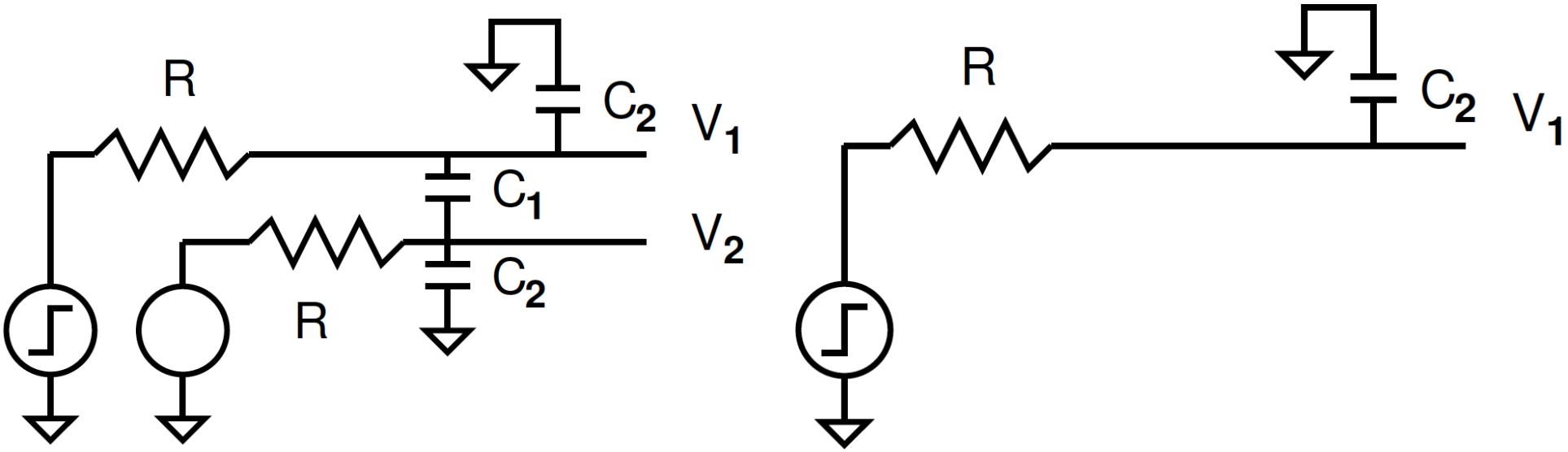


Spice: C_1=1pF, C_2=2pF



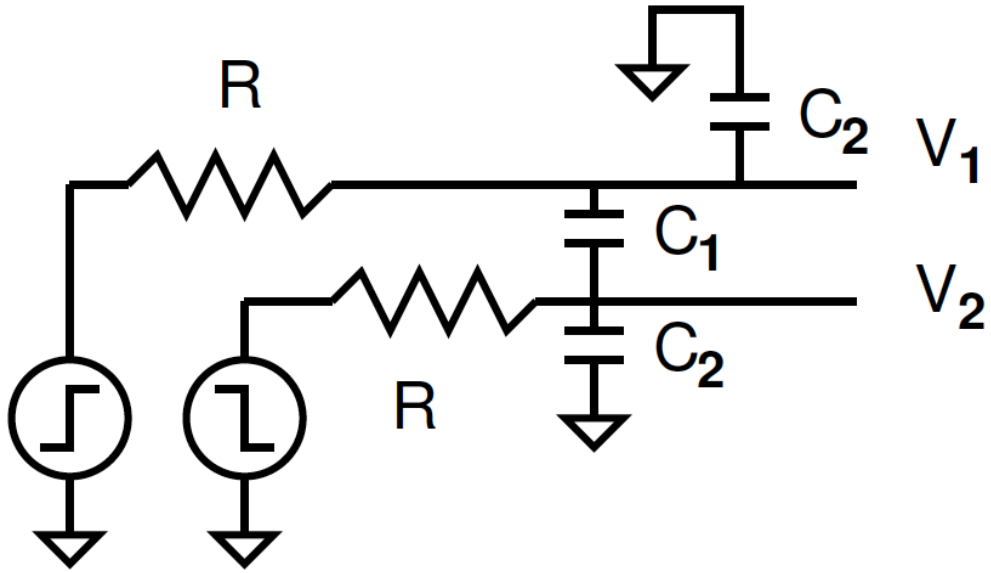
Switching Line with Finite Drive

- What impact does the presence of the neighbour line have on the **switching** line?
  - All previous questions were about noise on non-switching wire
  - Finite drive (R)



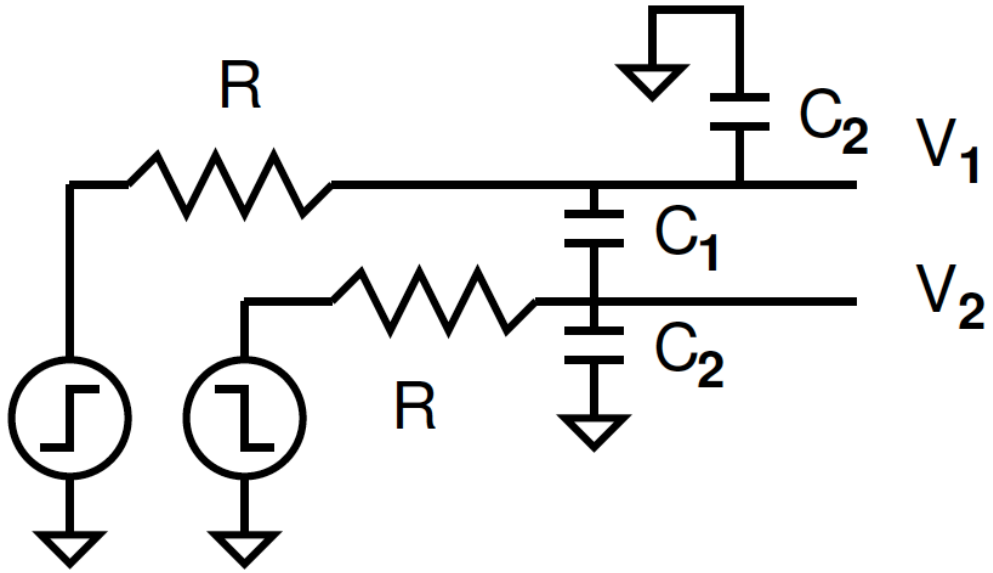
Simultaneous Transition

- What happens if lines transition in opposite directions?



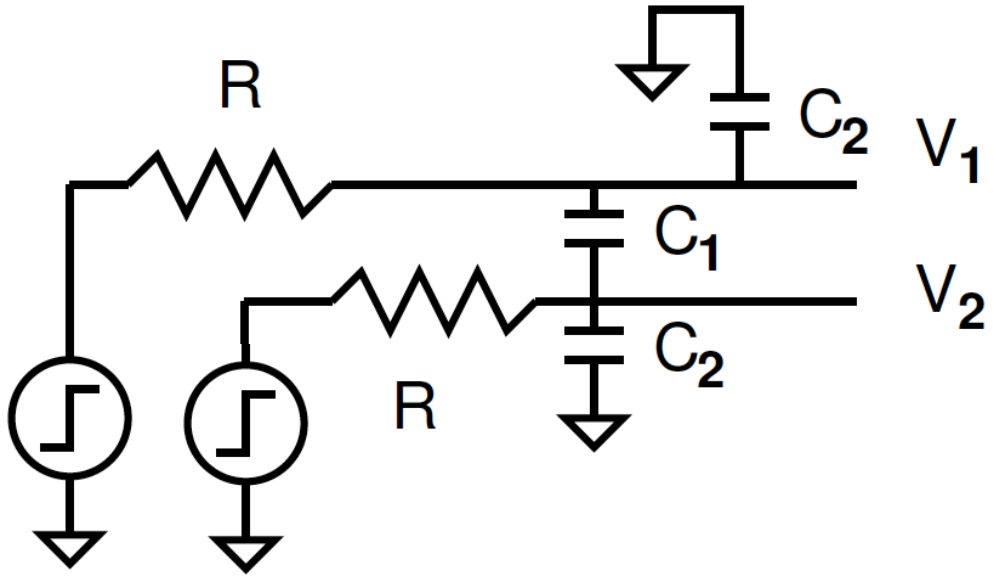
Simultaneous Transition

- What happens if lines transition in opposite directions?
  - Must charge C_1 by 2V
  - Or looks like $2C_1$ between wires



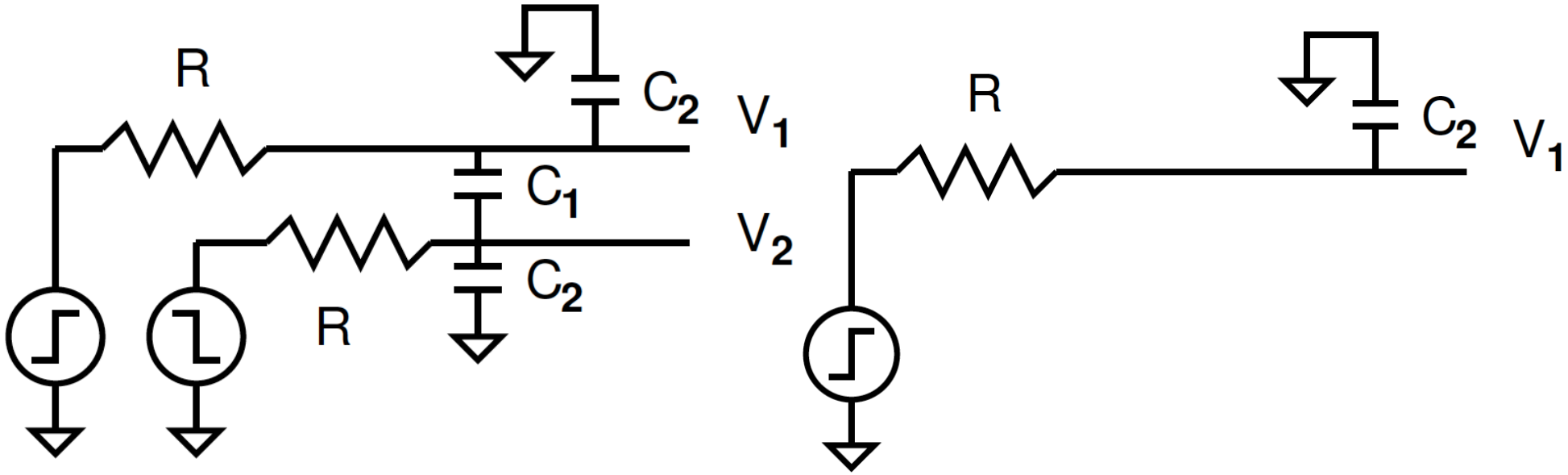
Simultaneous Transition

- What happens if lines transition in same direction?

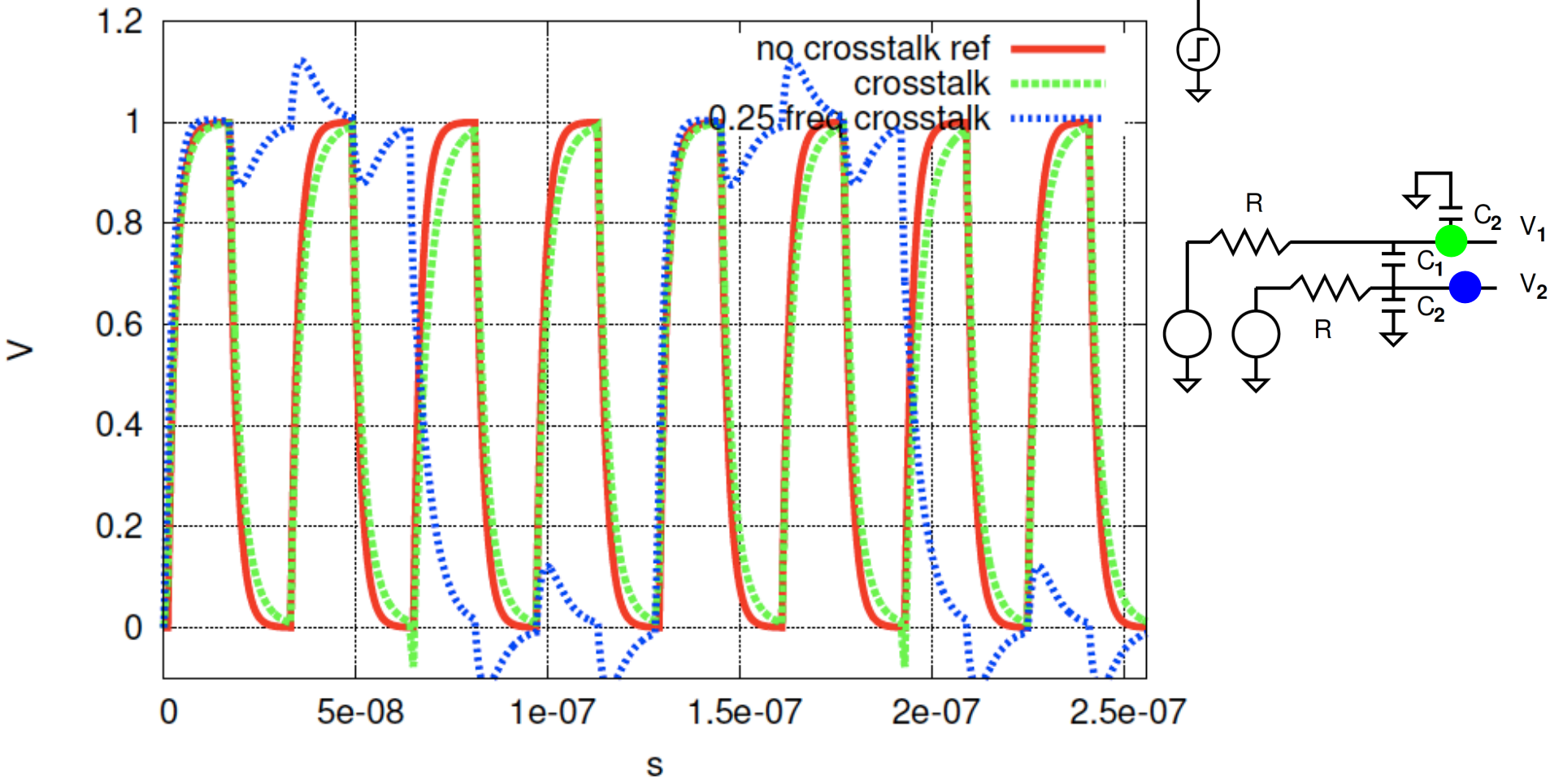


Simulation

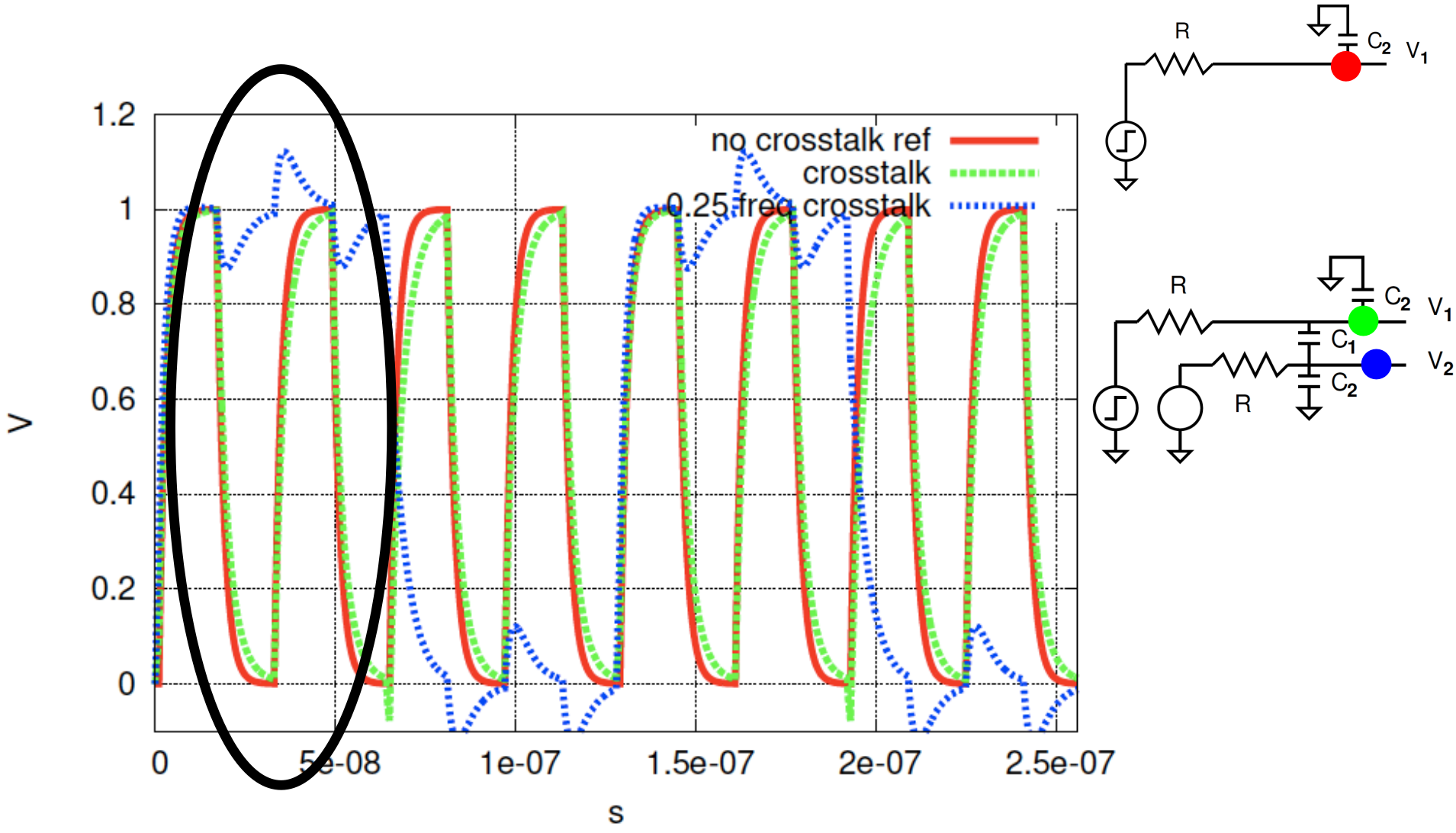
- V_2 switching at ¼ frequency of V_1
- No crosstalk reference case where no V_2



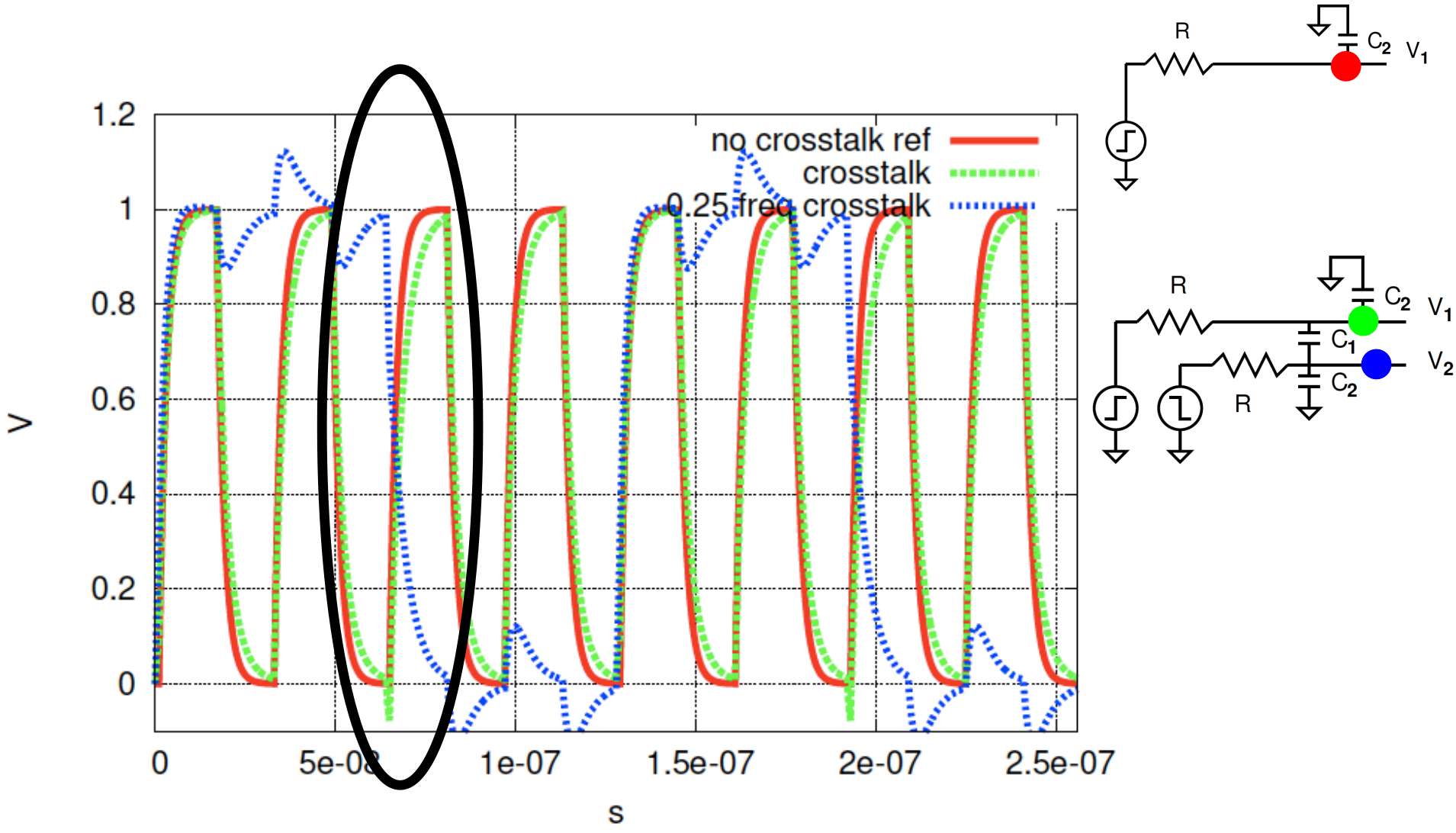
Crosstalk Neighbor Simulations



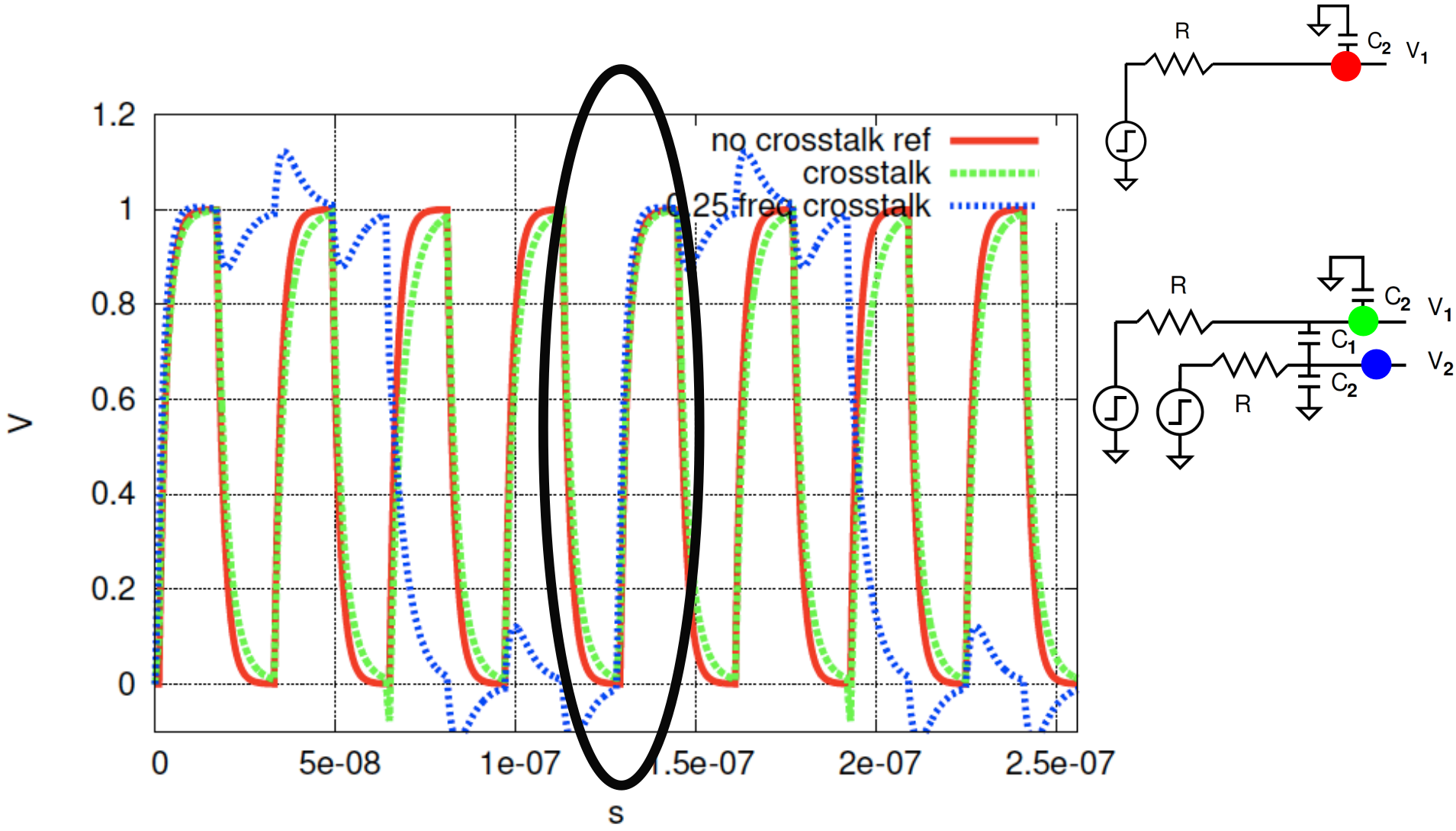
Crosstalk Neighbor Simulations



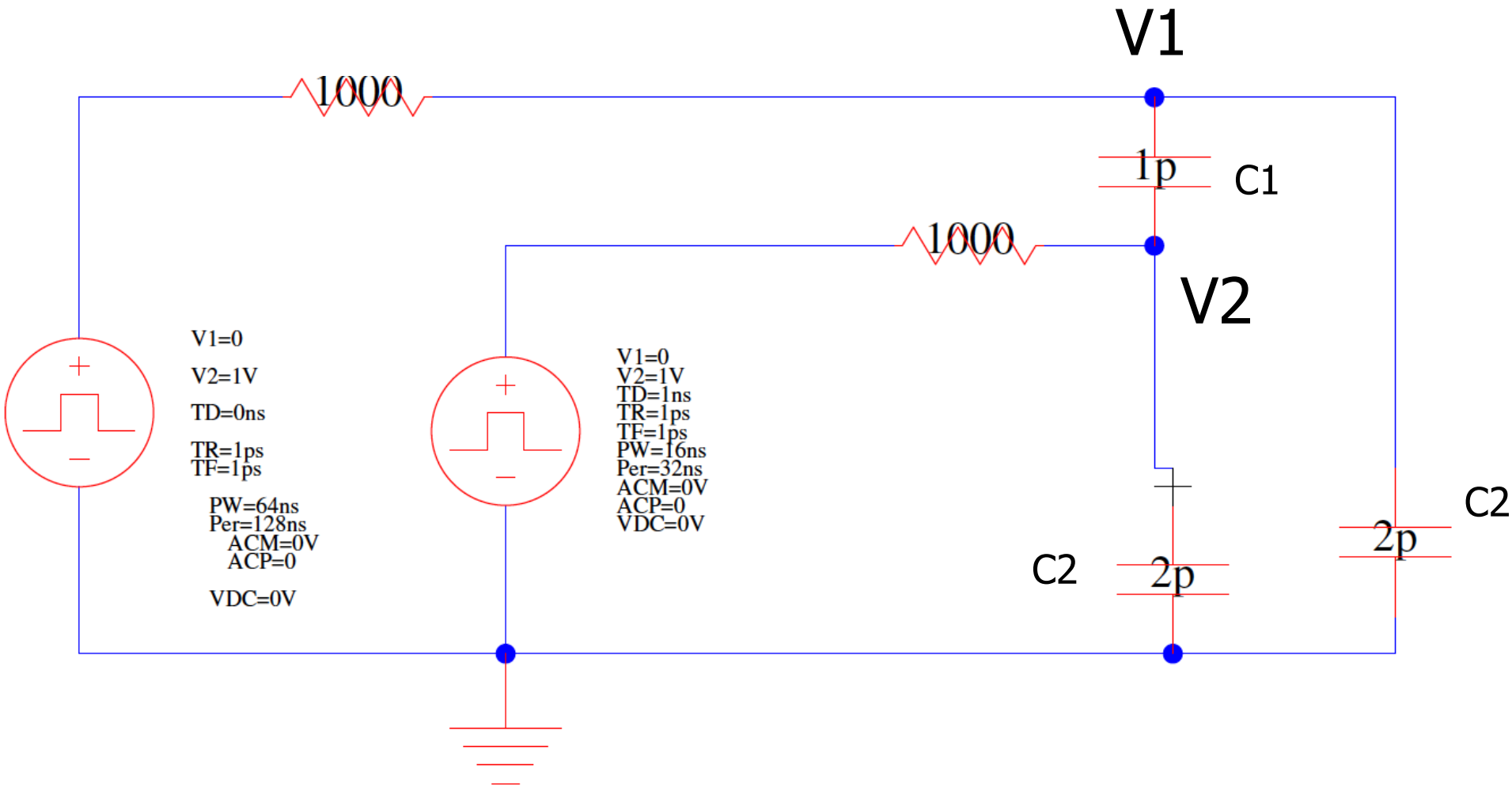
Crosstalk Neighbor Simulations



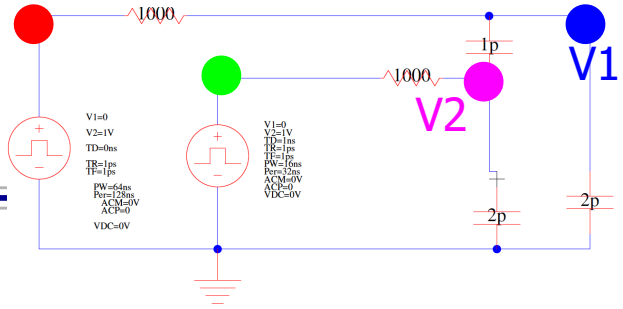
Crosstalk Neighbor Simulations

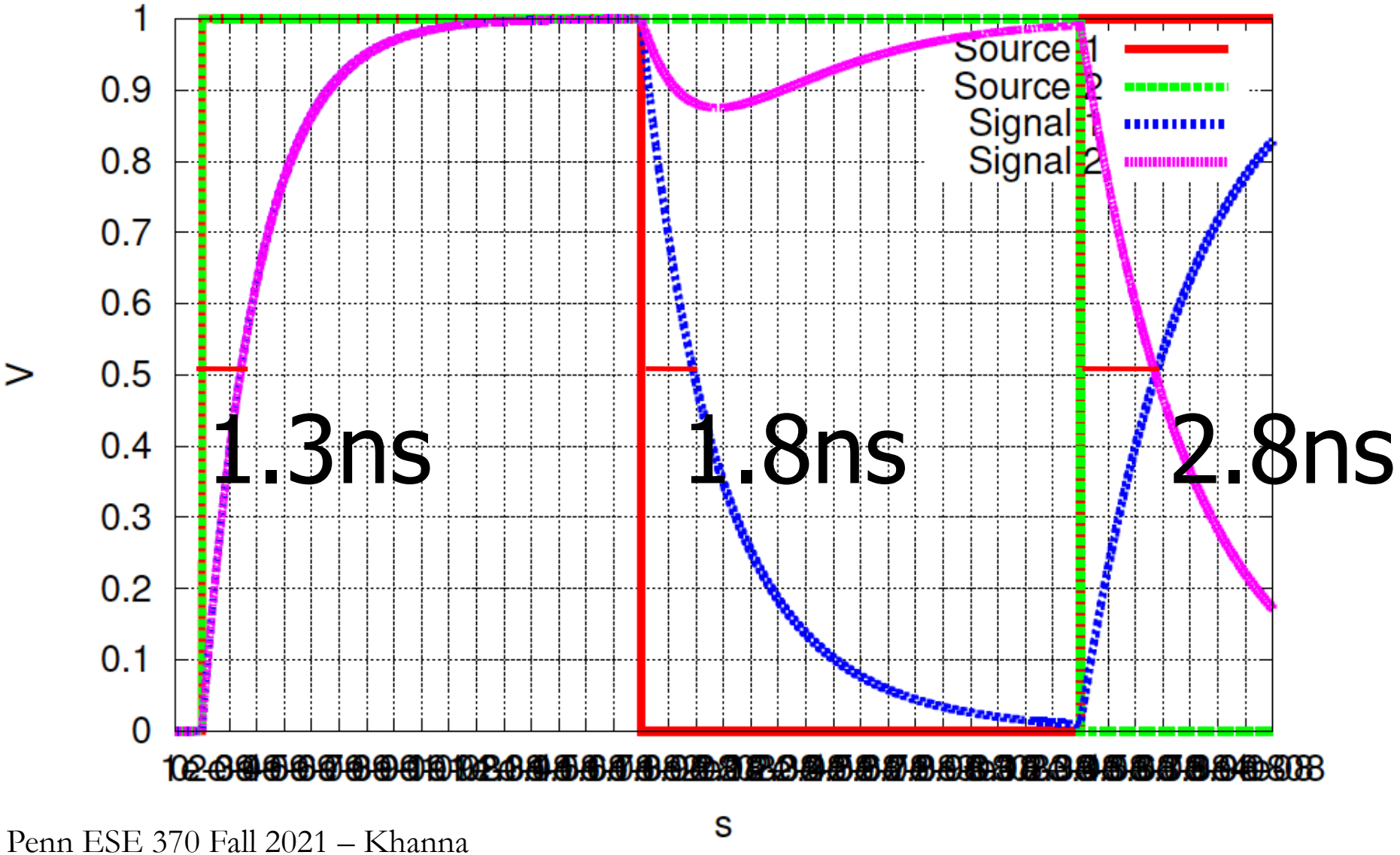


Simulation Setup



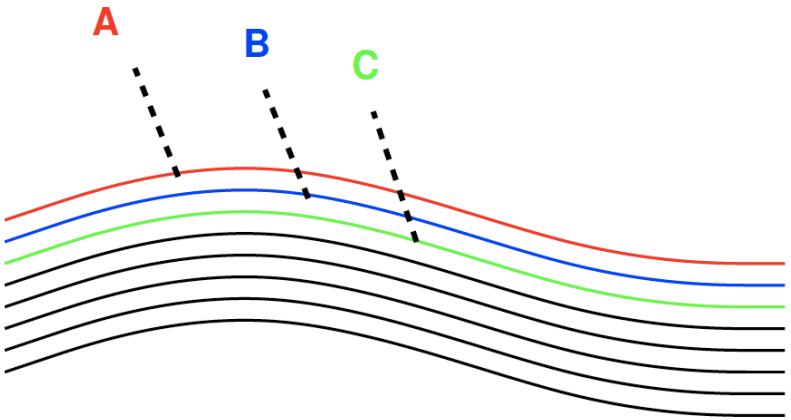
Crosstalk Simulation

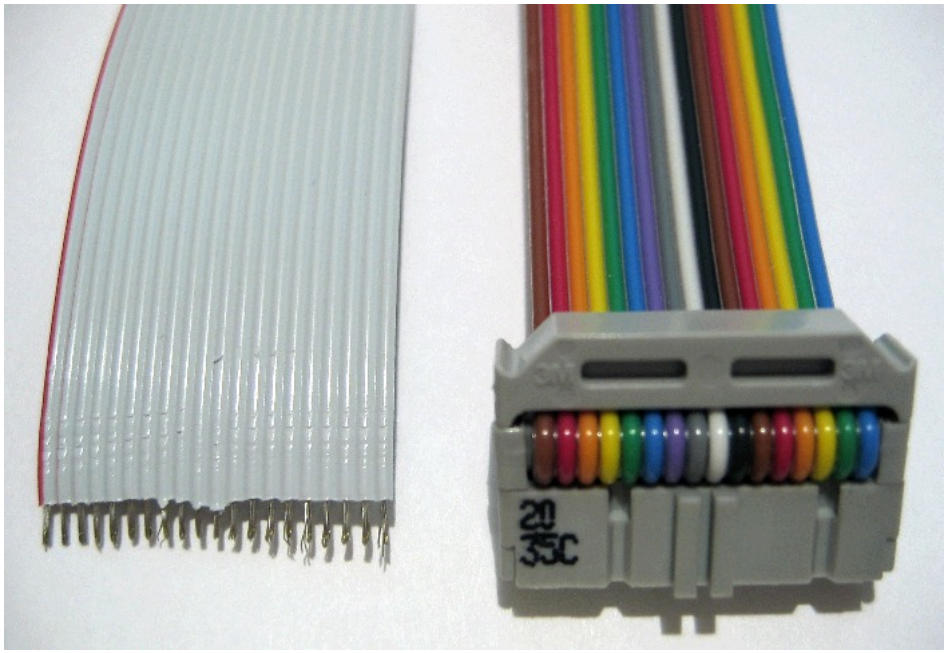




Where Does it Arise?

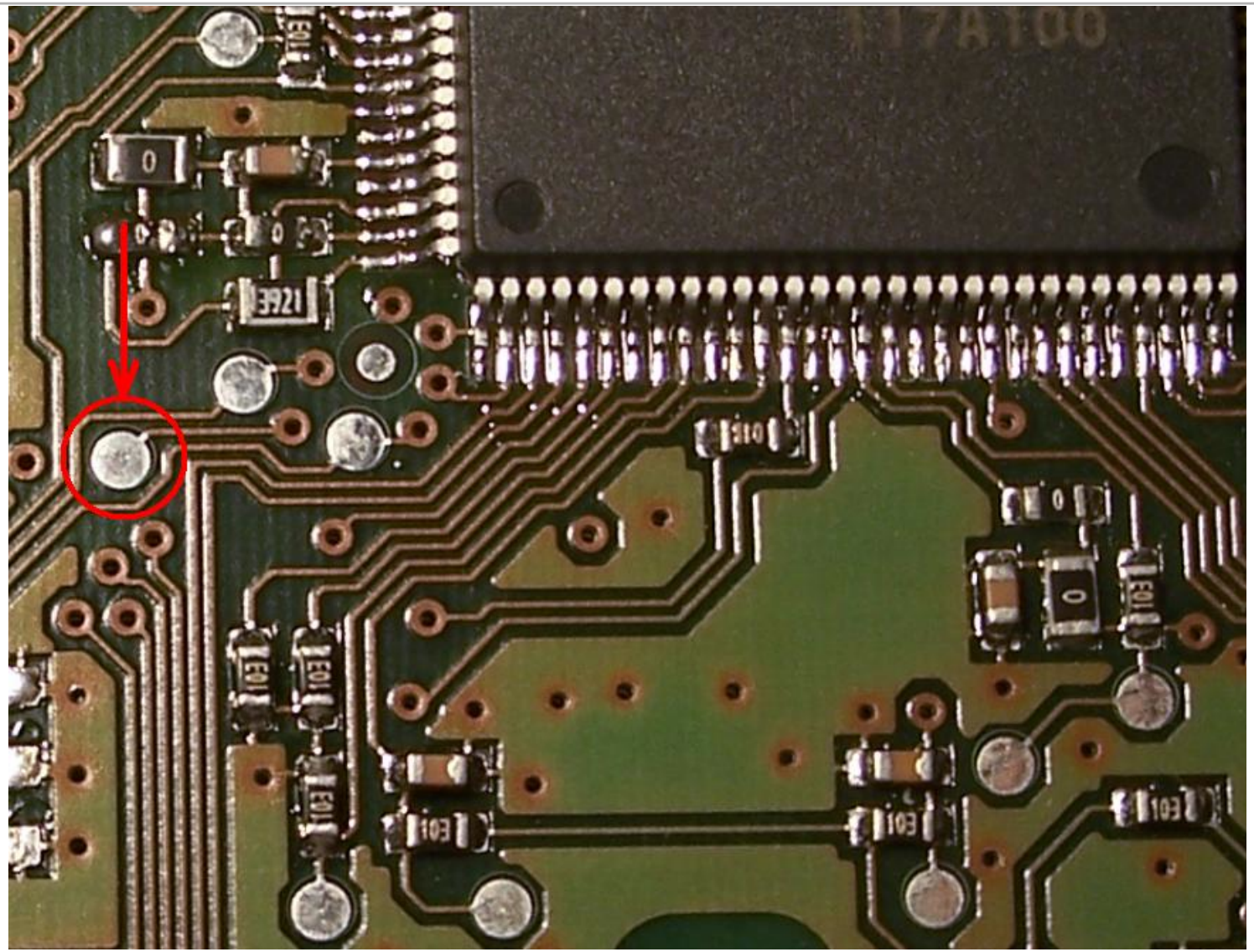
Cables and PCB Wires





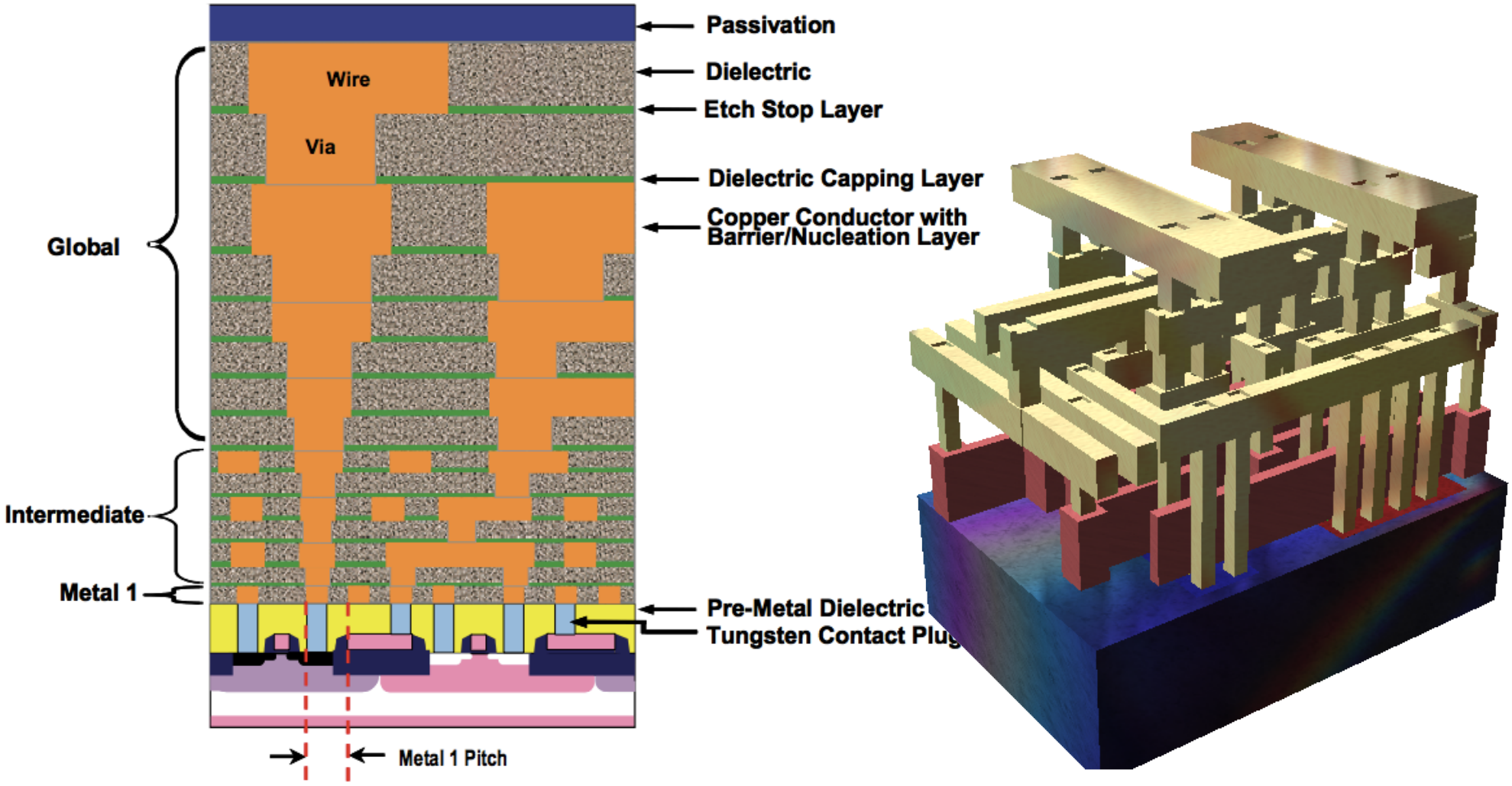
Source; http://en.wikipedia.org/wiki/File:Flachbandkabel.jpg

Printed Circuit Board

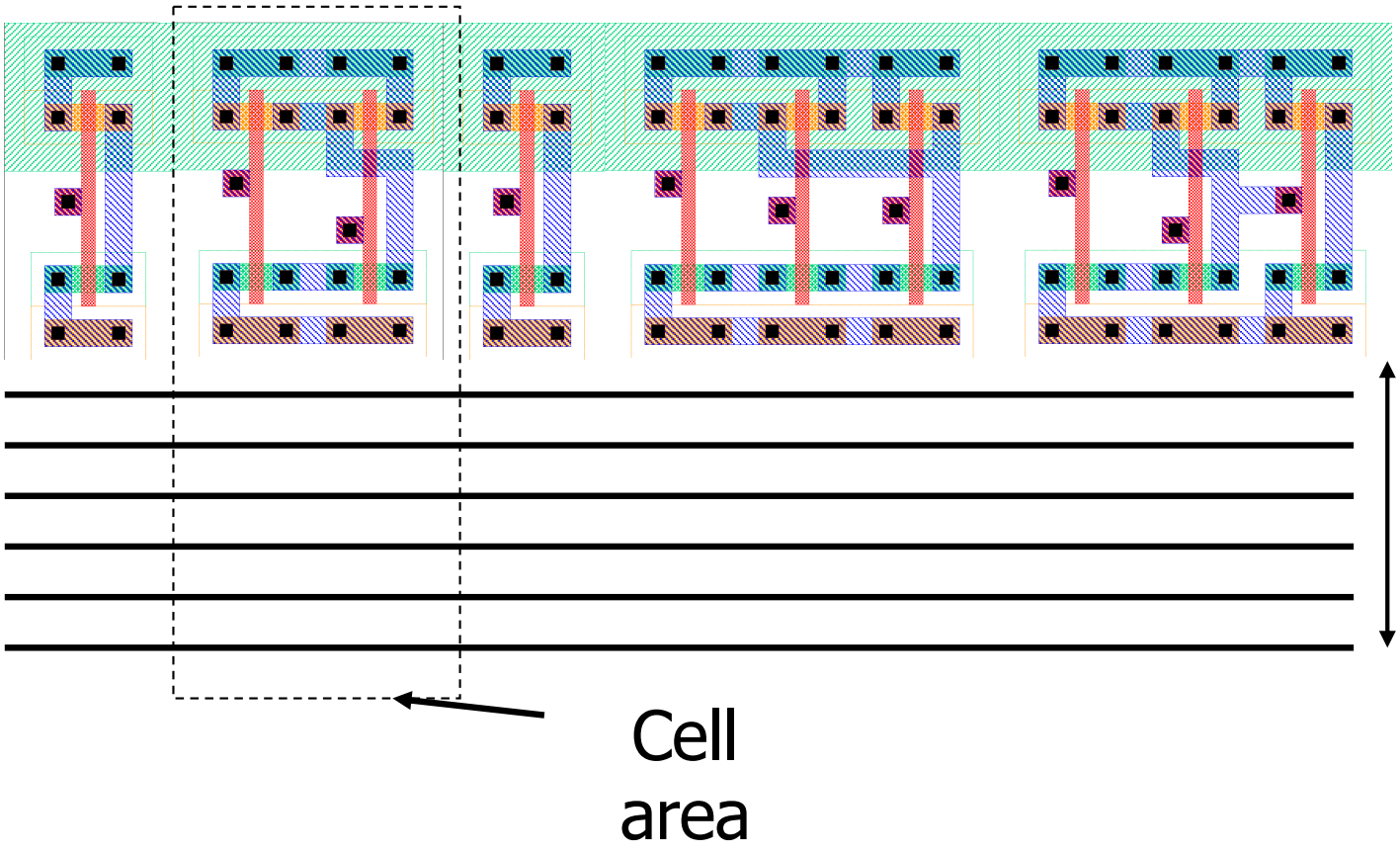


Source: http://en.wikipedia.org/wiki/File:Testpad.JPG

Interconnect Cross Section

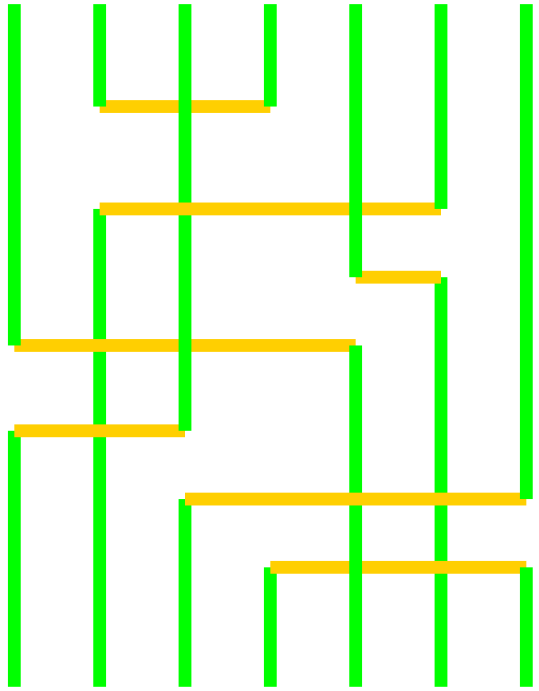


Standard Cell Area



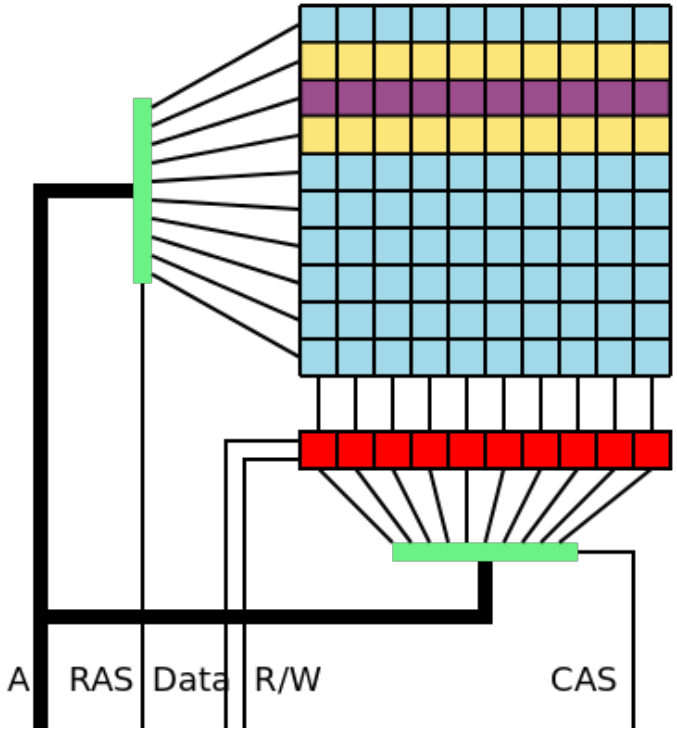
Wires

- Will be capacitively coupled to many adjacent wires of varying degrees



Rowhammer Attack

- Smaller and higher density DRAMs leads to increase electromagnetic interactions between memory cells
- Rapid wordline switching can affect adjacent words causing them to flip



Noise Implications

- *So what* if we have noise?
- If the noise is less than the noise margin, nothing happens
- Static CMOS logic will eventually settle to correct output even if disturbed by large noise spikes
  - But glitches cause extra delay
  - Also cause extra power from false transitions
- Dynamic logic never recovers from glitches
  - Can't correct mid-cycle, need precharge nodes
- Memories and other sensitive circuits also can produce the wrong result

Wire Engineering

- Goal: achieve delay, area, power goals with acceptable noise
- Degrees of freedom:

Wire Engineering

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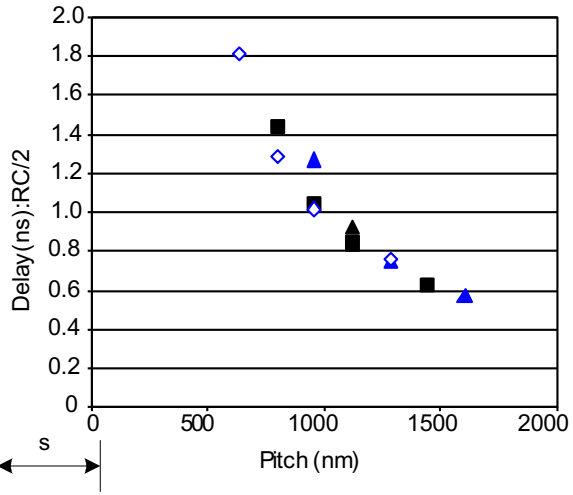
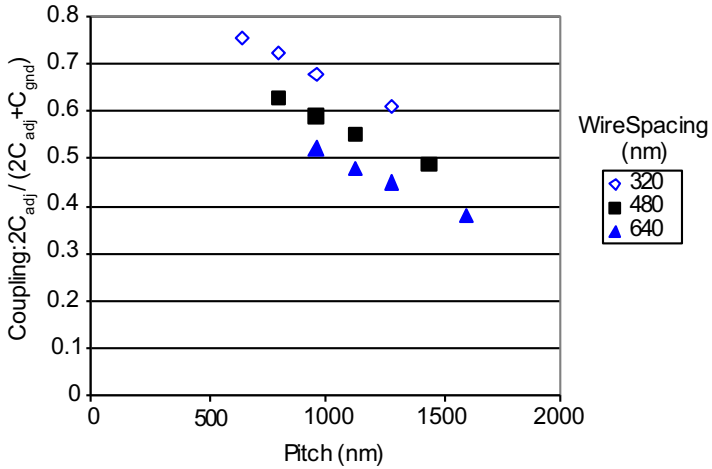
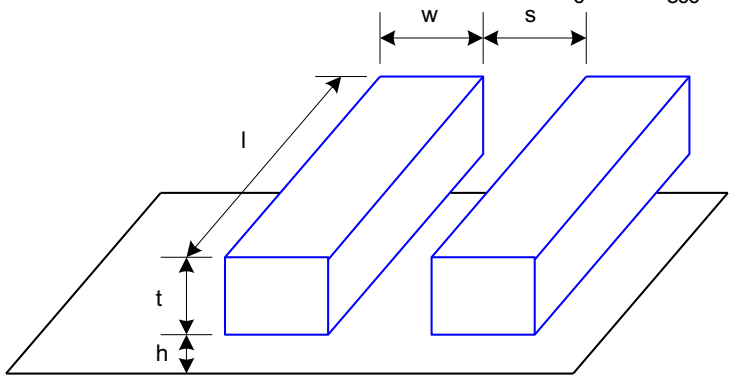
  - Width
  - Spacing
  - Layer

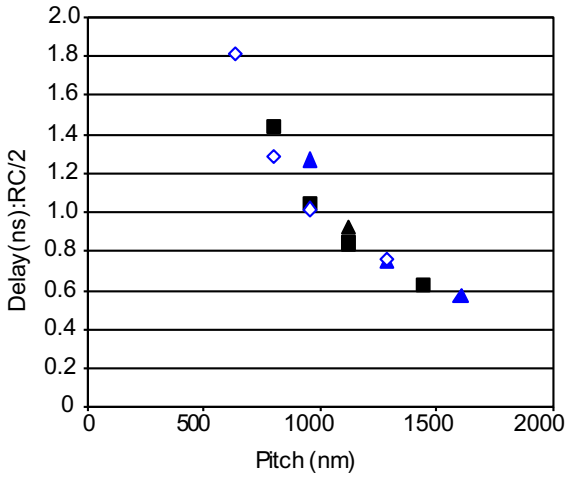


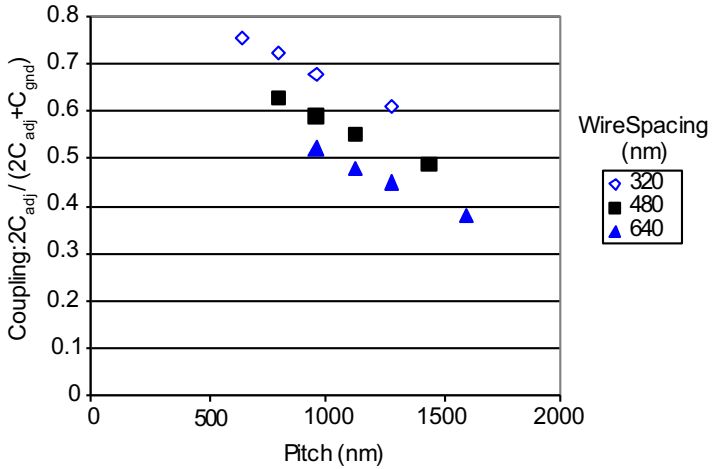


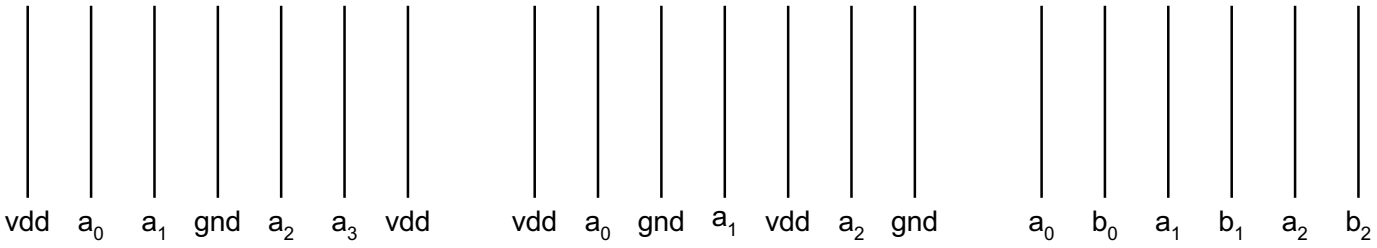


Wire Engineering

- Goal: achieve delay, area, power goals with acceptable noise
- Degrees of freedom:
  - Width
  - Spacing
  - Layer
  - Shielding







Idea

- Capacitance is everywhere
- Especially between adjacent wires
- Will get "noise" from crosstalk
- Clocked and driven wires
  - Slow down transitions
- Undriven wires voltage changed
- Can cause spurious transitions

Admin

- Monday 11/29 in Ketterer again, no lecture
- Project 2
  - Due Friday 12/3
  - Milestone feedback:
    - Don't forget about the clock
      - Controls registers to allow inputs to change at any time, but only affect memory at clk edge
      - Non-overlapping clocks!
    - Get SRAM column/row working first to make testing/debugging smoother
    - Can use a min size cell, just have to justify why that sizing