ESE370: Circuit-Level Modeling, Design, and Optimization for Digital Systems

Lec 33: December 3, 2021

Transmission Lines Termination

Transmission Line Agenda

- ~~See in action in lab~~
- ~~Where transmission lines arise?~~
- ~~General wire formulation~~
- ~~Lossless Transmission Line~~
- ~~Impedance~~
- End of Transmission Line?
  - Open, short, matched
- Termination
- Discuss Lossy
- Implications

Reminder: Propagation

- Signal propagates as wave down transmission line
  - Delay linear in wire length, if resistance negligible
  - Solution:

$$V(x,t) = A + Be^{x-wt}$$

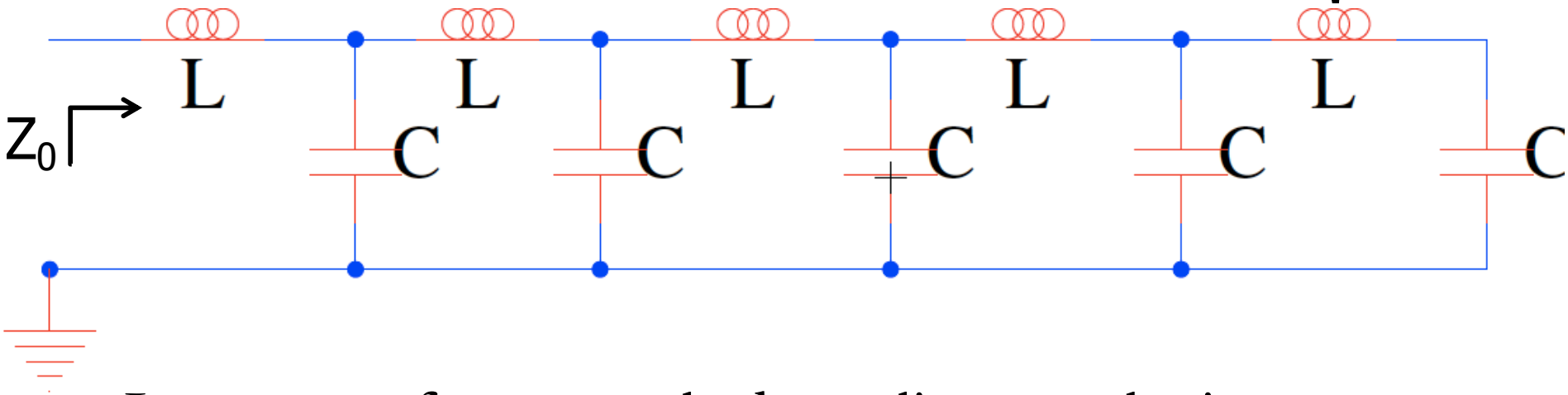
  - Rate of propagation (characteristic frequency), w:

$$w = \sqrt{\frac{1}{LC}} = \frac{c}{\sqrt{\varepsilon_r \mu_r}}$$

Infinite Lossless Transmission Line

- Transmission line looks like resistive load

$$Z_0 = \sqrt{\frac{L}{C}}$$



- Input waveform travels down line at velocity
  - Without distortion

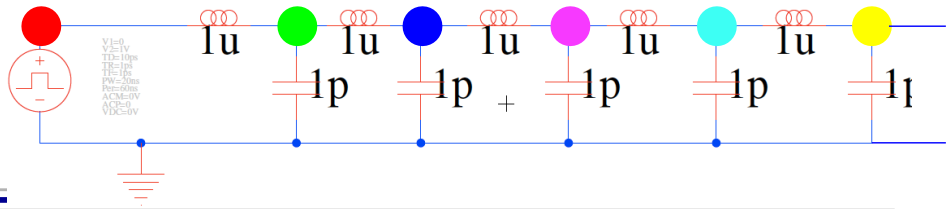
$$w = \frac{1}{\sqrt{LC}}$$

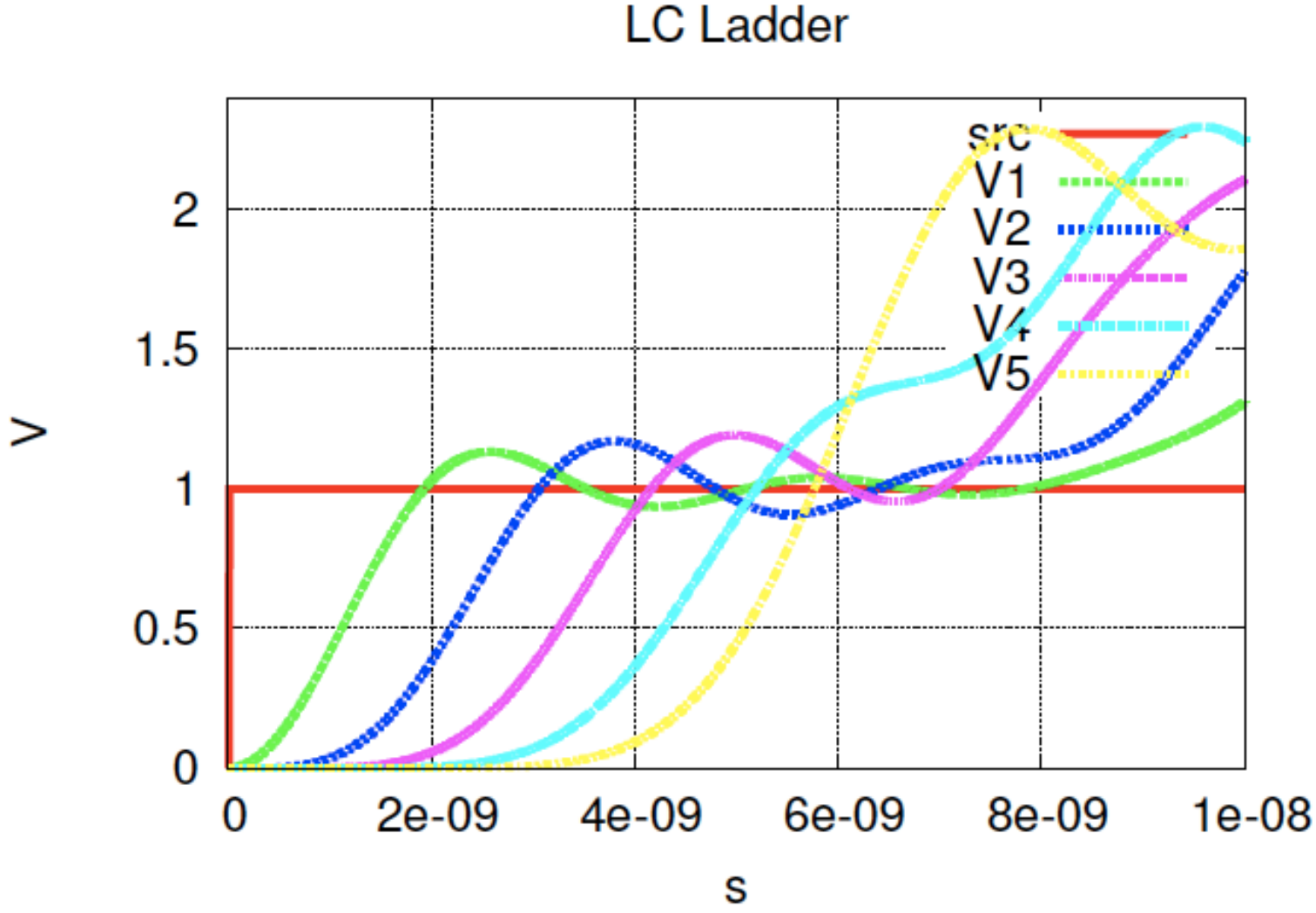
End of Line

- What happens at the end of the transmission line?
  - Short Circuit
  - Terminate with $R=Z_0$
  - Open Circuit

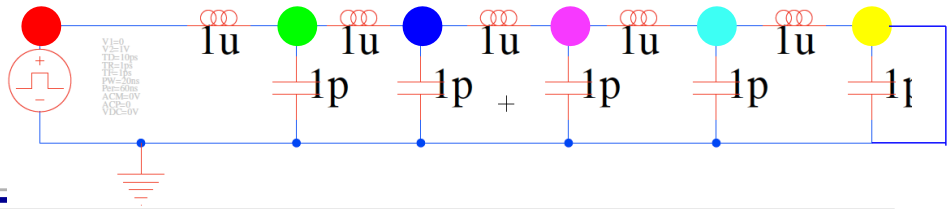
- What did the reflections look like in each case in lab?

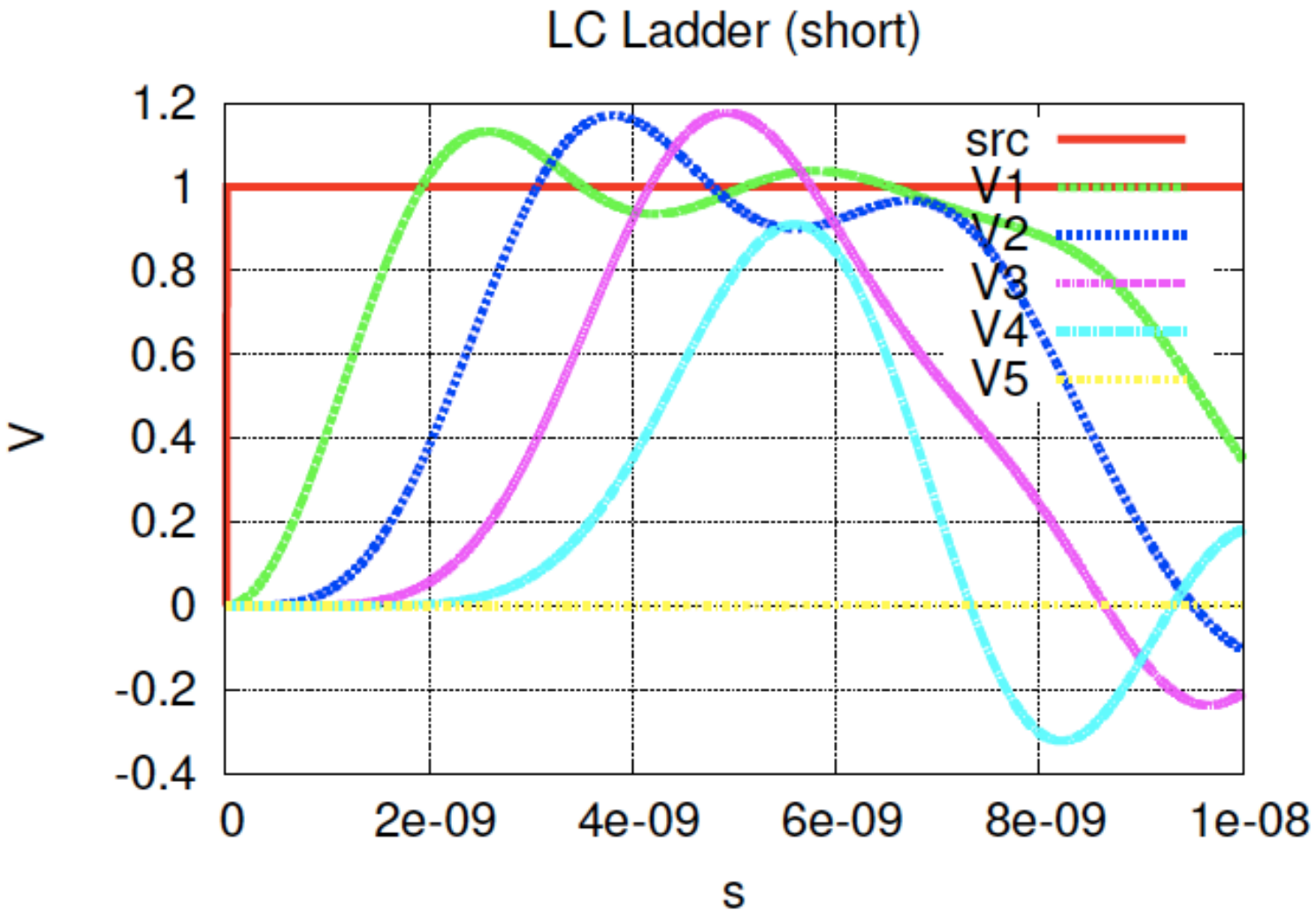
Open


1u
1u
1u
1u
1u
1p
1p
1p
1p
1p

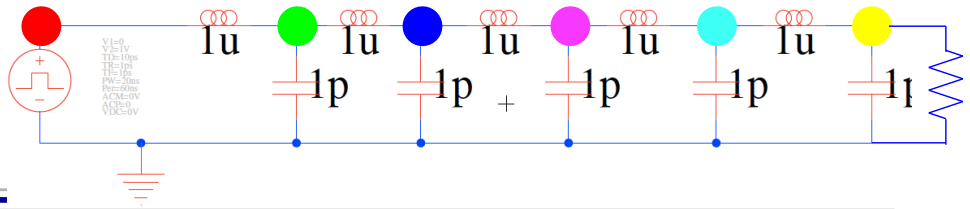

LC Ladder
src
V1
V2
V3
V4
V5
2
1.5
1
0.5
0
V
0
2e-09
4e-09
6e-09
8e-09
1e-08
s

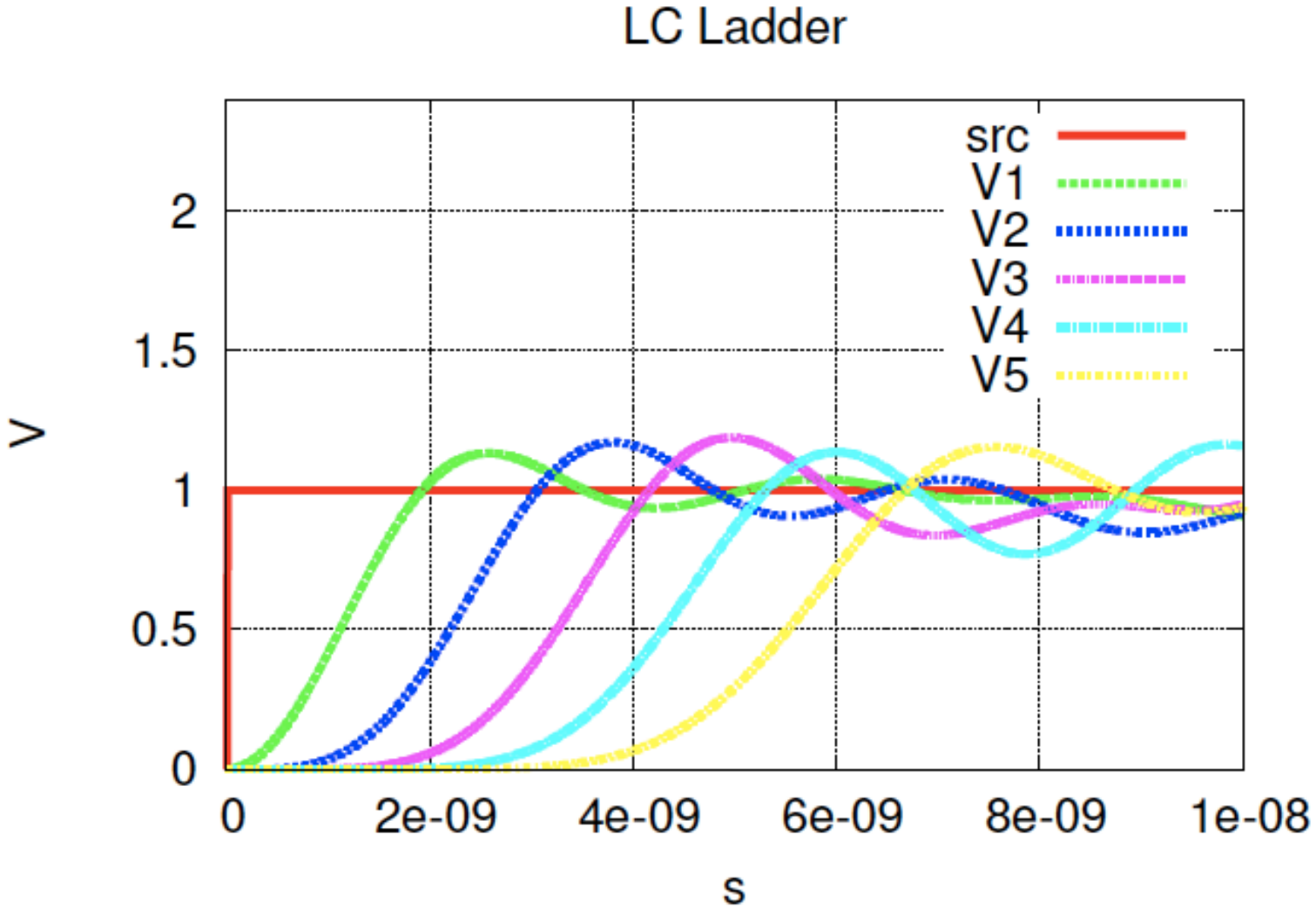
Short


1u
1u
1u
1u
1u
1p
1p
1p
1p
1p


LC Ladder (short)
1.2
1
0.8
0.6
0.4
0.2
0
-0.2
-0.4
V
0
2e-09
4e-09
6e-09
8e-09
1e-08
s
src
V1
V2
V3
V4
V5

Terminate R=Z_0



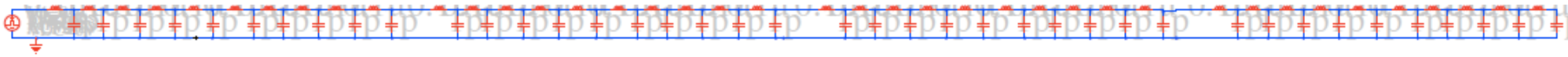


Longer LC (open)

- 40 Stages
- L=100nH
- C=1pF

$$w = \frac{1}{\sqrt{LC}} = \frac{c_0}{\sqrt{\varepsilon_r \mu_r}}$$

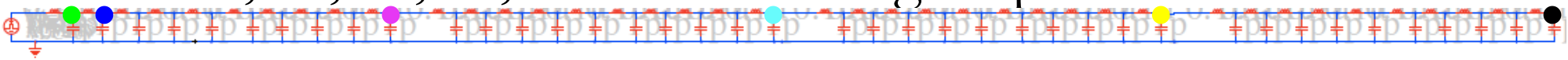
Stage delay? How long to propogate?

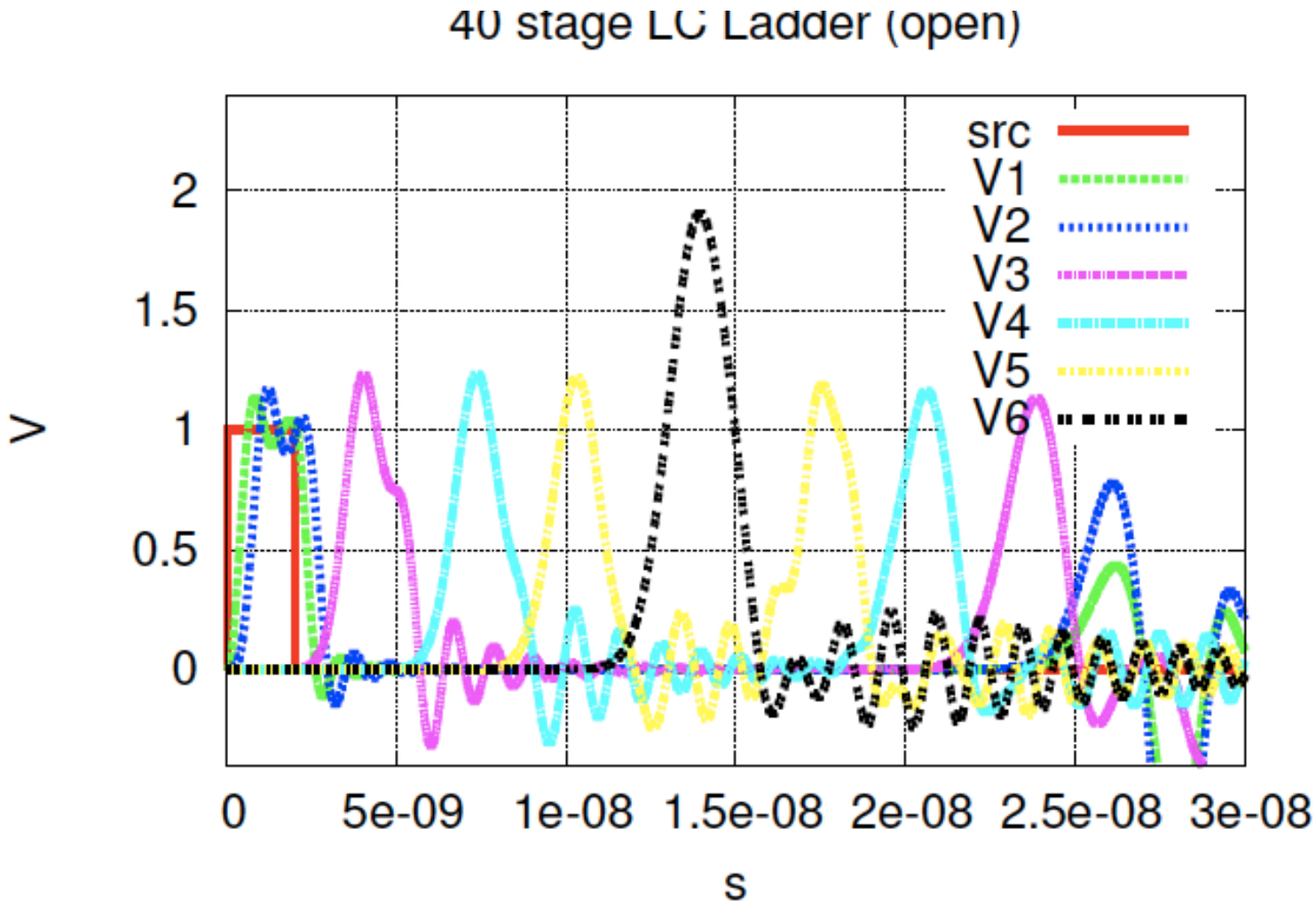


- Drive with 2ns Pulse
- No termination (open circuit)
  - What reflection do we expect?

Pulse Travel RC

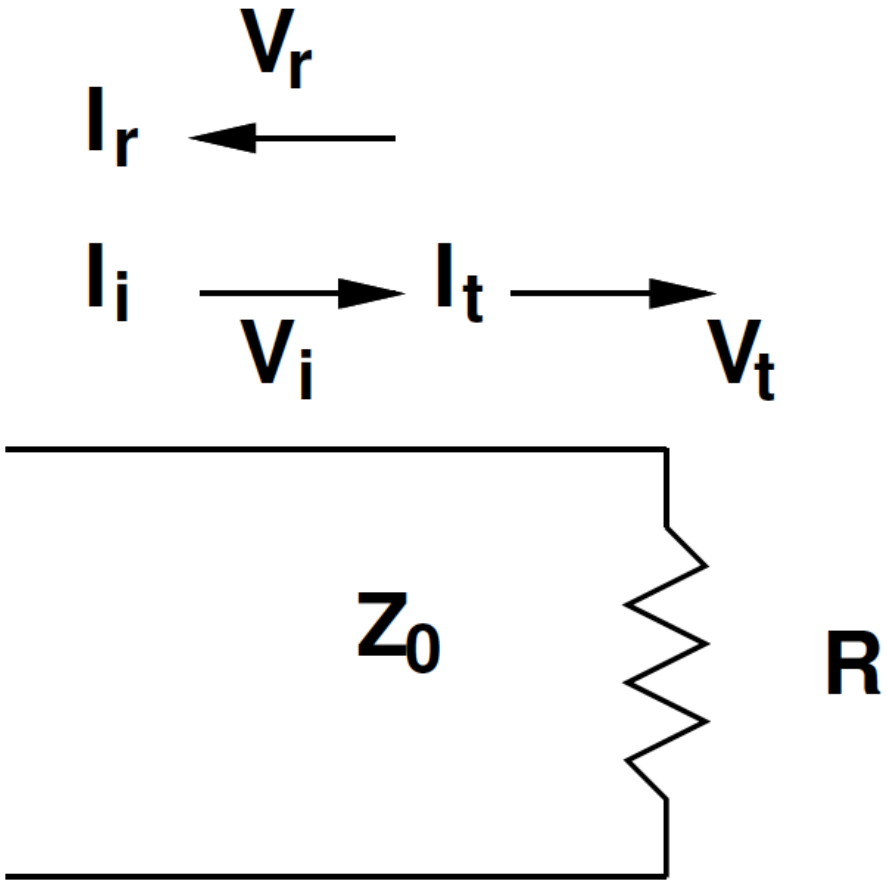
- V1,V3,V4,V5,V6 about 10 stages apart

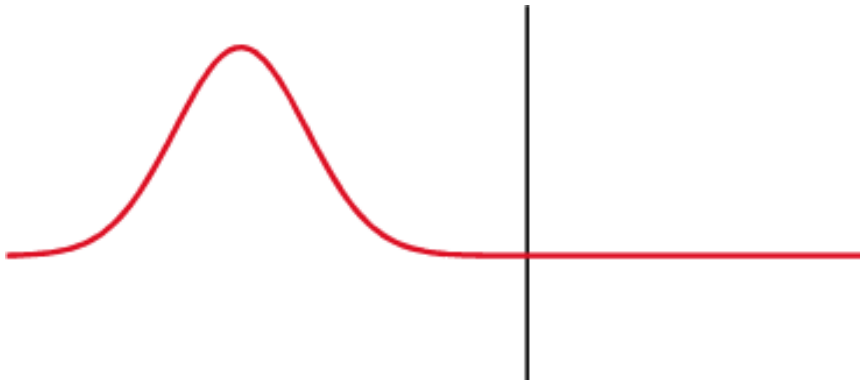




Analyze End of Line

- *I*ncident Wave, *R*eflected Wave, *T*ransverse Wave

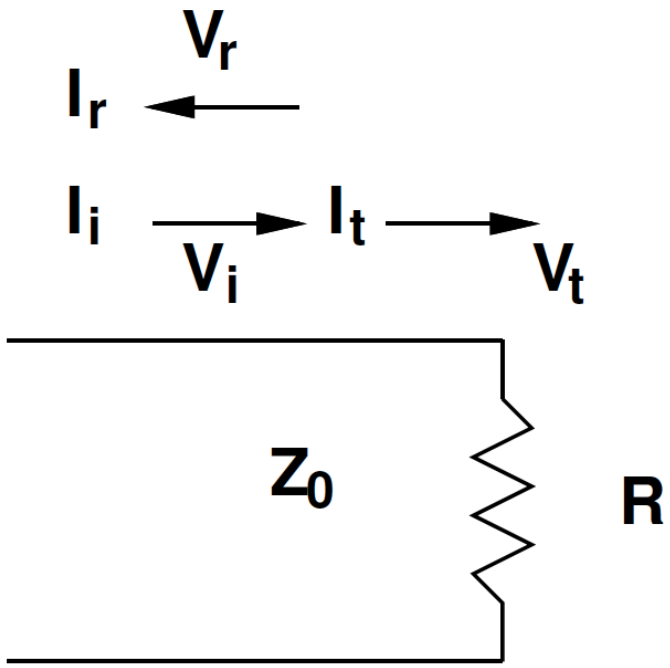




Source: https://en.wikipedia.org/wiki/Reflection_coefficient

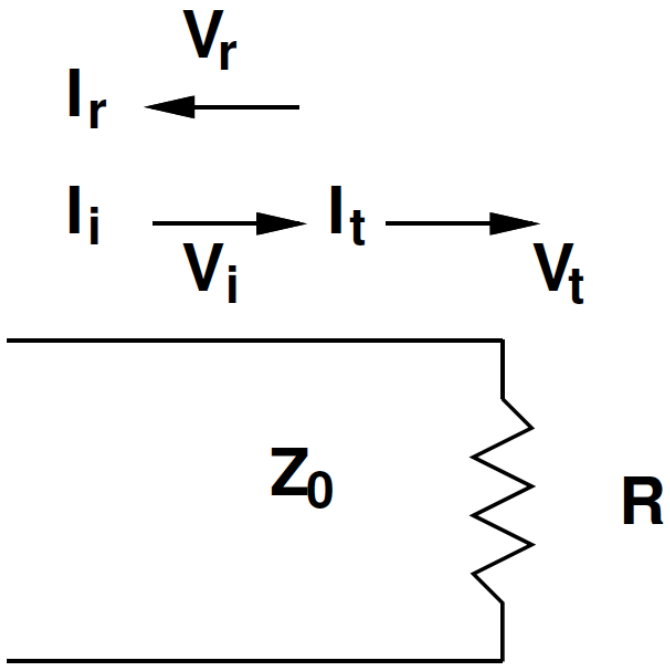
Analyze End of Line

- Incident wave $V_i = I_i \times Z_0$
- @ T-δ V_i is voltage on line
- V_t is what goes forward
  - Voltage seen by end of line at T
- V_r is the reflected voltage that starts moving back towards source at T+δ



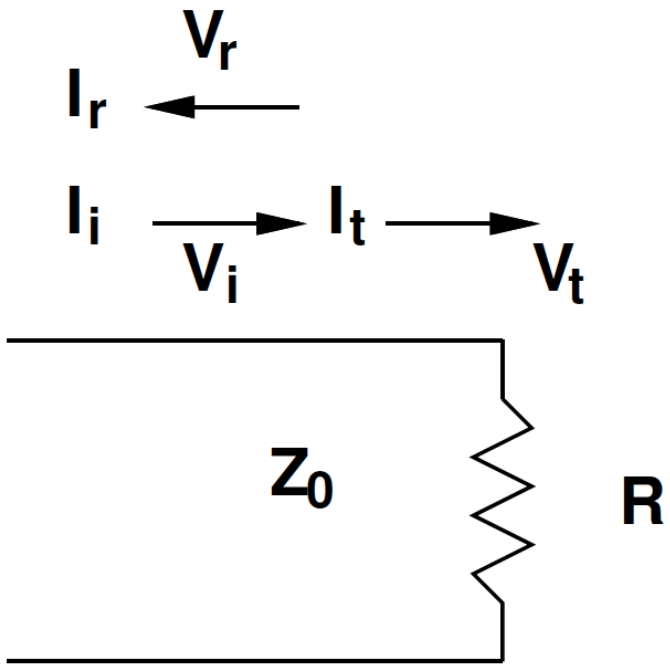
Analyze End of Line (Preclass 1)

- Incident wave $V_i = I_i \times Z_0$
- KCL @ end of line
- KVL @ end of line
- V=IR relationships?
  - Which resistances go with each V?
- Relate all three V's using R, Z_0



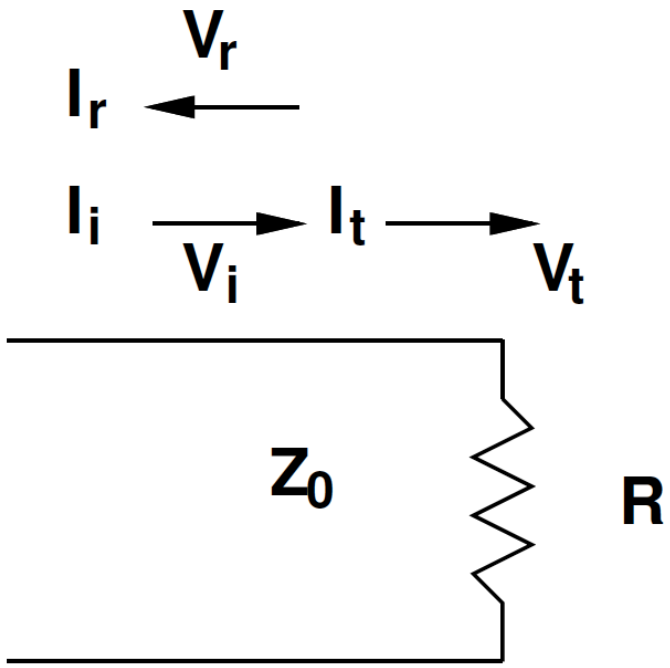
Analyze End of Line (Preclass 1a)

- Incident wave $V_i = I_i \times Z_0$
- KCL @ end of line
  - KCL: $I_i = I_r + I_t$



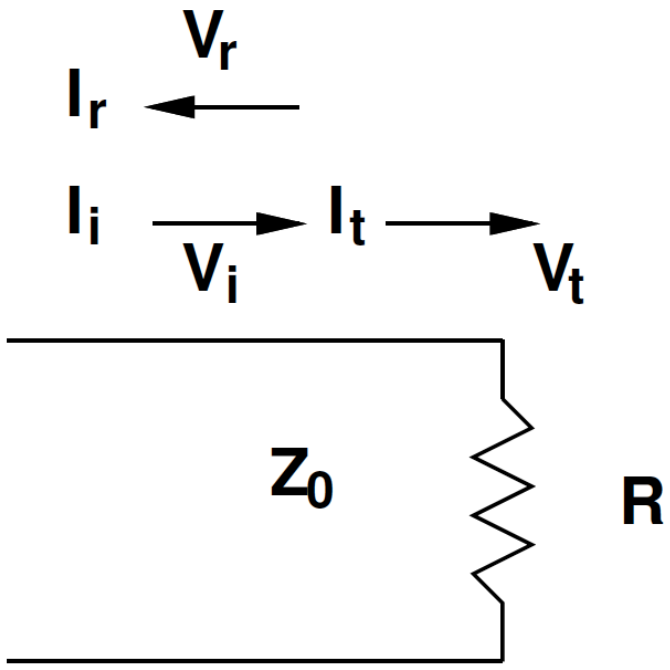
Analyze End of Line (Preclass 1a)

- Incident wave $V_i = I_i \times Z_0$
- KCL: $I_i = I_r + I_t$
- KVL @ end of line
  - KVL: $V_i + V_r = V_t$



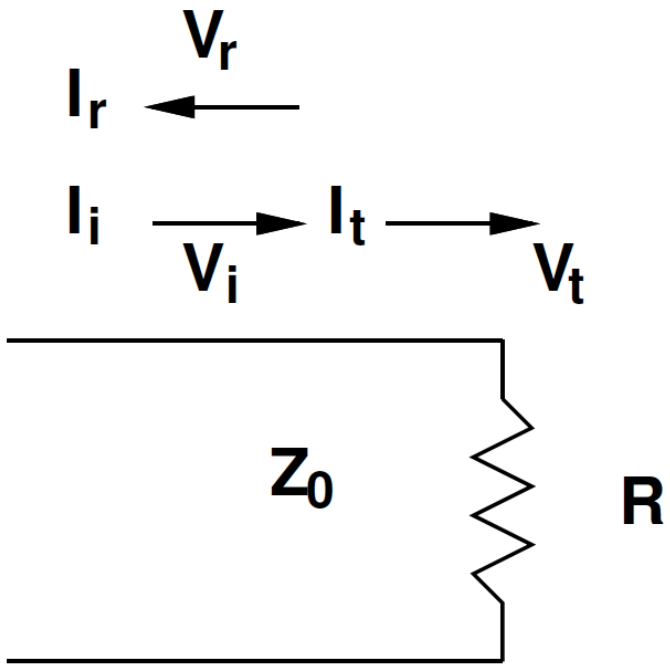
Analyze End of Line (Preclass 1b)

- Incident wave $V_i = I_i \times Z_0$
- KCL: $I_i = I_r + I_t$
- KVL: $V_i + V_r = V_t$
- V=IR relationships?
  - Which resistances go with each V?
  - $V_r = I_r \times Z_0 \rightarrow I_r = V_r / Z_0$
  - $V_t = I_t \times R \rightarrow I_t = V_t / R$
  - $V_i = I_i \times Z_0 \rightarrow I_i = V_i / Z_0$



Analyze End of Line

- Incident wave $V_i = I_i \times Z_0$
- KCL: $I_i = I_r + I_t$
- KVL: $V_i + V_r = V_t$
- $V_r = I_r \times Z_0$ → $I_r = V_r / Z_0$
- $V_t = I_t \times R$ → $I_t = V_t / R$
- $V_i = I_i \times Z_0$ → $I_i = V_i / Z_0$



$$\frac{V_i}{Z_0} = \frac{V_r}{Z_0} + \frac{V_t}{R}$$

Analyze End of Line (Preclass 1c)

- $V_i+V_r=V_t$ $\qquad \frac{V_i}{Z_0} = \frac{V_r}{Z_0} + \frac{V_t}{R}$

- Eliminate V_t

Analyze End of Line (Preclass 1c)

- $V_i + V_r = V_t$ $\quad \frac{V_i}{Z_0} = \frac{V_r}{Z_0} + \frac{V_t}{R}$

- Eliminate V_t

$$\frac{V_i}{Z_0} = \frac{V_r}{Z_0} + \frac{V_i + V_r}{R}$$

$$RV_i = RV_r + Z_0(V_i + V_r)$$

$$V_i(R - Z_0) = V_r(R + Z_0)$$

$$V_r = \left(\frac{R - Z_0}{R + Z_0}\right) V_i$$

Reflection coefficient

Analyze End of Line

- $V_i + V_r = V_t$

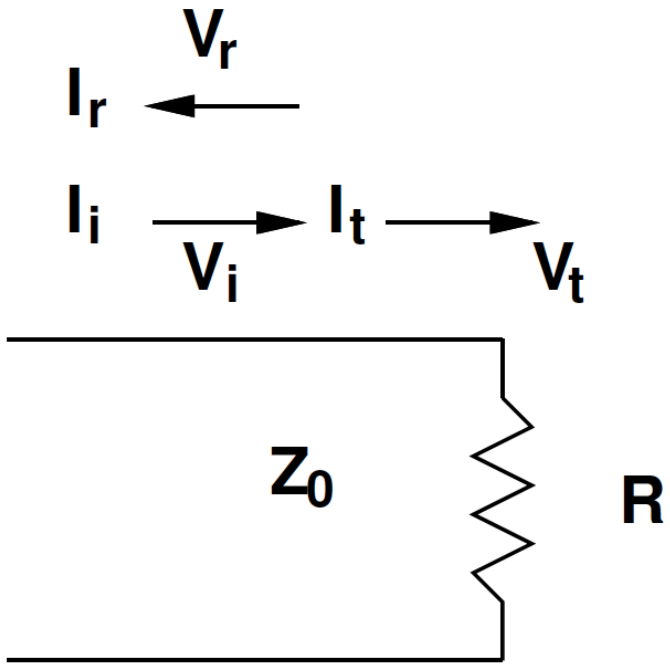
$$V_i + V_i\left(\frac{R - Z_0}{R + Z_0}\right) = V_t$$

$$V_i\left(1 + \frac{R - Z_0}{R + Z_0}\right) = V_t$$

$$V_i\left(\frac{2R}{R + Z_0}\right) = V_t$$

Reflection

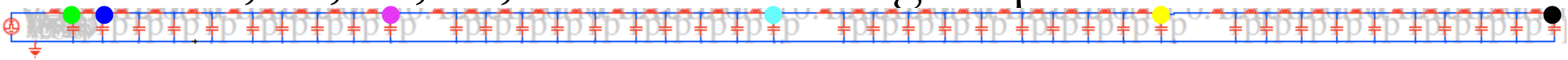
- Sanity check with previous
  - Short
  - Matched
  - Open

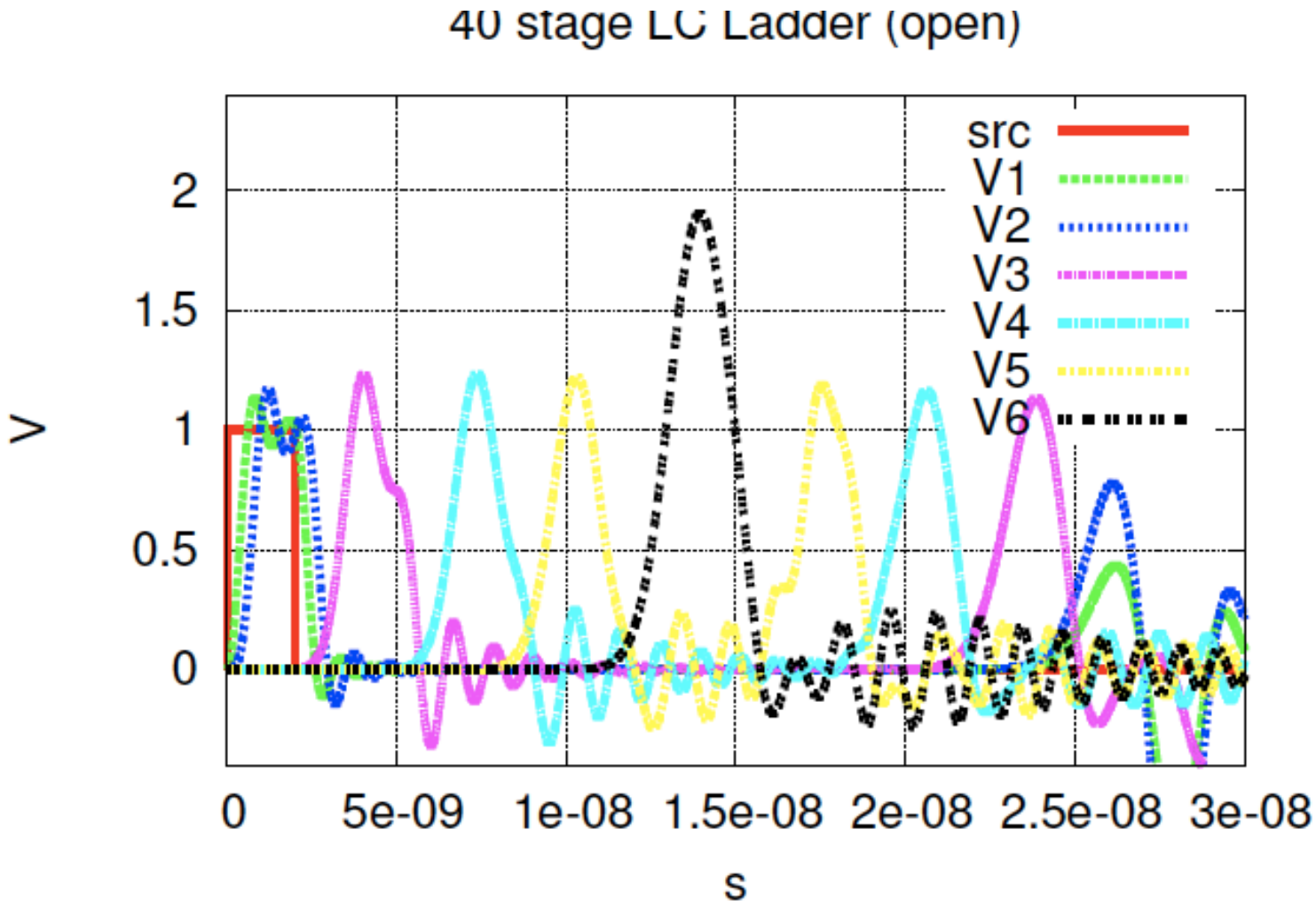


$$V_i\left(\frac{R-Z_0}{R+Z_0}\right)=V_r$$

Pulse Travel RC

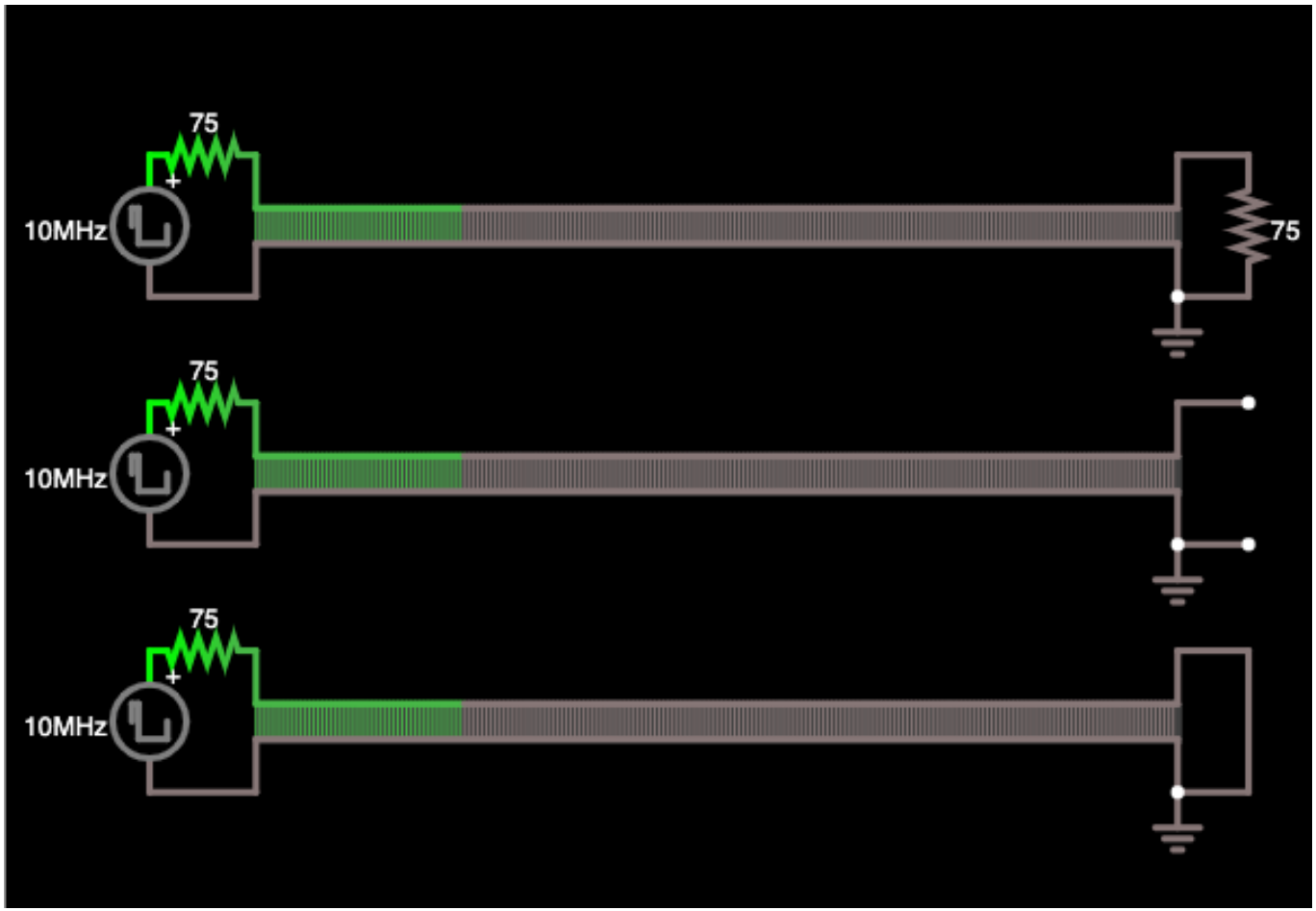
- V1,V3,V4,V5,V6 about 10 stages apart

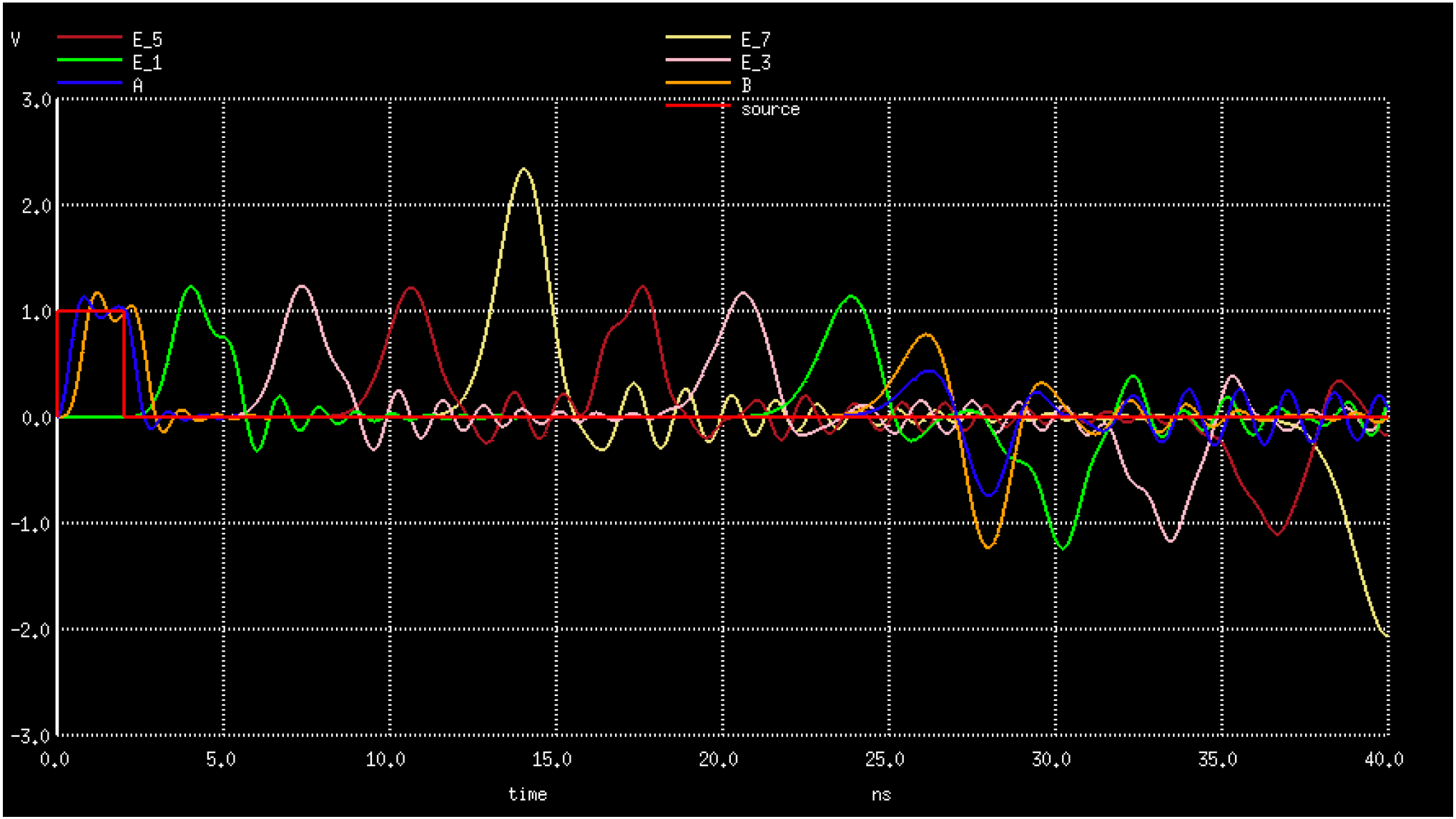




Visualization

- https://tinyurl.com/y2jortrq




V
E_5
E_1
A
E_7
E_3
B
source
3.0
2.0
1.0
0.0
-1.0
-2.0
-3.0
0.0
5.0
10.0
15.0
20.0
25.0
30.0
35.0
40.0
time
ns

Back to Source

Back at Source? (Preclass 2)

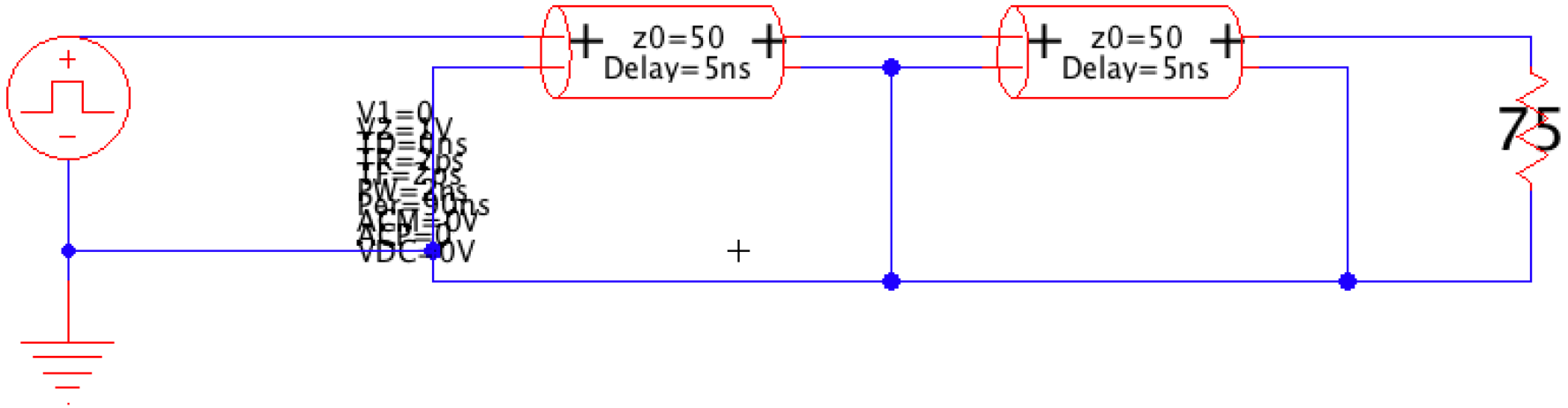
- What happens at source?
  - Depends on how it's terminated
  - Looks like a sink end now

$R \neq Z_0$

- What happens?
  - 75 Ω termination on 50 Ω line

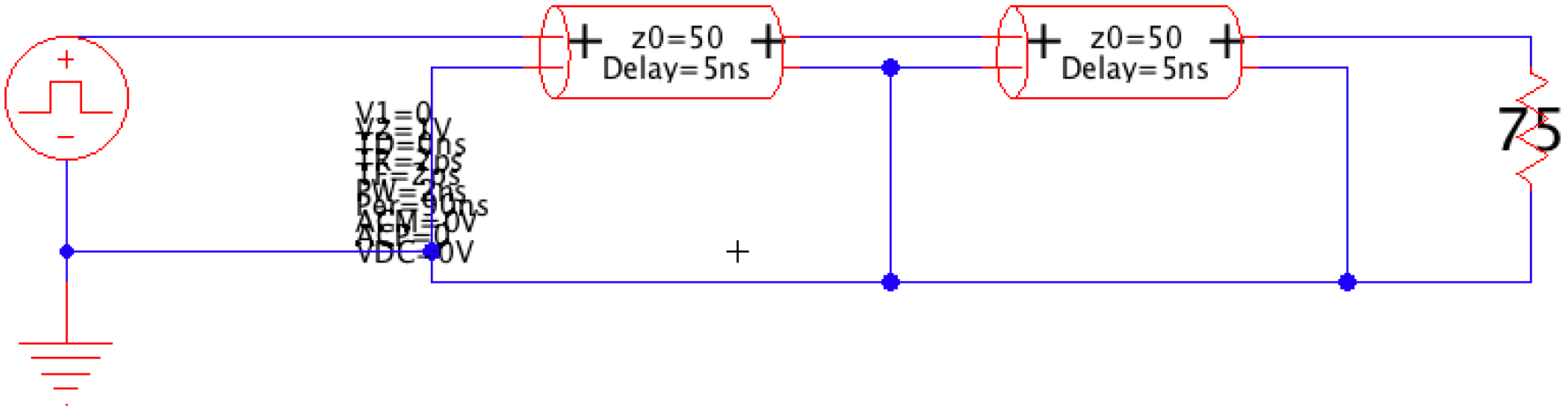
Transmission Line Symbol

- Specify delay of full Tline and characteristic impedance
- Need reference

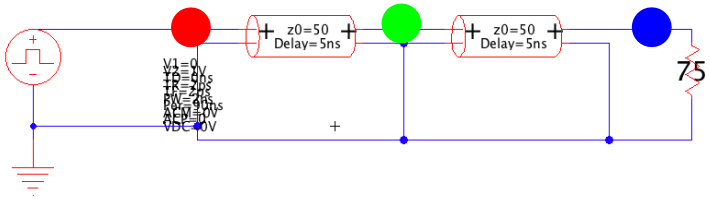


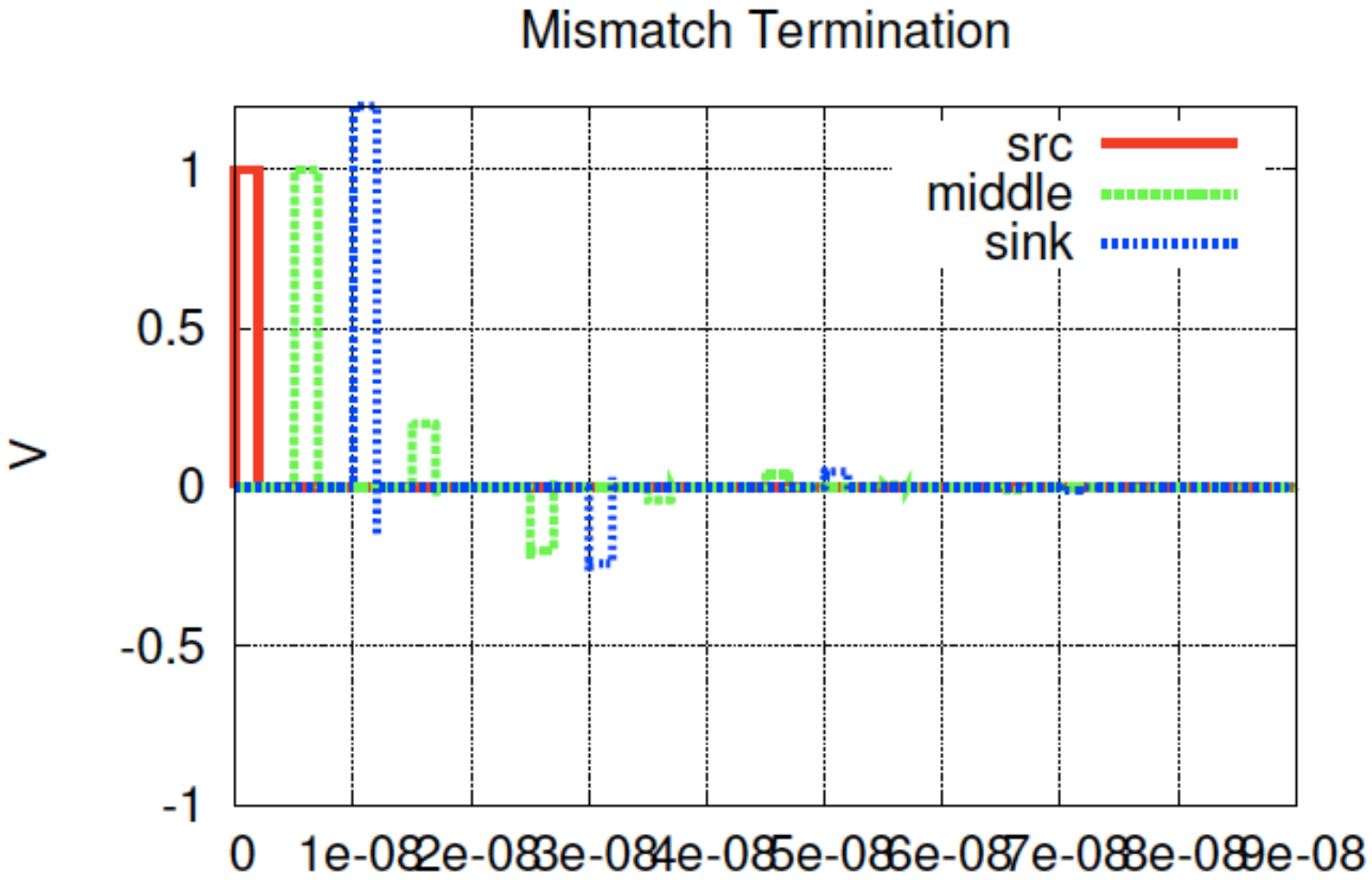
Simulation (Preclass 3)

- For these, with direct drive from voltage source
  - Source looks like short circuit (not typical of CMOS)
    - Source cannot be changed



50Ω line, 75Ω termination

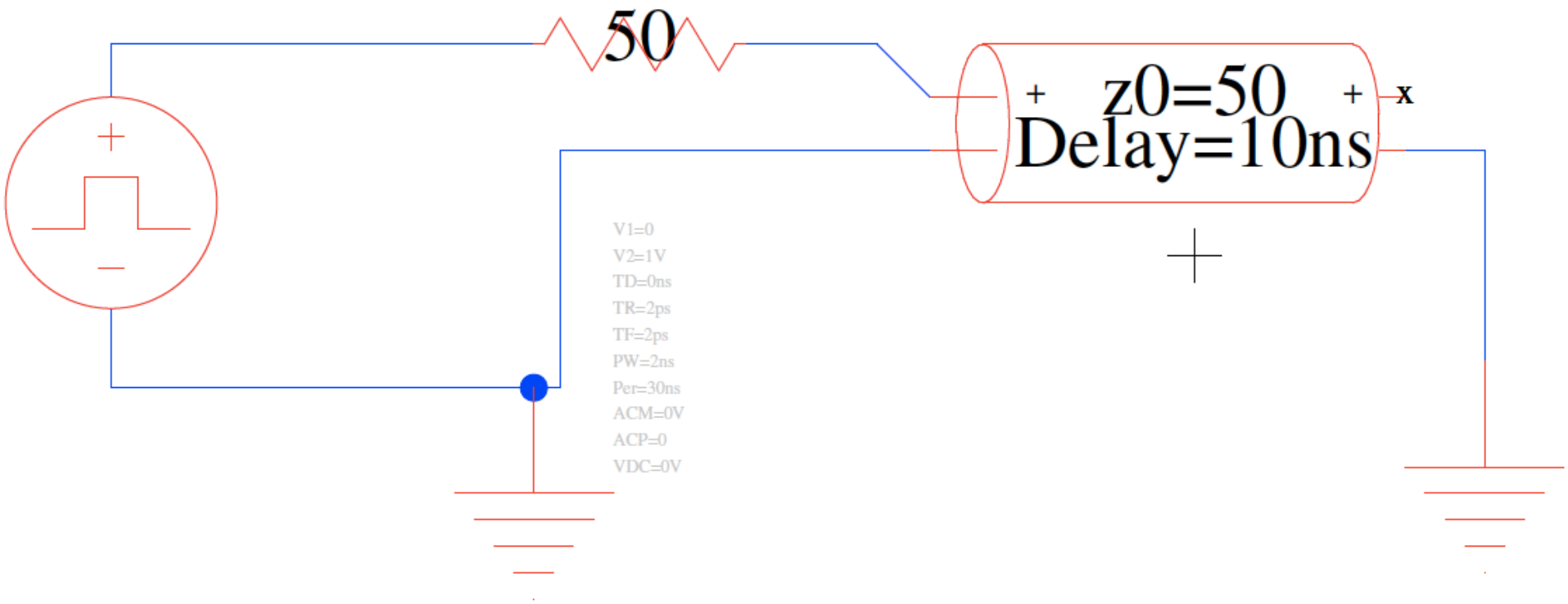




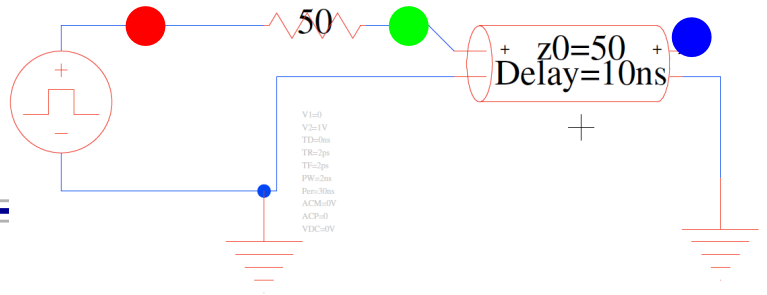
$$V_r = V_i\left(\frac{R - Z_0}{R + Z_0}\right) \overset{S}{=} V_i\left(\frac{75 - 50}{75 + 50}\right) = 0.2V_i$$

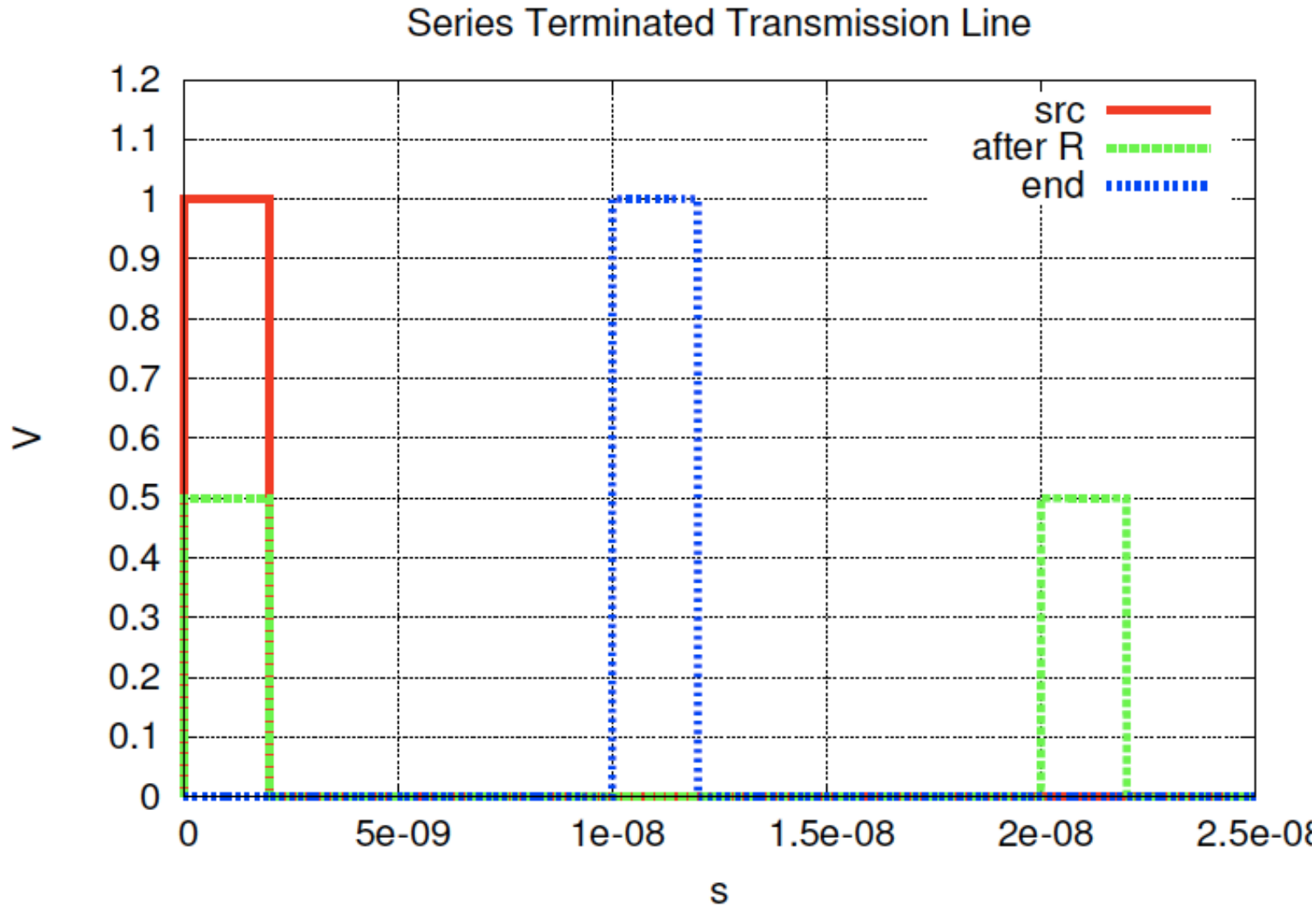
Source Series Termination

- What happens here?



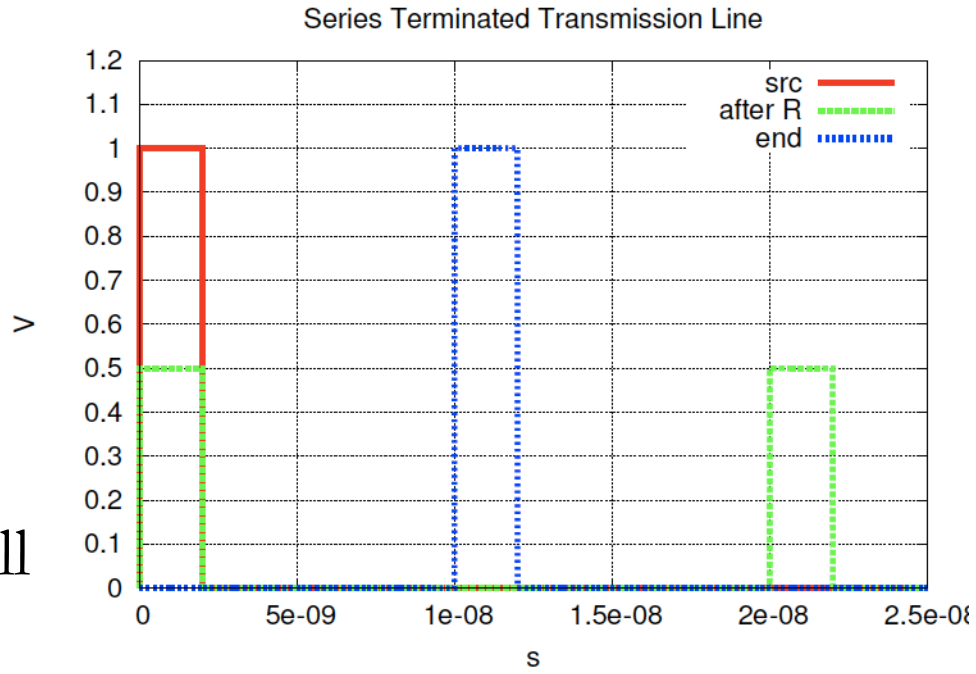
Simulation

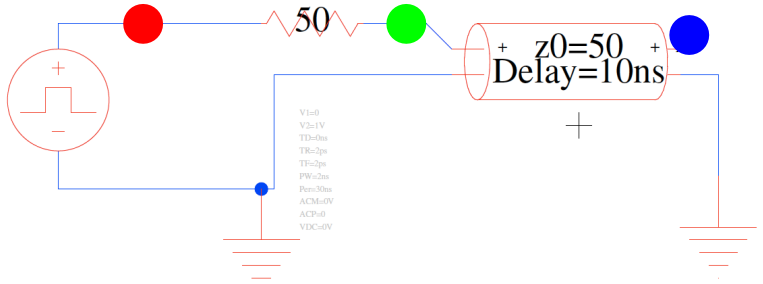

50
z0=50
Delay=10ns


Series Terminated Transmission Line
src
after R
end
1.2
1.1
1
0.9
0.8
0.7
0.6
0.5
0.4
0.3
0.2
0.1
0
V
0
5e-09
1e-08
1.5e-08
2e-08
2.5e-08
s

Series Termination

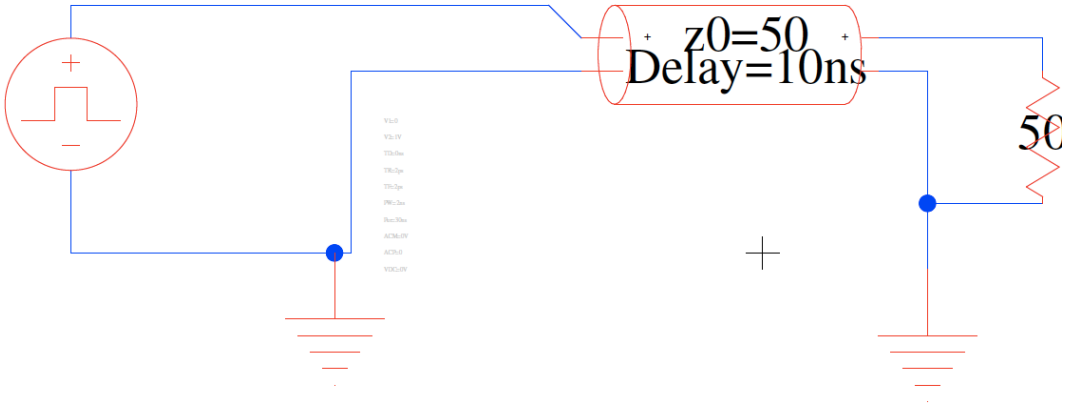
- $R_{series} = Z_0$
- Initial voltage divider
  - Half voltage pulse propogates down Tline
- End of line open circuit
  - Sees single transition to full voltage (full reflection)
- Reflection returns to source and sees termination $R_{series} = Z_0$
- No further reflections



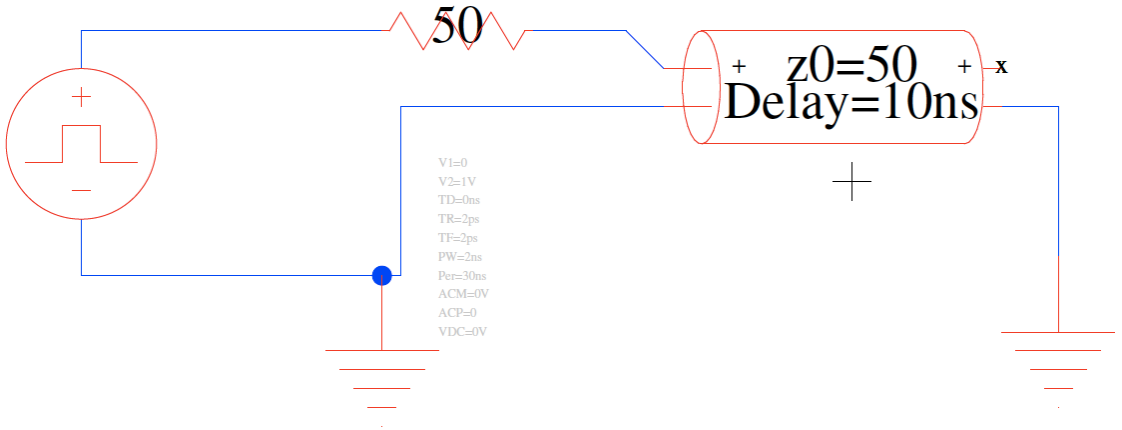


Termination Cases

- Termination in parallel at Sink

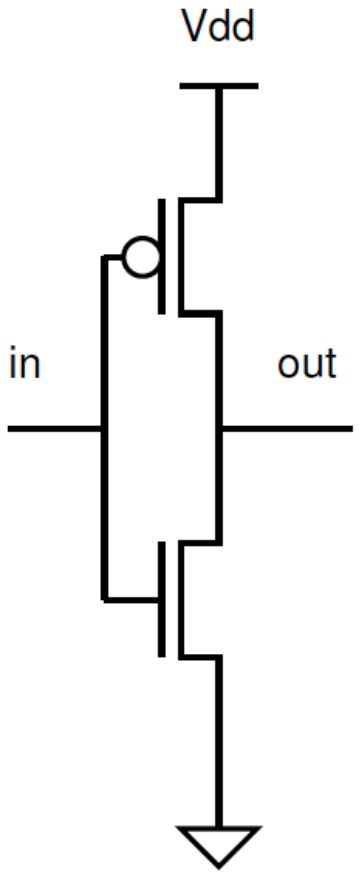


- Termination in series at Source



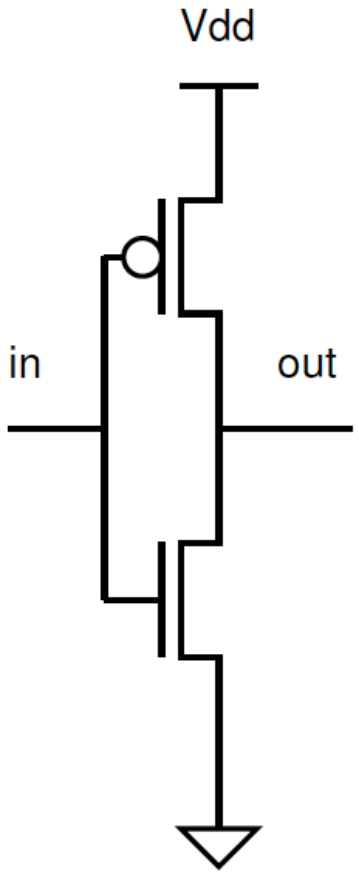
CMOS Driver / Receiver

- Driver: What does a CMOS driver look like at the source?
  - $I_{d,sat}$=1200μA/μm @ 45nm, V_{dd}=1V
- Receiver: What does a CMOS inverter look like at the sink?



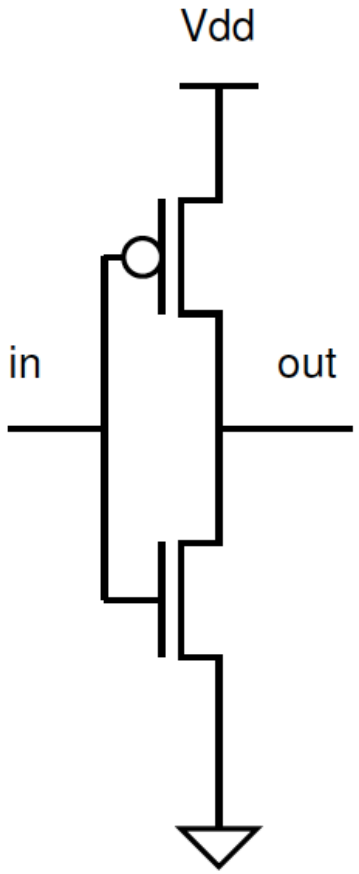
CMOS Driver

- Driver: What does a CMOS driver look like at the source?
  - $I_{d,sat}$=1200μA/μm @ 45nm, V_{dd}=1V
  - Min size:
    - I_{drive}=1200μA/μm*45nm=54μA
    - $R_{out}=V_{dd}/I_{drive}$=18kΩ



CMOS Driver

- Driver: What does a CMOS driver look like at the source?
  - $I_{d,sat}$=1200μA/μm @ 45nm, V_{dd}=1V
  - Min size:
    - I_{drive}=1200μA/μm*45nm=54μA
    - $R_{out}=V_{dd}/I_{drive}$=18kΩ
  - W=370
    - I_{drive}=1200μA/μm*45nm*370=20mA
    - $R_{out}=V_{dd}/I_{drive}$=50Ω



Idea

- Signal propagates as wave down transmission line
  - Delay linear in wire length
  - Speed
  - Impedance
- Behavior at end of line depends on termination
- Both src and sink are "ends" with reflections

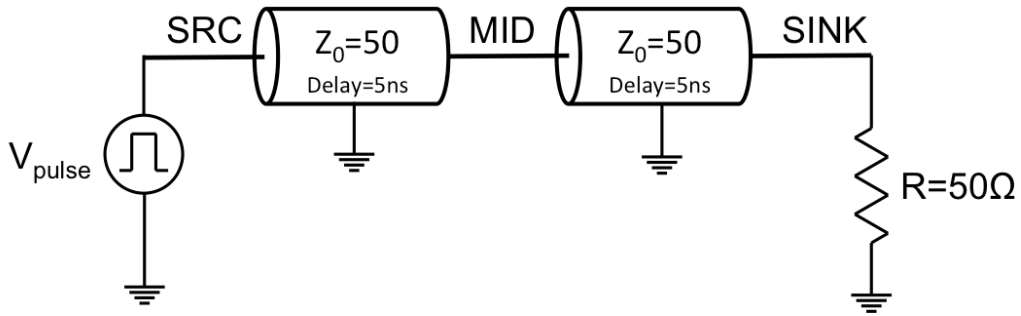
$$w = \frac{1}{\sqrt{LC}} = \frac{c_0}{\sqrt{\varepsilon_r \mu_r}}$$

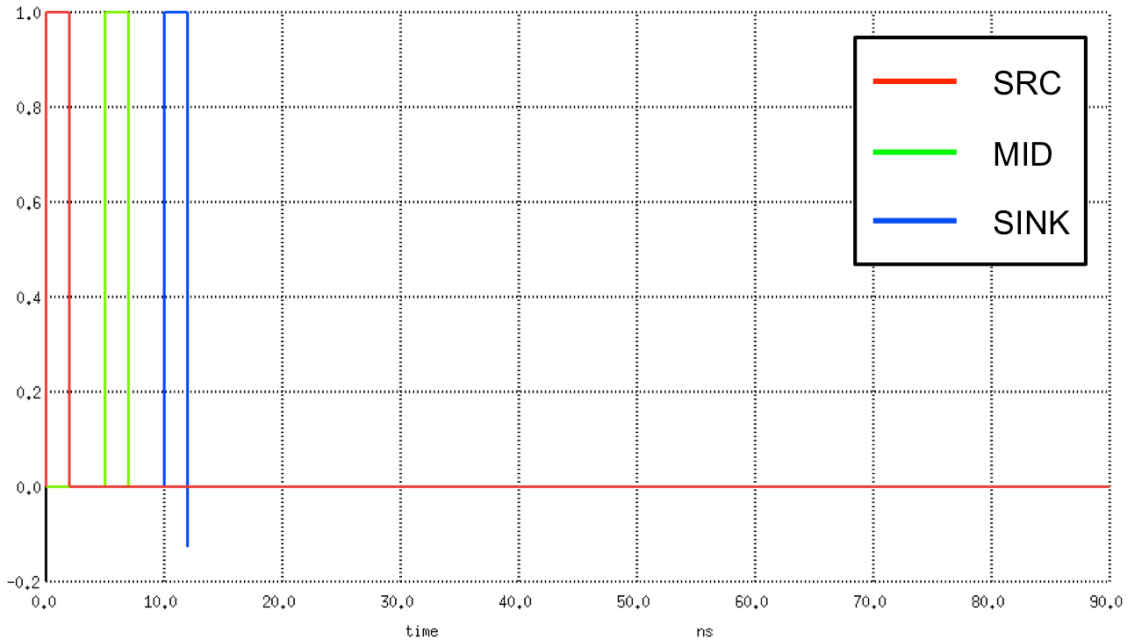
$$Z_0 = \sqrt{\frac{L}{C}}$$

$$V_r = V_i \left(\frac{R - Z_0}{R + Z_0} \right)$$

Tline Examples (Preclass 4)

- Will start with these next lecture





Admin

- Proj 2
  - EXTENDED: due Sunday 12/5 @ midnight
  - No late days allowed
- HW 7
  - Due Friday 12/10
  - Out now