ESE370: Circuit-Level Modeling, Design, and Optimization for Digital Systems

Lec 34: December 6, 2021

Transmission Lines

Implications

Transmission Line Agenda

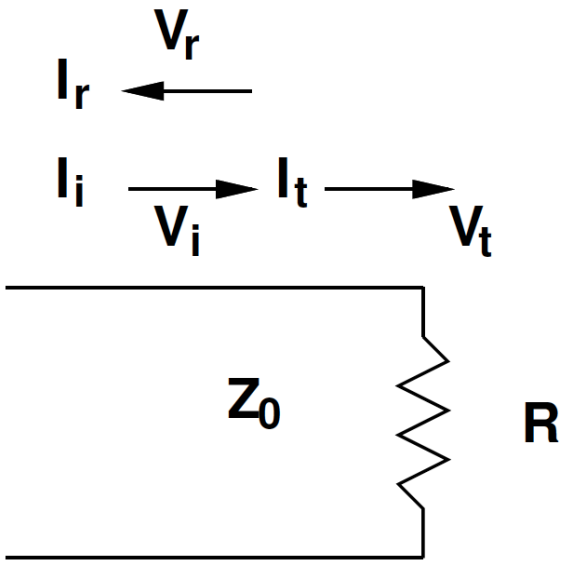
- ~~See in action in lab~~
- ~~Where transmission lines arise?~~
- ~~General wire formulation~~
- ~~Lossless Transmission Line~~
- ~~Impedance~~
- ~~End of Transmission Line?~~
  - ~~Open, short, matched~~
- Physical Geometry
- Discuss Lossy
- Implications/Effects

Reminder: Transmission Line

- Data travels as waves
- Line has Impedance
- May reflect at end of line

$$w = \frac{1}{\sqrt{LC}} = \frac{c_0}{\sqrt{\varepsilon_r \mu_r}}$$

$$Z_0 = \sqrt{\frac{L}{C}}$$

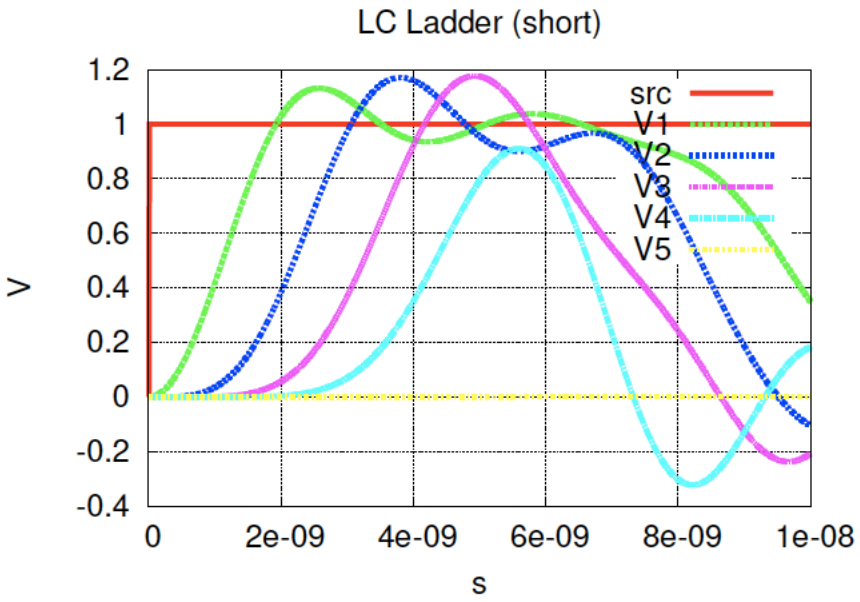


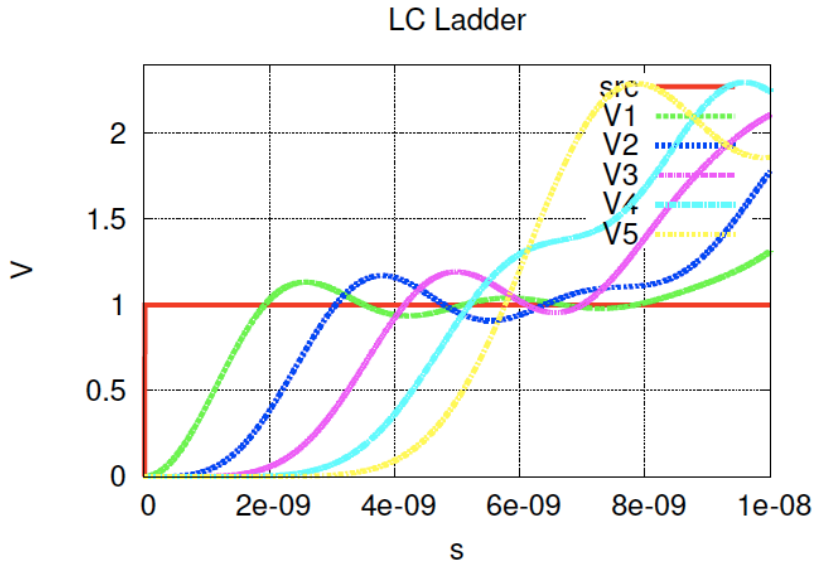
$$V_i\left(\frac{R - Z_0}{R + Z_0}\right) = V_r$$

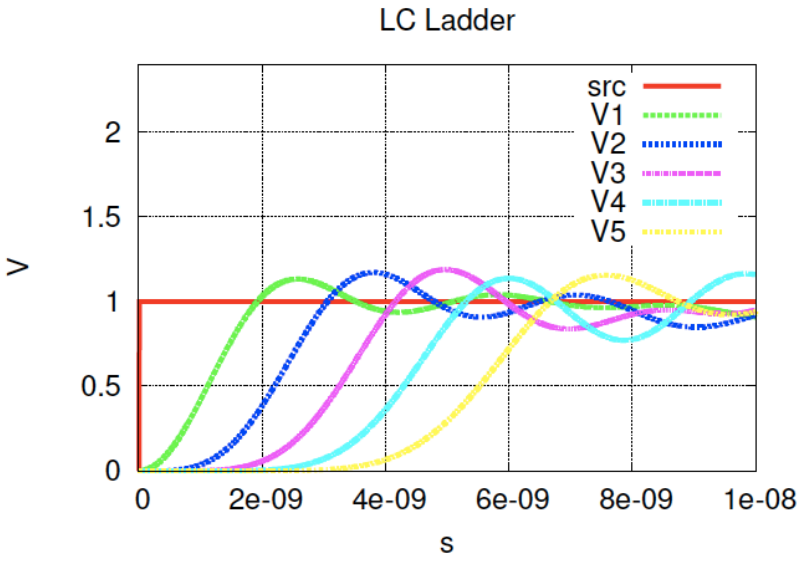
$$V_i\left(\frac{2R}{R + Z_0}\right) = V_t$$

Reminder: End of Line

- What happens at the end of the transmission line?

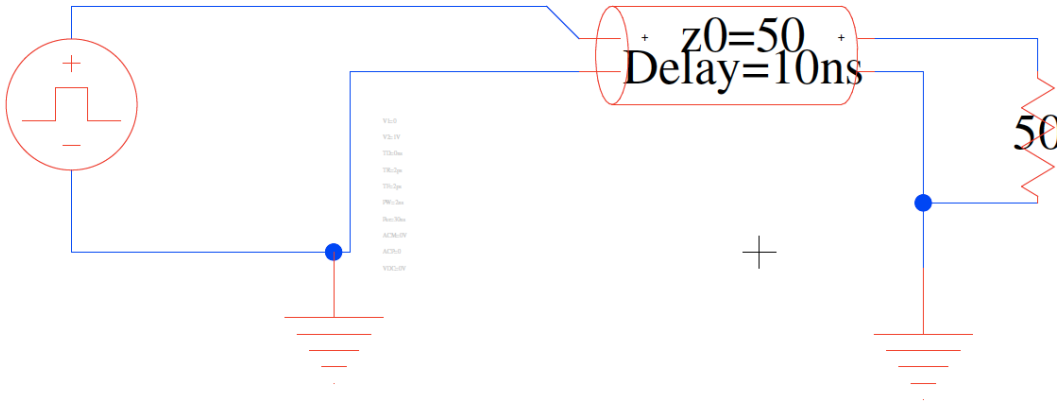




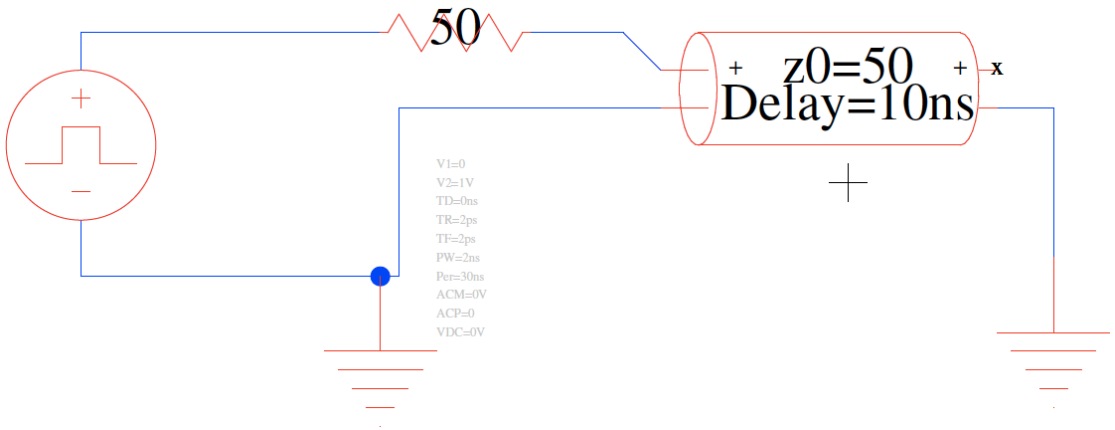


Termination Cases

- Termination in parallel at Sink



- Termination in series at Source

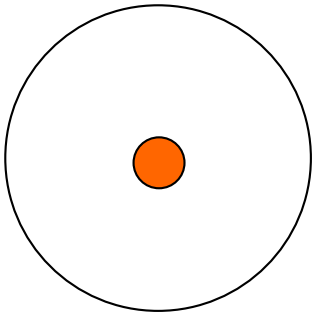


Transmission Lines Specifics

Characteristics arise form their geometry

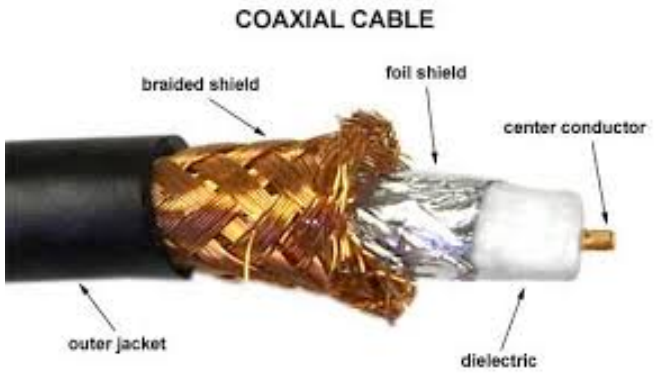
Coaxial Cable

- Inner core conductor: radius r
- Insulator: out to radius R
- Outer core shield (ground)



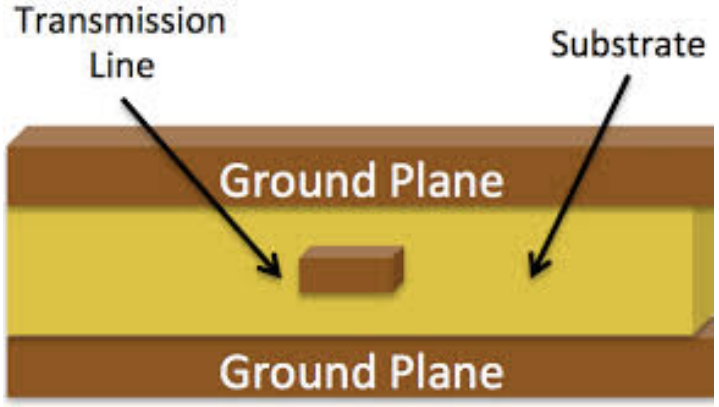
$$L = \left(\frac{\mu}{2\pi}\right)\ln\left(\frac{R}{r}\right) \qquad Z_0 = \left(\frac{1}{2\pi}\right)\left(\sqrt{\frac{\mu}{\varepsilon}}\right)\ln\left(\frac{R}{r}\right)$$

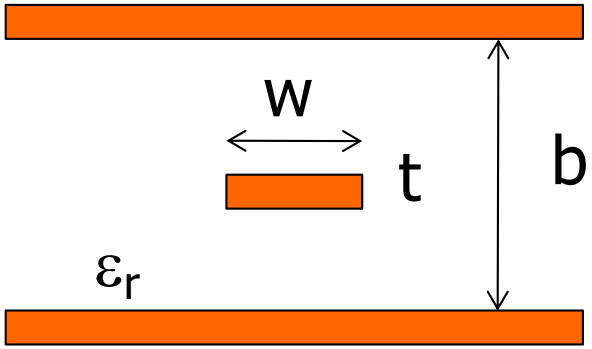
- RG-58 Z_0= 50Ω – networking
- RG-59 Z_0= 75Ω – video
- HDMI Z_0= 100Ω – video



Printed Circuit Board

- Stripline
  - Trace between ground planes

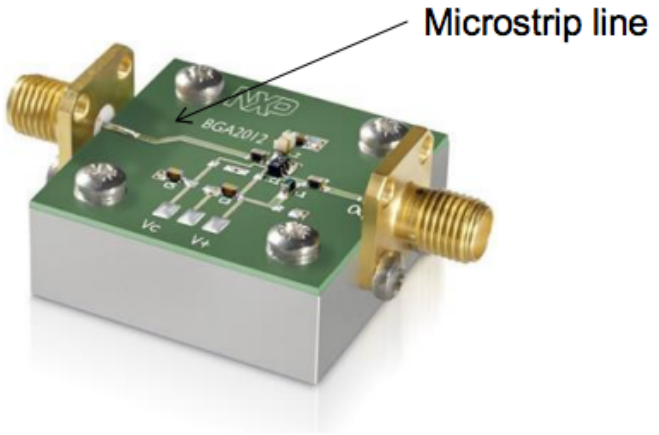


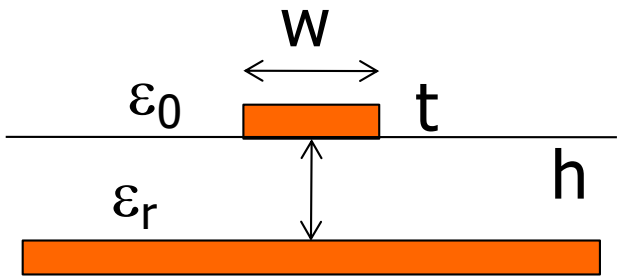


$$Z_0 = \left(\frac{1}{4}\right)\left(\sqrt{\frac{\mu}{\varepsilon}}\right)\ln\left(\frac{1 + W/b}{t/b + W/b}\right)$$

Printed Circuit Board

- Microstrip line
  - Trace over single supply plane





$$Z_0 = \left(\frac{1}{2\pi}\right)\left(\sqrt{\frac{\mu}{(0.475\varepsilon_r + 0.67)\varepsilon_0}}\right)\ln\left(\frac{4h}{0.536W + 0.67t}\right)$$

Twisted Pair

- Category 5 ethernet cable
  - $Z_0=100\Omega$
  - $w=0.64c_0$

Implications

(you should be able to reason about this)

Example (Preclass 2)

- 25 meter category-5e cable (Z_0=100Ω, w=0.64c)
  - c = $3x10^8$ m/s
- Supporting 1Gb/s ethernet
  - 4 pairs at 250Mb/s
- a) Time to send data from one end to the other?
- b) Time between bits at 250Mb/s?
- c) Bits on each pair in the cable?

Pipeline Bits

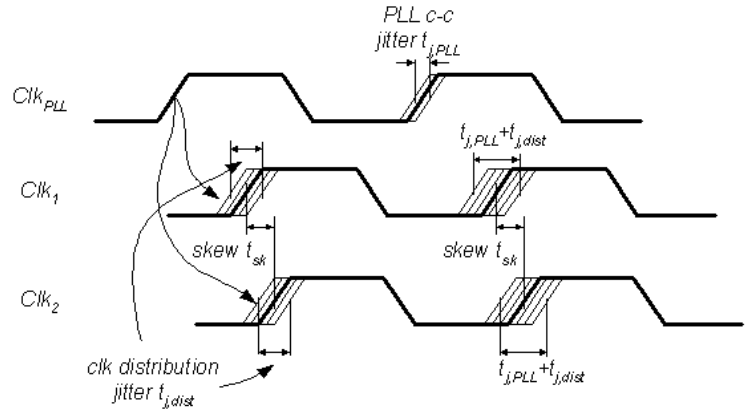
- For properly terminated transmission line
  - Do not need to wait for bits to arrive at sink
  - Can stick new bits onto wire

Limits to Bit Pipelining (Preclass 3)

- What limits? (why only 250Mb/s)

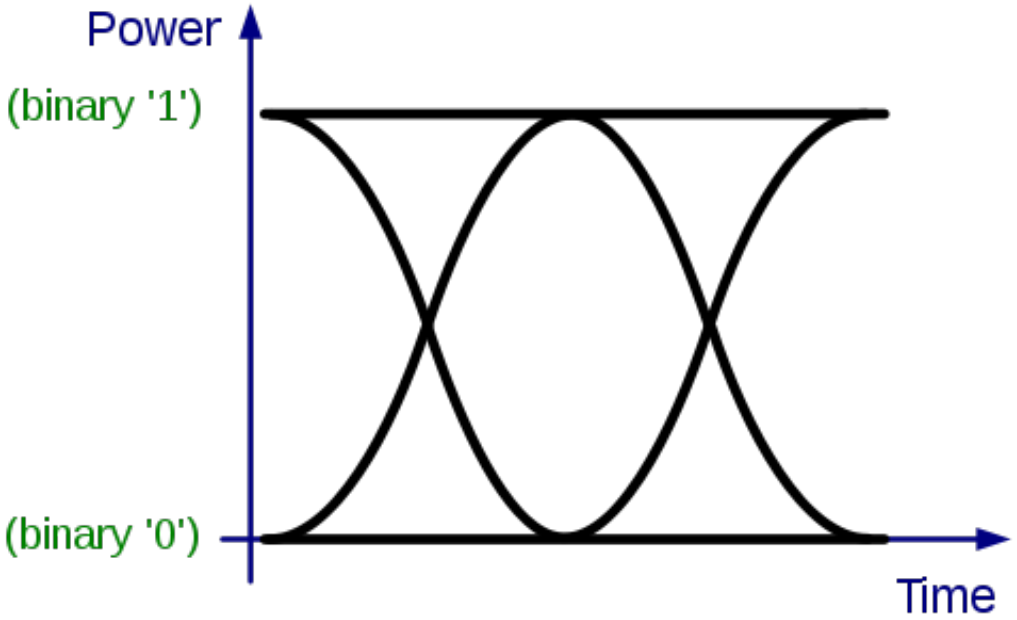
Limits to Bit Pipelining (Preclass 3)

- What limits? (why only 250Mb/s)
  - Risetime/signal distortion
  - Clocking
    - Skew
    - Jitter
  - For bus
    - Wire length differences between lines



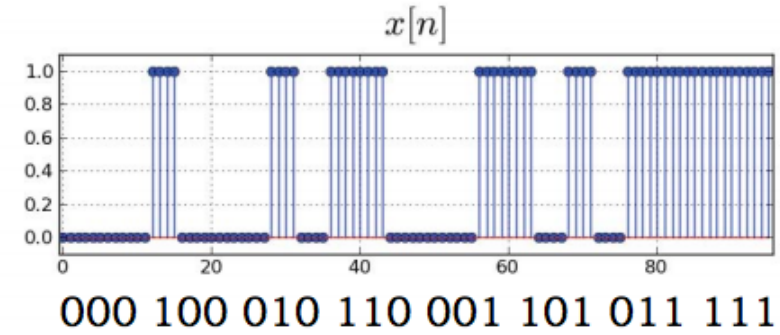
Eye Diagrams

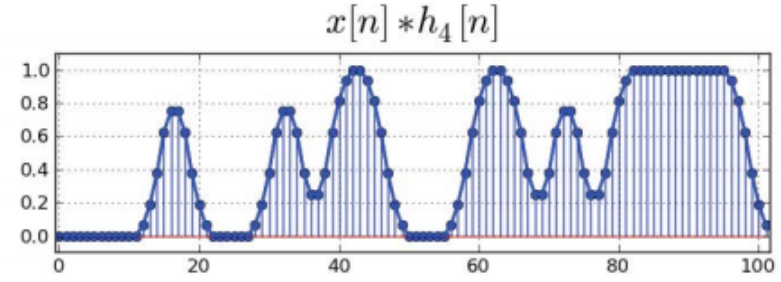
- Watch bits over line on scope
  - Look at distortion
  - "open" eye clean place to sample
    - Consistent timing of transitions
    - Well defined high/low voltage levels



Construct Eye Diagram

- Generate an input bit sequence pattern that contains all possible combinations of B bits (e.g., B=3 or 4), so a sequence of $2^{B*}B$ bits. (Otherwise, a random sequence of comparable length is fine.)
- Transmit the corresponding discrete time sequence x[n] over the channel ($2^{B*}B*N$ samples, if there are N samples/bit)

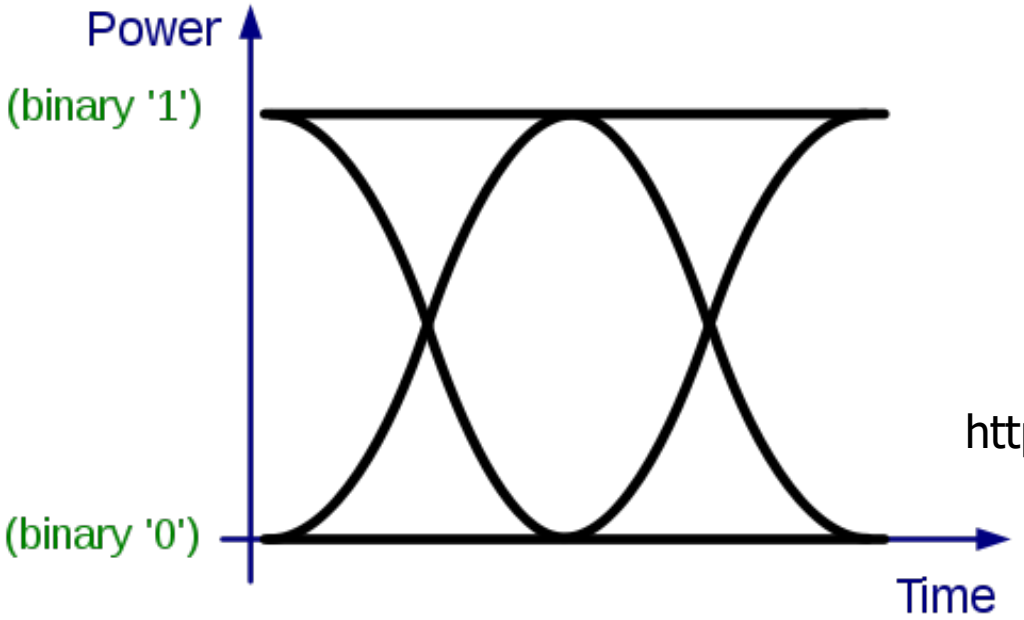


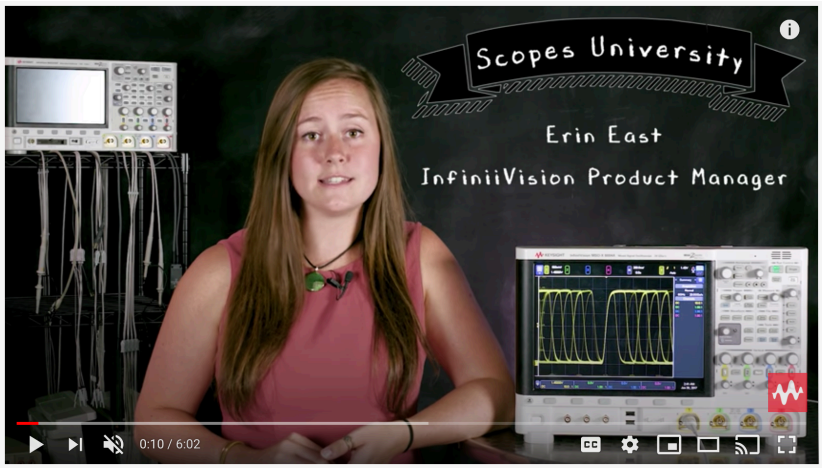


- Instead of one long plot of y[n], plot the response as an eye diagram:
  - a. break the plot up into short segments, each containing K*N samples, starting at sample 0, K*N, 2K*N, 3K*N, … (e.g., K=2 or 3 # bits at a time)
  - b. plot all the short segments on top of each other

Eye Diagrams

- Watch bits over line on scope
  - Look at distortion
  - "open" eye clean place to sample
    - Consistent timing of transitions
    - Well defined high/low voltage levels





https://www.youtube.com/watch?v=mnugUjaMN70

Eye Diagrams

- Watch bits over line on scope
  - Look at distortion
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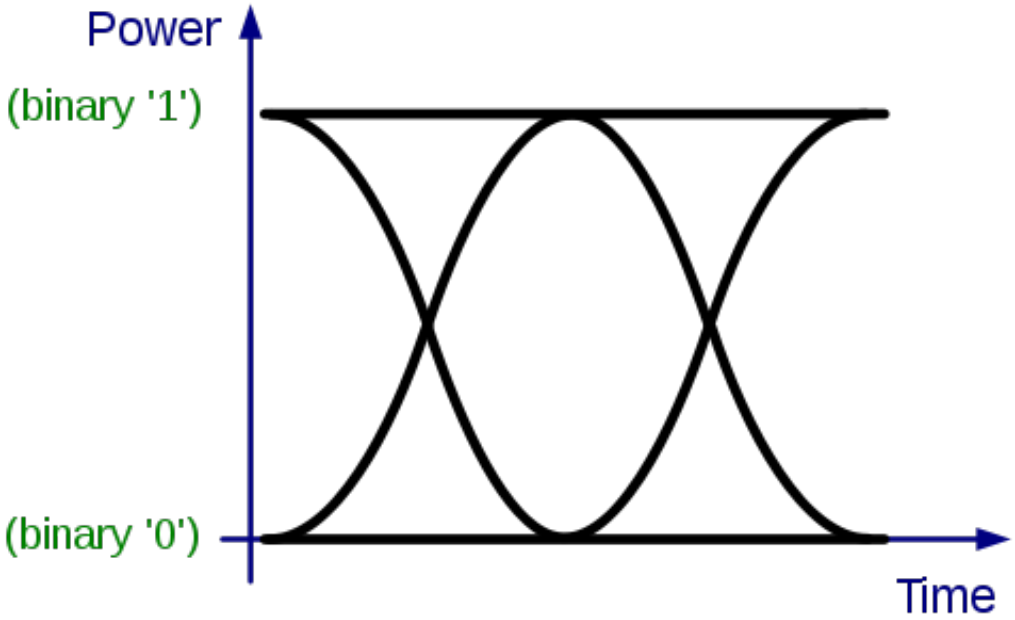
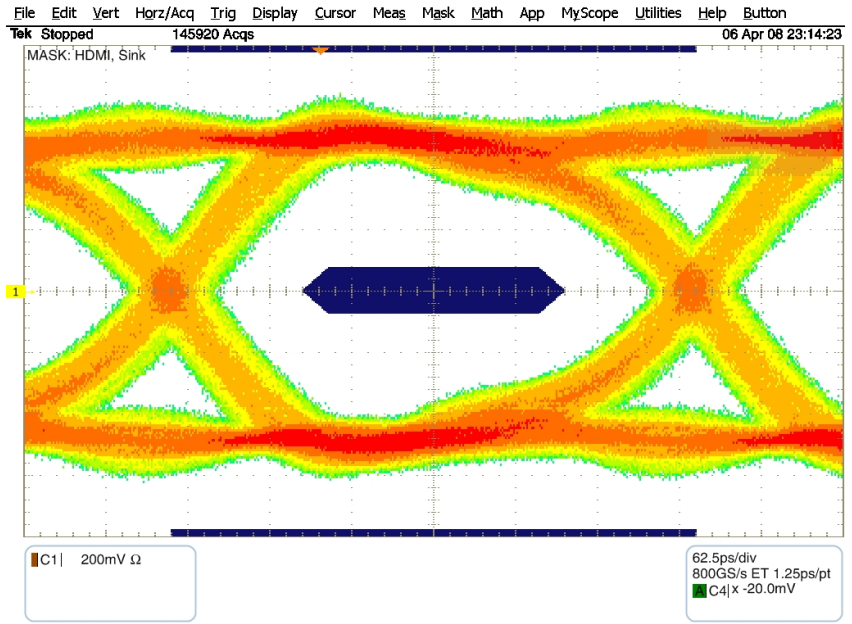
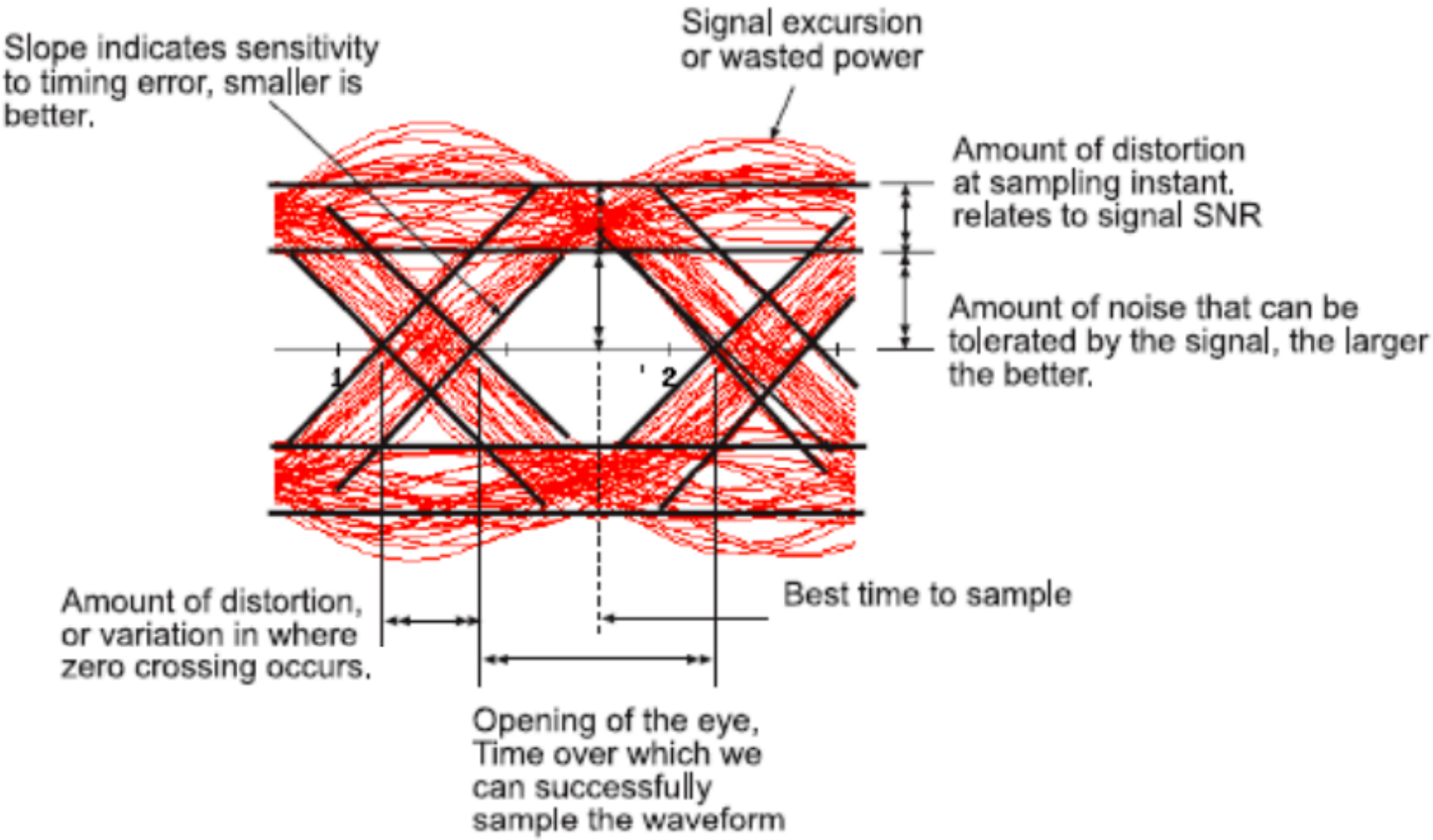
    - Consistent timing of transitions
    - Well defined high/low voltage levels

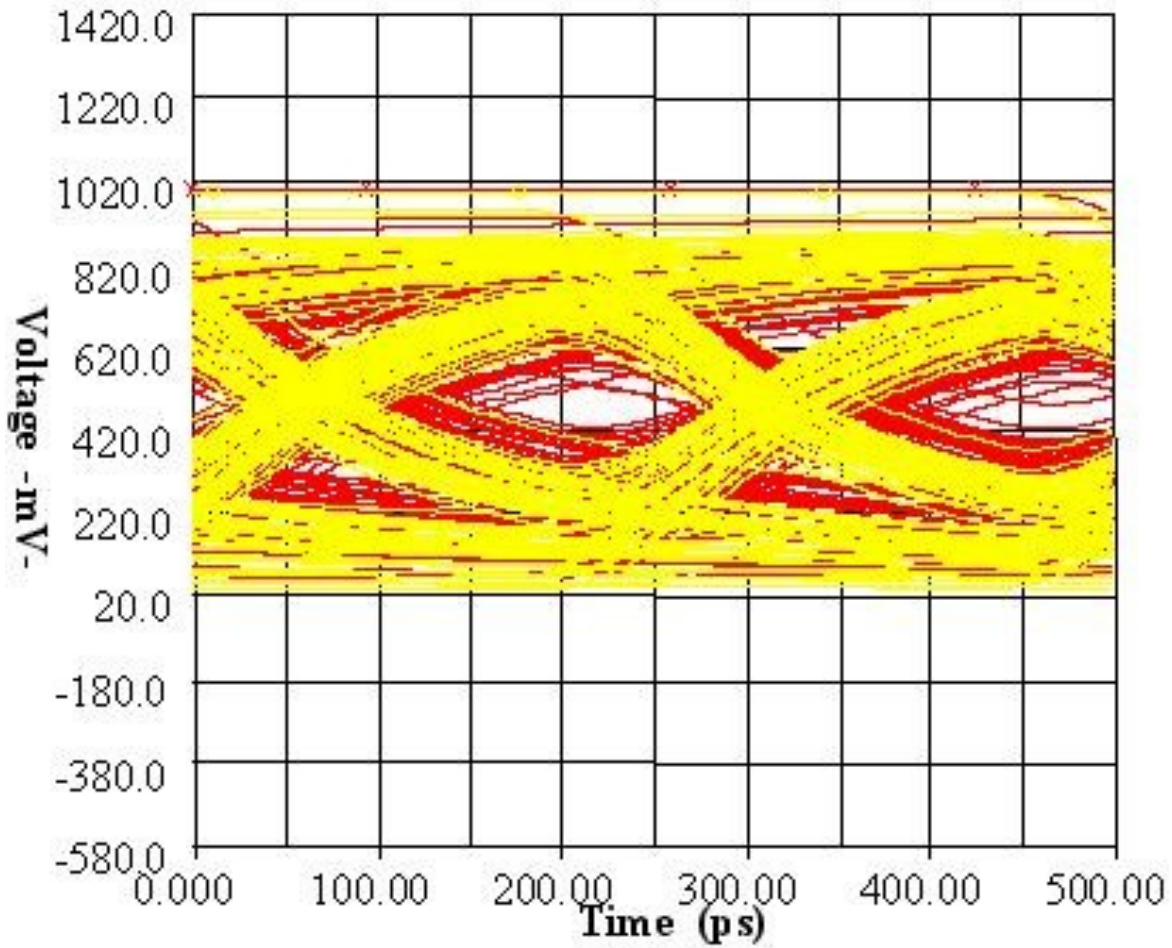




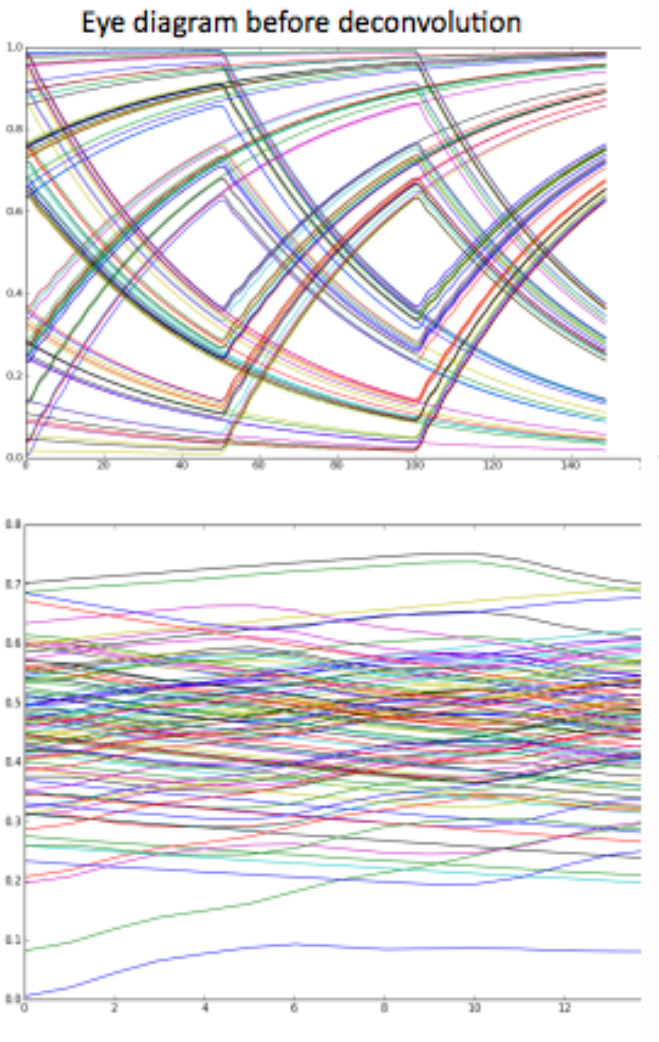
Interpretation of Eye Diagram



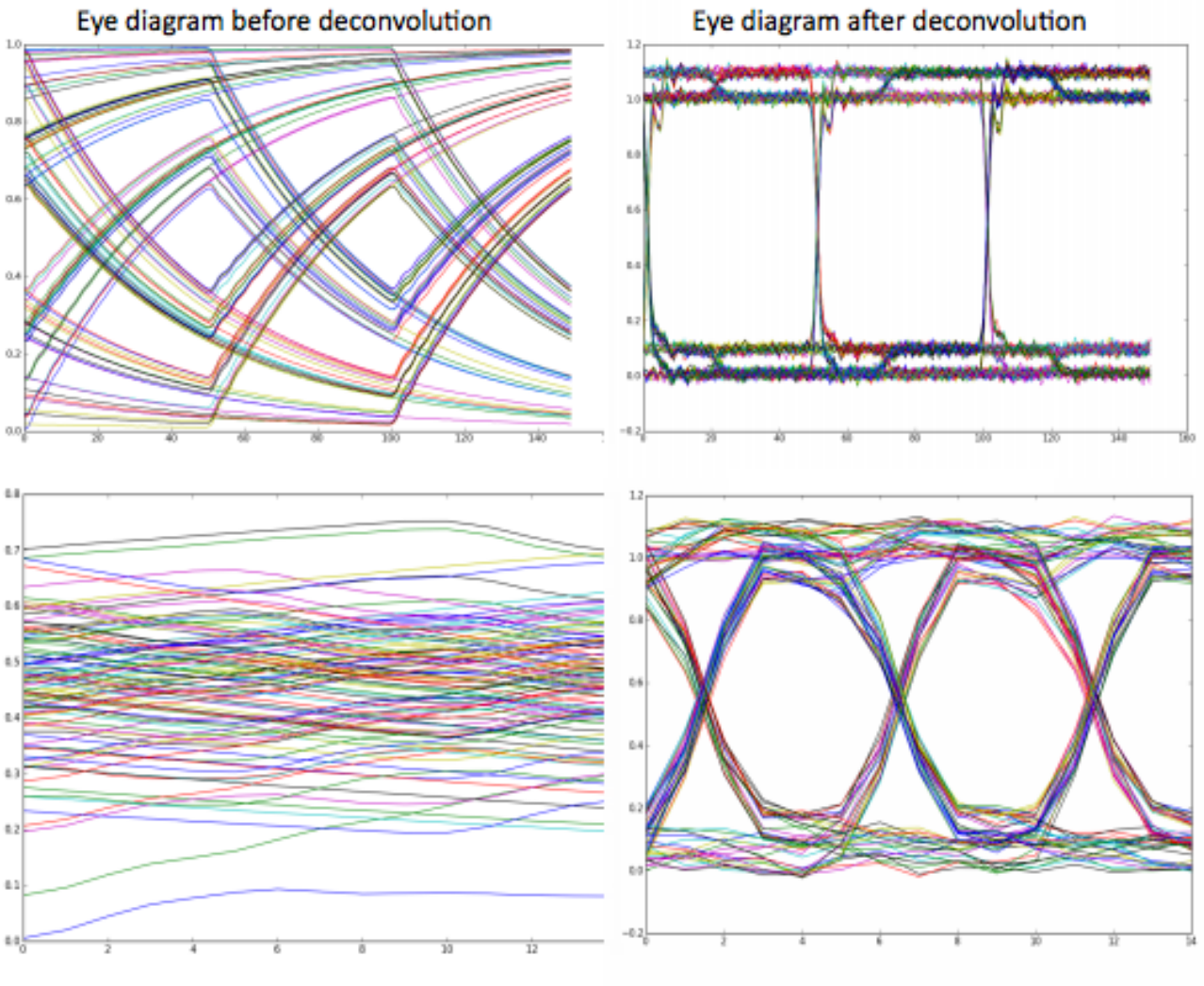
Bad "eye"


1420.0
1220.0
1020.0
820.0
620.0
420.0
220.0
20.0
-180.0
-380.0
-580.0
Voltage - mV
0.000
100.00
200.00
300.00
400.00
500.00
Time (ps)

Receiver Deconvolution



Receiver Deconvolution

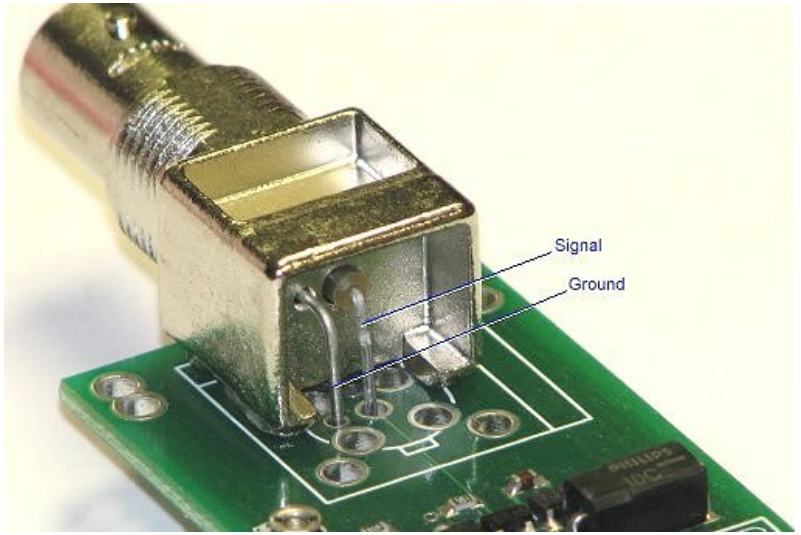


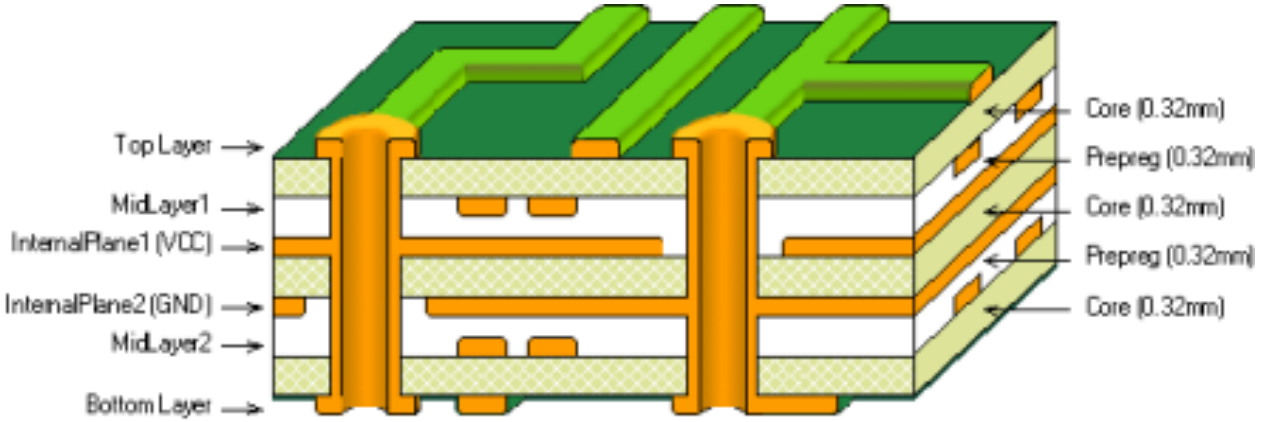
Termination / Mismatch

- Wires do look like these transmission lines
- We are terminating them in some way when we connect to chip (gate)
  - Need to be deliberate about how terminate, if we care about high performance

Where is Mismatch?

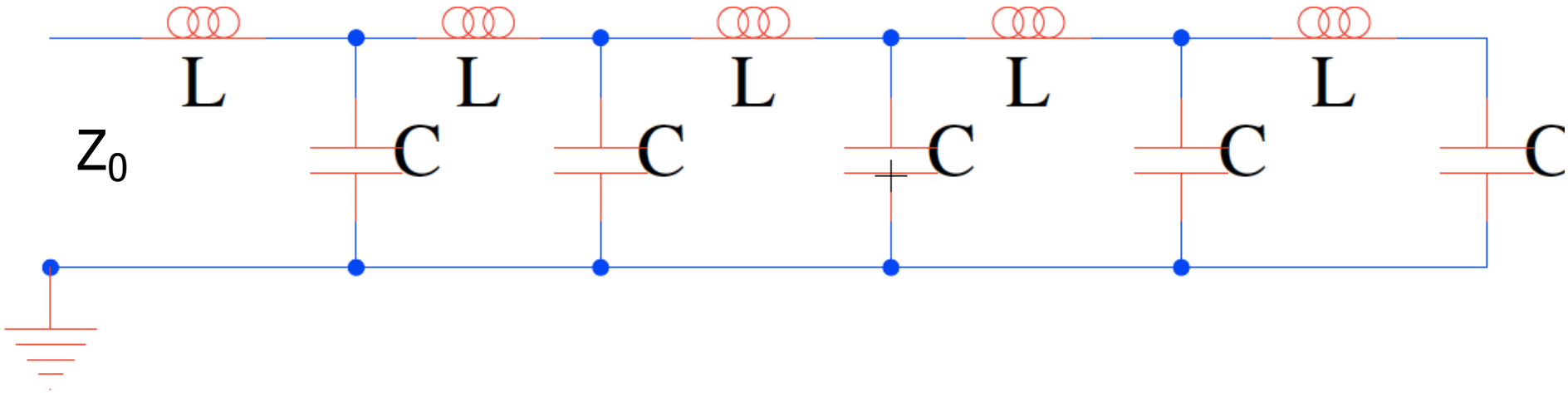
- Vias
- Wire corners
- Branches
- Connectors
- Board-to-cable
- Cable-to-cable





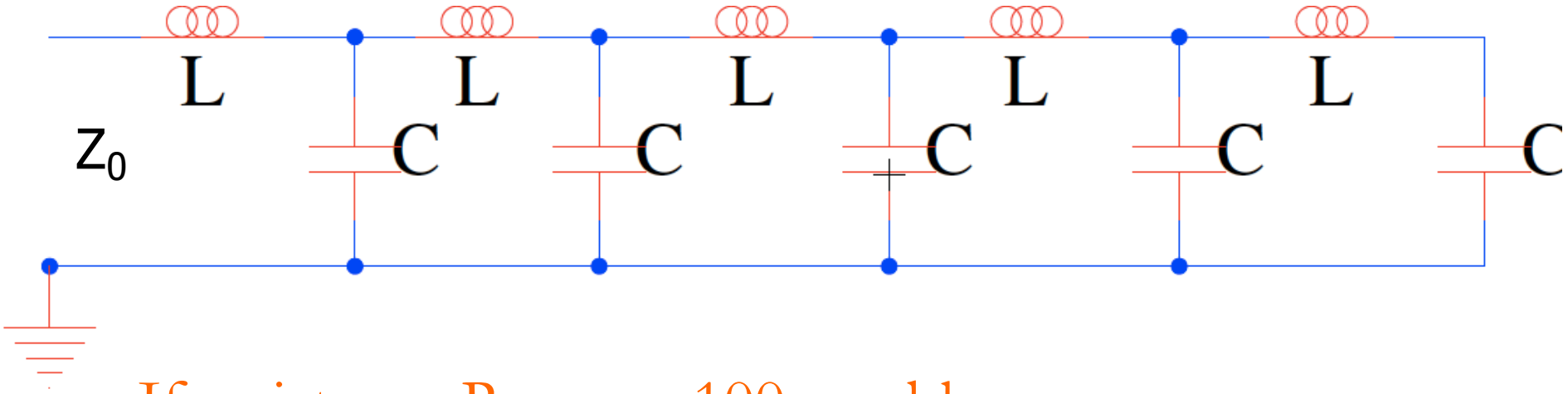
Lossless Transmission Line

- What prevents us from having a 500km cat-5 cable?



Lossless Transmission Line

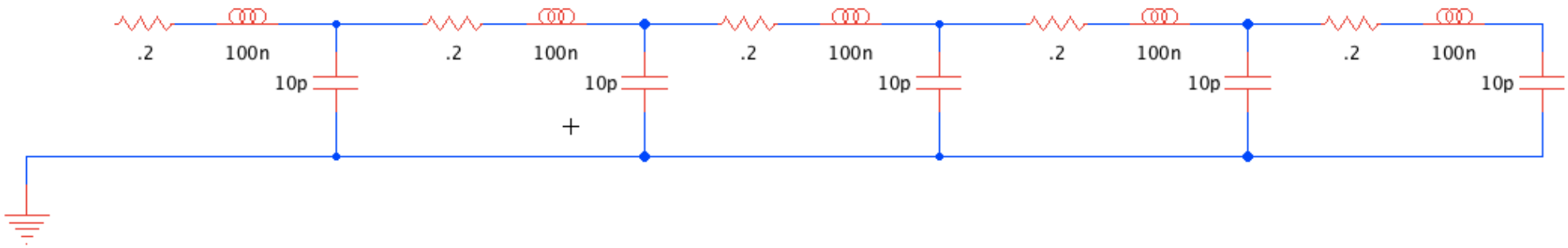
- How to measure resistance across a cable?



- If resistance R across 100m cable,
  what is resistance across 200m cable?

Lossy Transmission Line (Preclass 4)

- How do addition of R's change?
  - Concretely, discretely think about R=0.2Ω every meter on Z_0=100Ω
    - what does each R do? Voltage impact?



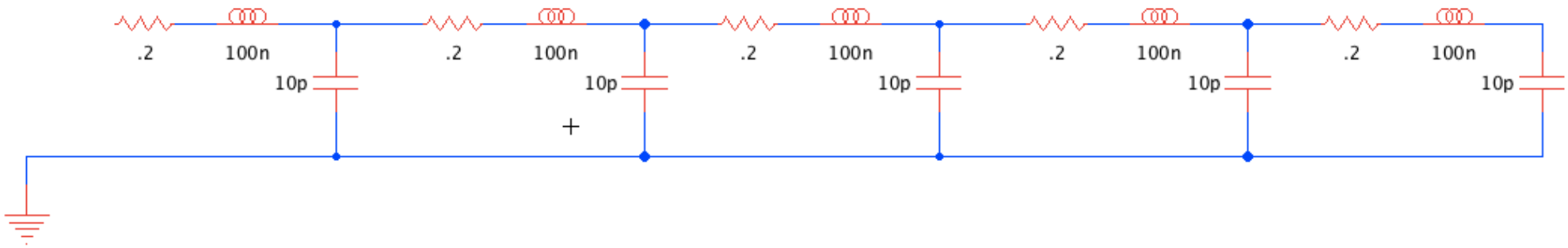
Lossy Transmission Line

- Each R is a mismatched termination

$$V_t = V_i\left(\frac{2(R+Z_0)}{(R+Z_0)+Z_0}\right)$$

- Each R is a voltage divider

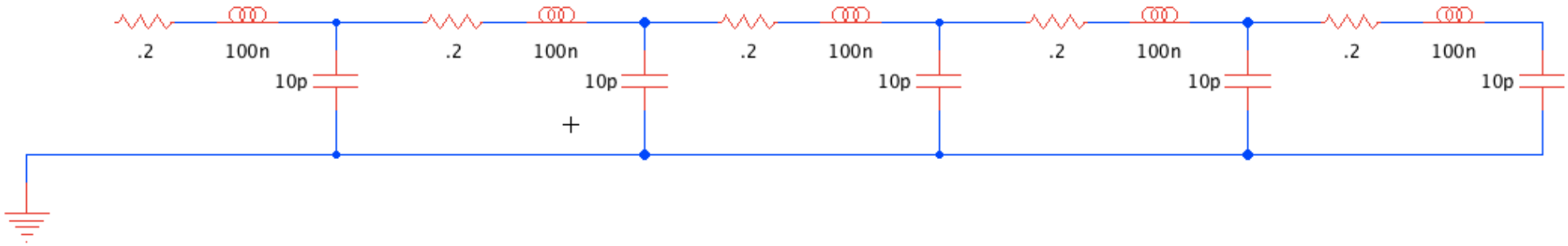
$$V_{i+1} = V_t\left(\frac{Z_0}{R+Z_0}\right)$$



Lossy Transmission Line

$$V_{i+1} = V_i \left(\frac{2(R + Z_0)}{(R + Z_0) + Z_0} \right) \left(\frac{Z_0}{R + Z_0} \right)$$

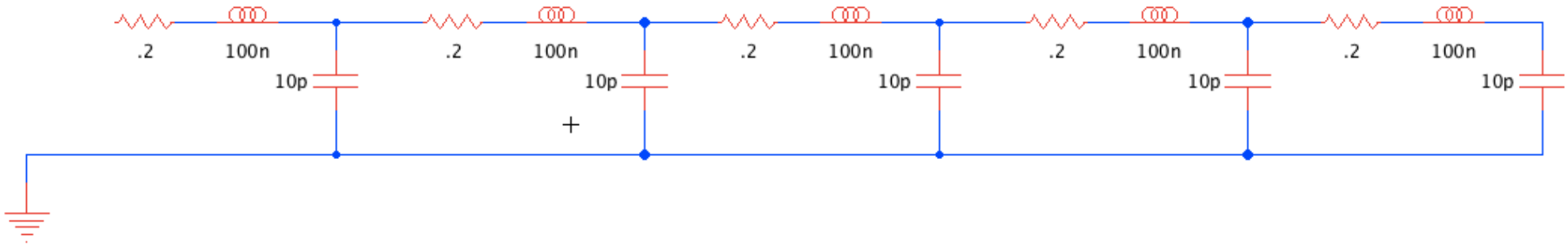
$$V_{snk} = V_{src} \left(\left(\frac{2(R + Z_0)}{(R + Z_0) + Z_0} \right) \left(\frac{Z_0}{R + Z_0} \right) \right)^N$$



Lossy Transmission Line (Preclass 4)

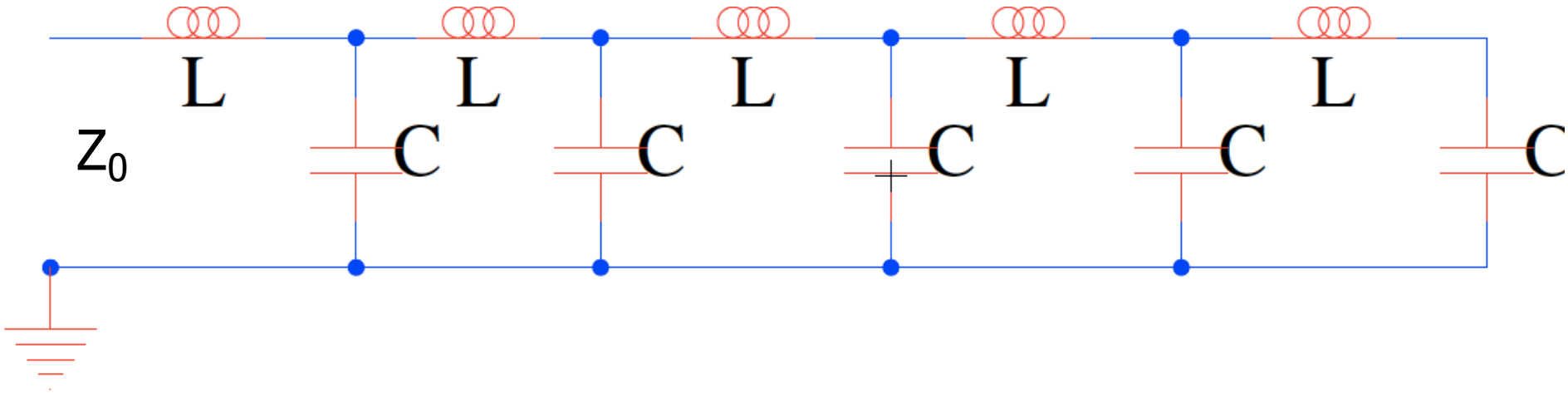
- How long before drop voltage by half?
  R=0.2Ω every meter on Z_0=100Ω

$$V_{snk} = V_{src}\left(\left(\frac{2(R+Z_0)}{(R+Z_0)+Z_0}\right)\left(\frac{Z_0}{R+Z_0}\right)\right)^N$$



Lossless Transmission Line

- What prevents us from having a 500km cat-5 cable?
  - Not actually lossless!

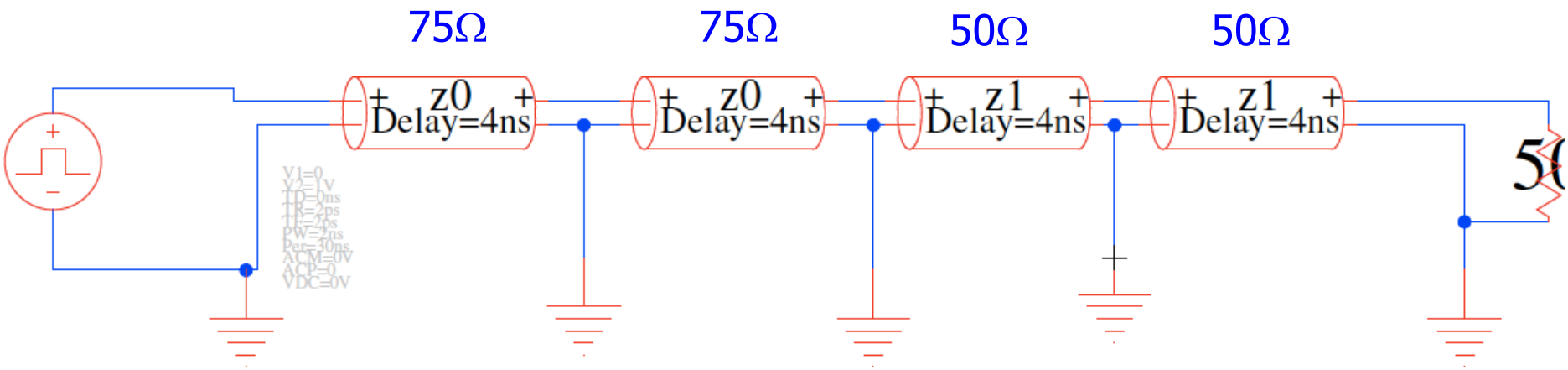


More Examples…

Time Permitting

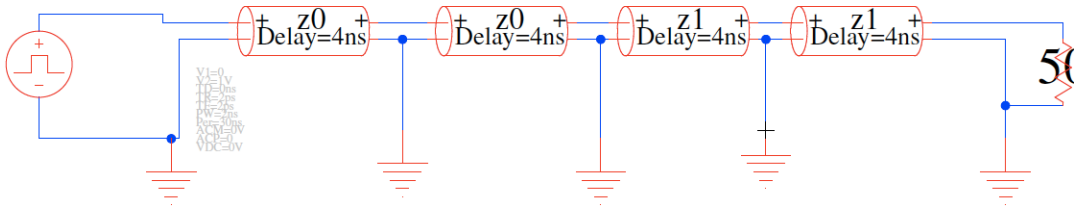
Impedance Change (Preclass 5)

- What happens if there is an impedance change in the wire? Z_0=75Ω, Z_1=50Ω
  - What reflections and transmission do we get?



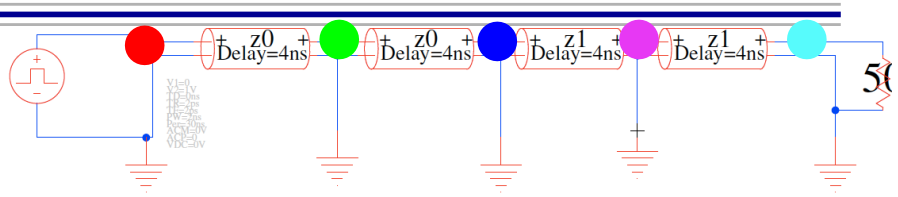
Z_0=75, Z_1=50 (Preclass 5)

- At junction:
  - Reflects
    - $V_r=(50-75)/(50+75)V_i=-0.2V_i$
  - Transmits
    - $V_t=(100/(50+75))V_i=0.8V_i$



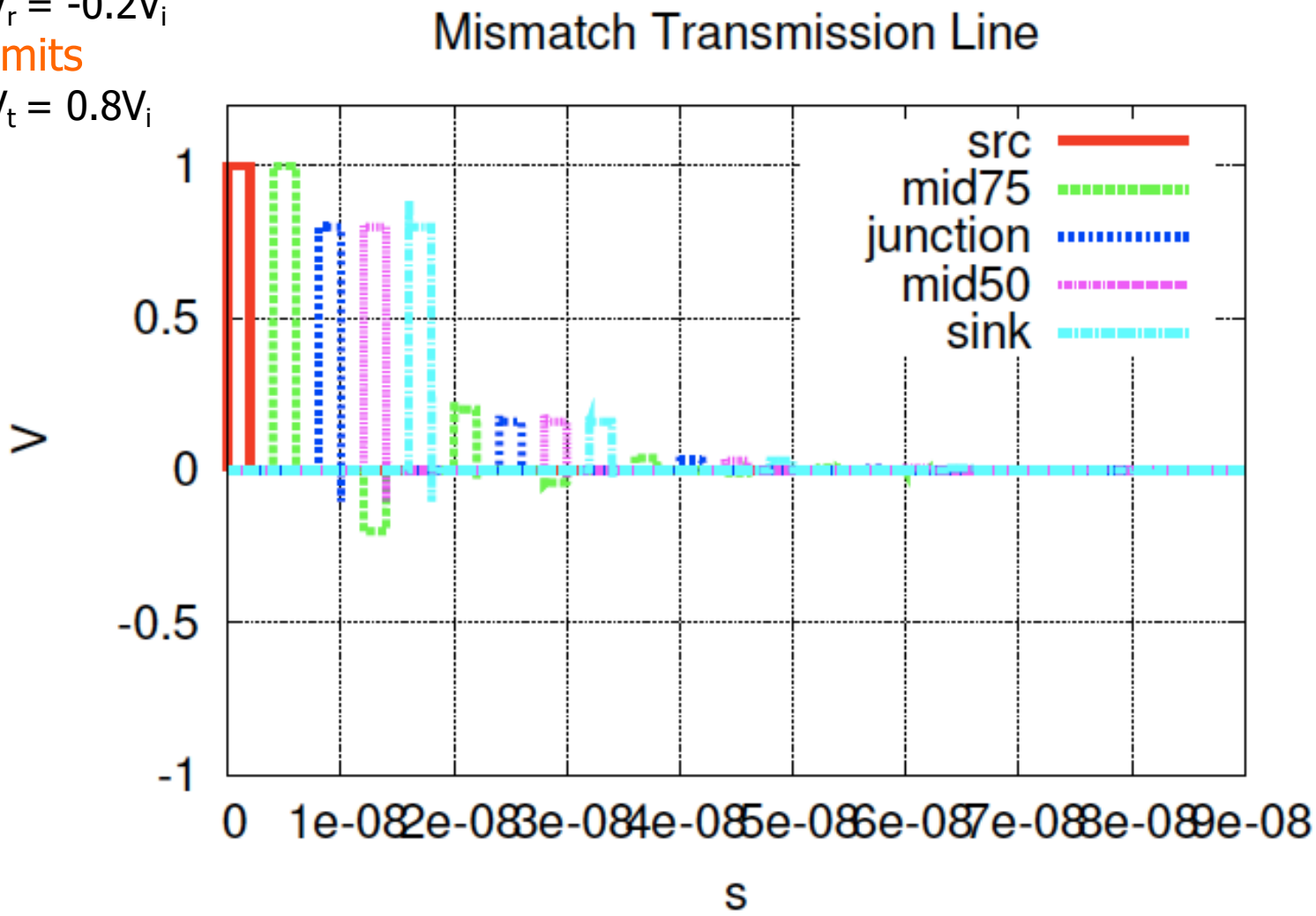
$$V_i\left(\frac{R-Z_0}{R+Z_0}\right)=V_r \qquad V_i\left(\frac{2R}{R+Z_0}\right)=V_t$$

Impedance Change Z_0=75, Z_1=50 (Preclass 5)

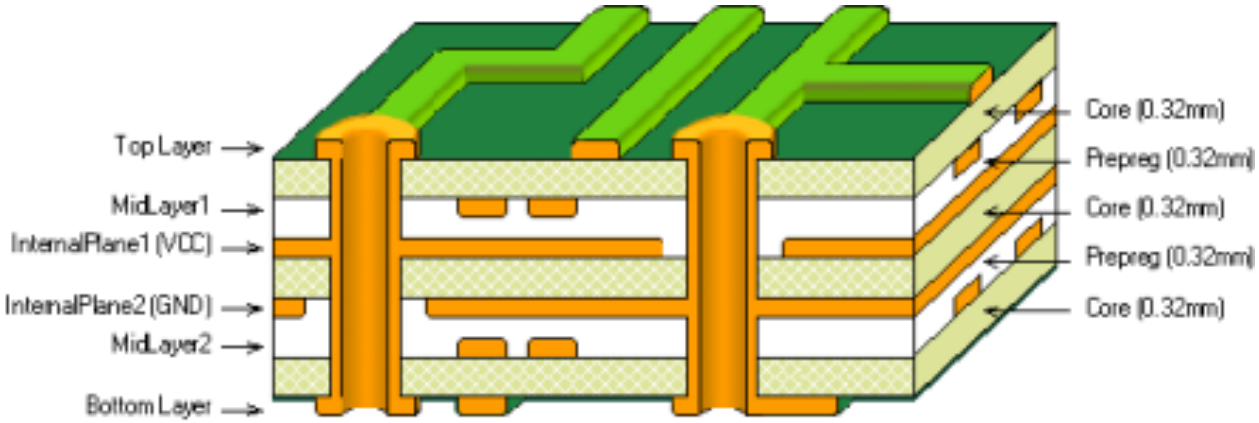


At junction:

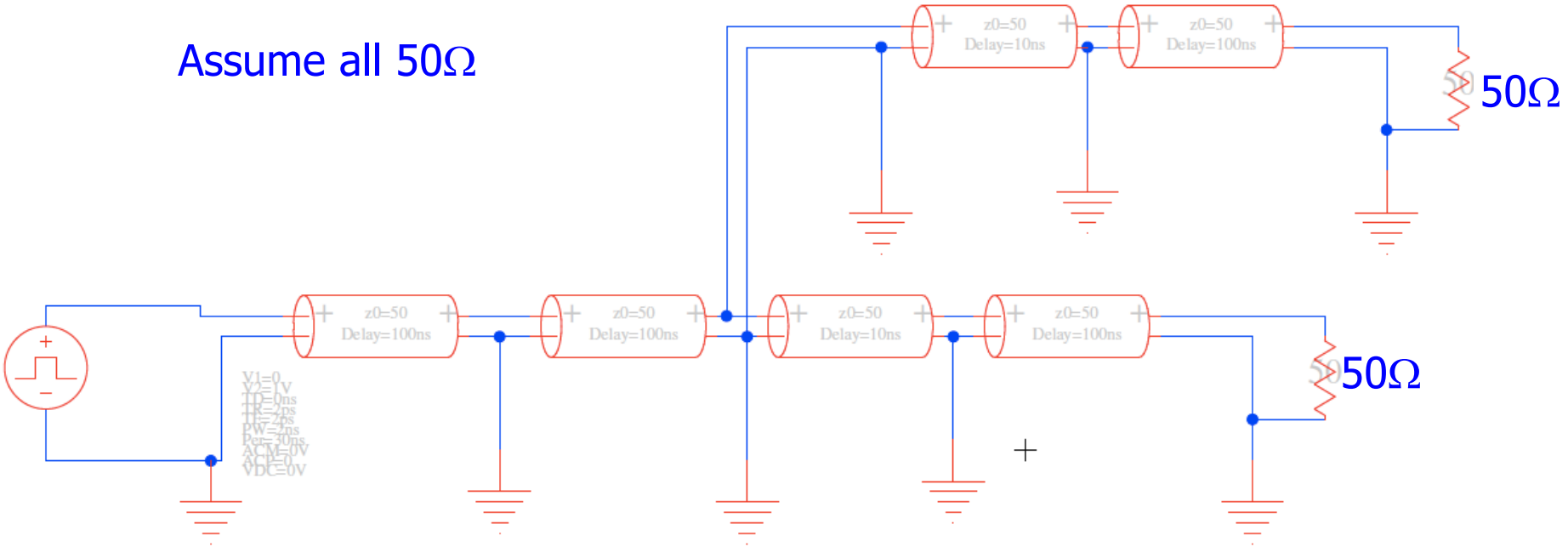
- Reflects
  - $V_r = -0.2V_i$
- Transmits
  - $V_t = 0.8V_i$



What happens at branch?

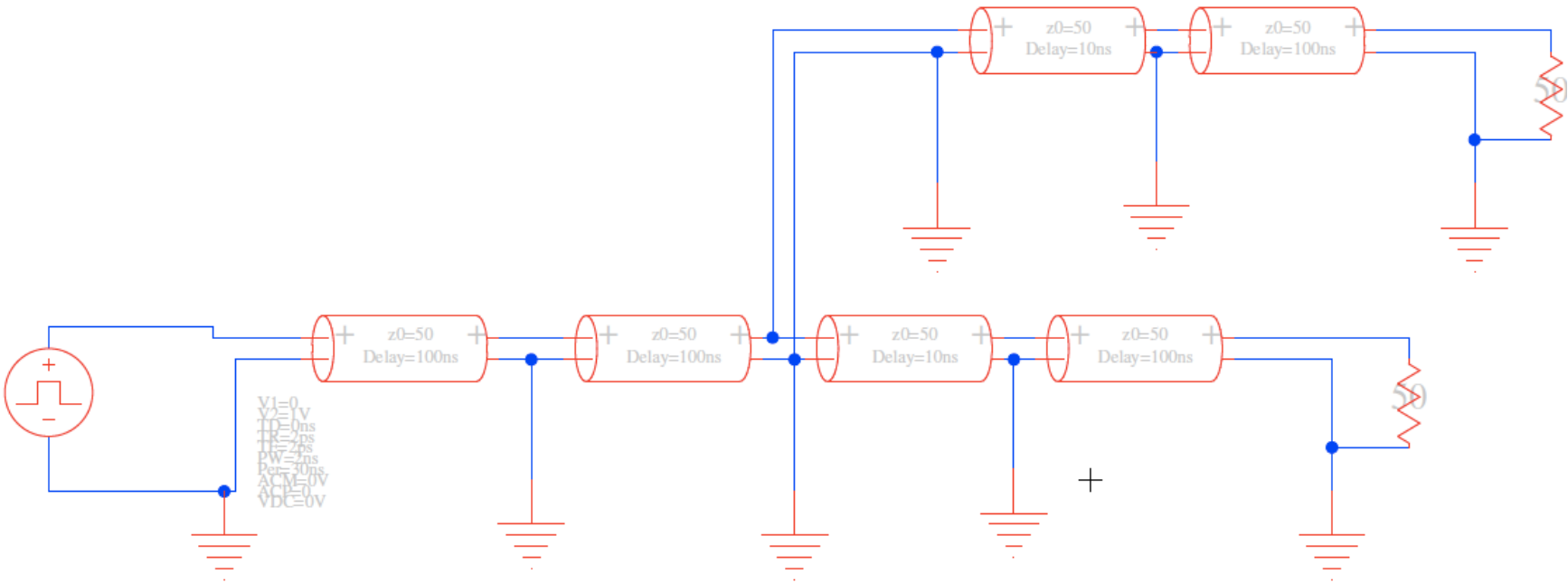


Assume all 50Ω

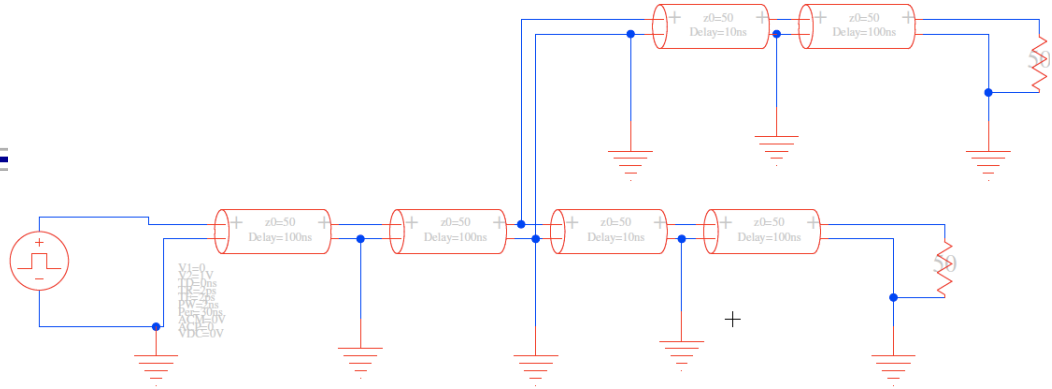


Branch

- Transmission line sees two Z_0 in parallel
  - Looks like $Z_0/2$



$Z_0=50, Z_1=25$

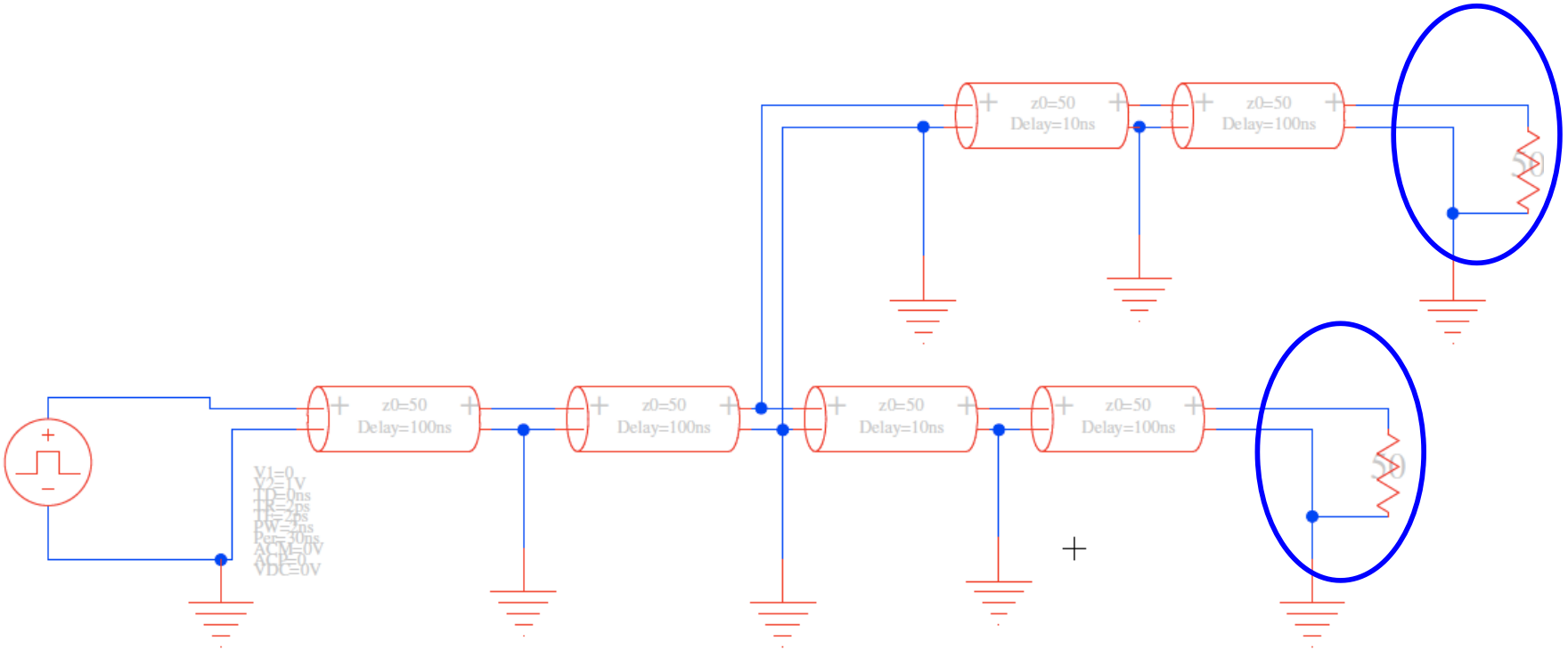


- At junction:
  - Reflects
    - $V_r=(25-50)/(25+50)V_i=-0.33V_i$
  - Transmits
    - $V_t=(50/(25+50))V_i=0.67V_i$

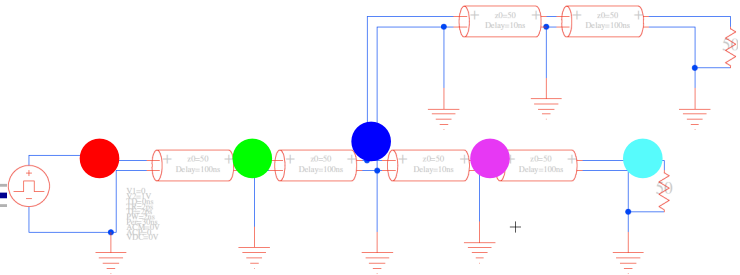
$$V_i\left(\frac{R-Z_0}{R+Z_0}\right)=V_r \qquad V_i\left(\frac{2R}{R+Z_0}\right)=V_t$$

End of Branch

- What happens at end?
- If ends in matched, parallel termination
  - No further reflections

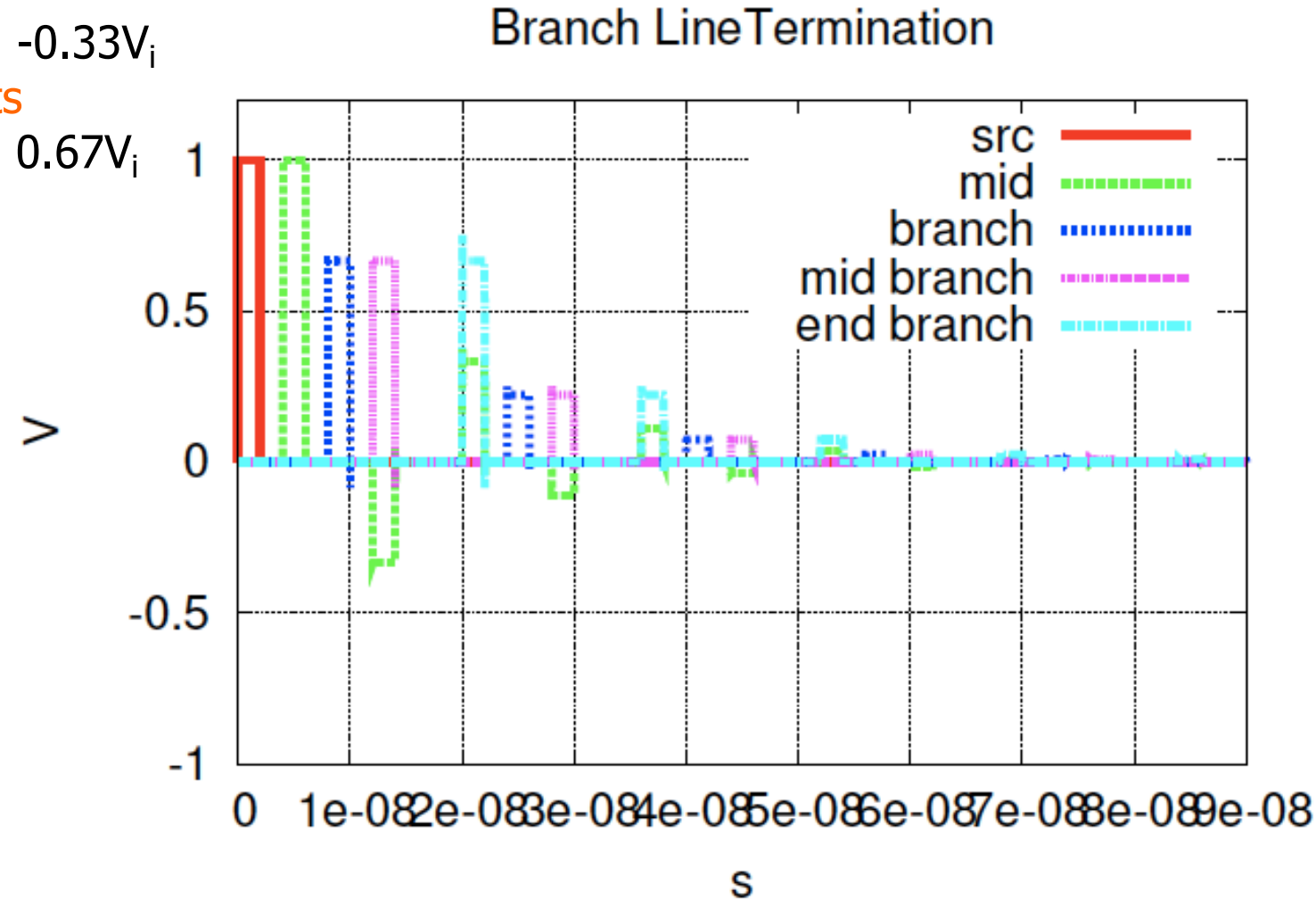


Branch Simulation



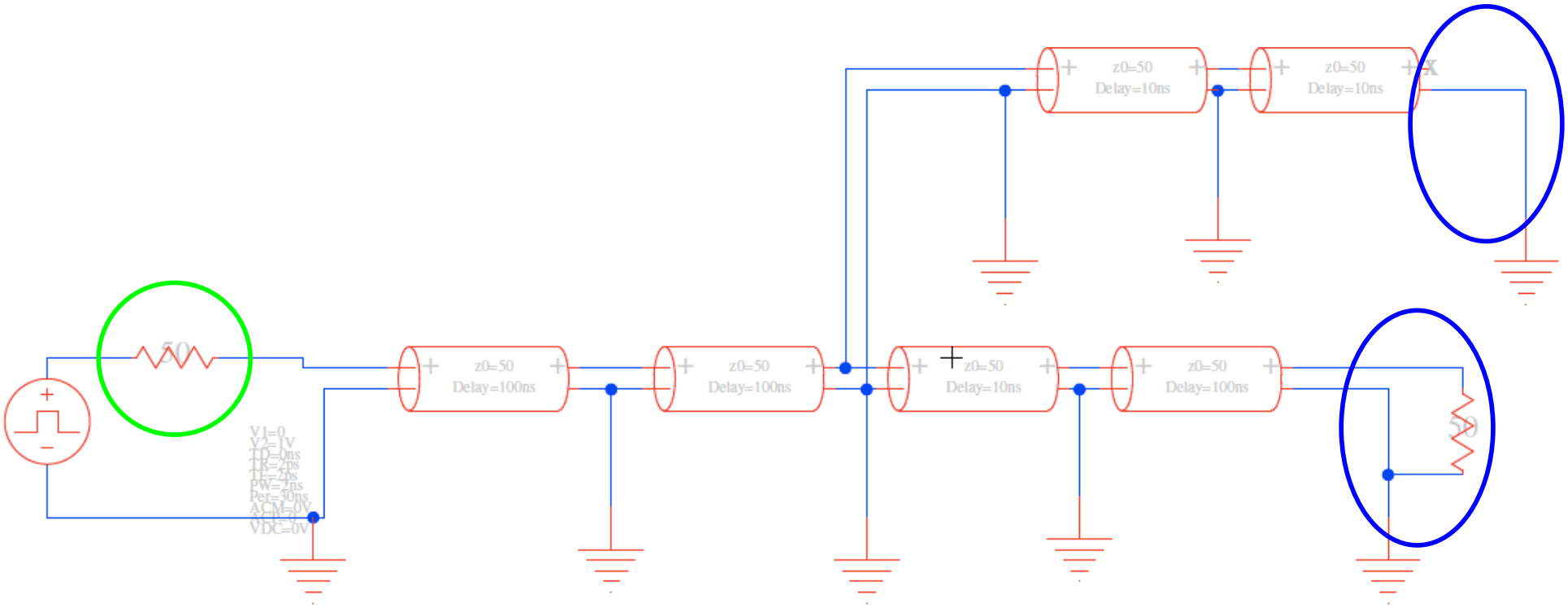
At junction:

- Reflects
  - $V_r = -0.33V_i$
- Transmits
  - $V_t = 0.67V_i$



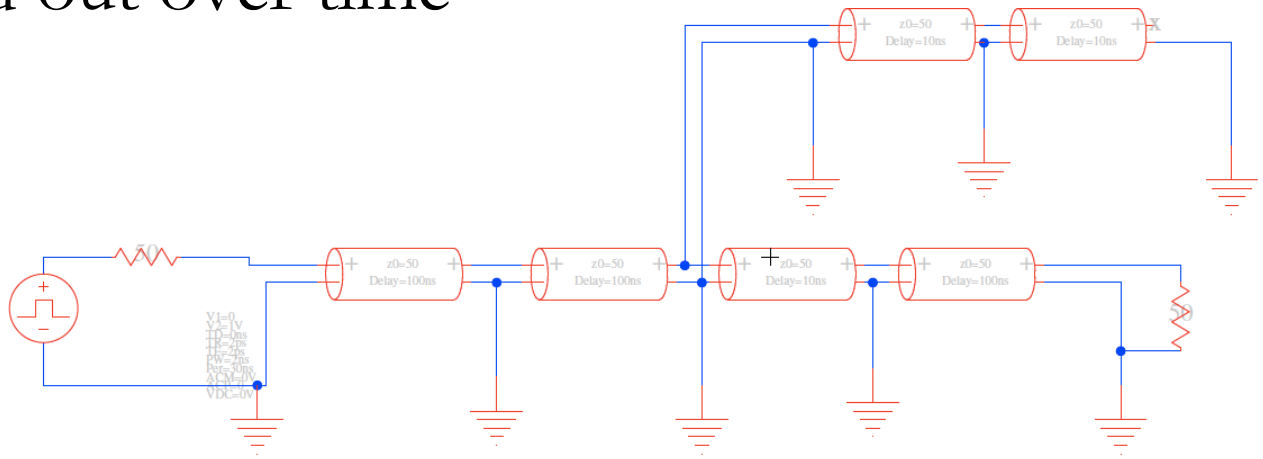
Branch with Open Circuit?

- What happens if branch open circuit?
- And source termination?

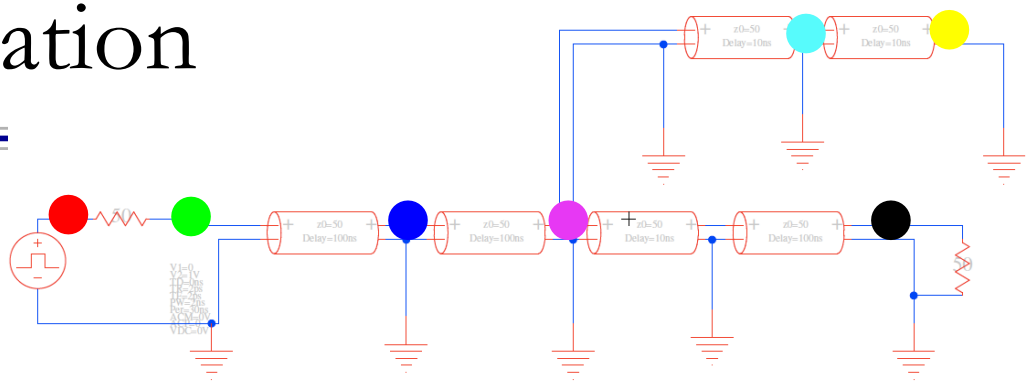


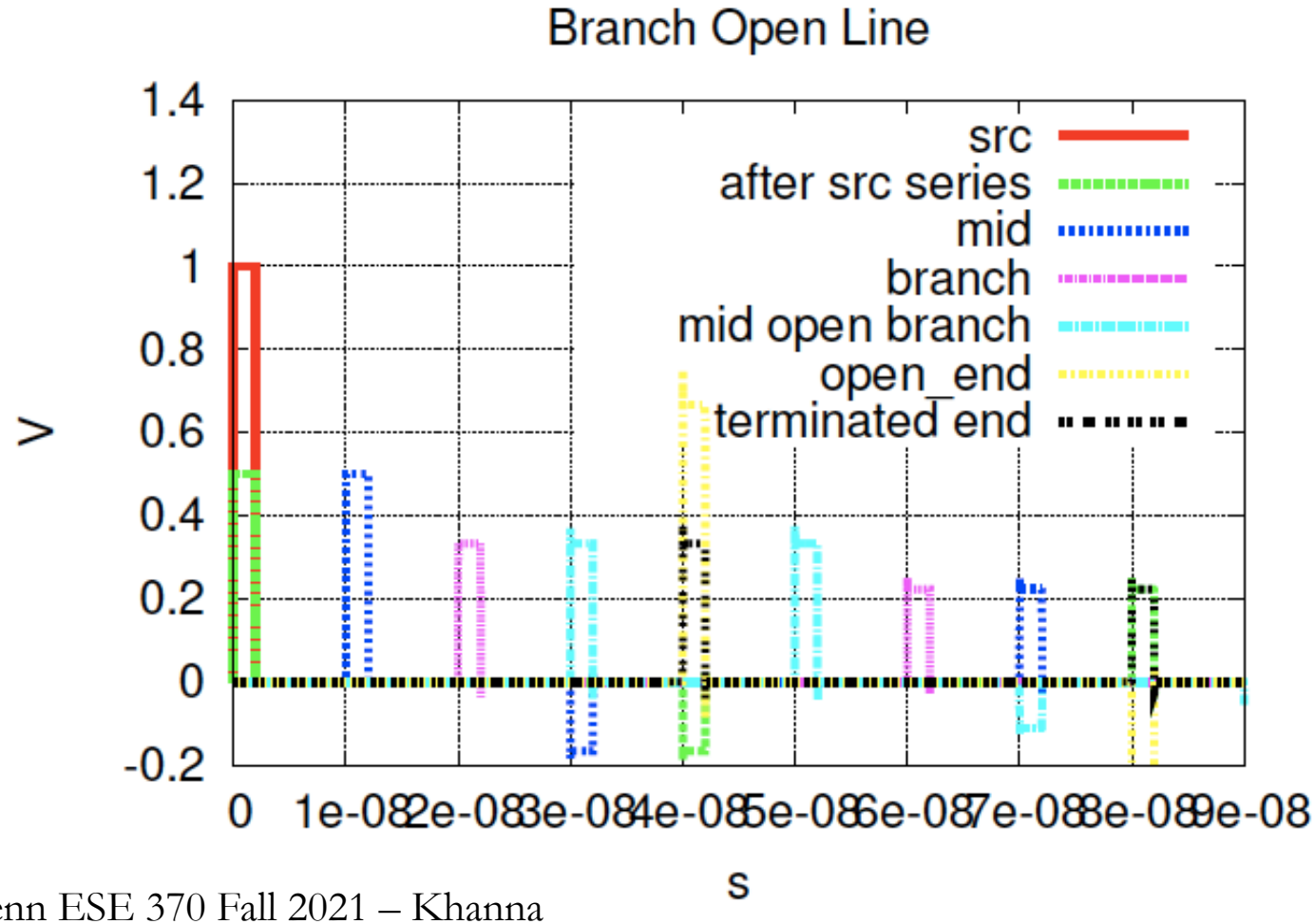
Branch with Open Circuit

- Reflects at end of open-circuit stub
- Reflection returns to branch
  - …and encounters branch again
  - Send transmission pulse to both
    - Source and other branch
- Sink sees original pulse as multiple smaller pulses spread out over time

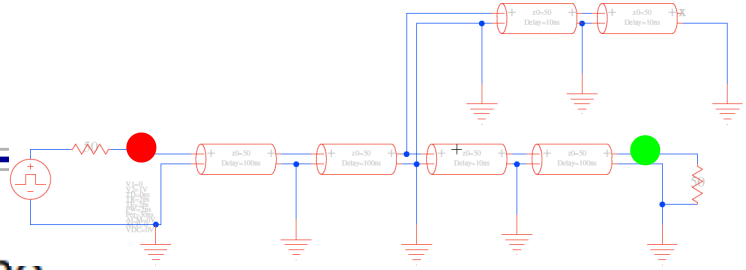


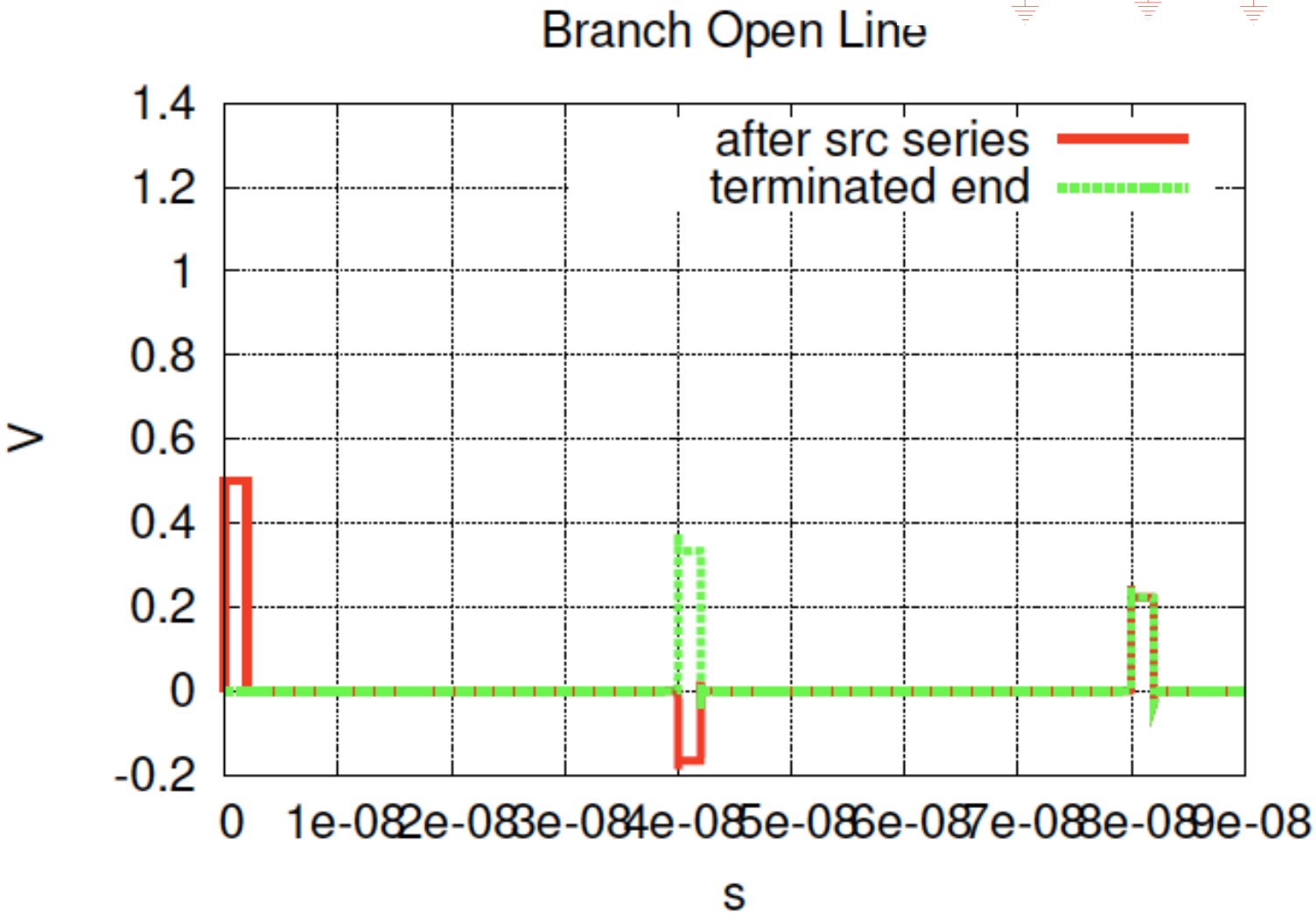
Open Branch Simulation





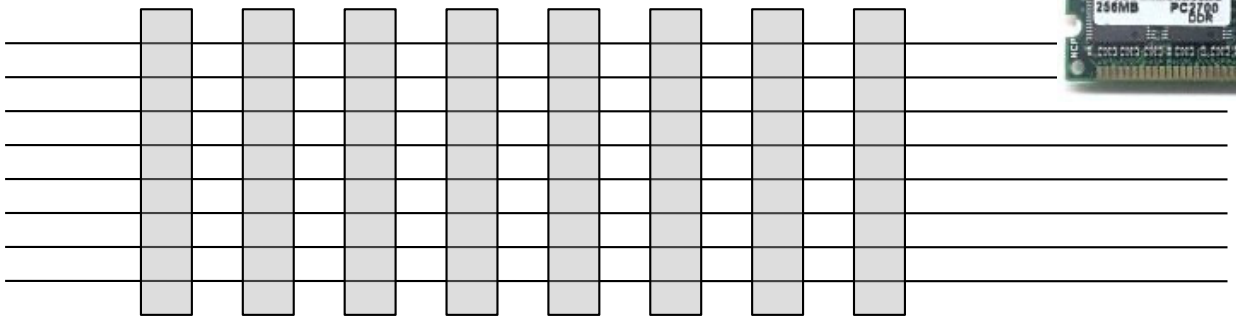
Open Branch Simulation





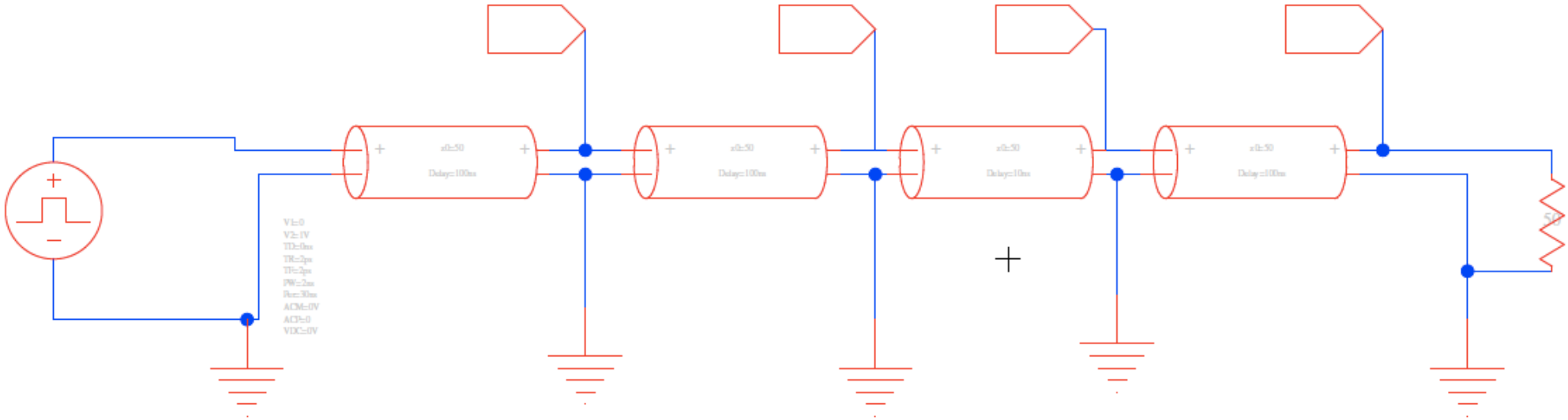
Bus

- Common to have many modules on a bus
  - E.g. PCI slots
  - DIMM slots for memory
- High speed → bus lines are trans. lines



Multi-drop Bus

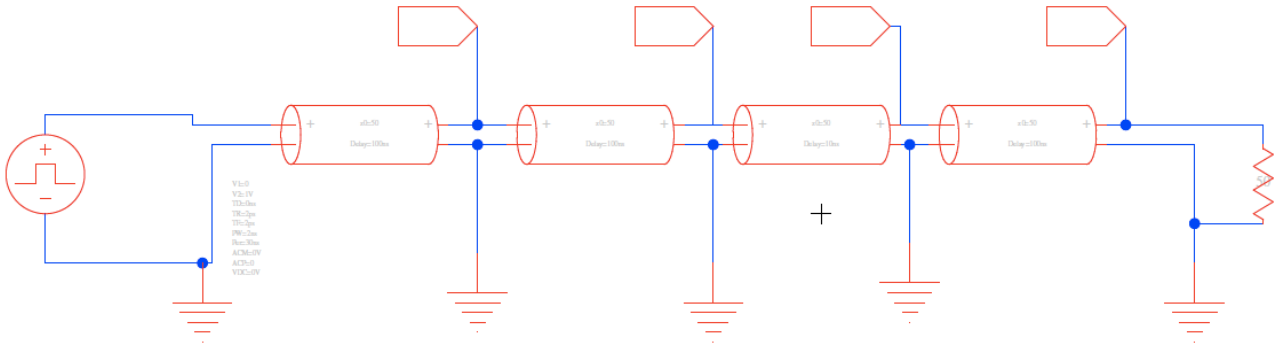
- Ideal
  - Open circuit, no load

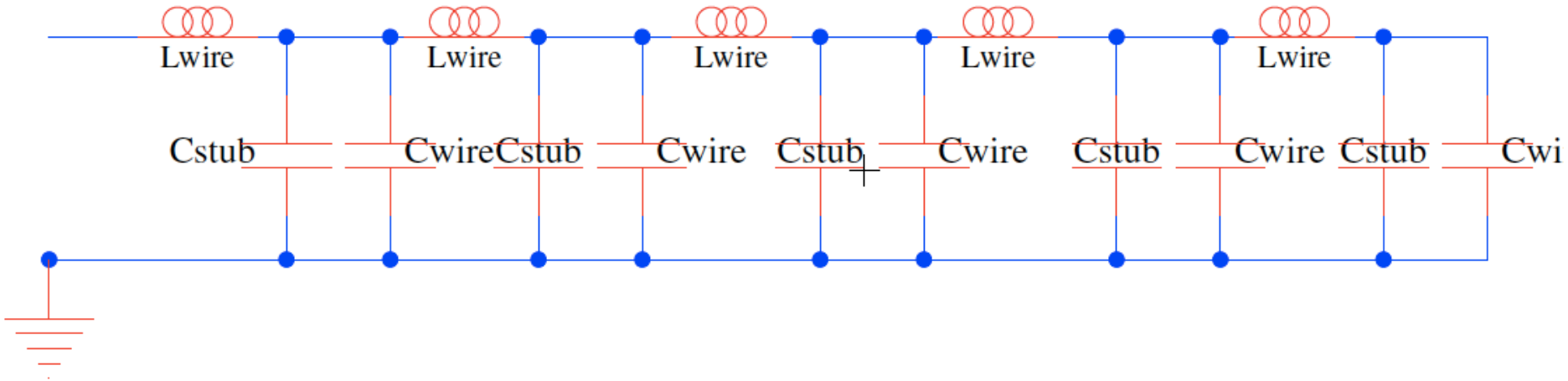


Multi-Drop Bus

- Impact of capacitive load (stub) at drop?
  - If tight/regular enough, change Z of line

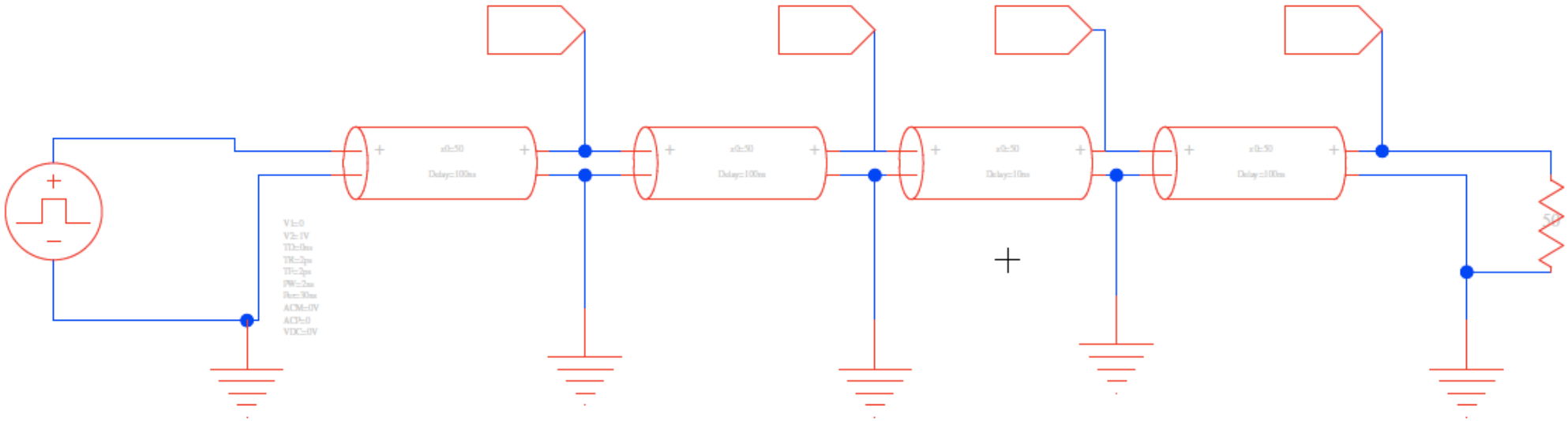
$$Z_0 = \sqrt{\frac{L}{C}}$$





Multi-Drop Bus

- Long wire stub?
  - Looks like branch
    - may produce reflections



Transmission Line Noise

- Frequency limits
- Imperfect termination
- Mismatched segments/junctions/vias/connectors
- Loss due to resistance in line
  - Limits length

Idea

- Transmission lines
  - high-speed
  - high throughput
  - long-distance signaling
- Termination
- Signal quality losses

$$w = \frac{1}{\sqrt{LC}} = \frac{c_0}{\sqrt{\varepsilon_r \mu_r}}$$

$$Z_0 = \sqrt{\frac{L}{C}}$$

$$V_r = V_i \left(\frac{R - Z_0}{R + Z_0} \right)$$

Admin

- Friday HW 7 due
- Final (F 12/17)
  - 12-2pm in Moore 212
  - Cumulative: Lec 1 – 35
    - Big Idea slides from each lecture
  - Finals 2010—2020 online
  - Friday lecture review
  - TA review session before exam
    - TBD, watch Piazza. Maybe a poll.