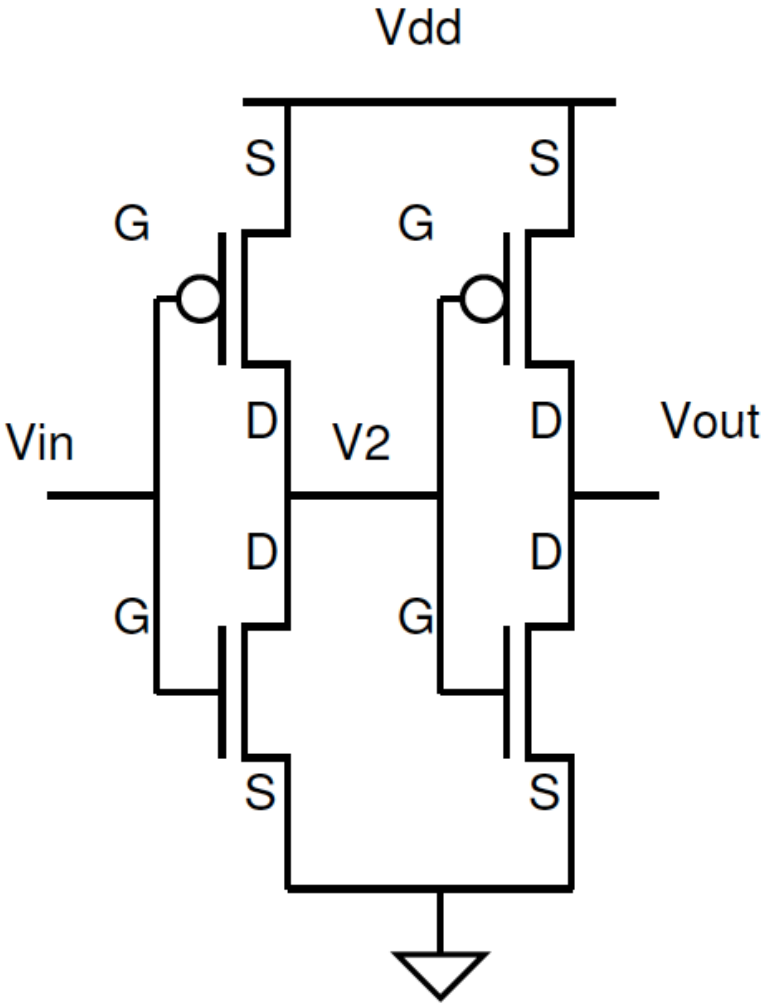
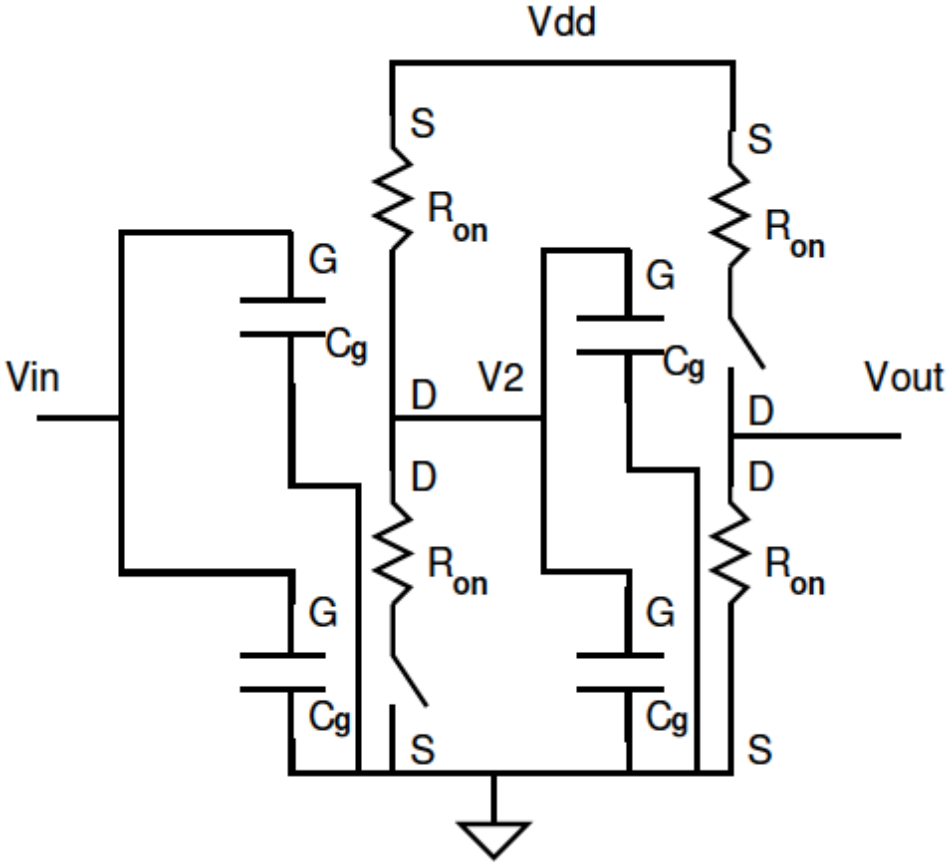
ESE370: Circuit-Level Modeling, Design, and Optimization for Digital Systems

Lec 5: September 15, 2021

Delay and RC Response

Delay is RC Charging

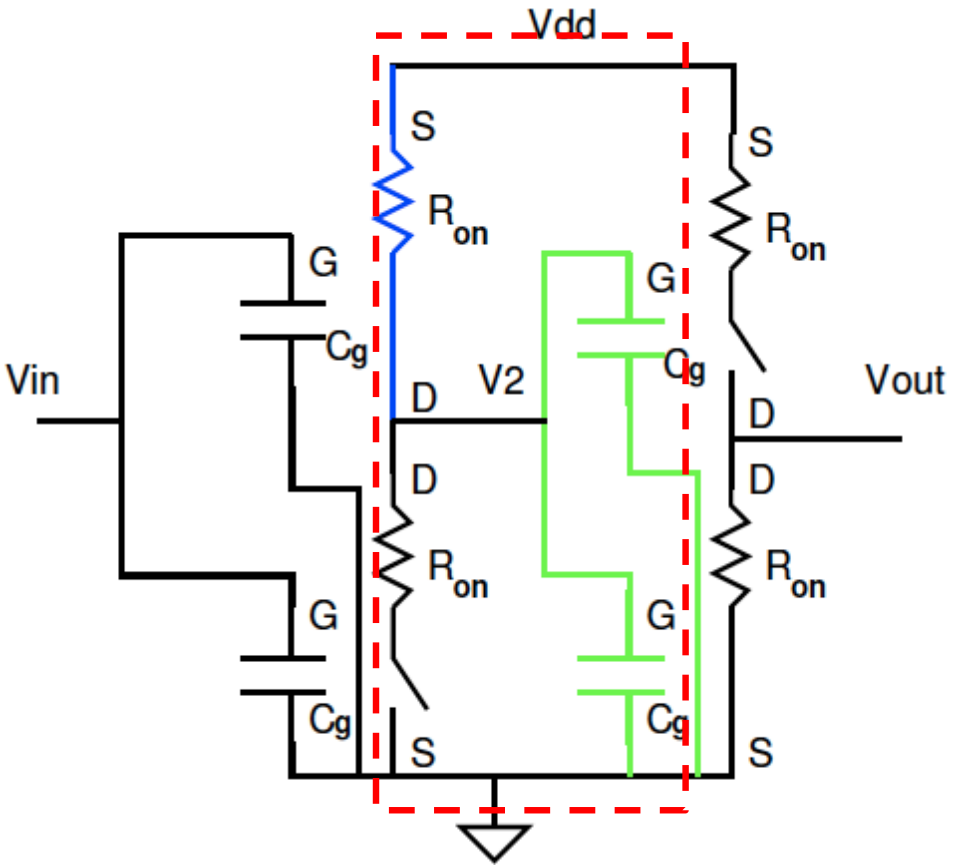




Gate Delay is RC Charging

Strategy:

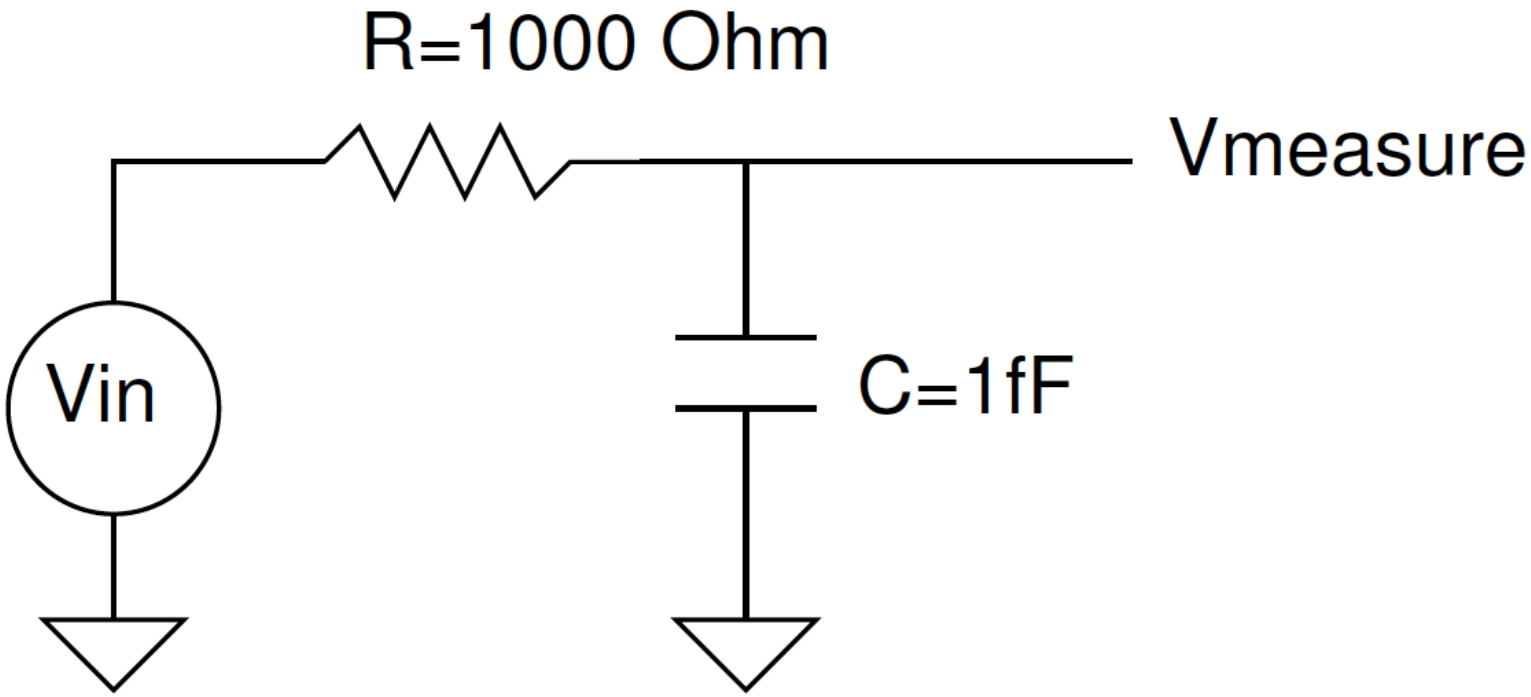
- Use zero-order model to understand switch state
- Break into output/input stages
- For each stage
  - Understand R_{drive}
  - Understand C_{load}



Today

- RC Charging
  - RC Step Response Curve
- What is the C?
  - Capacitive load on logic gate output node
- What is the R?
  - Equivalent output resistance on the current path driving the output node
- Approximating and Measuring Delay
  - Tau estimate!

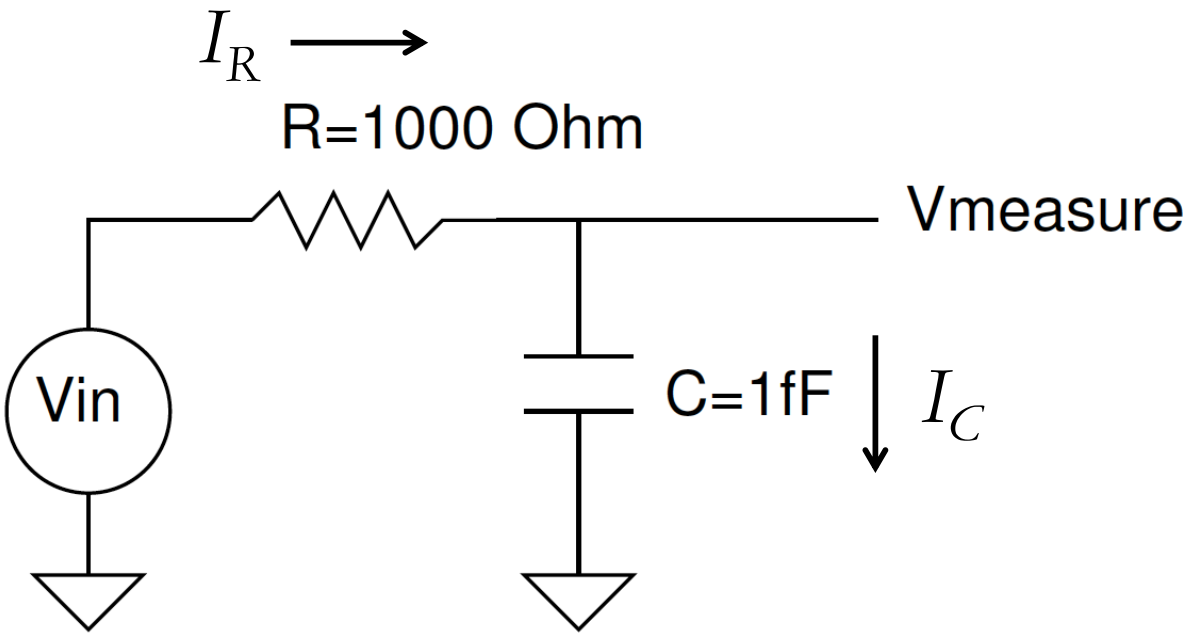
90% Rise Time? (preclass 1ab)



What is final $V_{measure}$?

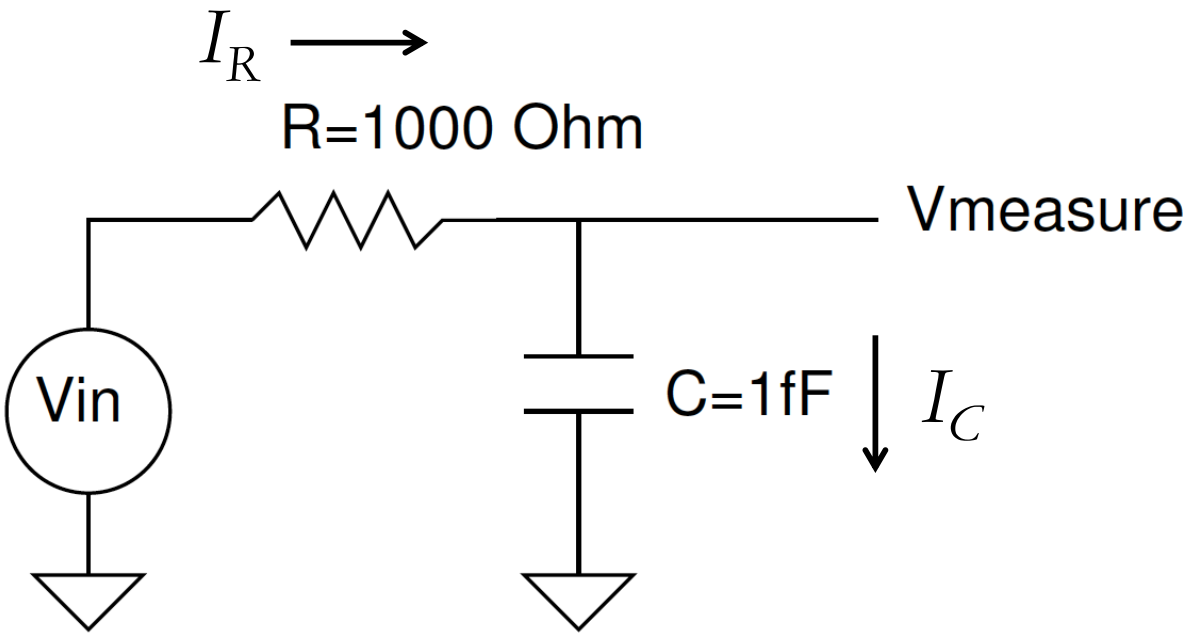
What is time constant, τ?

Governing Equations? (KCL)



- KCL @ $V_{measure}$
  - Kirchoff's Current Law
    - Sum of all currents into a node = 0
    - Current entering a node = current exiting a node
  - $I_R = I_C$

Governing Equations? (KCL)

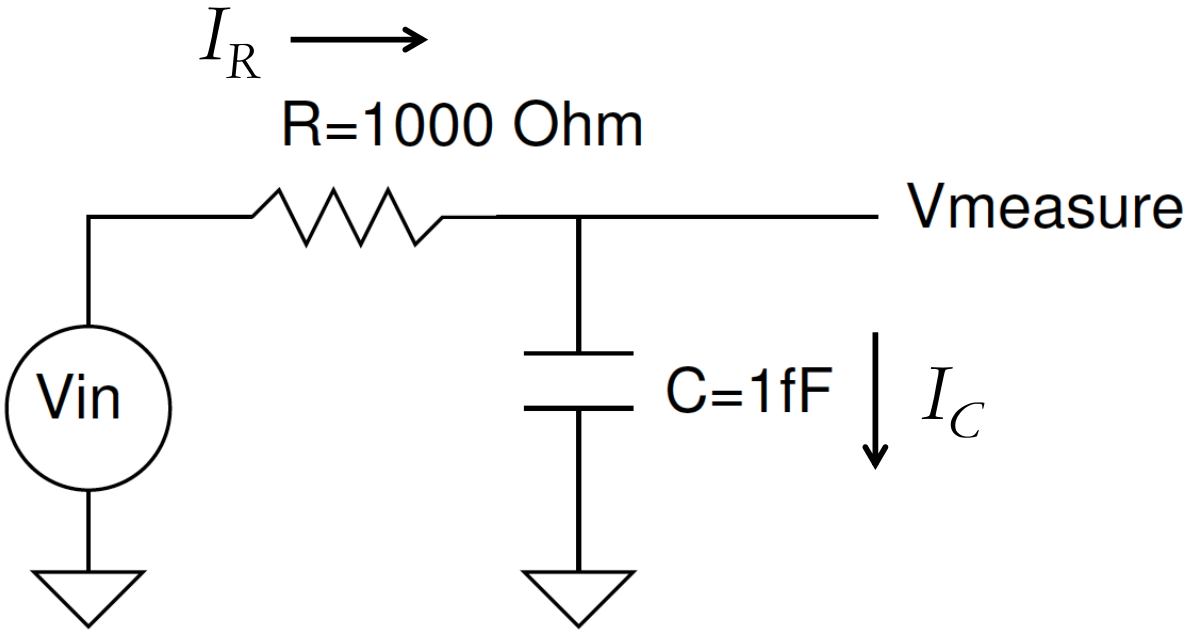


$$I_R = I_C$$

$$\frac{V_R}{R} = C\frac{dV_C}{dt}$$

$$\frac{V_{in} - V_{measure}}{R} = C\frac{dV_{measure}}{dt}$$

Governing Equations? (KCL)



$$I_R = I_C$$

$$\frac{V_R}{R} = C\frac{dV_C}{dt}$$

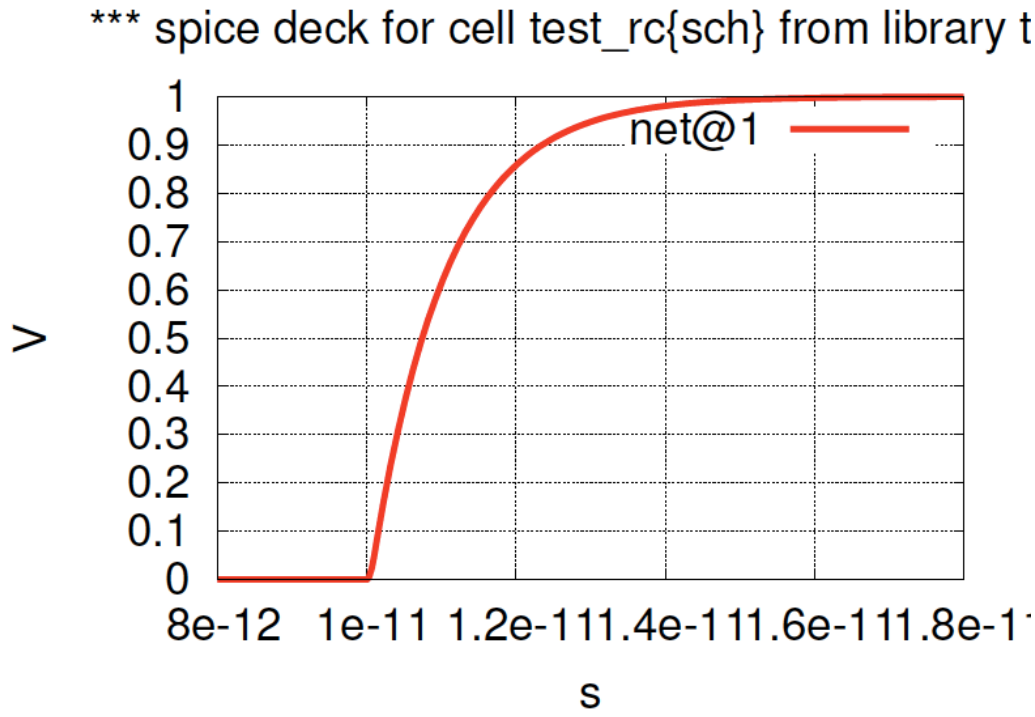
$$\frac{V_{in} - V_{measure}}{R} = C\frac{dV_{measure}}{dt}$$

$$0 = \frac{dV_{measure}}{dt} + \frac{1}{RC}V_{measure} - \frac{V_{in}}{RC}$$

$$V_{measure} = V_{in}\left(1 - \left(e^{-t/RC}\right)\right)$$

$$\tau = RC$$

What does look like?



$$V_{measure} = V_{in}\left(1 - \left(e^{-t/RC}\right)\right)$$

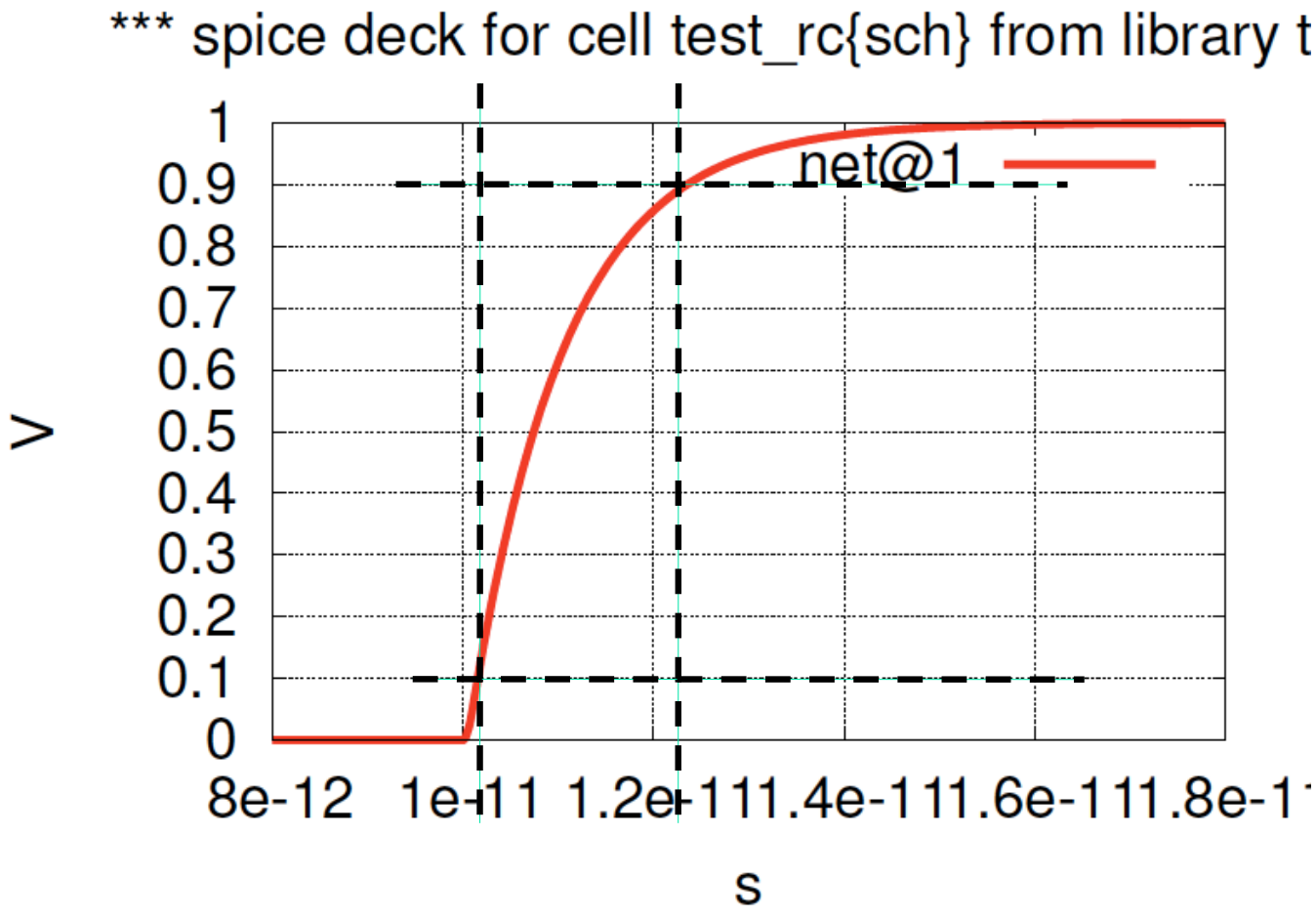
Shape of Curve (preclass 1c)

t (in ps)	$e^{-t/RC}$	$1-e^{-t/RC}$
0		
0.1		
1		
2		
2.3		

$V_{in}=1$

$$V_{measure} = V_{in}\left(1-\left(e^{-t/RC}\right)\right)$$

Rise Time: 10—90%



$t_{rise} \sim= 2.2ps \sim= 2.2\tau$

Shape of Curve (preclass 1d)

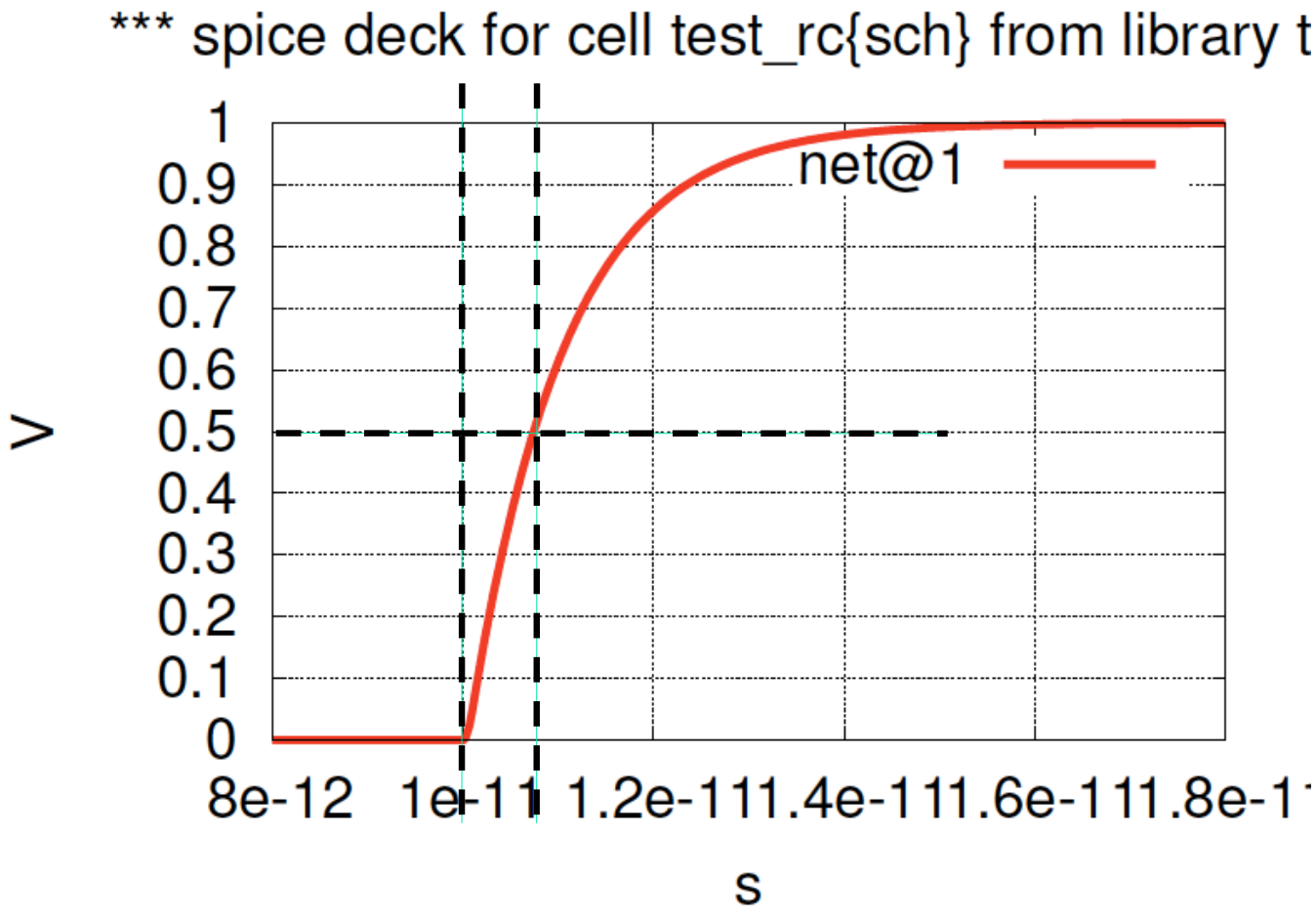
t (in ps)	$e^{-t/RC}$	$1-e^{-t/RC}$
0		
0.1		
1		
2		
2.3		

$V_{in}=1$

$$V_{measure} = V_{in}\left(1-\left(e^{-t/RC}\right)\right)$$

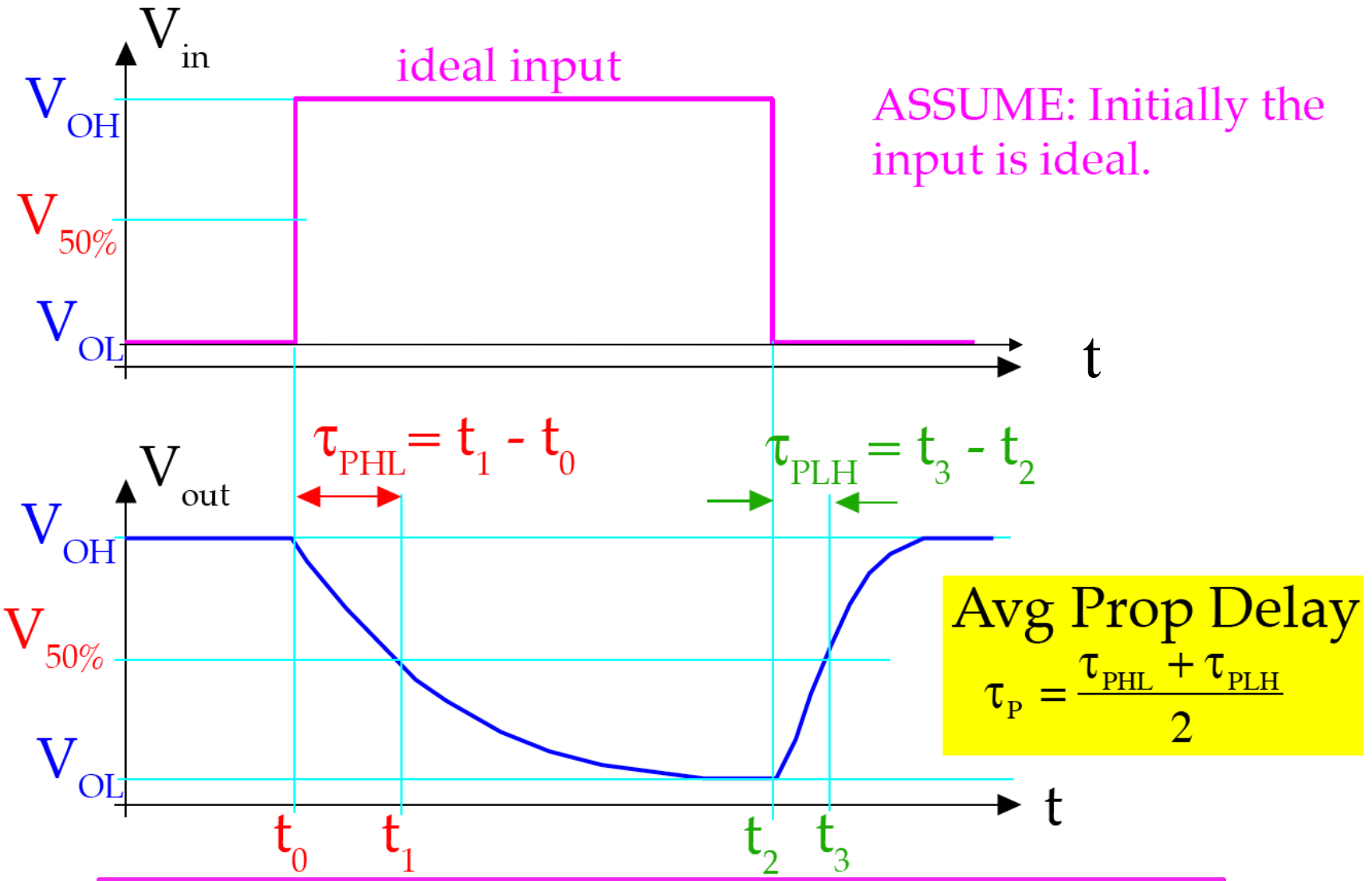
At what time is $V_{measure}$ 50% of its value?

Delay Time: 50% (in)—50% (out)



$t_{PLH} \sim= .69ps \sim= .69\tau$

Propagation Delay Definitions

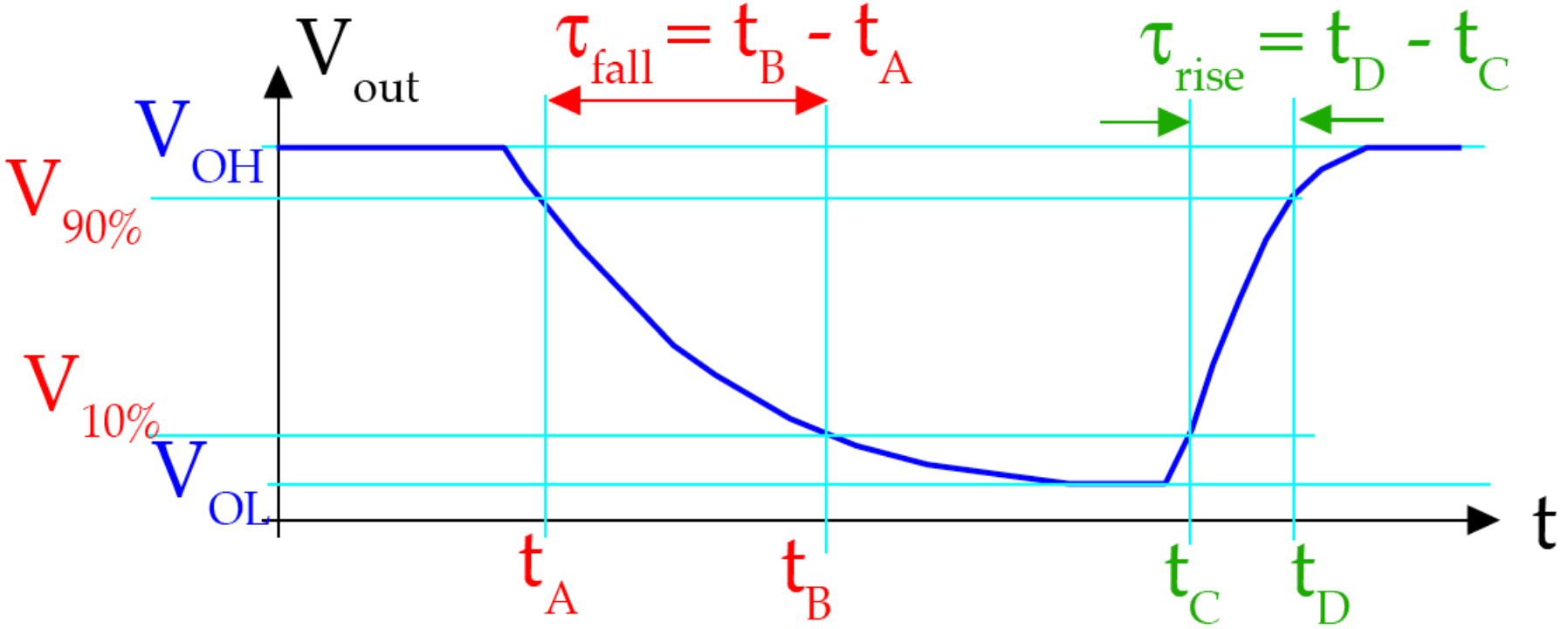


Avg Prop Delay

$$\tau_P = \frac{\tau_{PHL} + \tau_{PLH}}{2}$$

$$V_{50\%} = V_{OL} + 0.5\,[V_{OH} - V_{OL}] = 0.5\,[V_{OL} + V_{OH}]$$

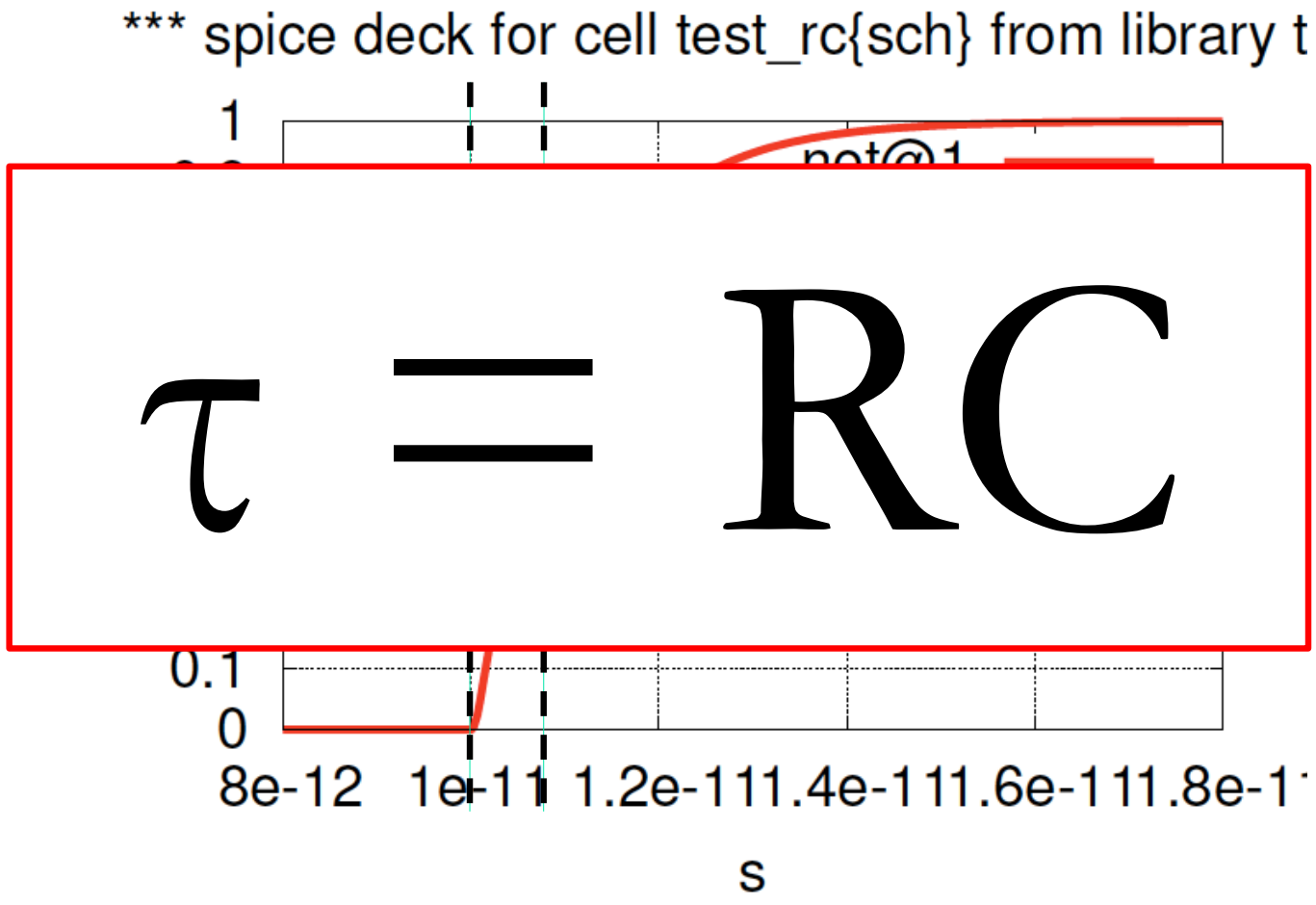
Rise/Fall Times



$$V_{10\%} = V_{OL} + 0.1\,[V_{OH} - V_{OL}]$$

$$V_{90\%} = V_{OL} + 0.9\,[V_{OH} - V_{OL}]$$

Delay Time: 50% (in)—50% (out)



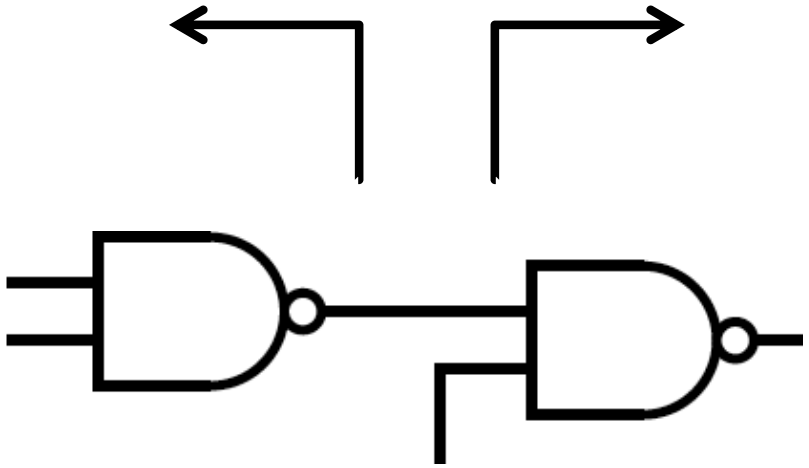
$$\tau = RC$$

$$t_{PLH} \sim= .69ps \sim= .69\tau$$

Voltage Waveform at Output/Input Node

R_{drive} from looking into output stages

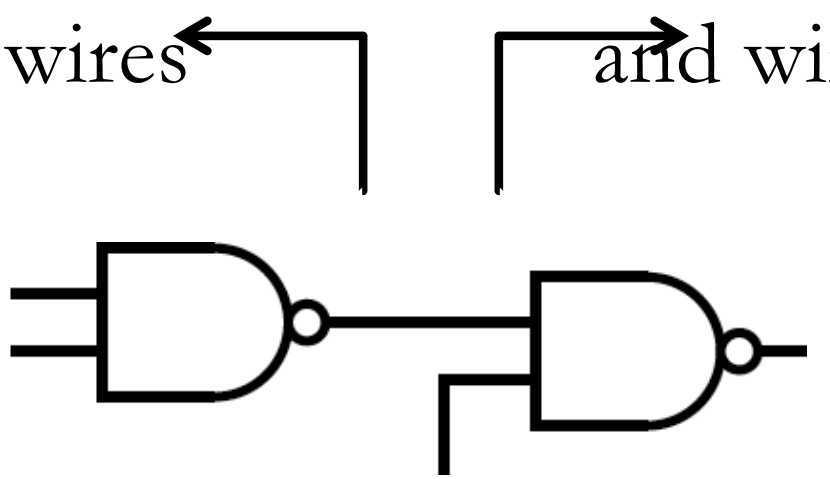
C_{load} from looking into input stages



Voltage Waveform at Output/Input Node

R_{drive} from looking into output stages and wires

C_{load} from looking into input stages and wires



What is C?

Capacitance

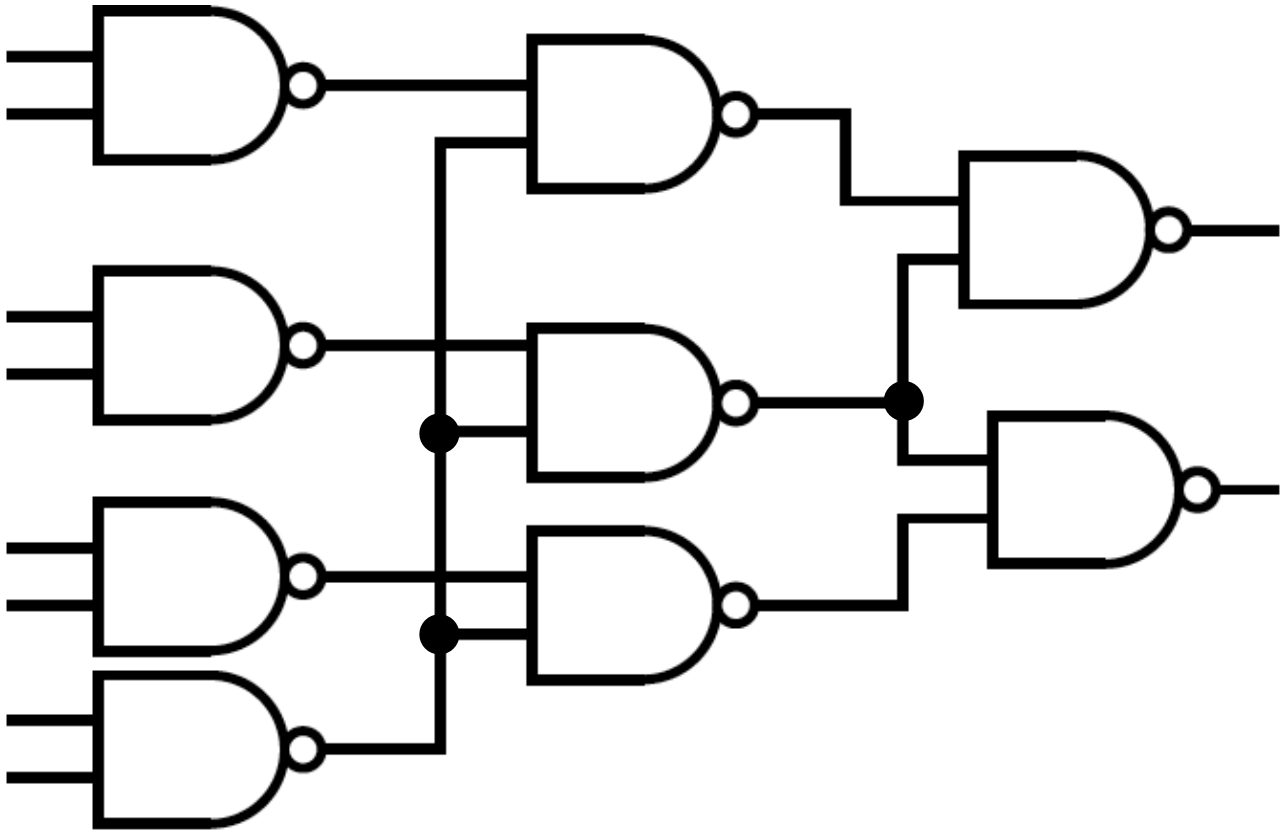
- Wire
- Fanout -- Total gate load
  - Logical Gate
    - MOSFET gate

Fanout

- Number of things to which a gate output connects

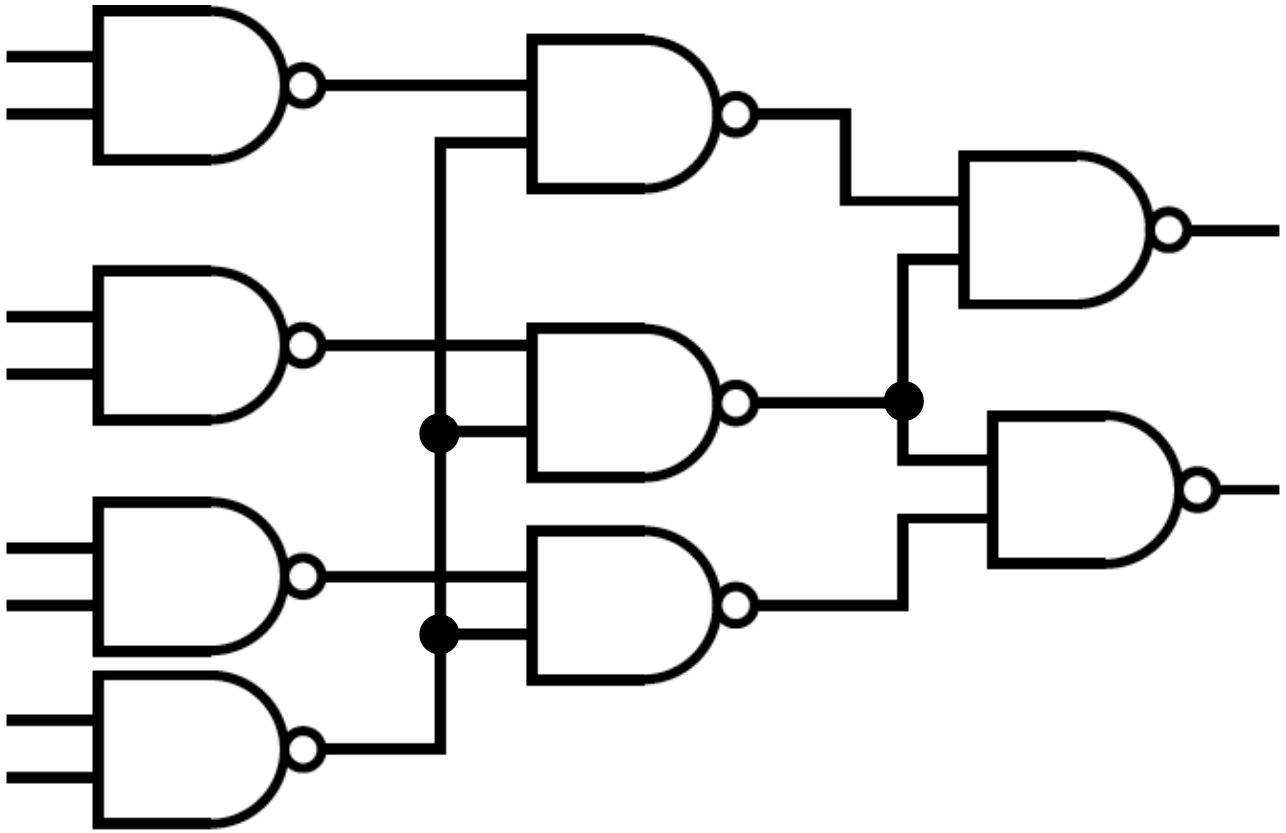
Fanout in Circuit

- Output routed to many gate inputs



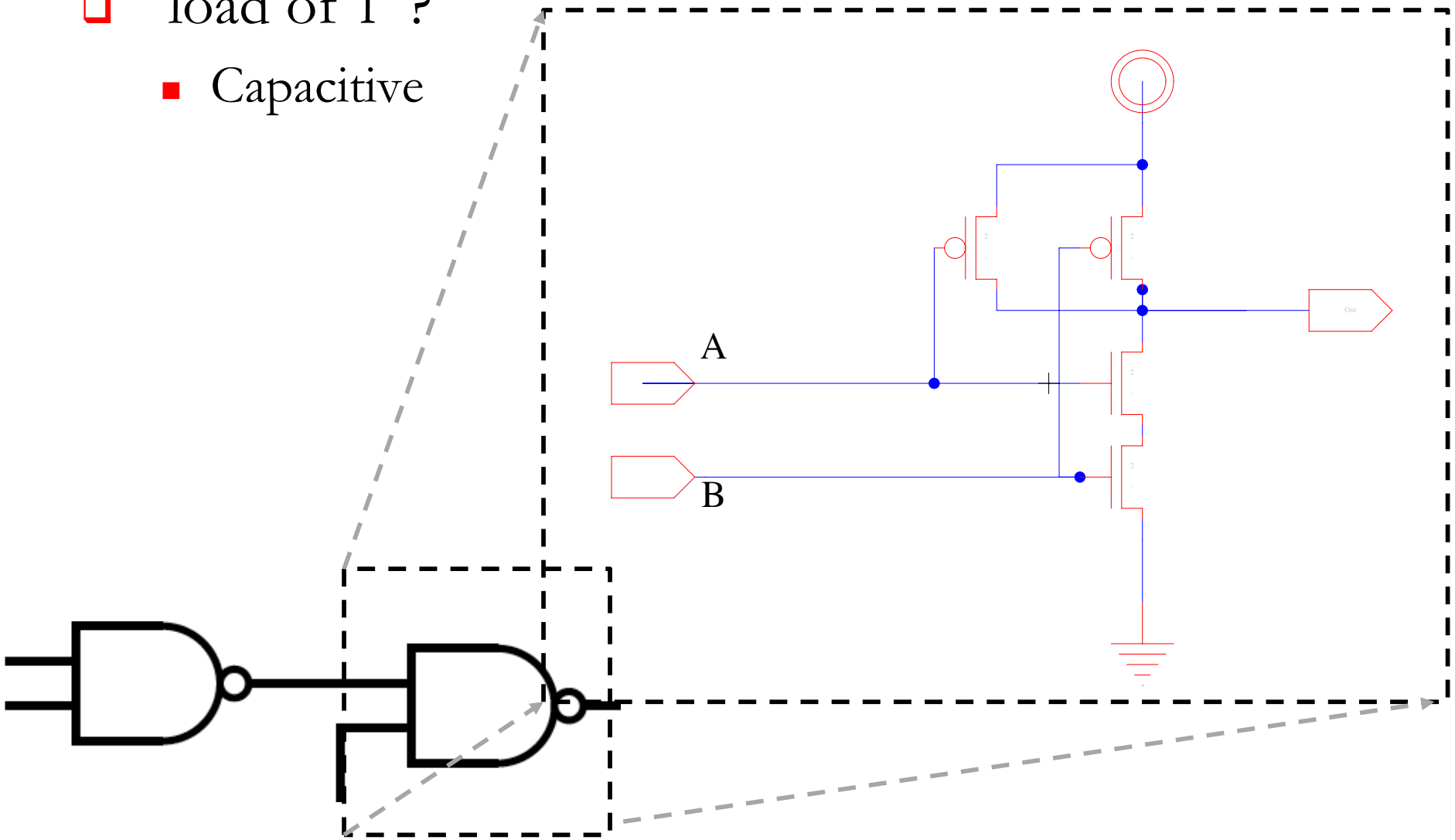
Fanout in Circuit (preclass 2)

- Maximum fanout?
- Second?
- Min?



MOSFET Capacitance

- "load of 1"?
  - Capacitive



MOSFET Capacitance

- "load of 1"?
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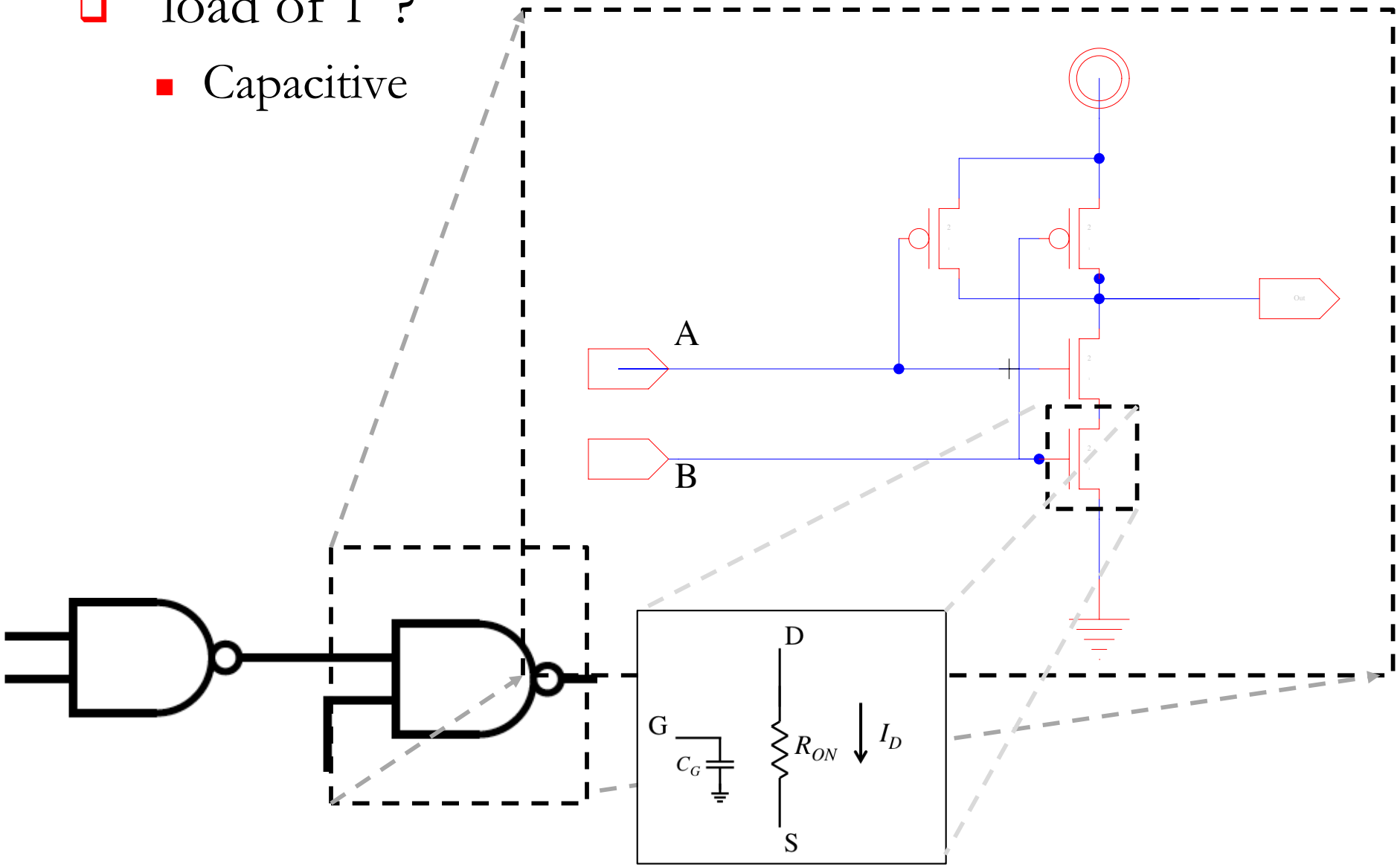
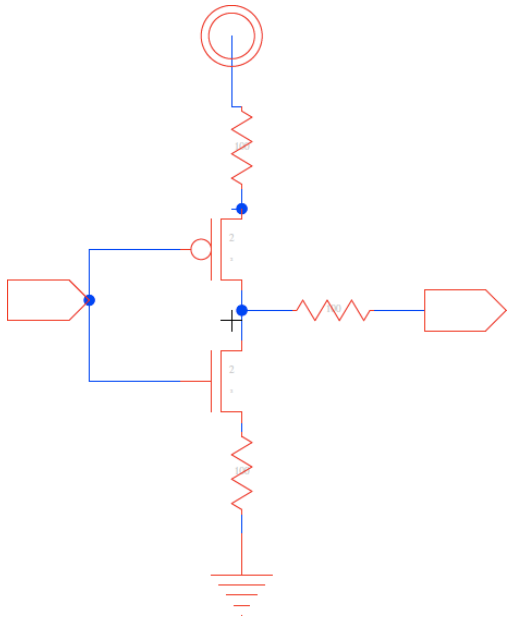


Lumped Capacitive Load

$$C_{load} = \sum_{i \in fanout} C_{G_i} + \sum_{i \in wires} C_{w_i}$$

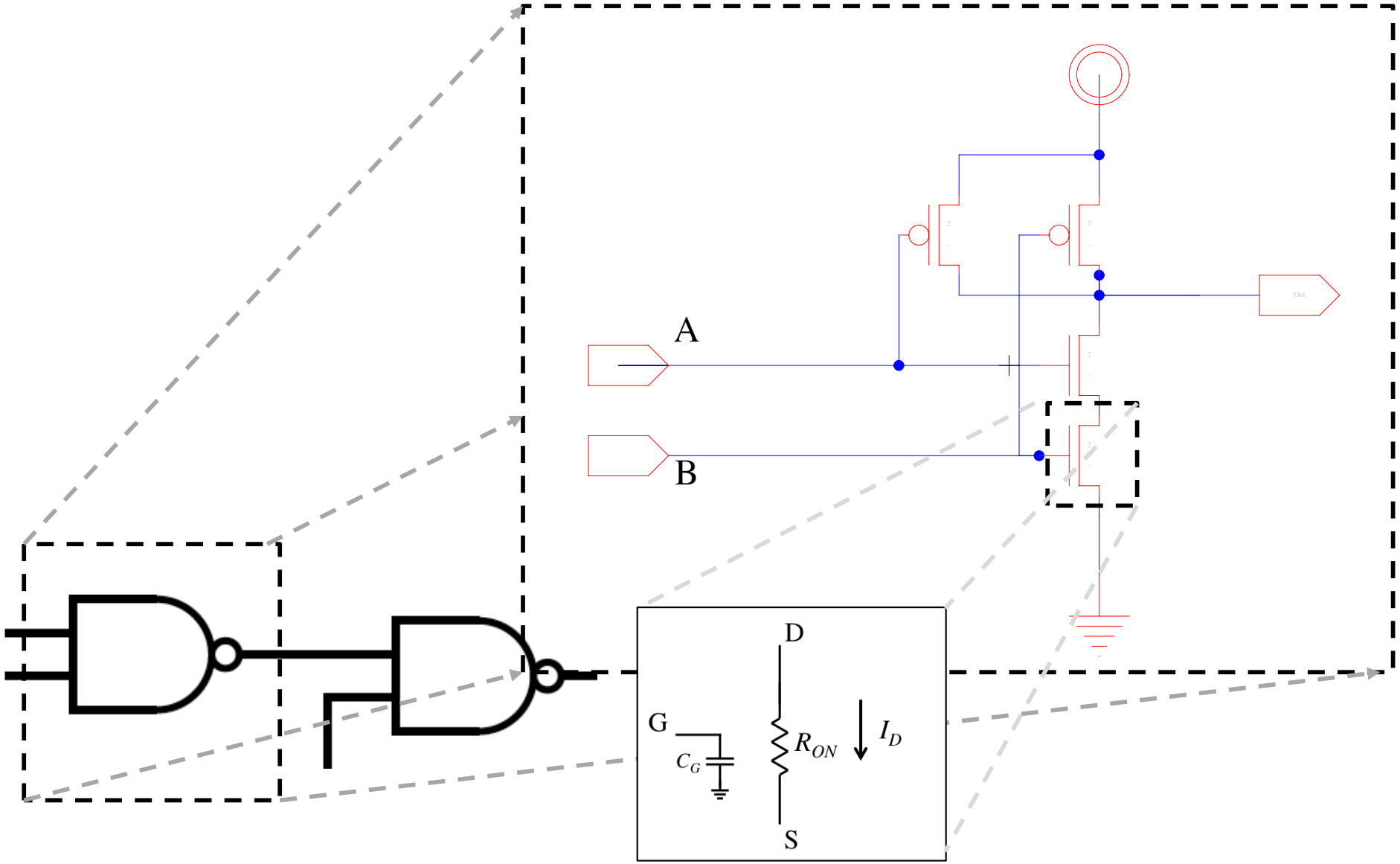
What is R?

Resistance



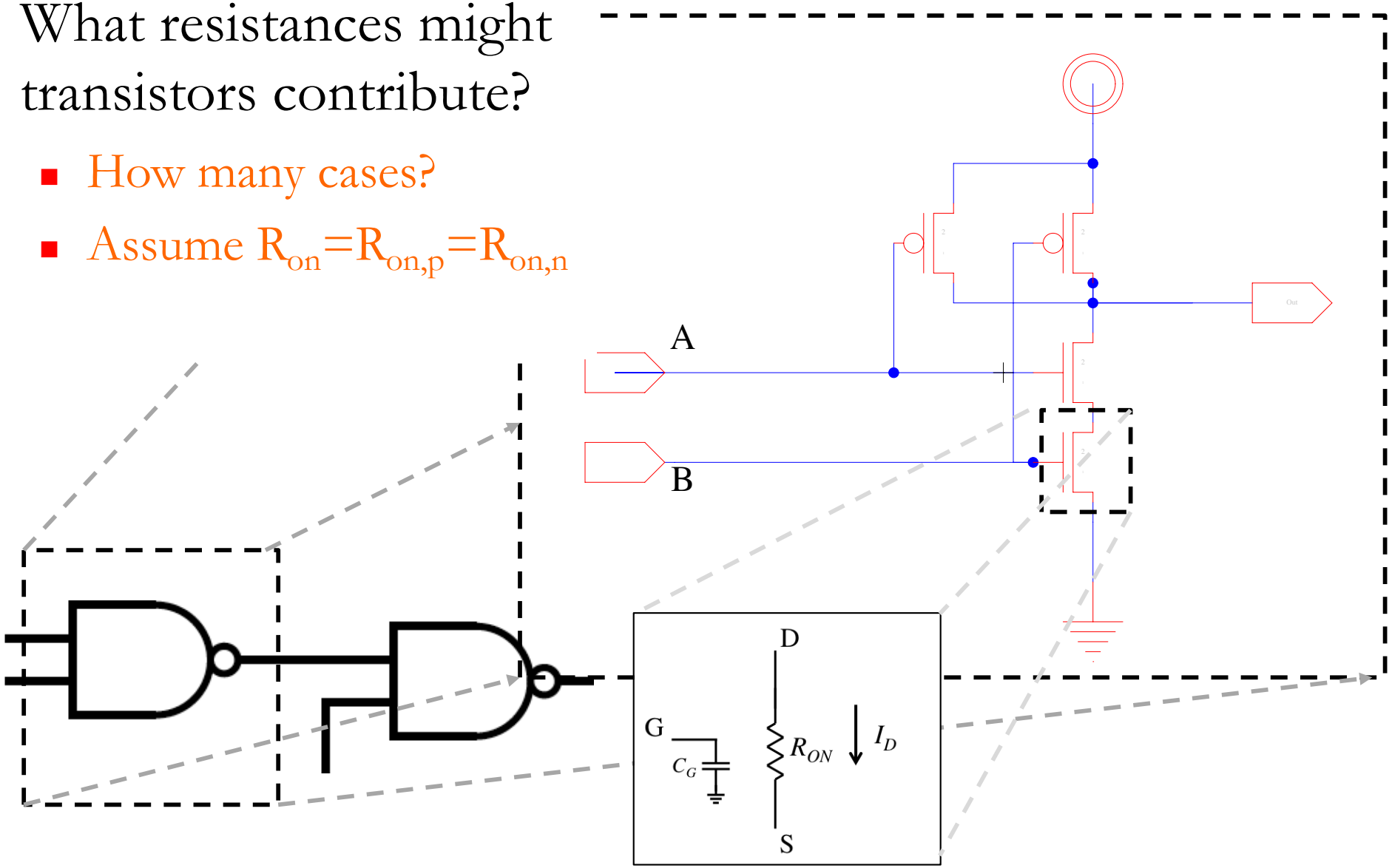
- Wire resistance
  - From supply (Vdd or Gnd) to transistor source
  - From transistor output to gate it is driving
- Transistor equivalent resistance (R_{on})

Equivalent Resistance



Equivalent Resistance (prelcass 3)

- What resistances might transistors contribute?
  - How many cases?
  - Assume $R_{on}=R_{on,p}=R_{on,n}$



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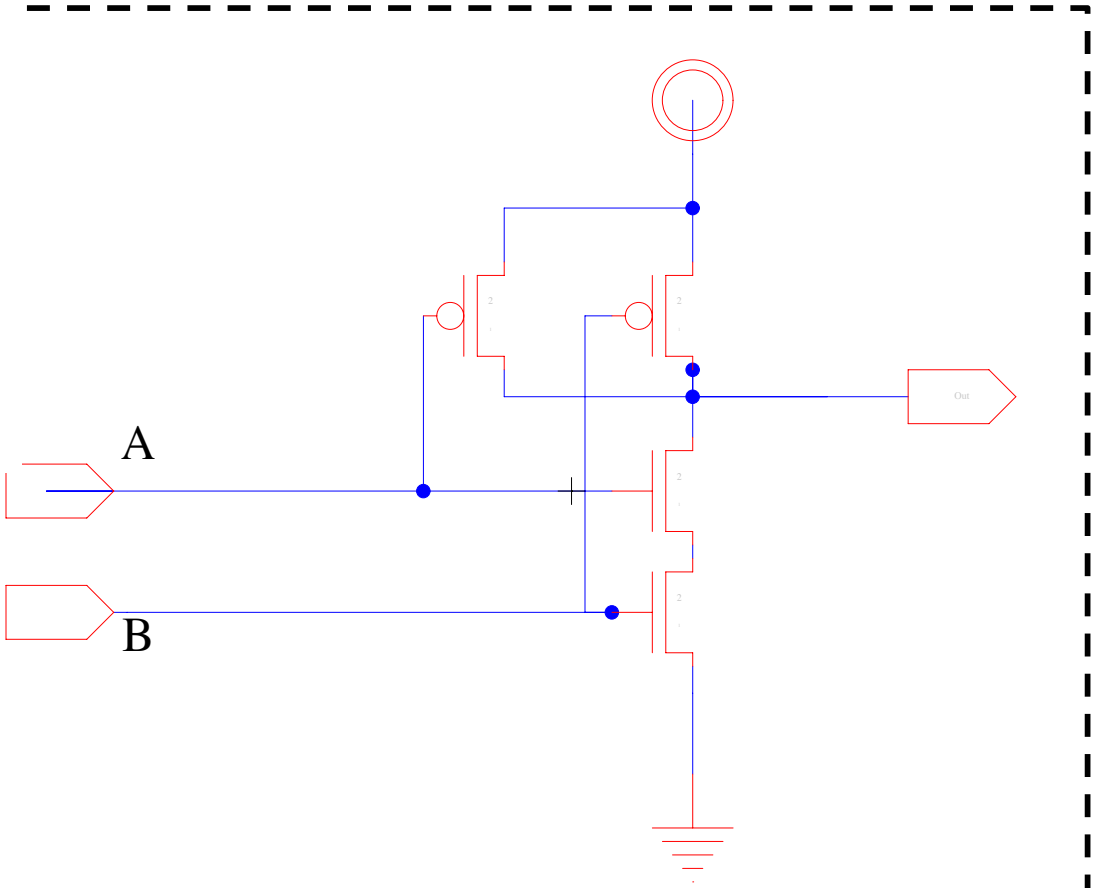
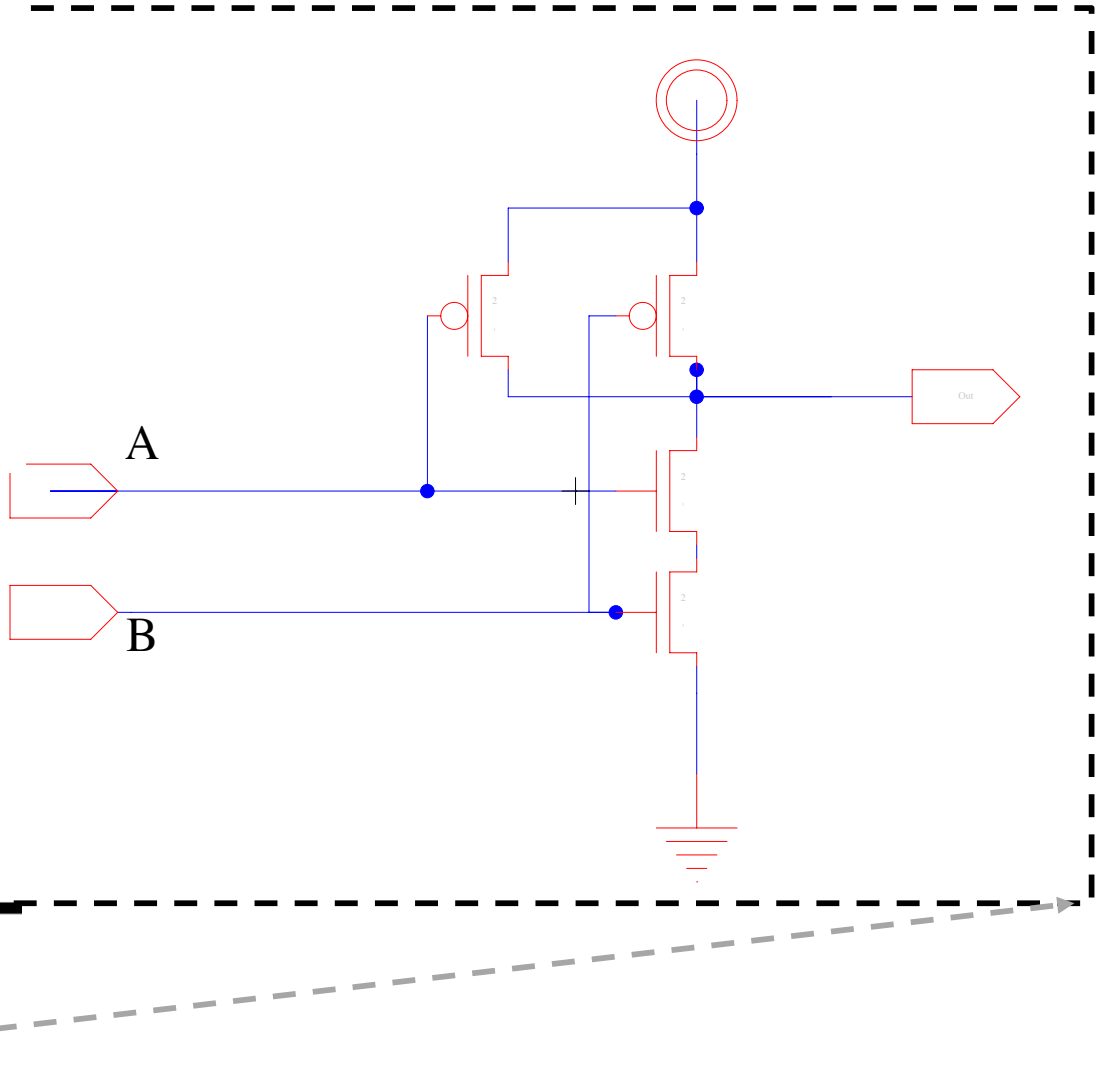


Input	Rout
00	
01	
10	
11	

Rise/Fall Times

- Rise and Fall time may differ
  - Why?
  - What is worst case?
  - What is best case?

Input	Rout
00	
01	
10	
11	



Lumped Resistive Source

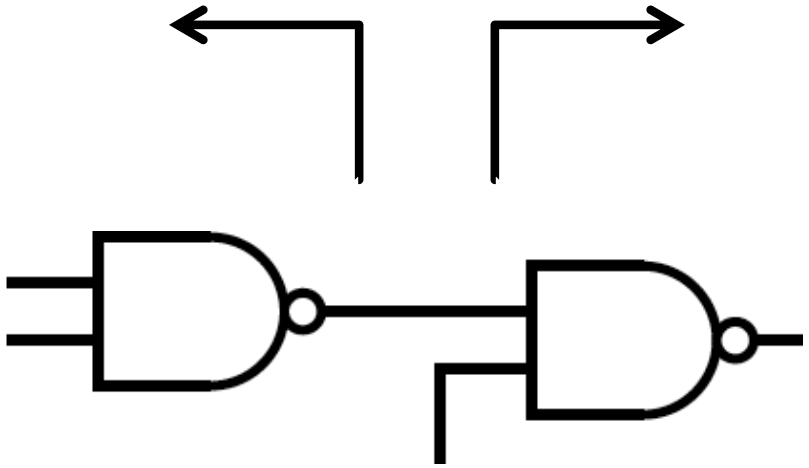
$$R_{drive} = R_{tr,net} + \sum_{i \in wires} R_{w_i}$$

$R_{tr,net}$ = transistor network resistance = parallel and series combination of R_{tr}

Voltage Waveform at Output/Input Node

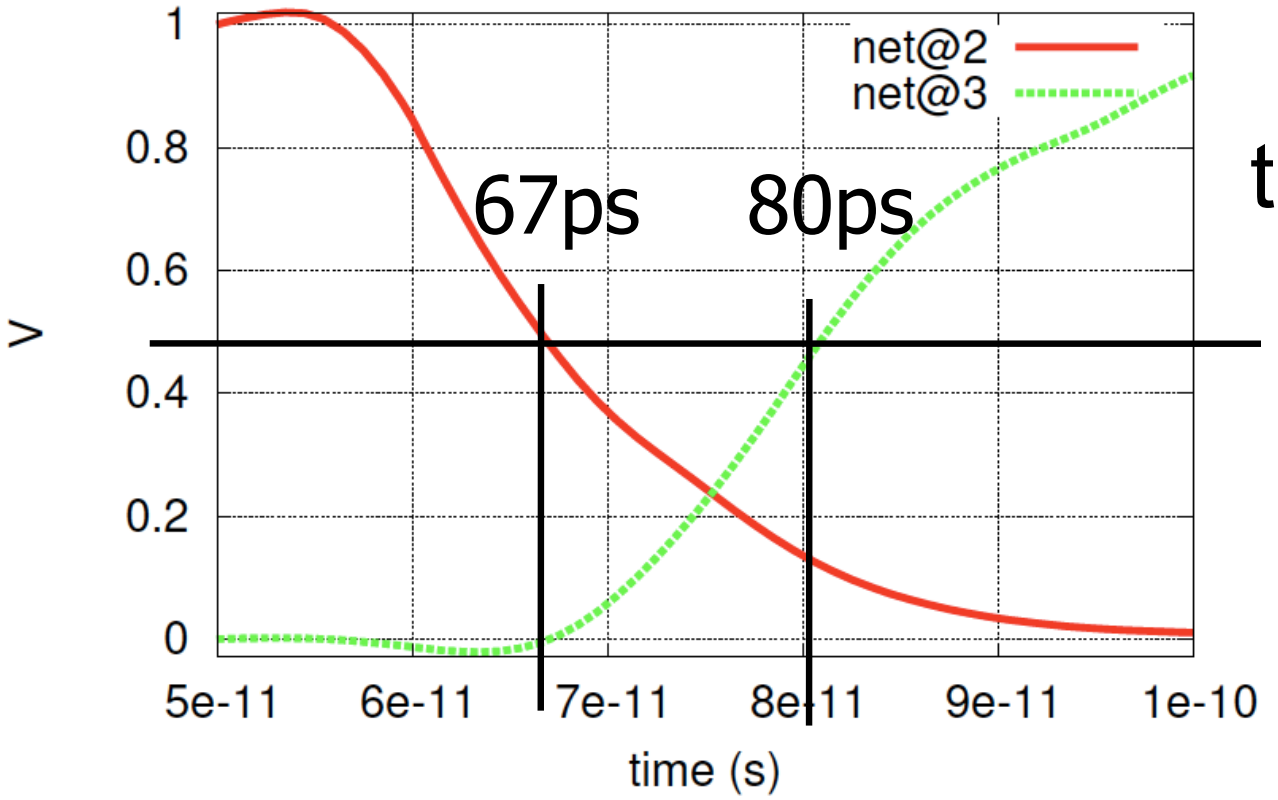
R_{drive} from output stages and wires

C_{Load} from input stages and wires



Measuring Delay

Measuring Gate Propagation Delay



t_{plh} = 13ps

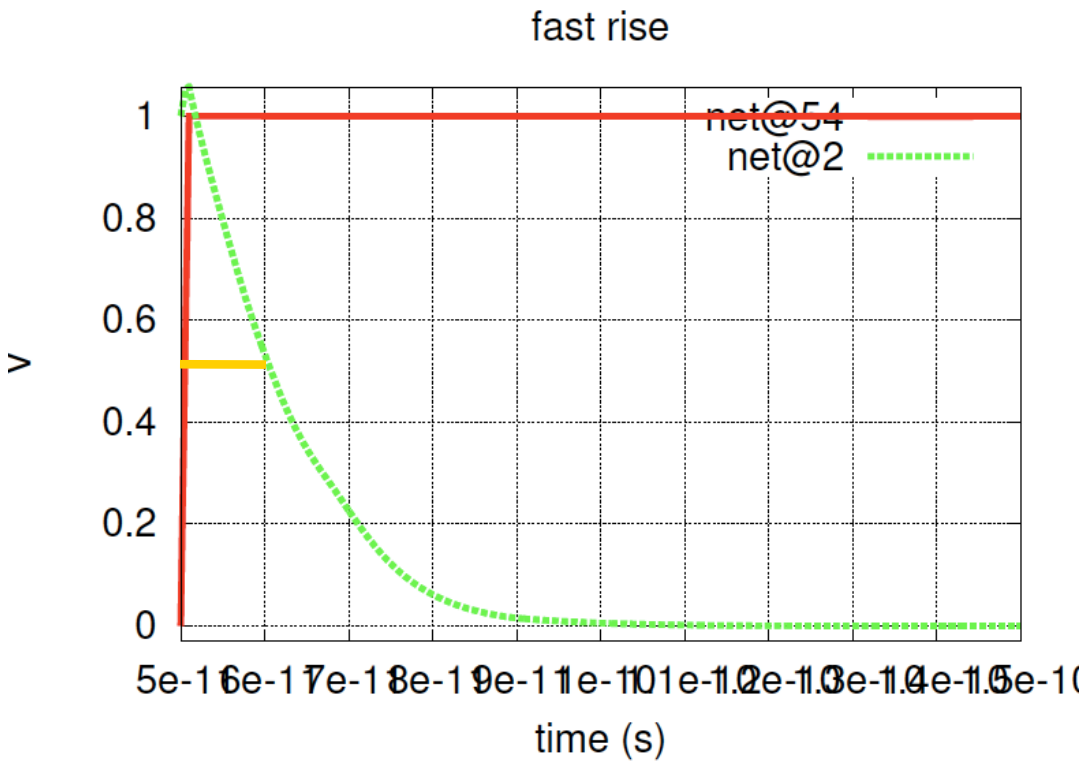
- Next stage starts to switch before first finishes
- Measure from 50% of input swing to 50% of output swing

Characterizing Gate/Technology

- Delay measure of a logic gate will be
  - Function of load on logic gate
  - Function of input signal rise time
    - Which, in turn, may be a function of input loading from the driving logic gate

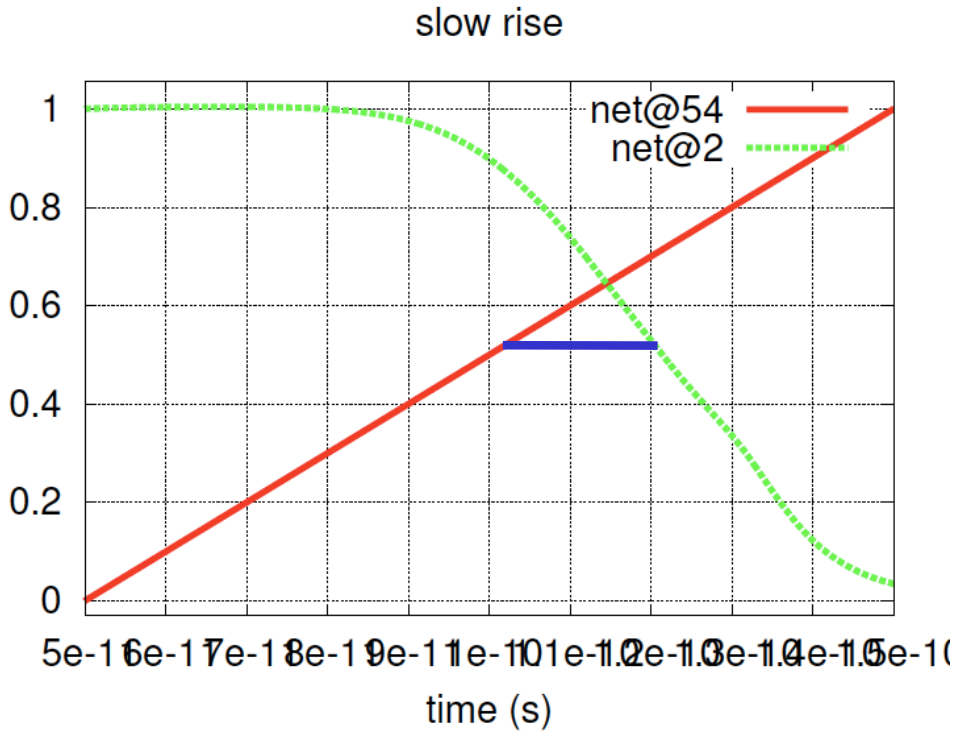
Delay vs. Risetime

1ps input rise



10ps delay

100ps input rise



20ps delay

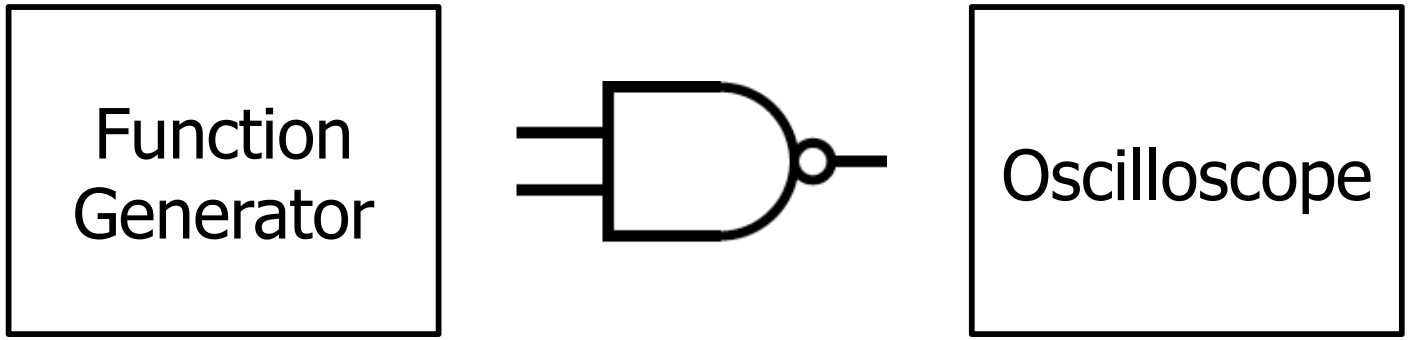
- If we didn't know the input rise time, we wouldn't know what a 13ps delay meant

Characterizing Gate/Technology

- Delay measure will be
  - Function of load on gate
  - Function of input signal rise time
    - Which, in turn, may be a function of input loading
- Want to understand typical delay times
  - Allows us to compare designs with a (somewhat) normalized delay metric

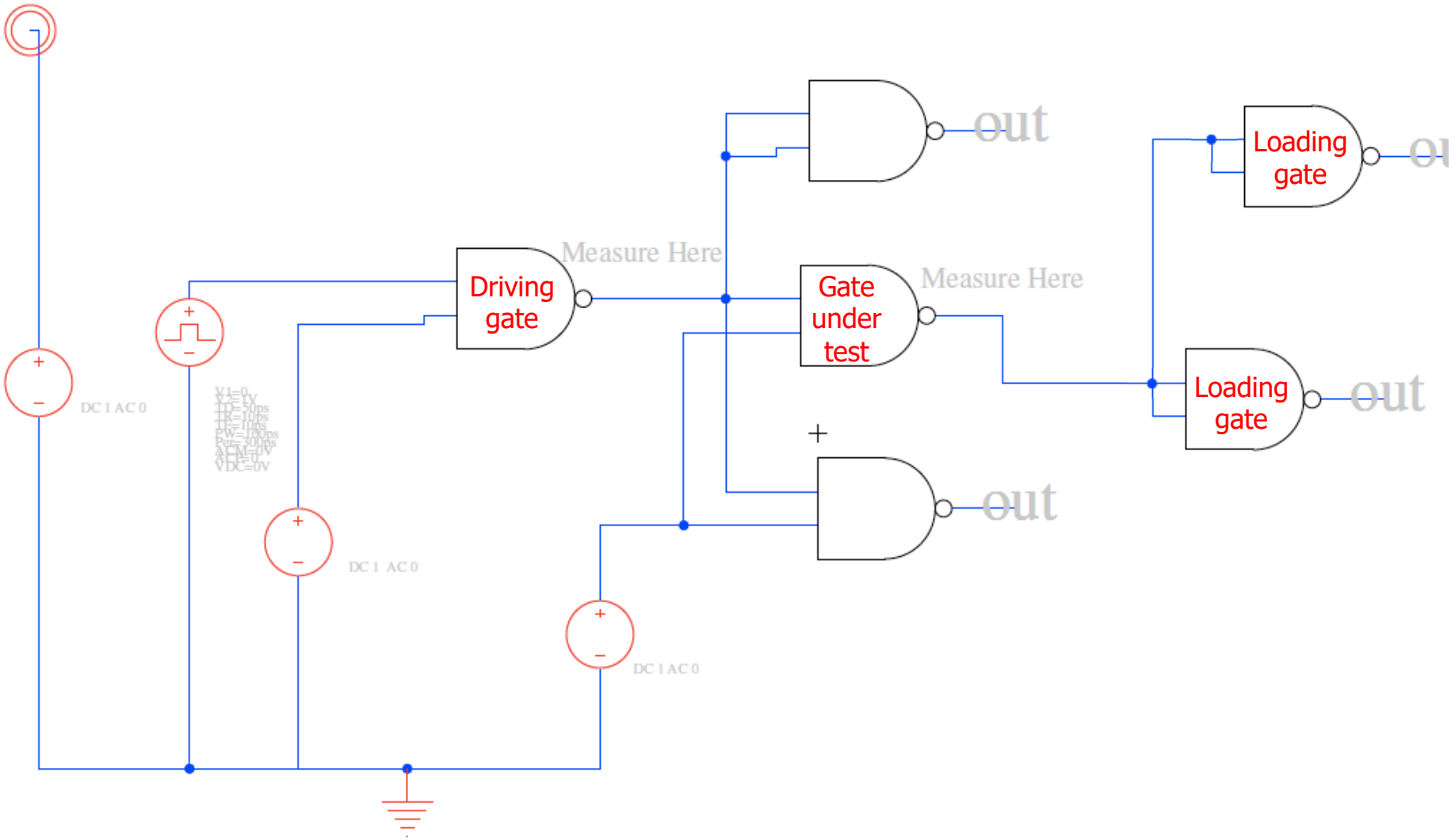
Standard Measurement for Characterization

- Drive with a gate
  - **Not** an ideal source
  - Input rise time typically would see in circuit
- Measure loaded gate
  - Typical loading – FO4



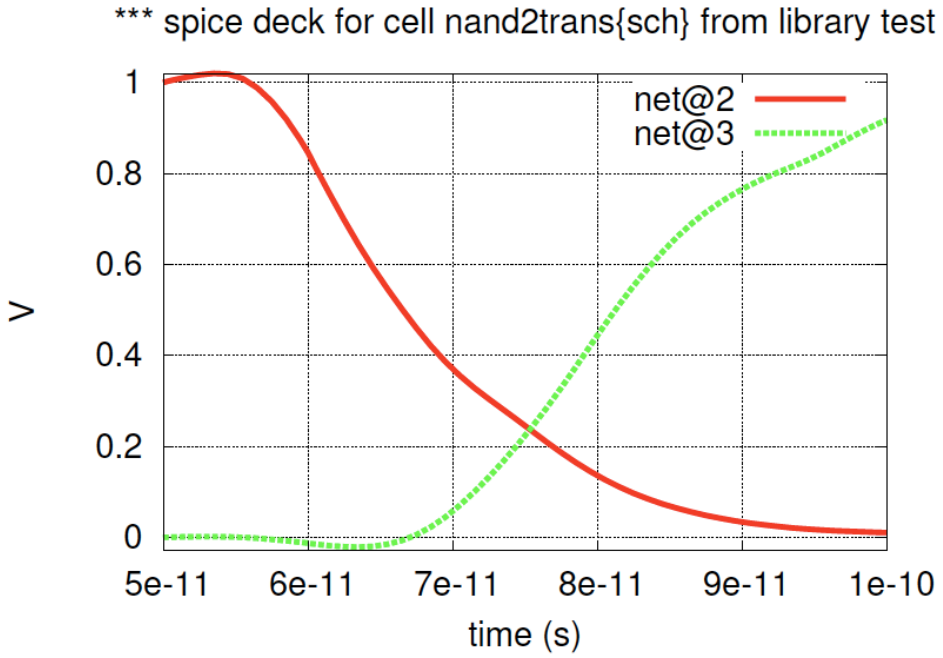
Not realistic measurement

HW2 Measurement Setup



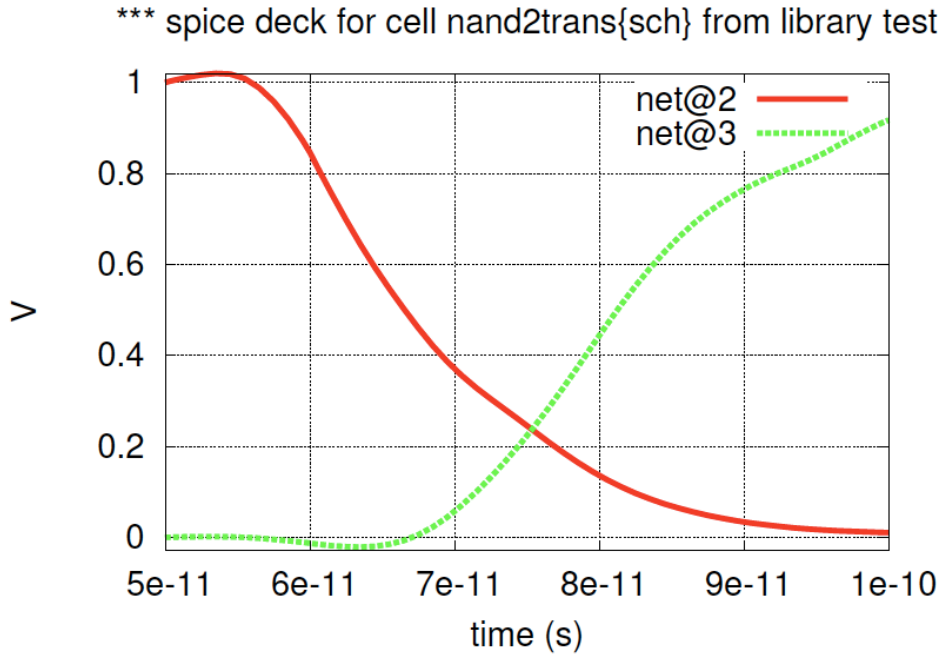
Measurement for Characterization

- Drive with a gate
  - **Not** an ideal source (how does delay change if drive is ideal?)
  - Input rise time typically would see in circuit
- Measure loaded gate
  - Typical loading – FO4

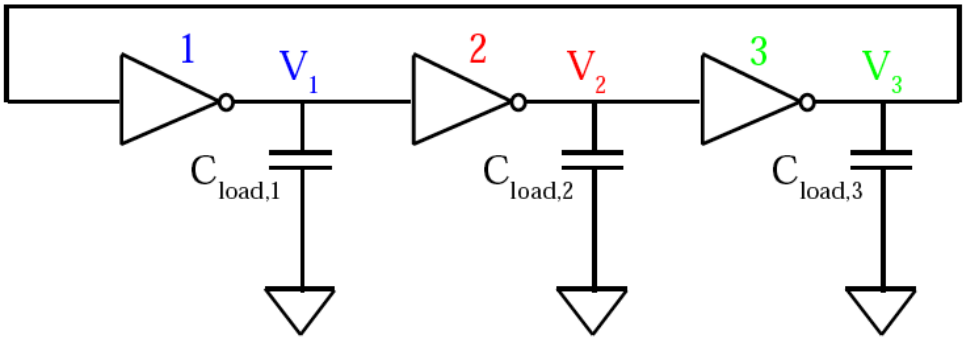


Measurement for Characterization

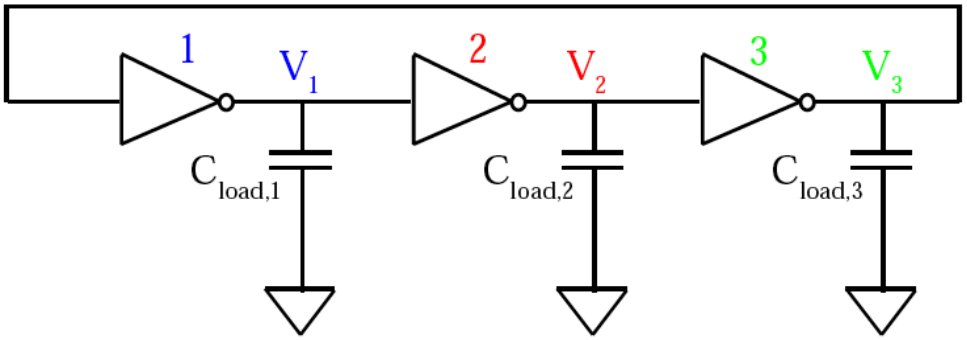
- Drive with a gate
  - **Not** an ideal source
  - Input rise time typically would see in circuit
- Measure loaded gate
  - Typical loading – FO4 (how does delay change if gate is unloaded?)

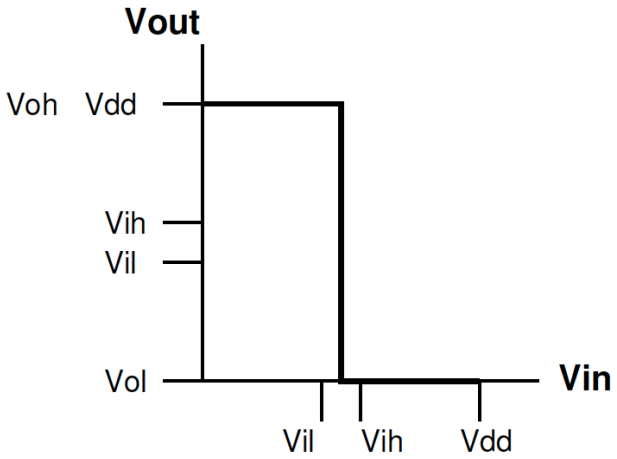


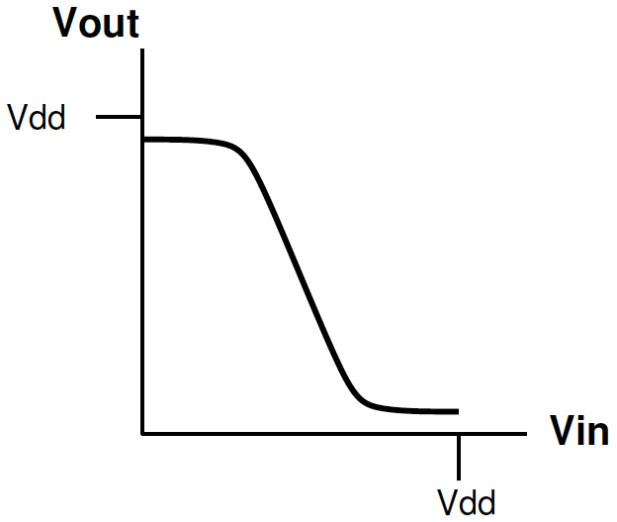
Ring Oscillator (If time)



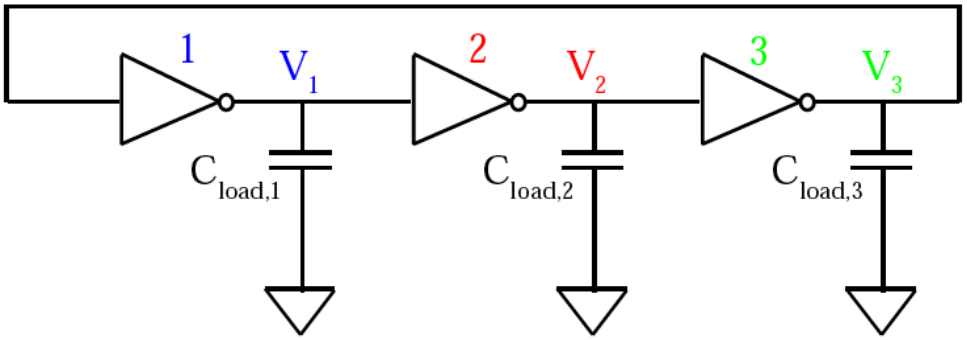
Ring Oscillator (If time)



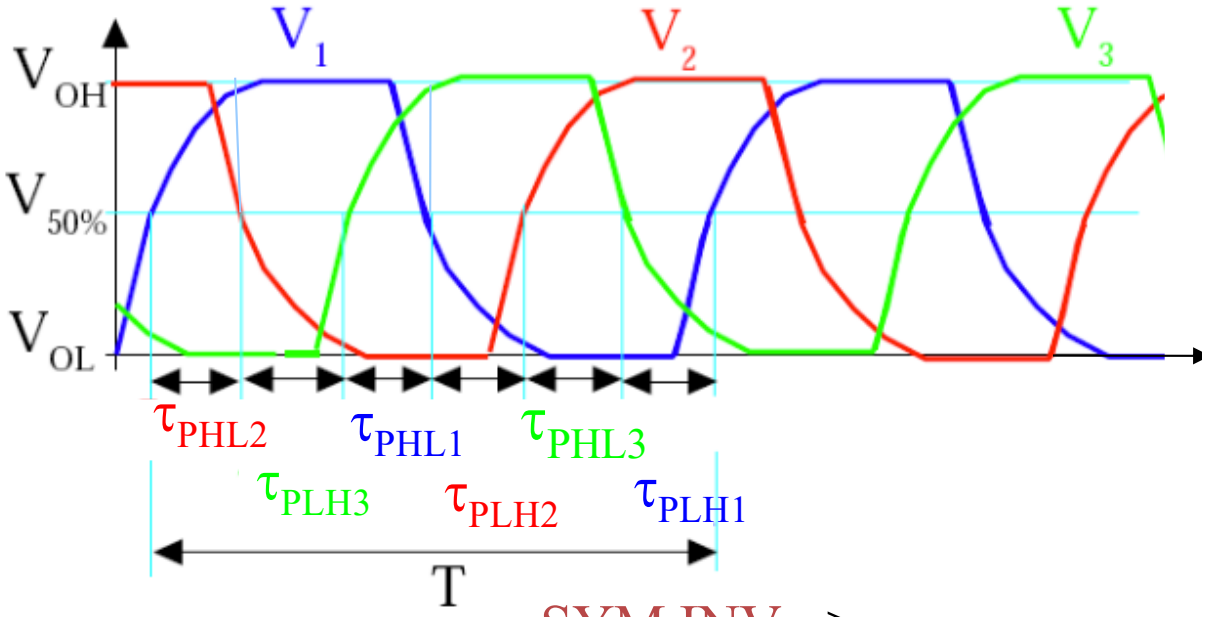


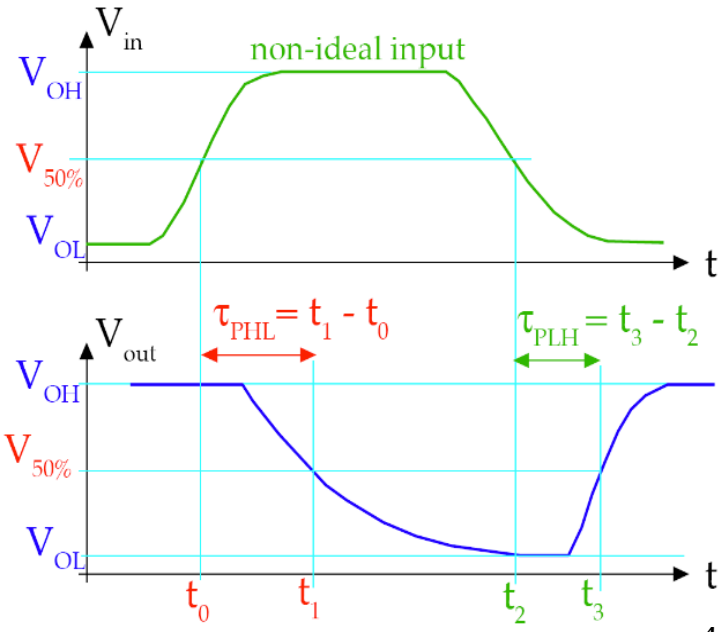


Ring Oscillator (If time)



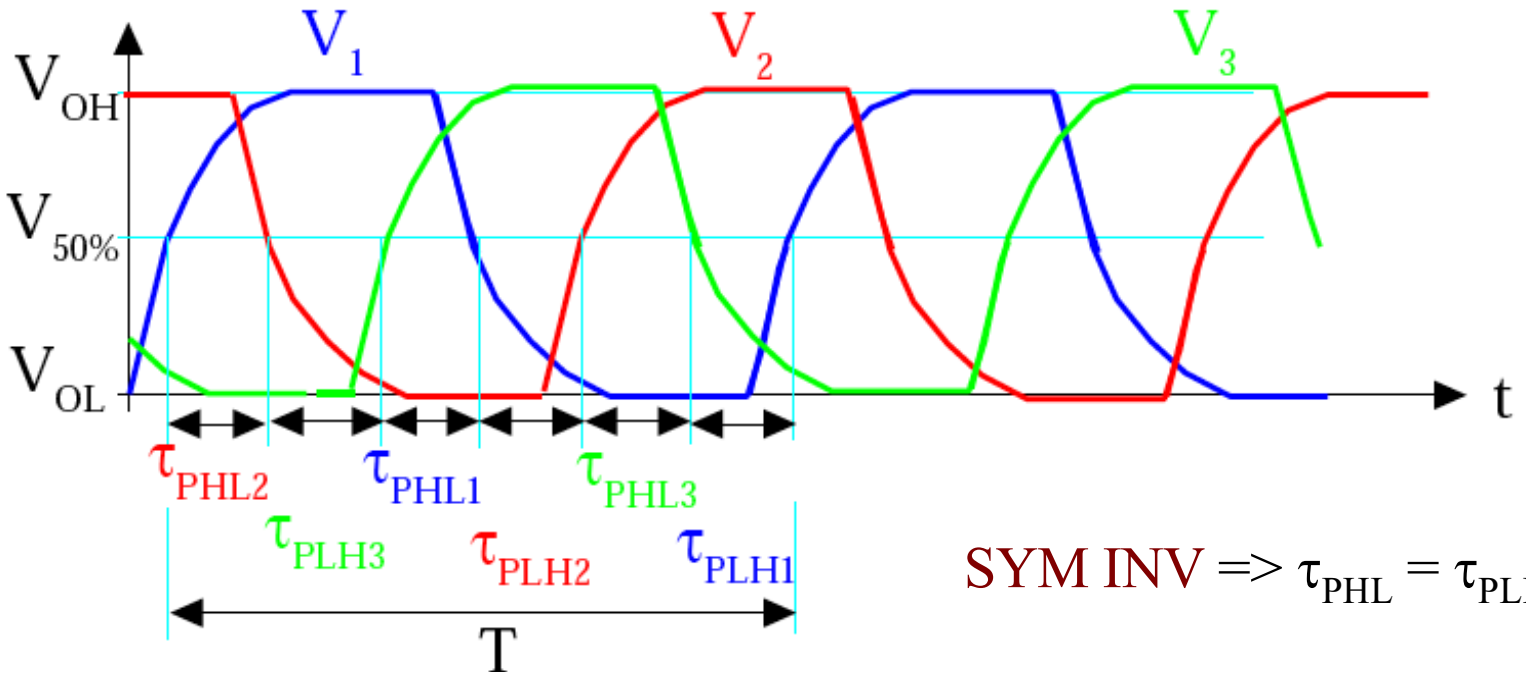
$C_{load,1} = C_{load,2} = C_{load,3}$ and INV1 = INV2 = INV3 = SYM INV





SYM INV => $\tau_{PHL} = \tau_{PLH}$

Ring Oscillator (If time)



SYM INV => $\tau_{PHL} = \tau_{PLH} = \tau_p$

$$T = \tau_{PHL2} + \tau_{PLH3} + \tau_{PHL1} + \tau_{PLH2} + \tau_{PHL3} + \tau_{PLH1} = 6\tau_P$$

$$f = \frac{1}{T} = \frac{1}{6\tau_p} = \frac{1}{2n\tau_p} \rightarrow \tau_p = \frac{1}{2nf}$$

Admin

- HW 2 due 9/20
  - If you haven't started, start now!
  - Office hours on every weekday
- Setup Spice Work Flow
    - access to electric, setup for spice, run ngspice
      - See tool guides on website
      - https://www.seas.upenn.edu/~ese370/#tools
    - read spice style guide on webpage:
      - https://www.seas.upenn.edu/~ese370/fall2021/handouts/spice_style_guide.pdf