ESE370: Circuit-Level Modeling, Design, and Optimization for Digital Systems

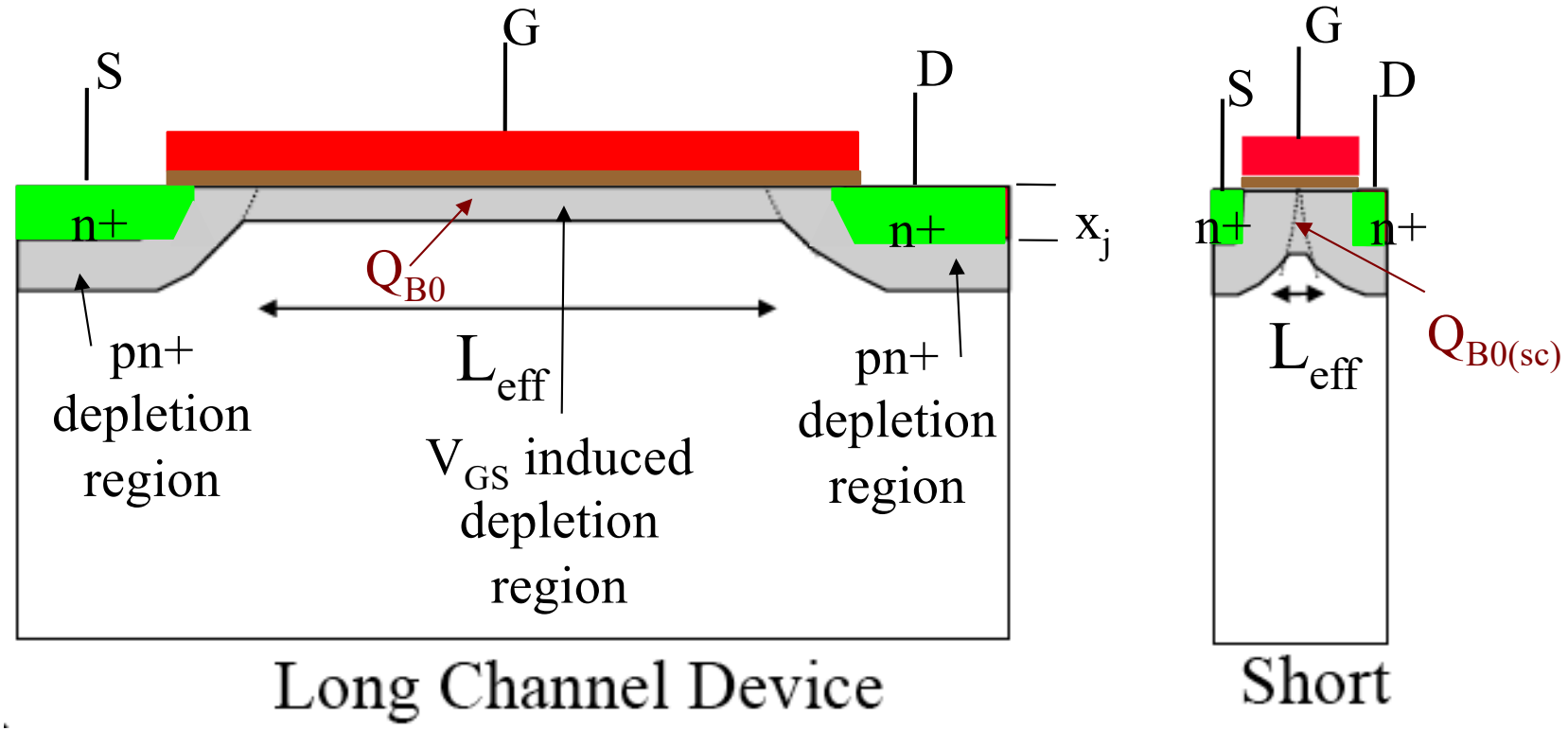
Lec 9: September 24, 2021

MOS Transistor Details

Capacitance

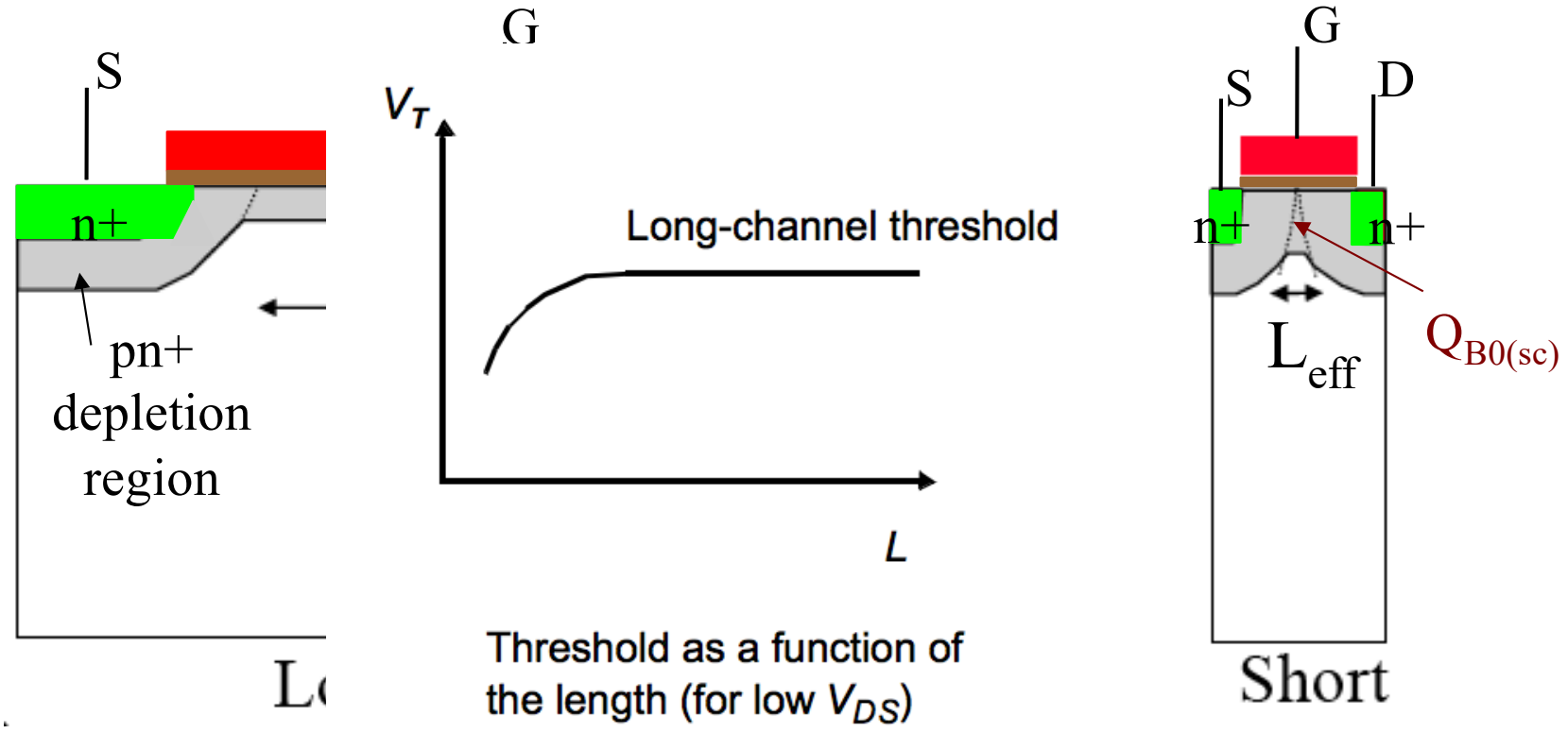
Threshold

Short Channel Effects – V_T Reduction



V_{T0} (short channel) = V_{T0} - ΔV_{T0}

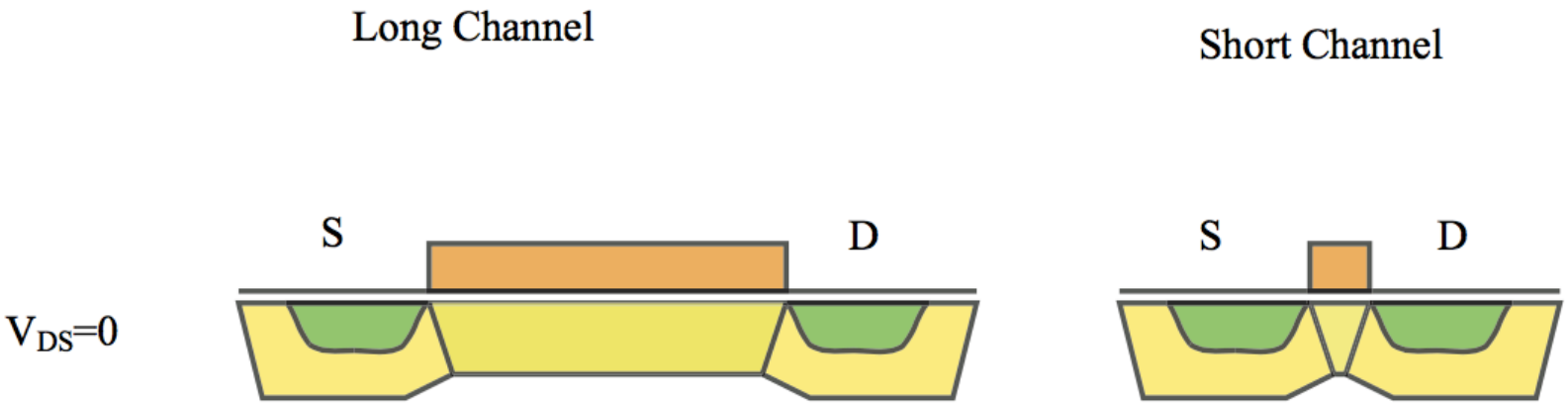
Short Channel Effects – V_T Reduction



V_{T0} (short channel) = V_{T0} - ΔV_{T0}

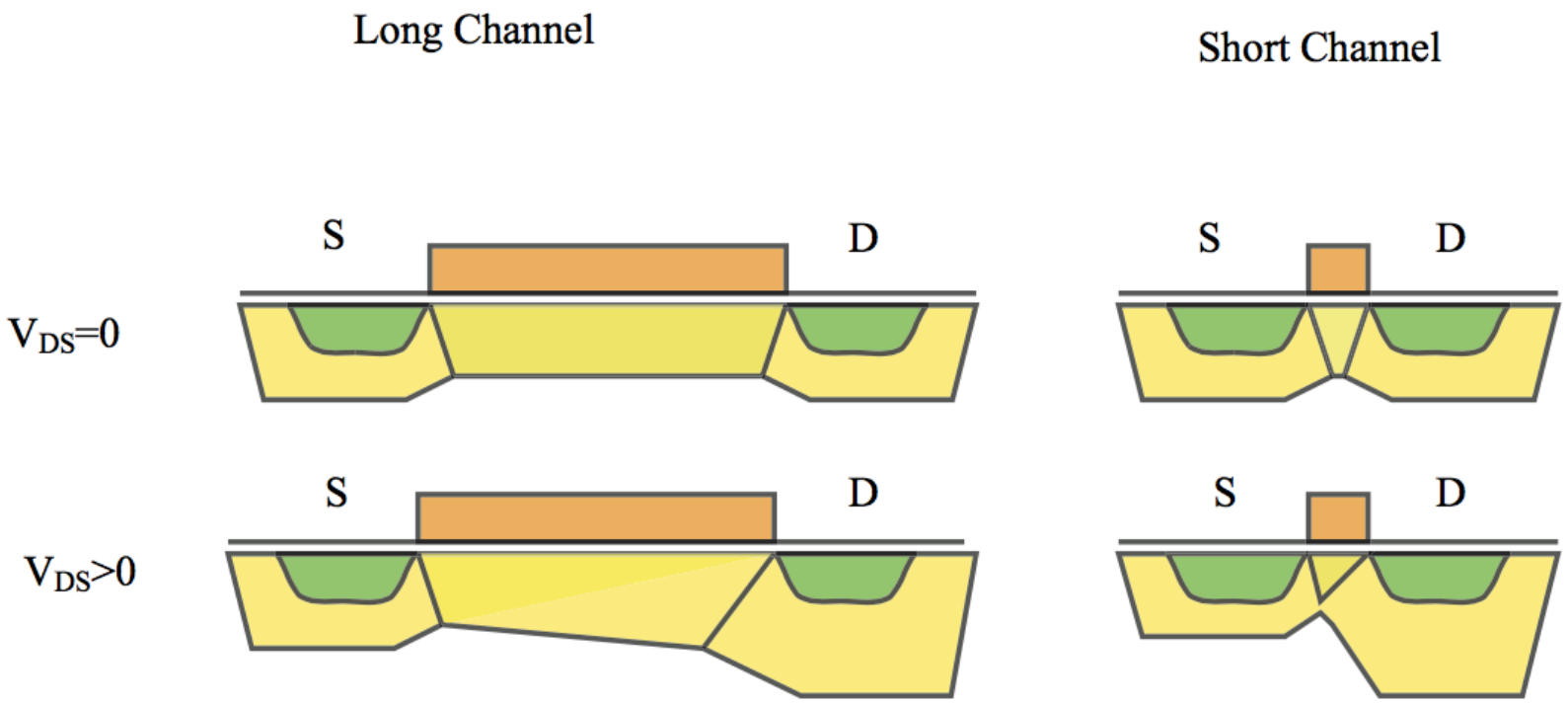
Short Channel Effects - DIBL

- Drain Induced Barrier Lowering
  - V_T Reduction with Drain Bias



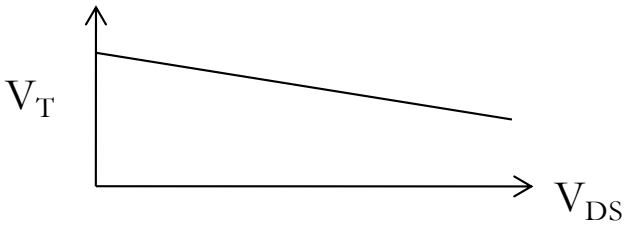
Short Channel Effects - DIBL

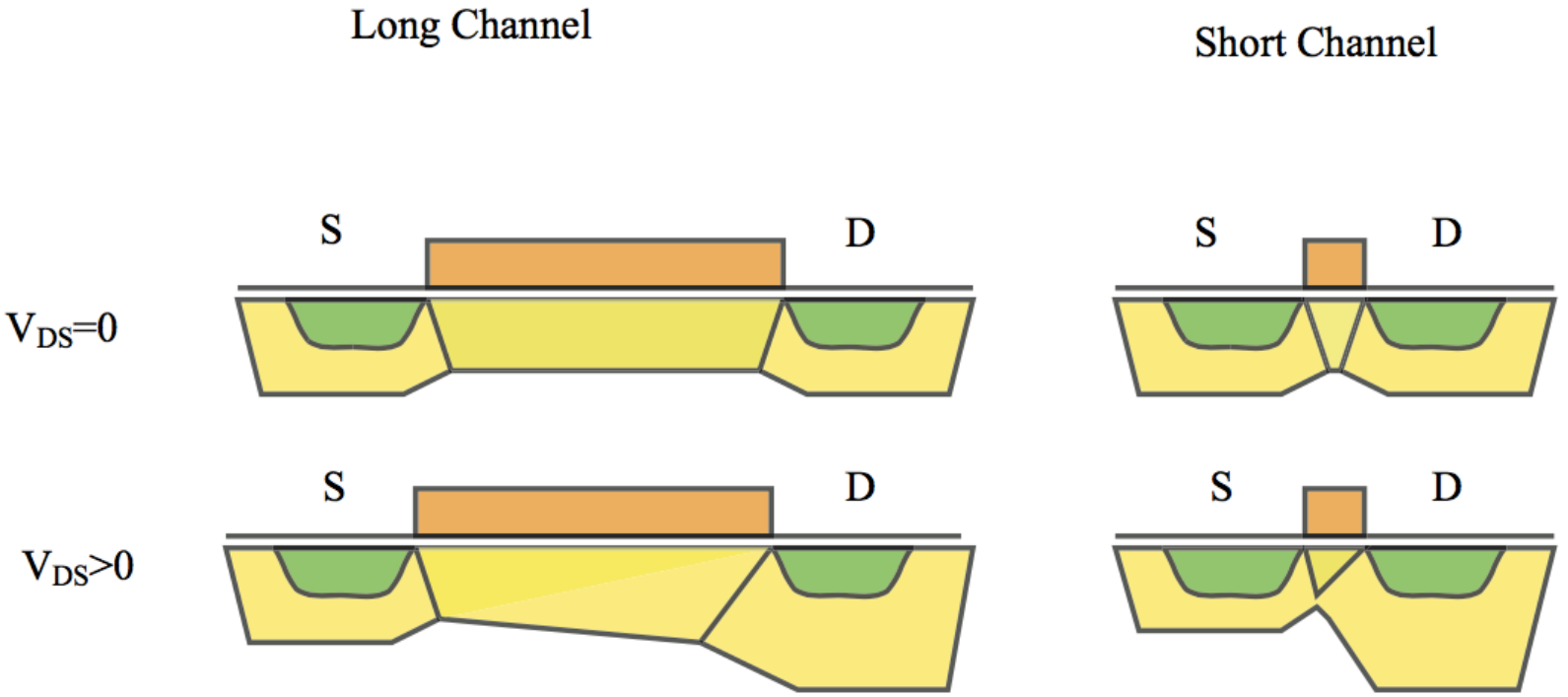
- Drain Induced Barrier Lowering
  - V_T Reduction with Drain Bias



Short Channel Effects - DIBL

- Drain Induced Barrier Lowering
  - V_T Reduction with Drain Bias

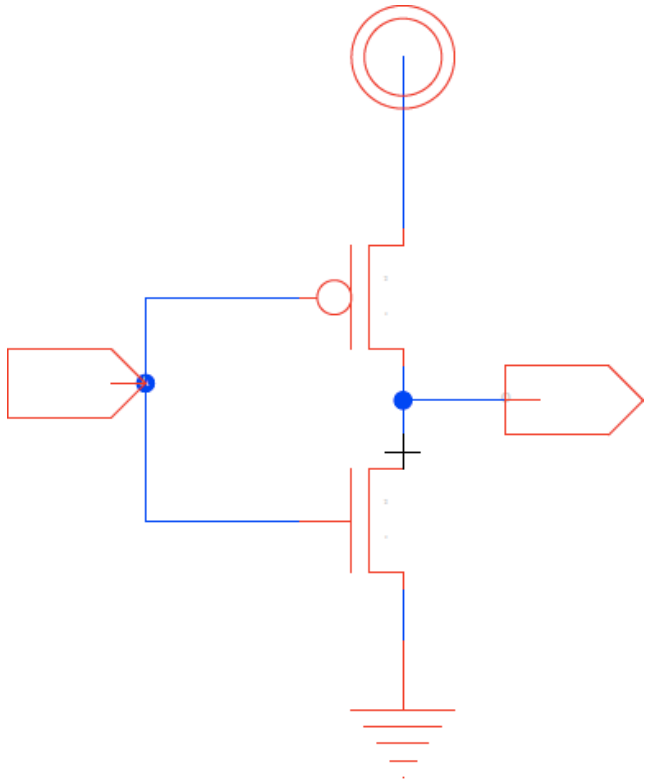




Threshold Reduction Impact

In a Gate?

- What does it impact most?
  - Which device, has large V_{ds}?
  - How does this effect operation?
    - Speed of switching?
    - Leakage?



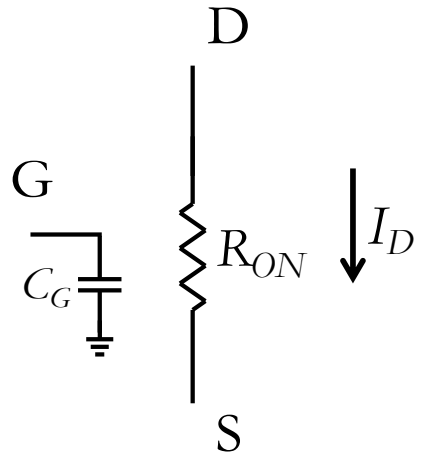
Simplified Design Flow

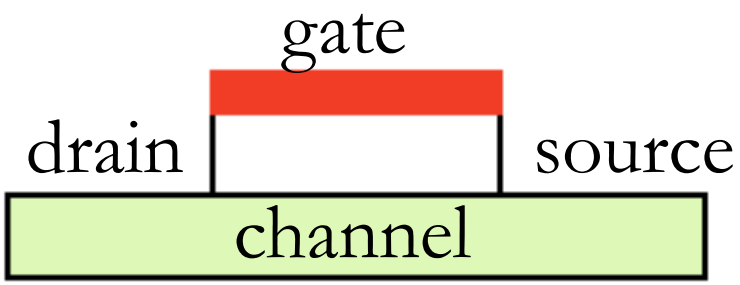
- Design a circuit to perform a function with specified minimum speed and optimized power (minimized with an upper bound)
  - Zero order model to design topology
  - First order model to meet speed spec
    - Rise/fall times, propagation delay, gate capacitance, output stage equivalent resistance
  - Transistor IV curves
    - Iterative SPICE simulation – tweak knobs to optimize for power (switching (dynamic), leakage (static), etc.)

today

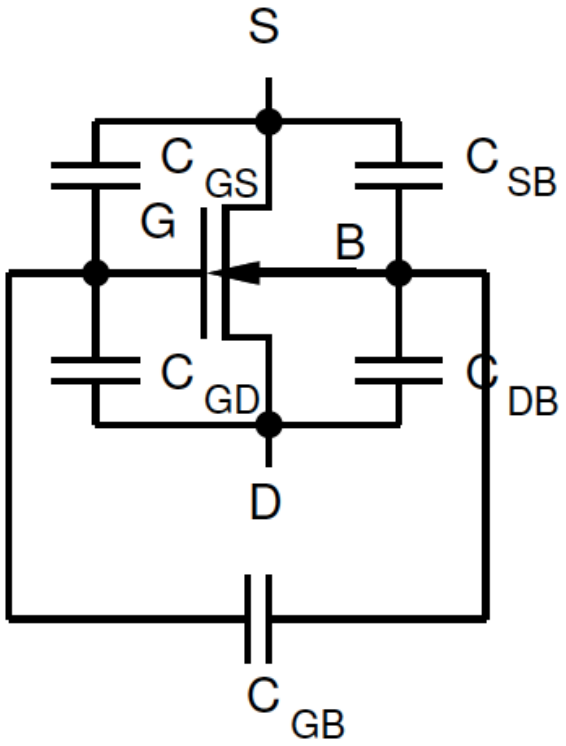
Capacitance

- First order: gate input looks like a capacitor





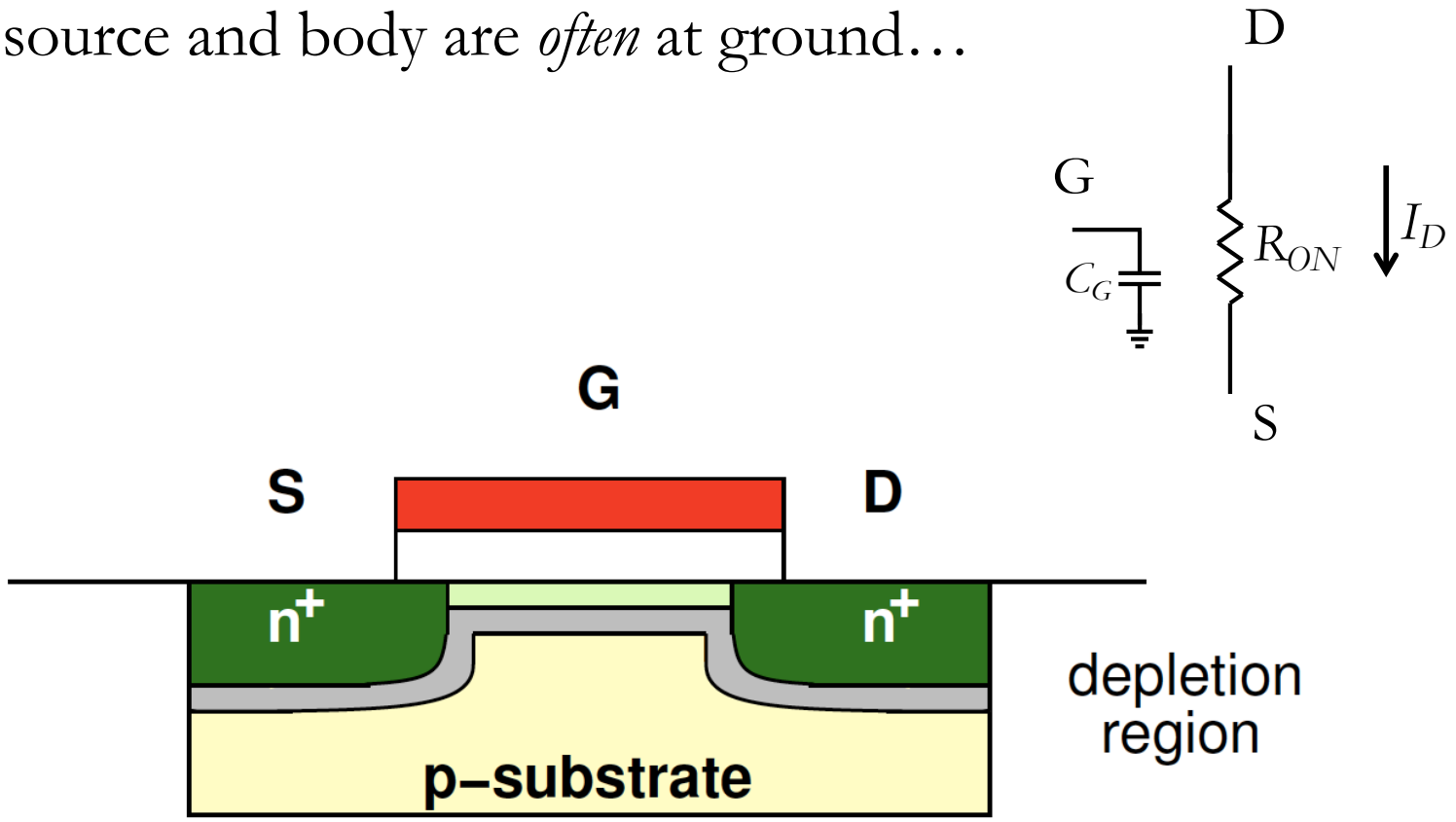
- Today:
  - Capacitance is not constant
  - Capacitance not physically to gnd
    - Modeled as such



Capacitance Setup

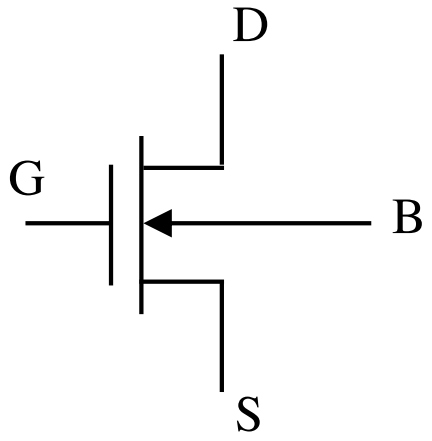
Capacitance

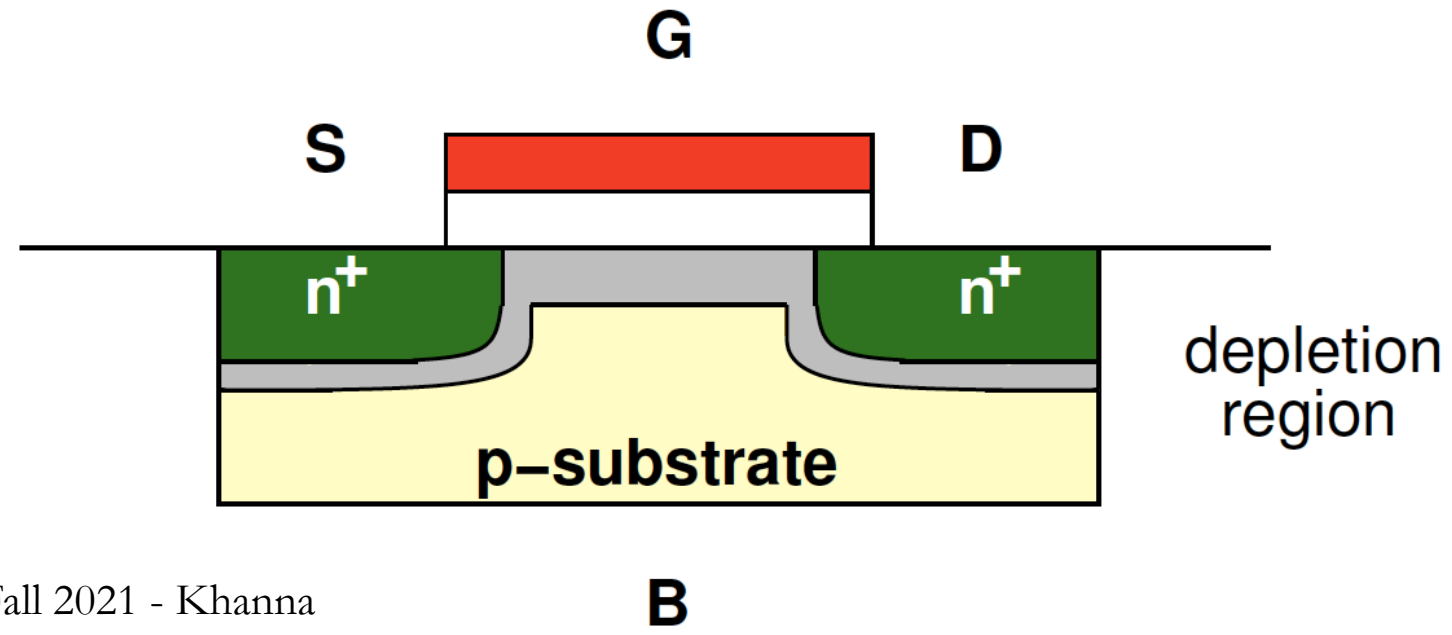
- Modeled gate with a capacitor to ground
- …but ground isn't really one of our terminals
  - Don't connect directly to it
  - …source and body are *often* at ground…



Capacitance (Preclass 1)

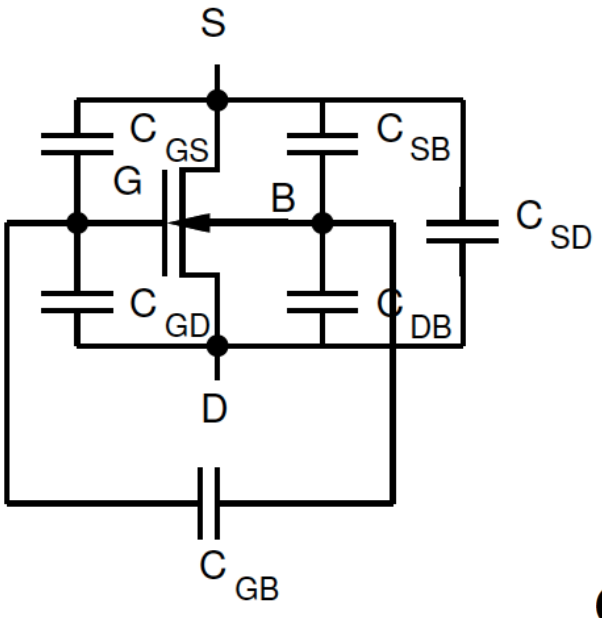
- Four Terminals
- How many combinations?
  - 4 things taken 2 at a time?

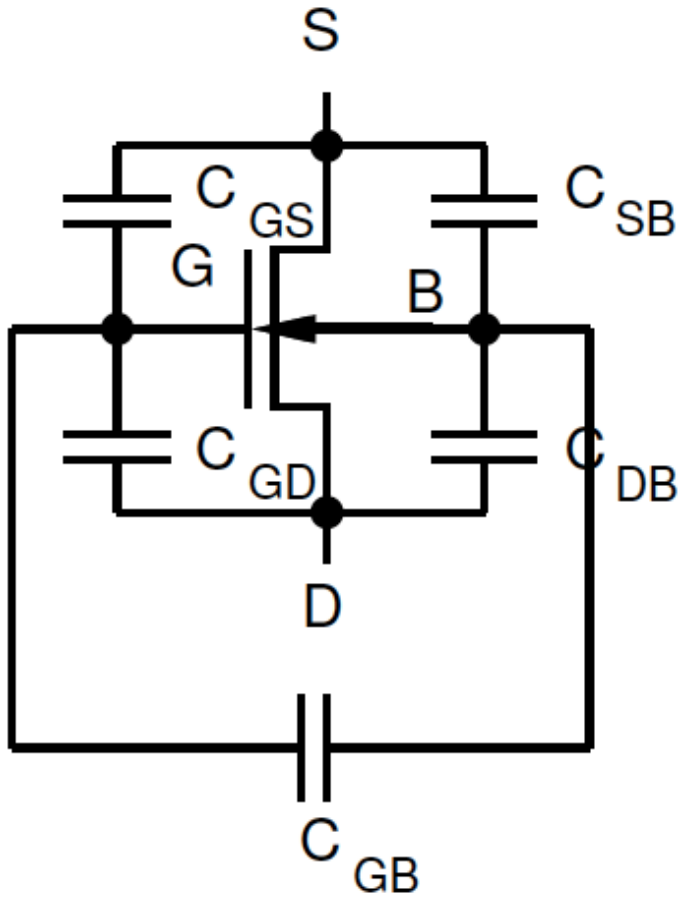


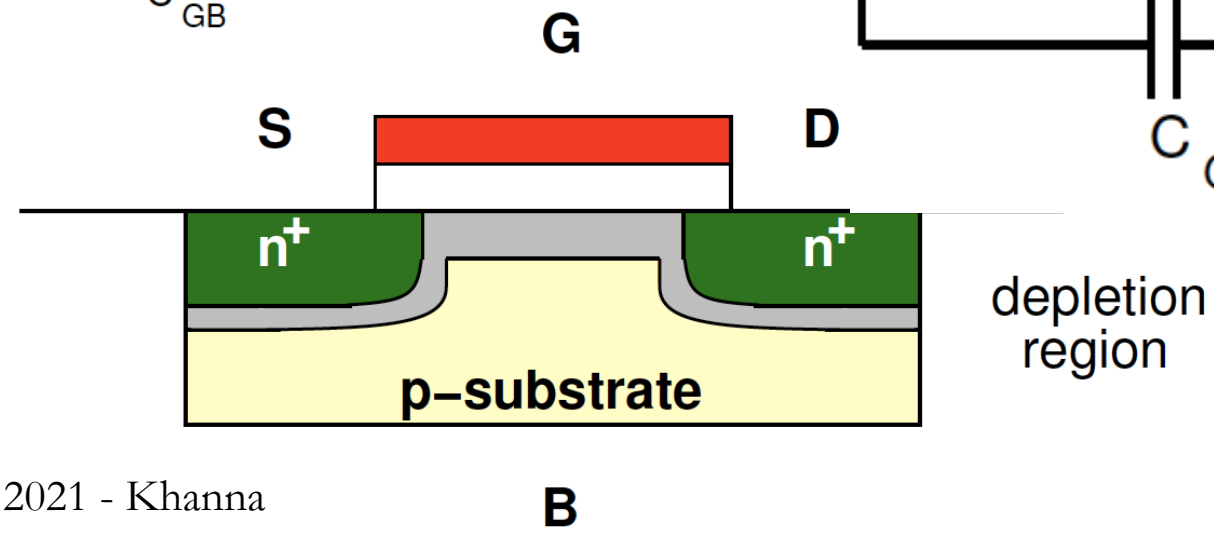


Capacitances

- GS, GB, GD, SB, DB, SD

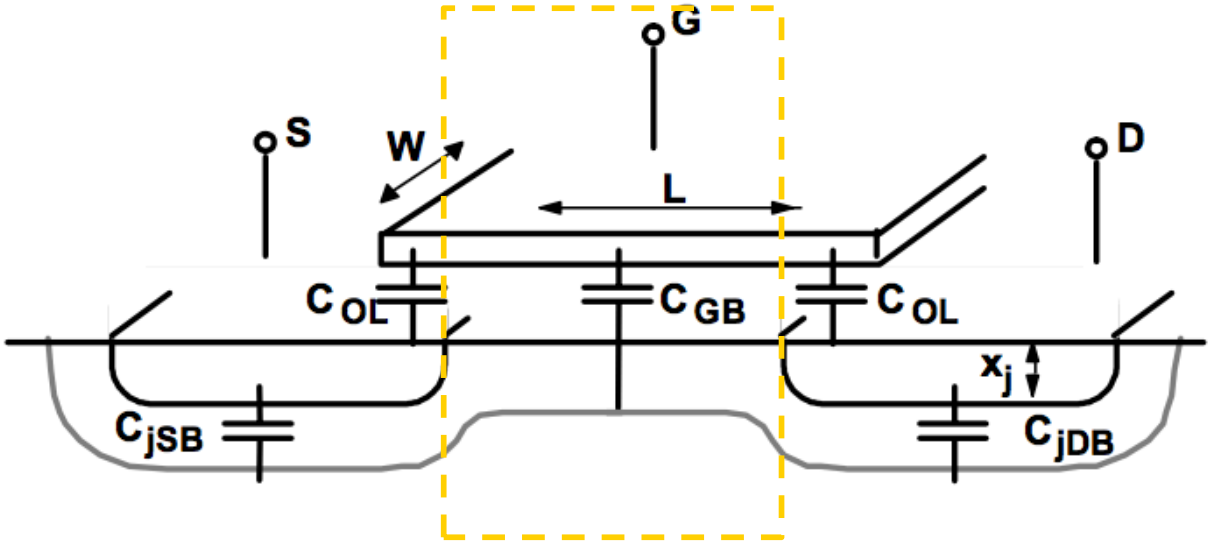






Capacitance Decomposition

MOSFET Parasitic Capacitance

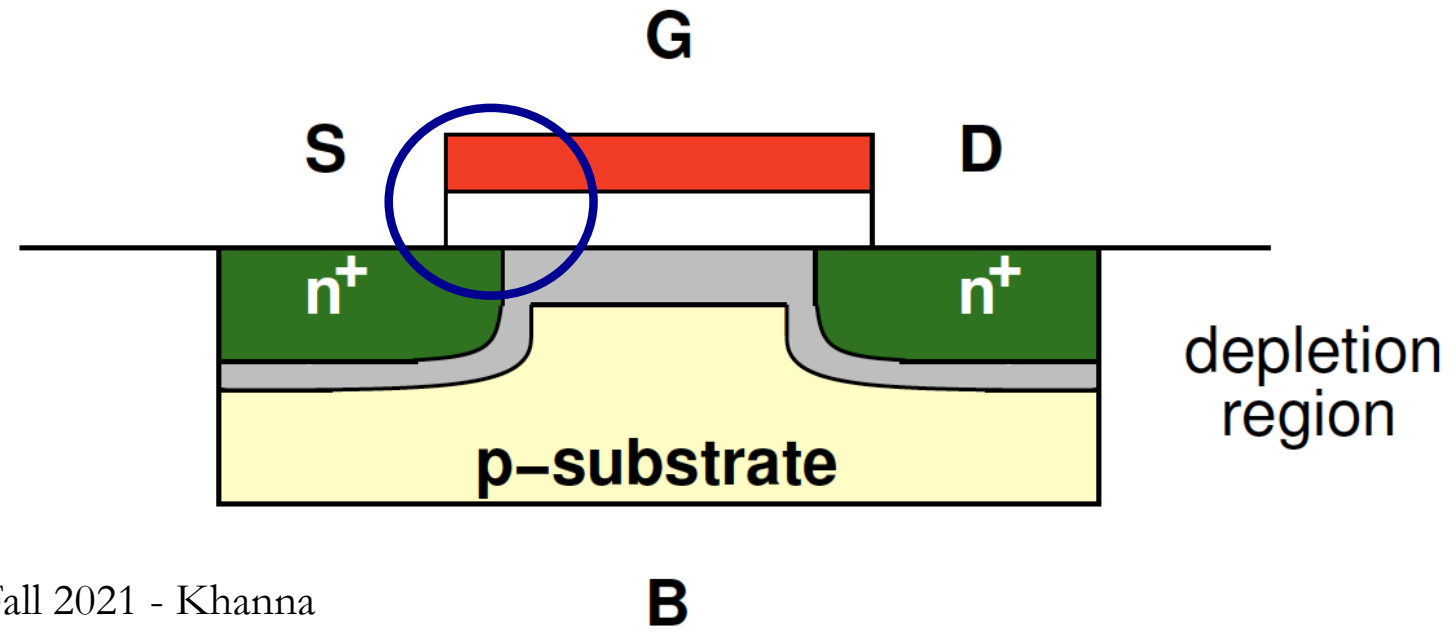


- Any two conductors separated by an insulator form a parallel-plate capacitor
- Two types
  - Extrinsic – Outside the box (e.g. junction, overlap)
  - Intrinsic – Inside the box (e.g. gate-to-channel)

Overlap Capacitance

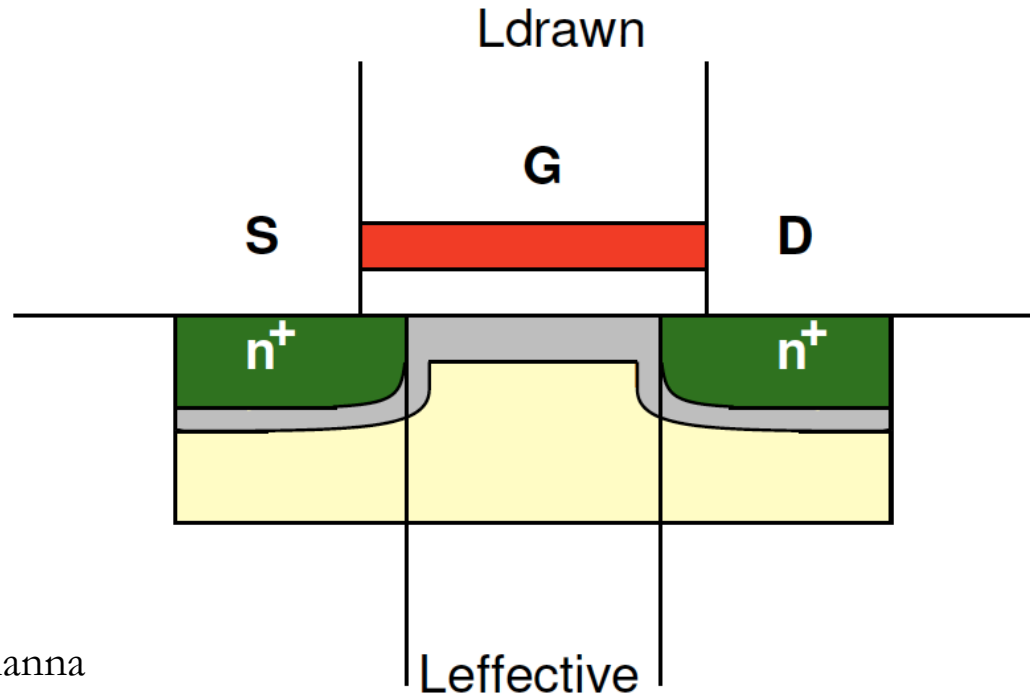
Overlap

- What is the capacitive implication of gate/source and gate/drain overlap?

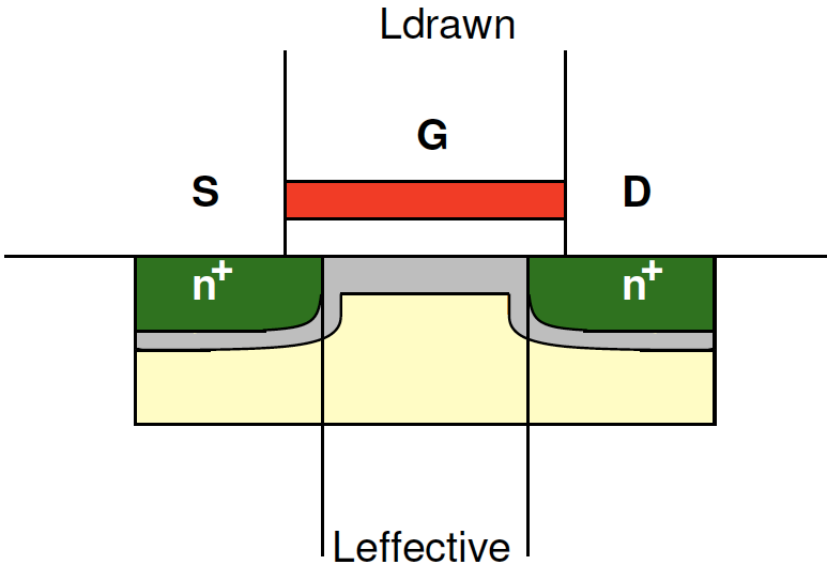


Overlap

- Length of overlap?



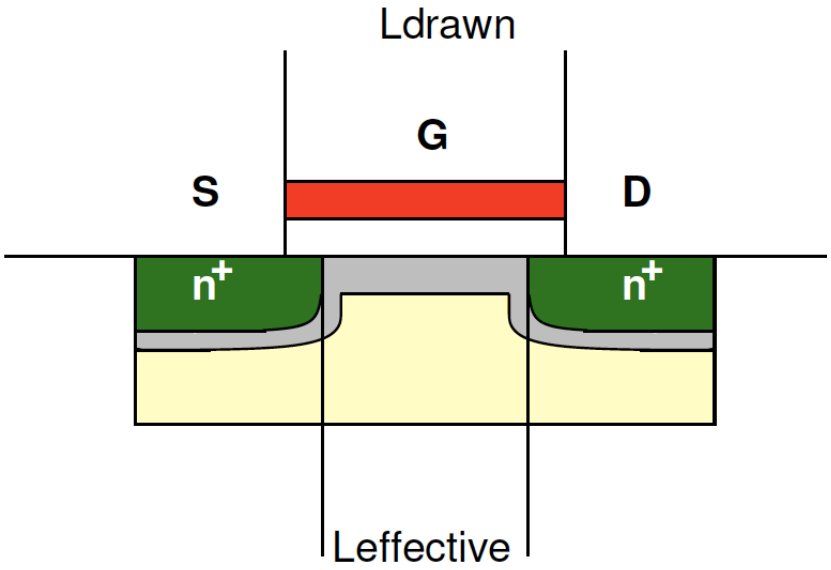
Overlap Capacitance



$$C = \varepsilon_r \varepsilon_0 \frac{A}{d}$$

$$C_o = \varepsilon_{ox} \frac{W\left(L_{drawn} - L_{effective}\right)/2}{t_{ox}}$$

Overlap Capacitance



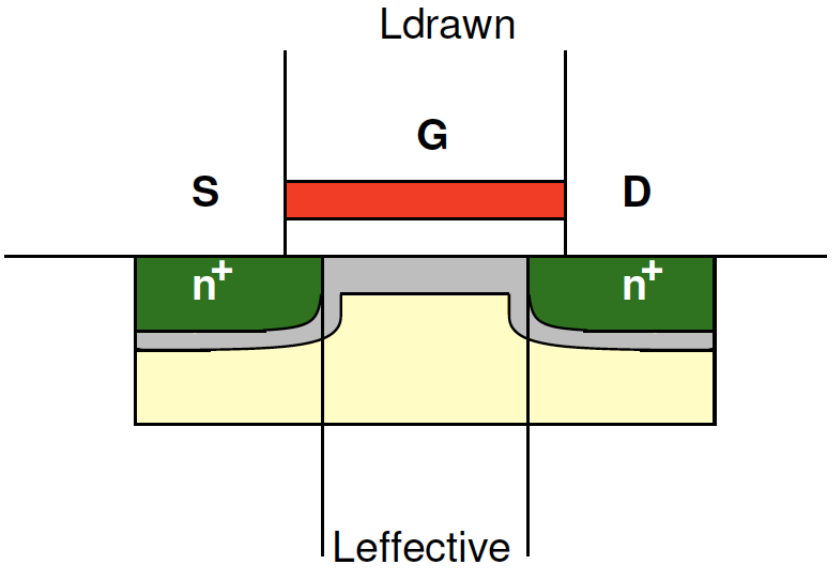
$$C = \varepsilon_r \varepsilon_0 \frac{A}{d}$$

$$C_{OX} = \frac{\varepsilon_{OX}}{t_{OX}}$$

$$C_o = \varepsilon_{ox} \frac{W\left(L_{drawn} - L_{effective}\right)/2}{t_{ox}}$$

$$C_o = \frac{1}{2} C_{ox} W\left(L_{drawn} - L_{effective}\right)$$

Overlap Capacitance



$$C = \varepsilon_r \varepsilon_0 \frac{A}{d}$$

$$C_{OX} = \frac{\varepsilon_{OX}}{t_{OX}}$$

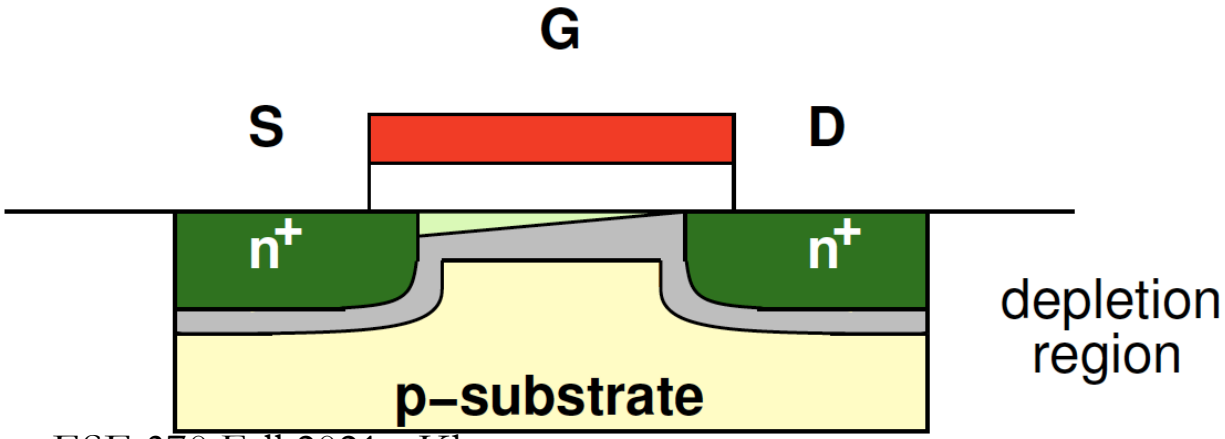
$$C_o = \varepsilon_{ox} \frac{W\left(L_{drawn} - L_{effective}\right)/2}{t_{ox}}$$

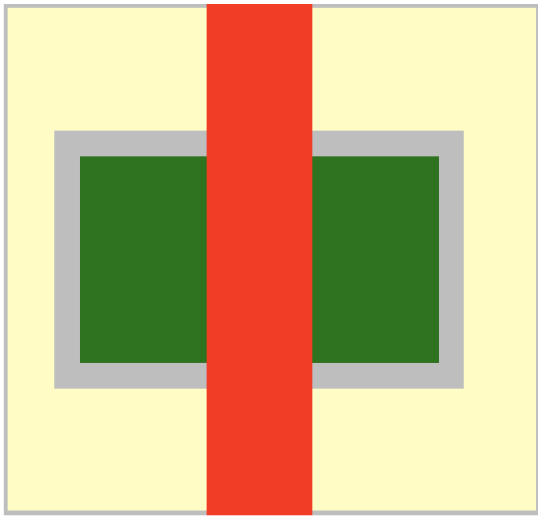
$$C_o = \frac{1}{2} C_{ox} W\left(L_{drawn} - L_{effective}\right) = C_{GSO} = C_{GDO}$$

Junction Capacitances

Junction (diffusion) Capacitance

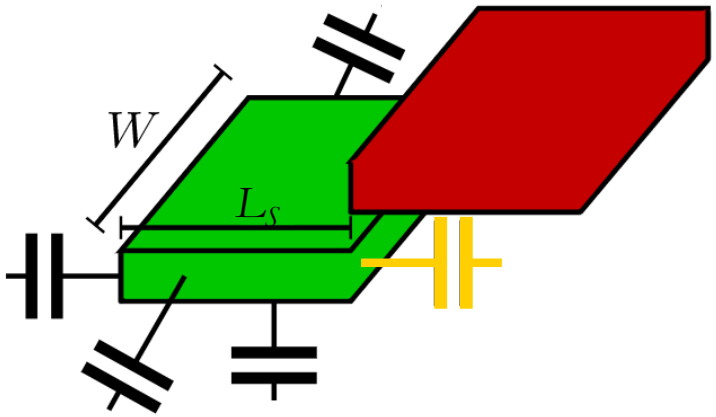
- n^+ contacts are formed by doping = diffusion
- Depletion under diffusion region (bottom-plate)
  - Due to reverse biased PN junction
  - Bottom-plate junction capacitance, C_j
- Depletion around perimeter (sidewall) of diffusion region
  - Sidewall junction capacitance, C_{jsw}

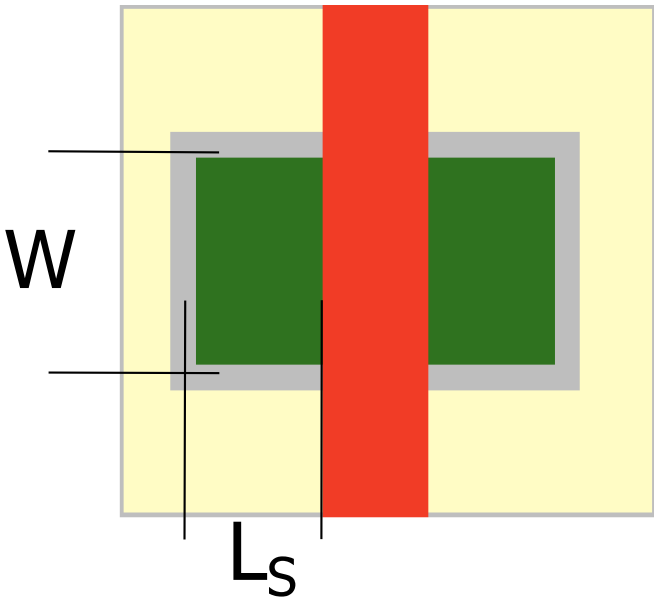




Junction (Diffusion) Capacitance

- C_j – Bottom-plate junction capacitance (F/Area)
- C_{jsw} – Sidewall junction capacitance (F/Length)
- L_S – length of diffusion region

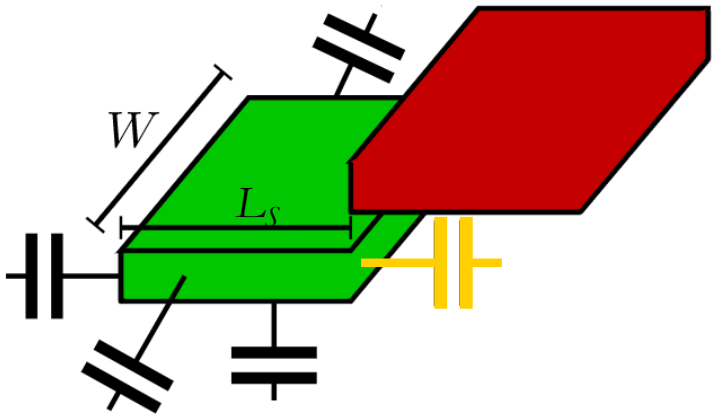


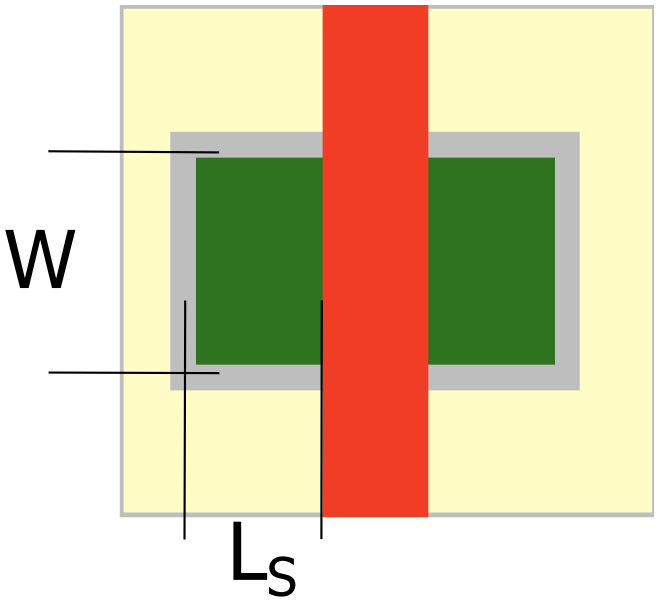


$$C_{diff} = C_j L_S W +$$

Junction (Diffusion) Capacitance

- C_j – Bottom-plate junction capacitance (F/Area)
- C_{jsw} – Sidewall junction capacitance (F/Length)
- L_S – length of diffusion region

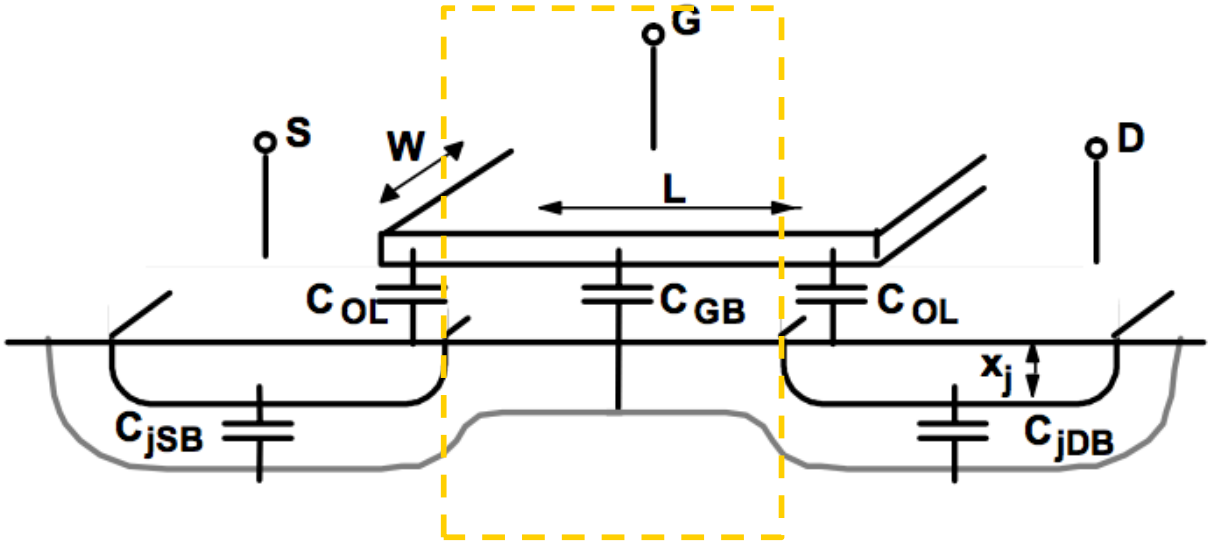




$$C_{diff} = C_j L_S W + C_{jsw}\left(2L_S + W\right)$$

Gate-to-channel

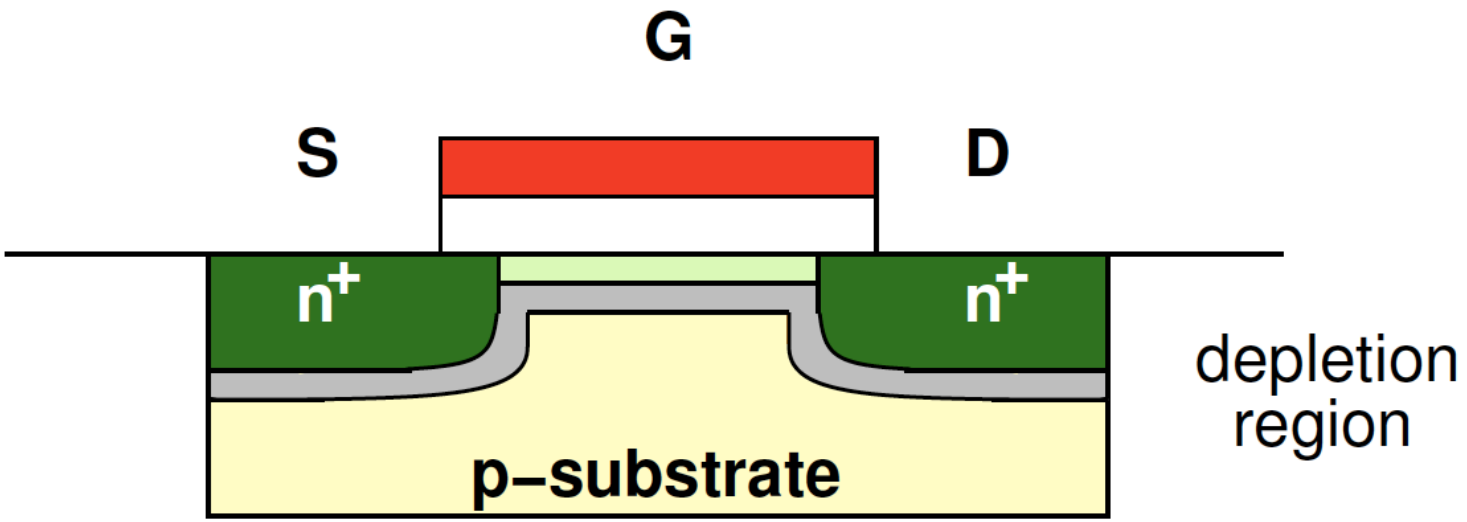
MOSFET Parasitic Capacitance



- Any two conductors separated by an insulator form a parallel-plate capacitor
- Two types
  - Extrinsic – Outside the box (e.g. junction, overlap)
  - Intrinsic – Inside the box (e.g. gate-to-channel)

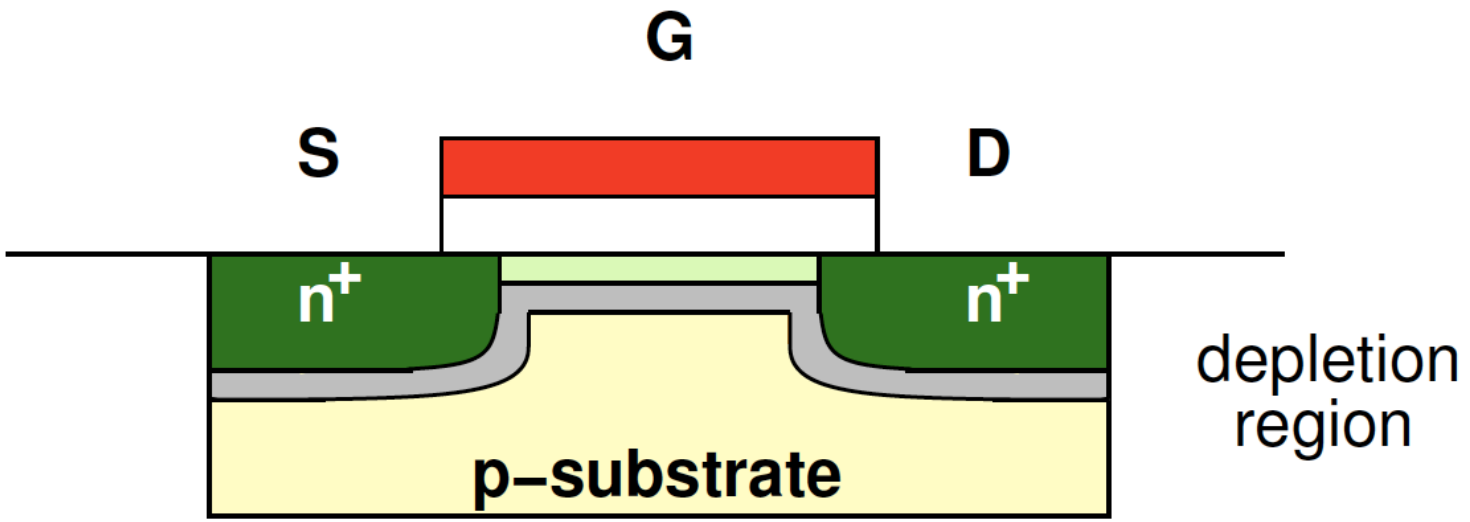
Gate-to-Bulk Capacitance

- Looks like parallel plate capacitance
- Two components:
  - What is C_{GC}? (C_{GCS}, C_{GCD})
  - What is C_{GCB}?



Gate-to-Channel Capacitance

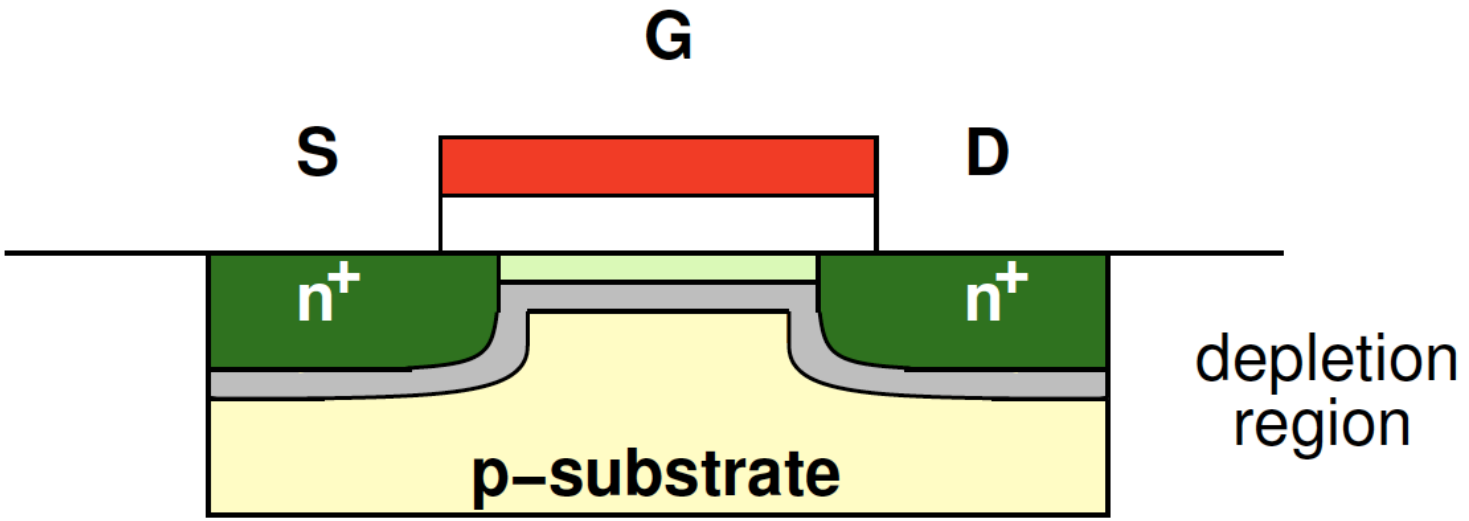
- Looks like parallel plate capacitance
- Two components: Case: Strong Inversion (small Vds)
  - C_{GC}
  - C_{GCB}



Gate-to-Channel Capacitance

- Looks like parallel plate capacitance
- Two components: Case: Strong Inversion
  - C_{GC}
  - $C_{GCB}=0$

$$C_{GC} = C_{ox} W L_{effective}$$

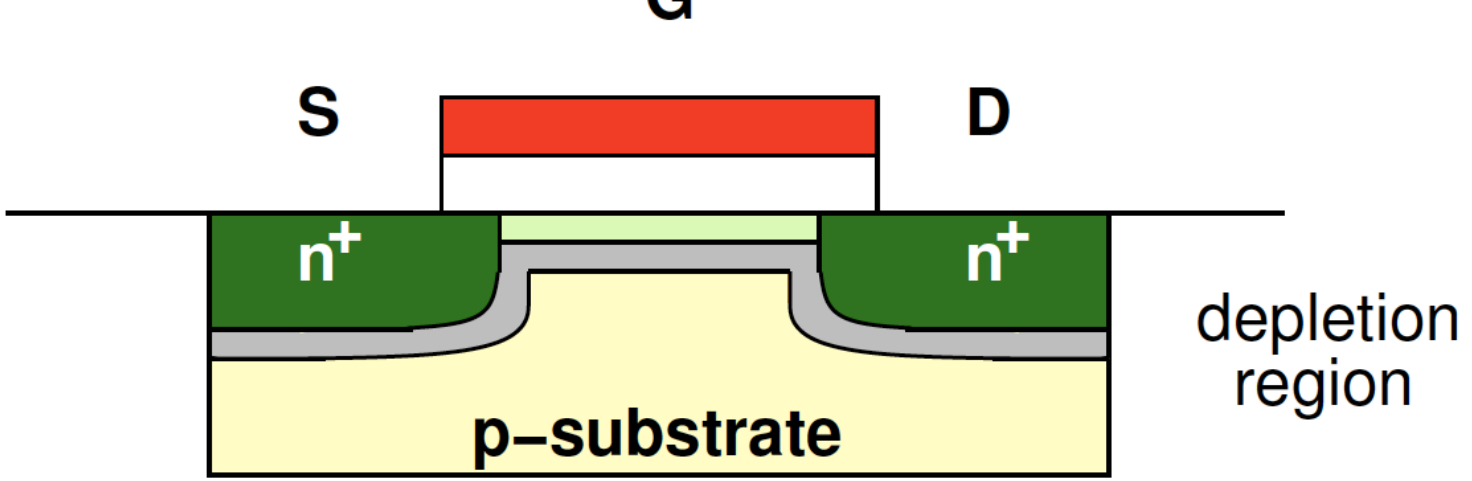


Gate-to-Channel Capacitance

- Looks like parallel plate capacitance
- Two components: Case: Strong Inversion
  - C_{GC} – Split evenly between S and D
  - C_{GB}=0

$$C_{GC} = C_{ox} WL_{effective}$$

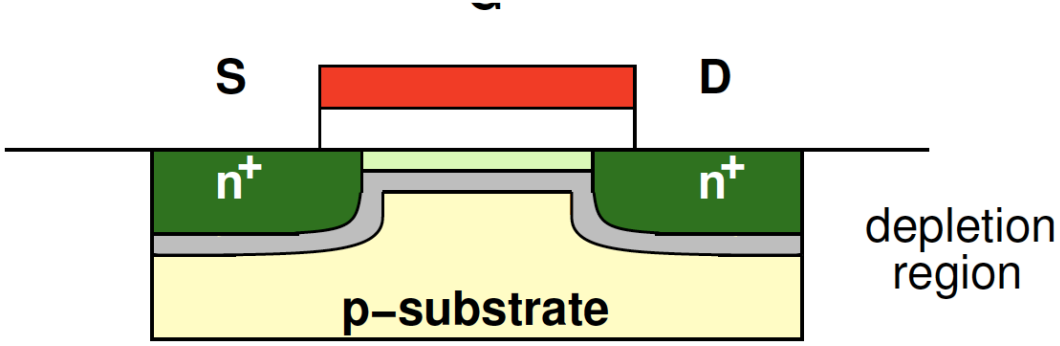
$$C_{GCS} = C_{GCD} = \frac{1}{2} C_{ox} WL_{effective}$$



Gate-to-Source Capacitance

- Channel + Overlap

$$C_{GS} = C_{GCS} + C_{GSO}$$



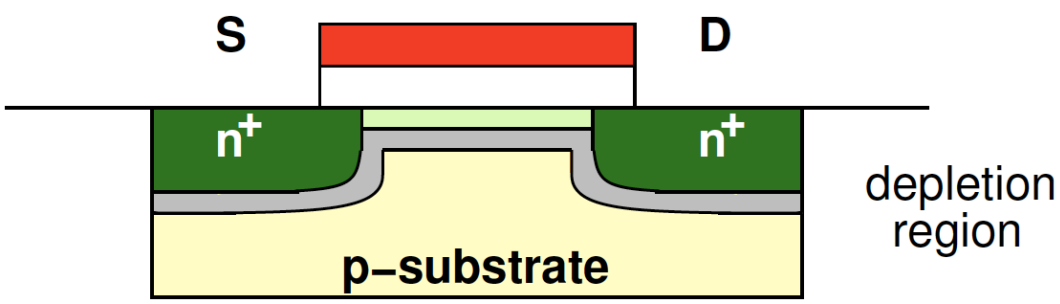
Gate-to-Source Capacitance

- Channel + Overlap

$$C_{GS} = C_{GCS} + C_{GSO}$$

$$C_{GS} = \frac{1}{2} C_{OX} W (L_{drawn} - L_{effective}) + \frac{1}{2} C_{OX} W L_{effective}$$

$$C_{GS} = \frac{1}{2} C_{OX} W L_{drawn}$$



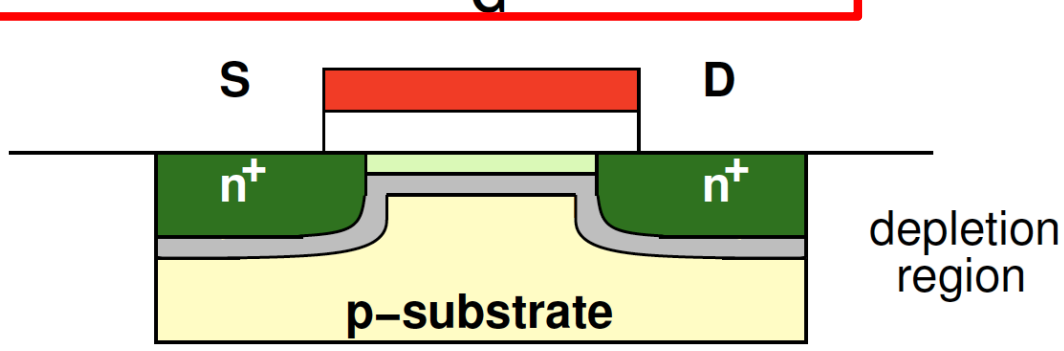
Gate-to-Drain Capacitance

- Channel + Overlap

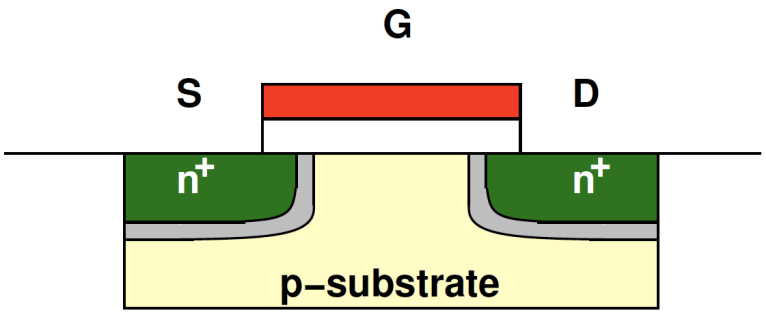
$$C_{GD} = C_{GCD} + C_{GDO}$$

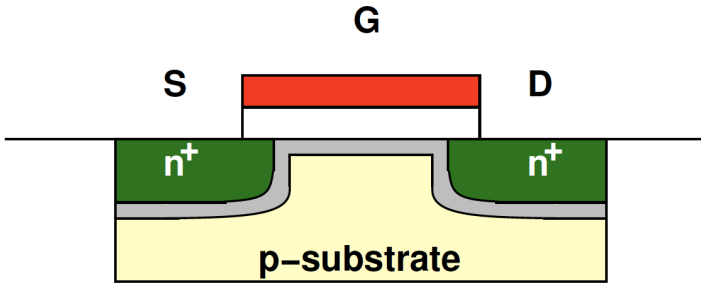
$$C_{GD} = \frac{1}{2} C_{OX} W (L_{drawn} - L_{effective}) + \frac{1}{2} C_{OX} W L_{effective}$$

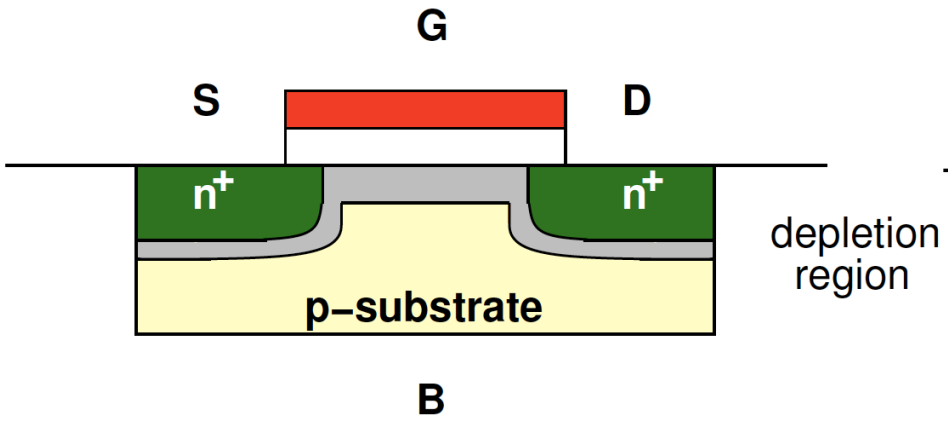
$$C_{GD} = \frac{1}{2} C_{OX} W L_{drawn}$$

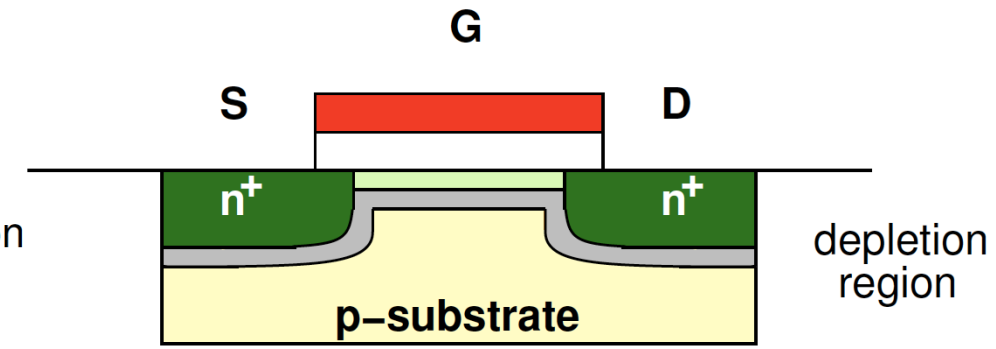


Channel Evolution: Weak Inversion



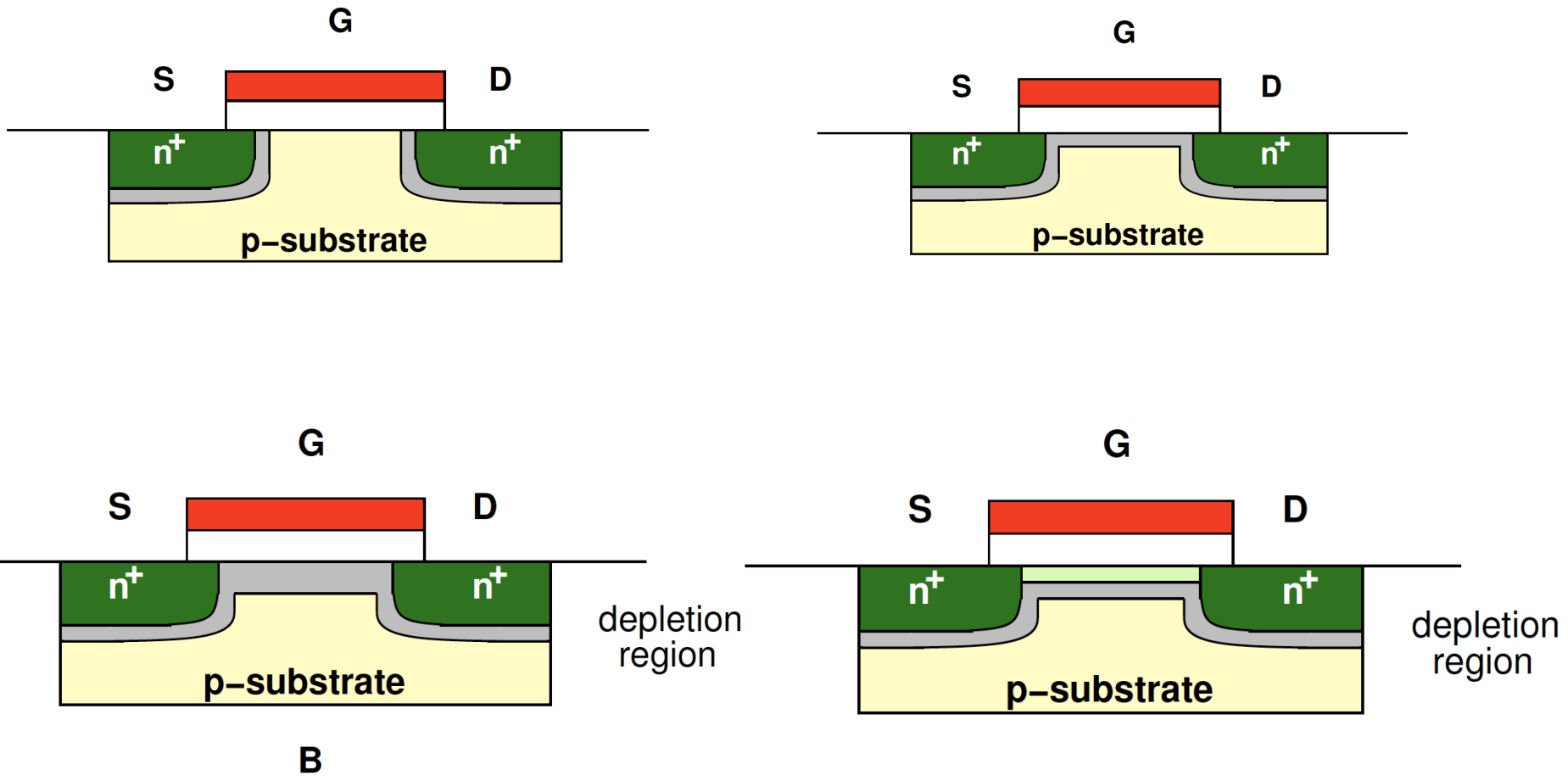






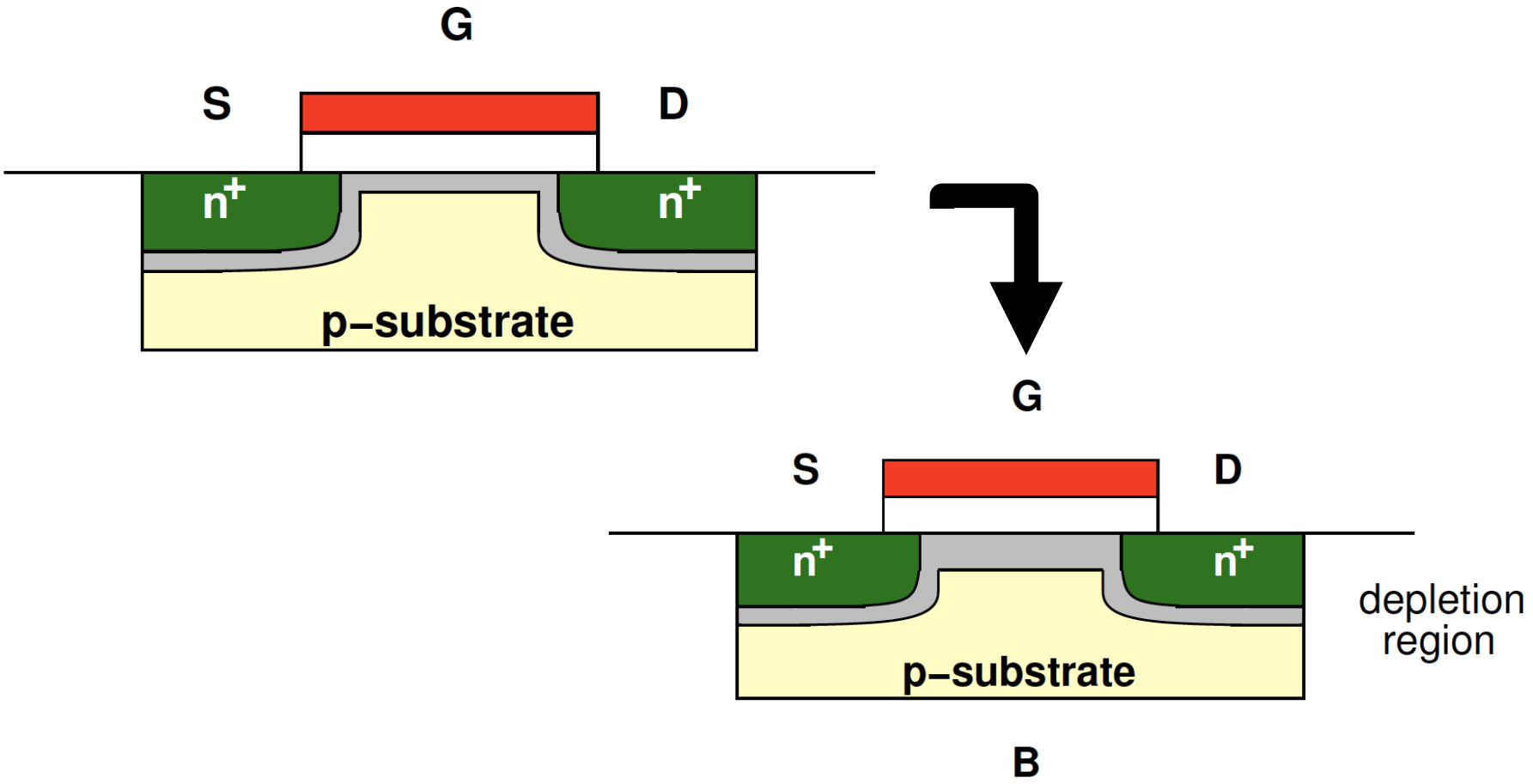
Channel Evolution: Weak Inversion

- $V_{GS} = 0 \rightarrow C_{GC}=0, C_{GCB}=WLC_{ox}$



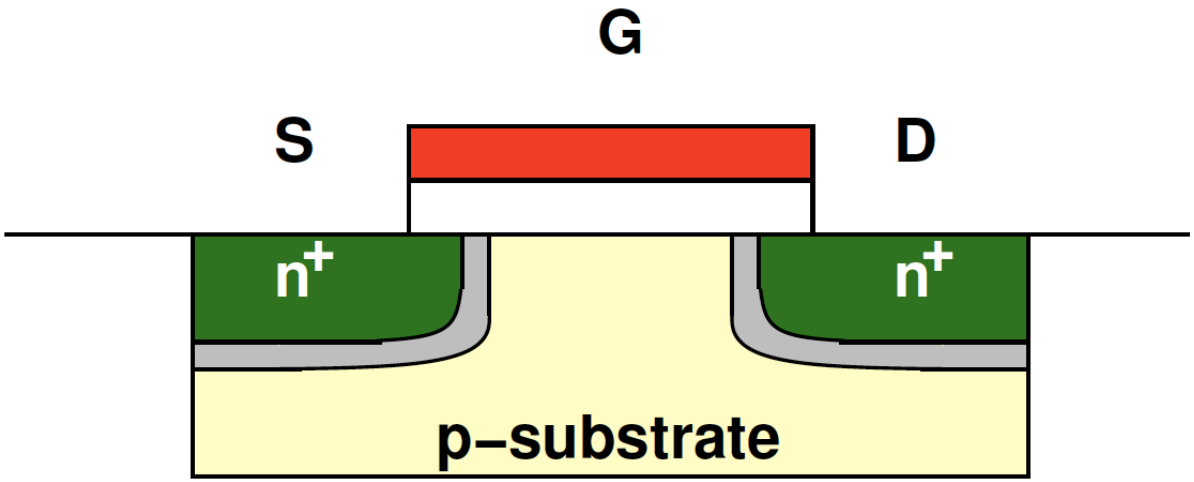
Channel Evolution: Weak Inversion

- What happens to capacitance here as V_{GS} increases?
  - Capacitor plate distance?

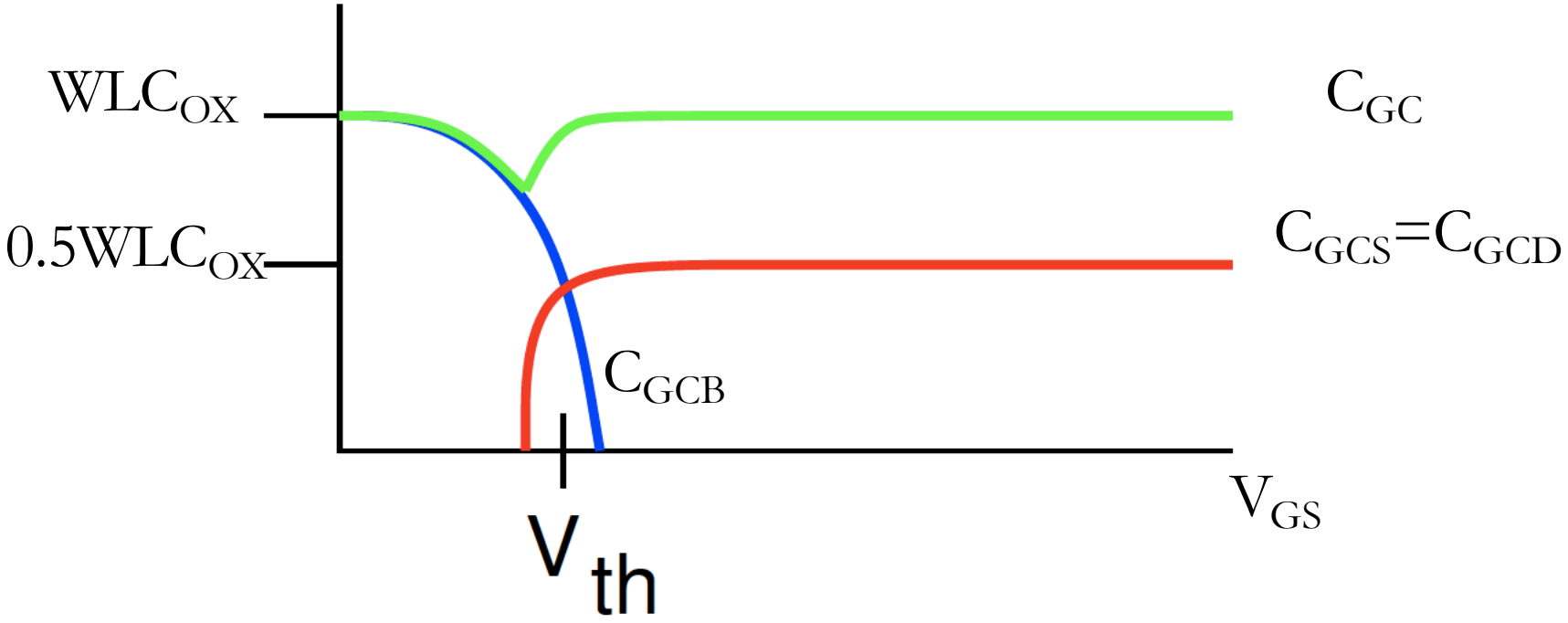


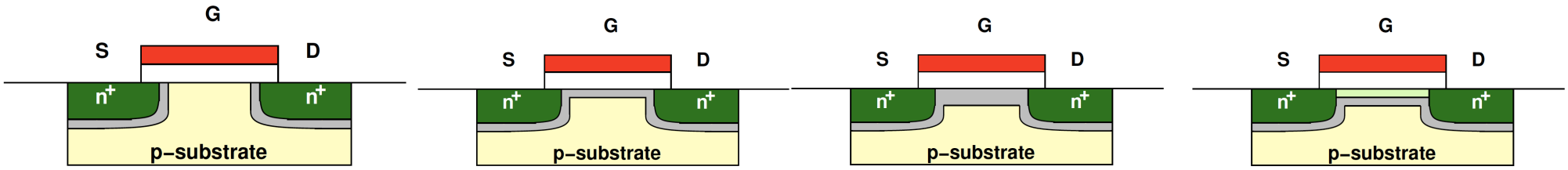
Channel Evolution: Weak Inversion

- Capacitance is initially dominated by Gate-to-bulk capacitance ($C_{GCS,D}$=0)
- Gate-to-bulk capacitance drops as V_{GS} increases toward V_{th}



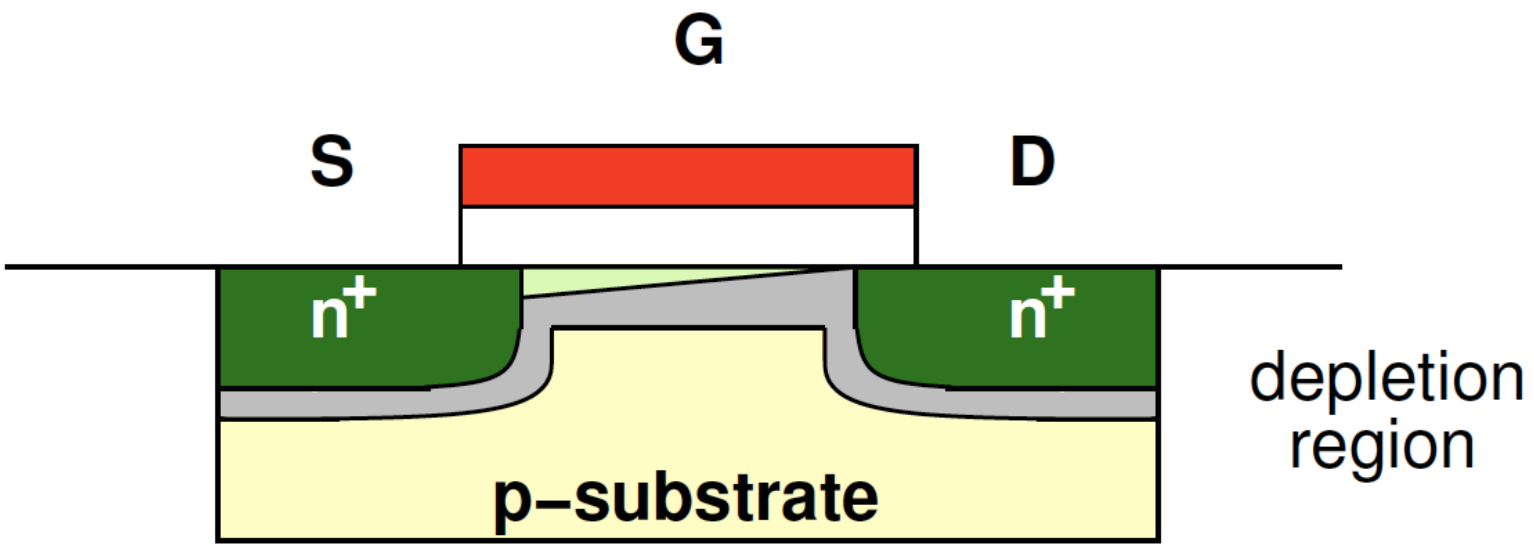
Capacitance vs V_{GS} (V_{DS}=0)





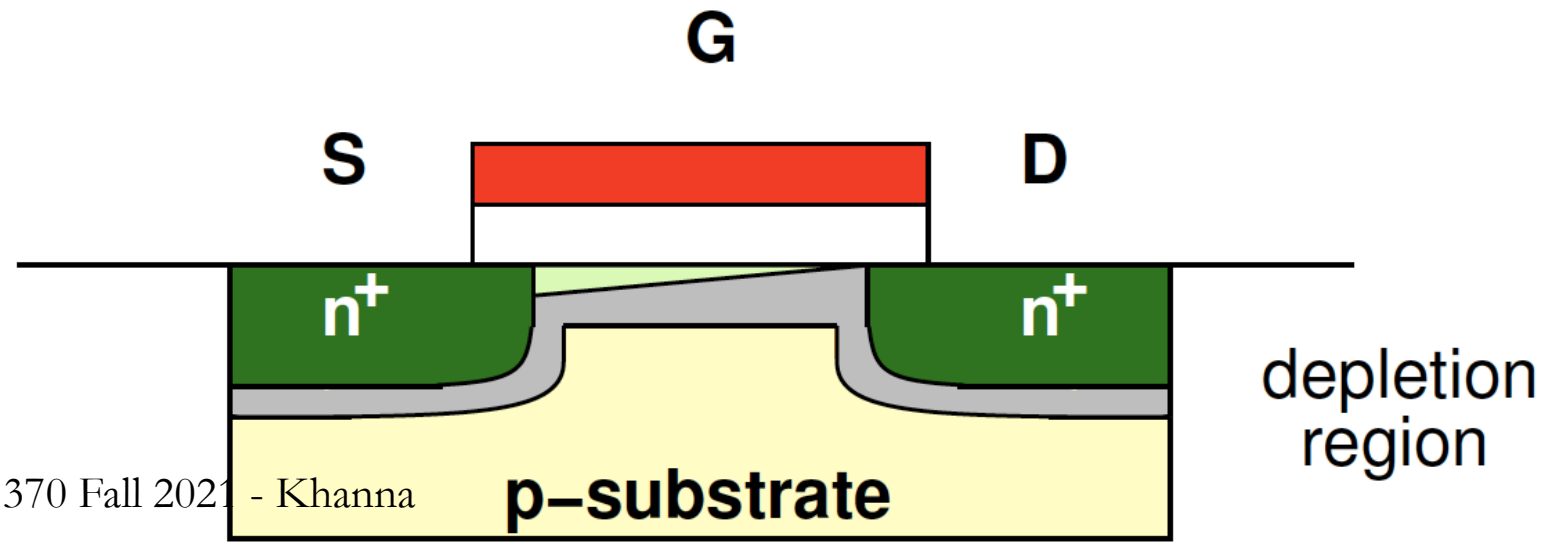
Increasing V_{GS} ⟶

Saturation Capacitance?

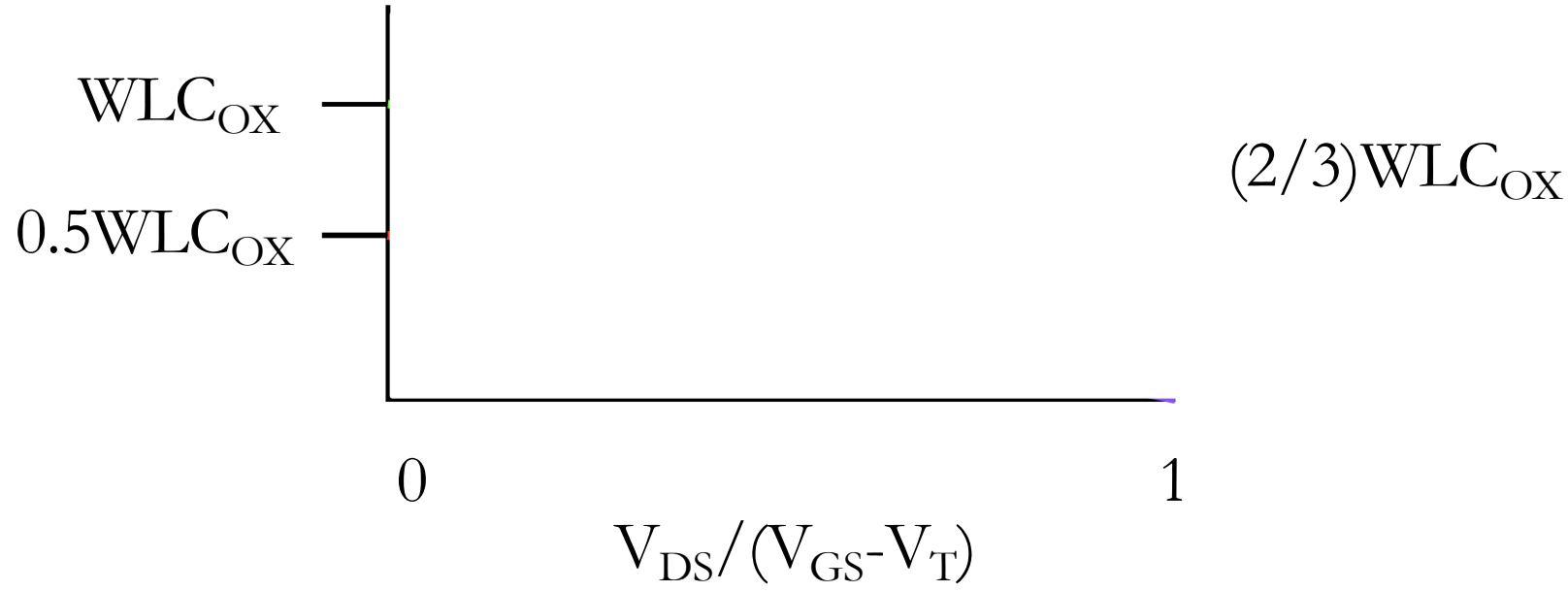


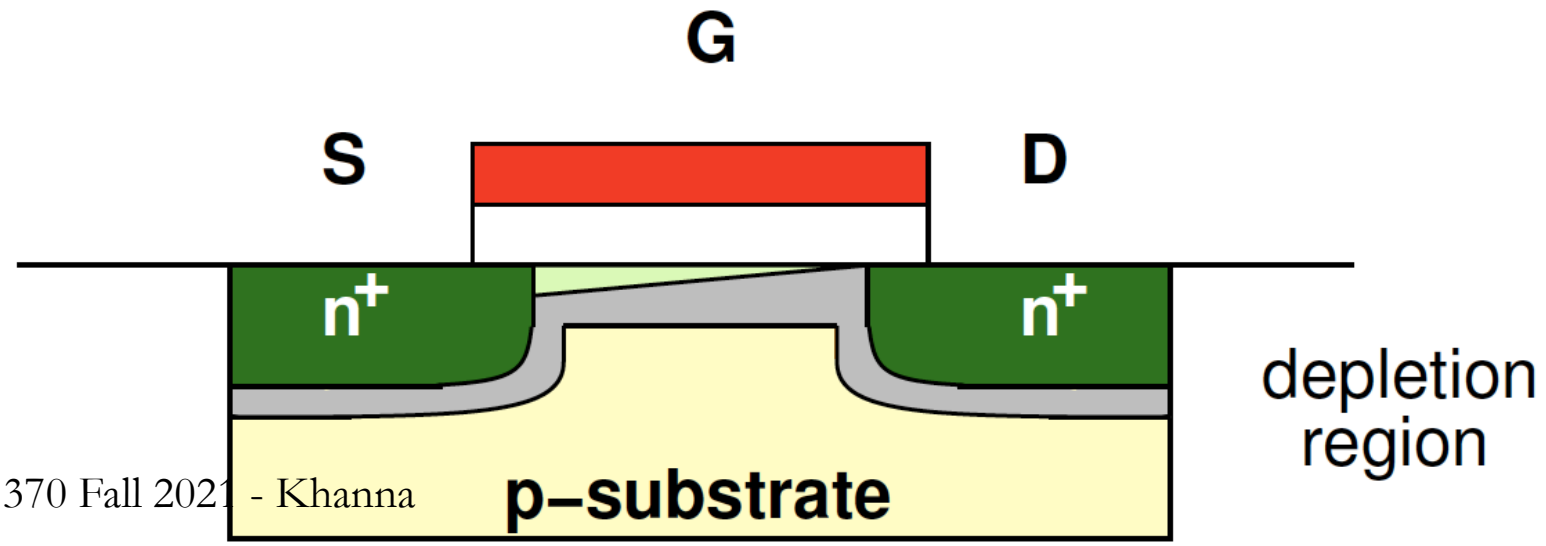
Saturation Capacitance?

- Source end of channel in inversion
- Voltage at drain end of channel at or below threshold
- Capacitance shifts to source
  - Total capacitance reduced

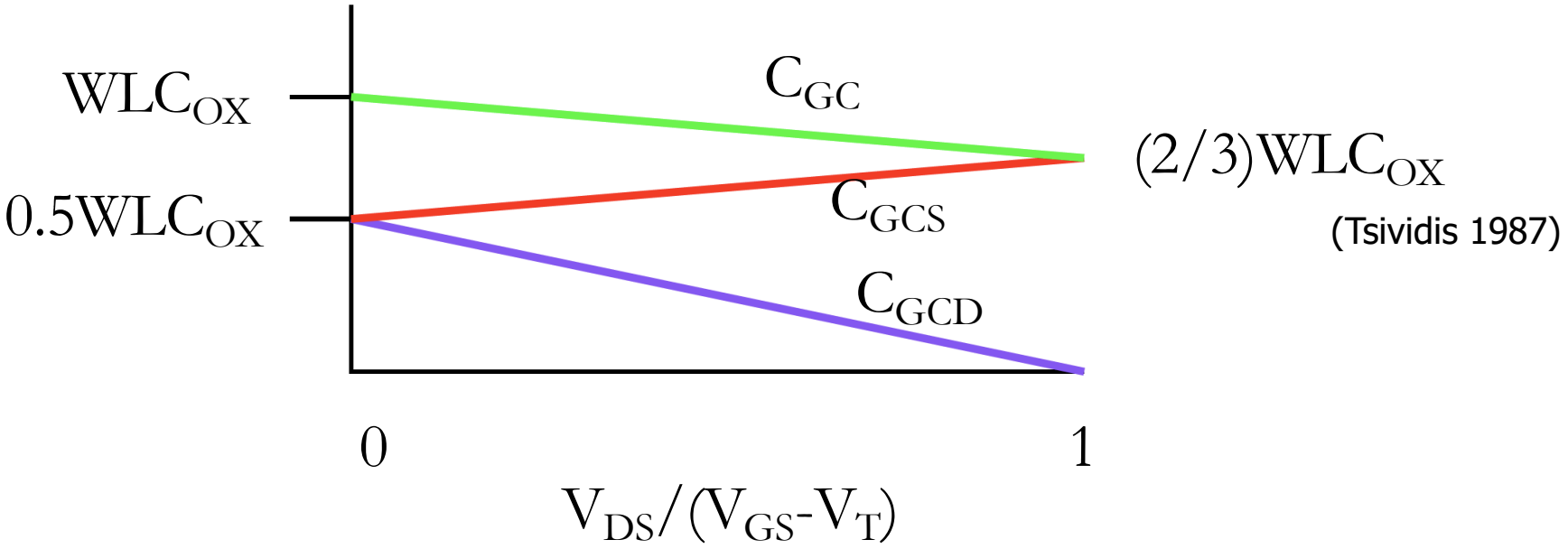


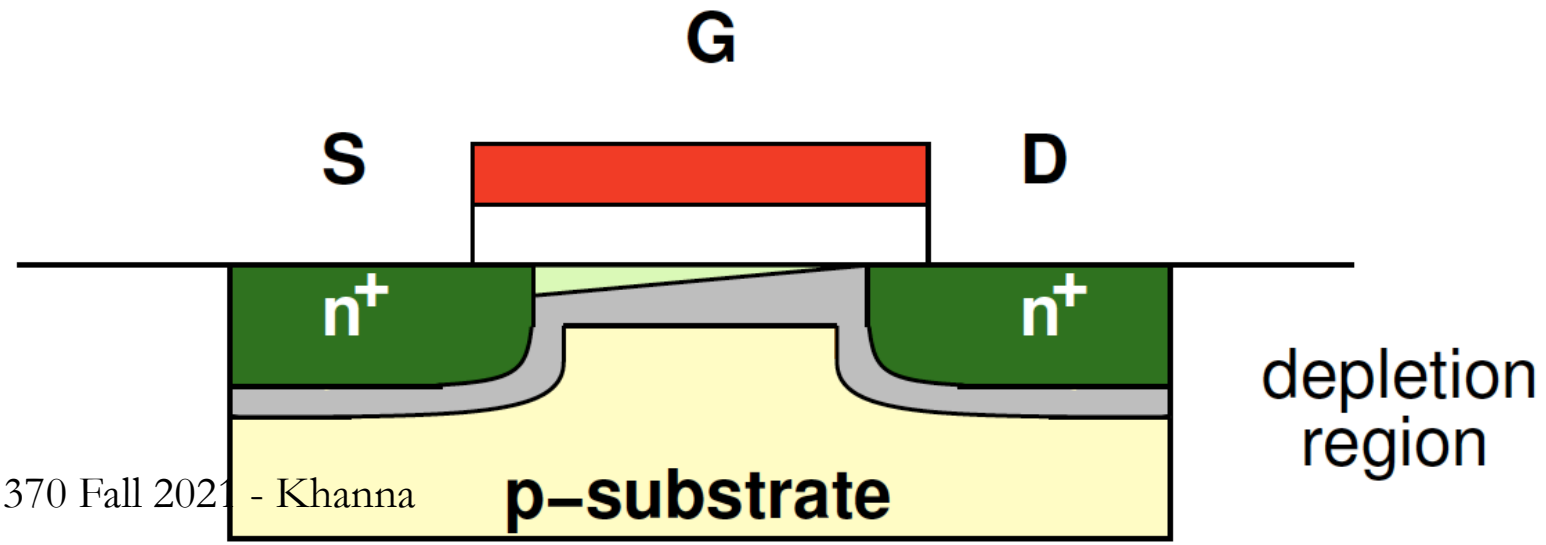
Saturation Capacitance





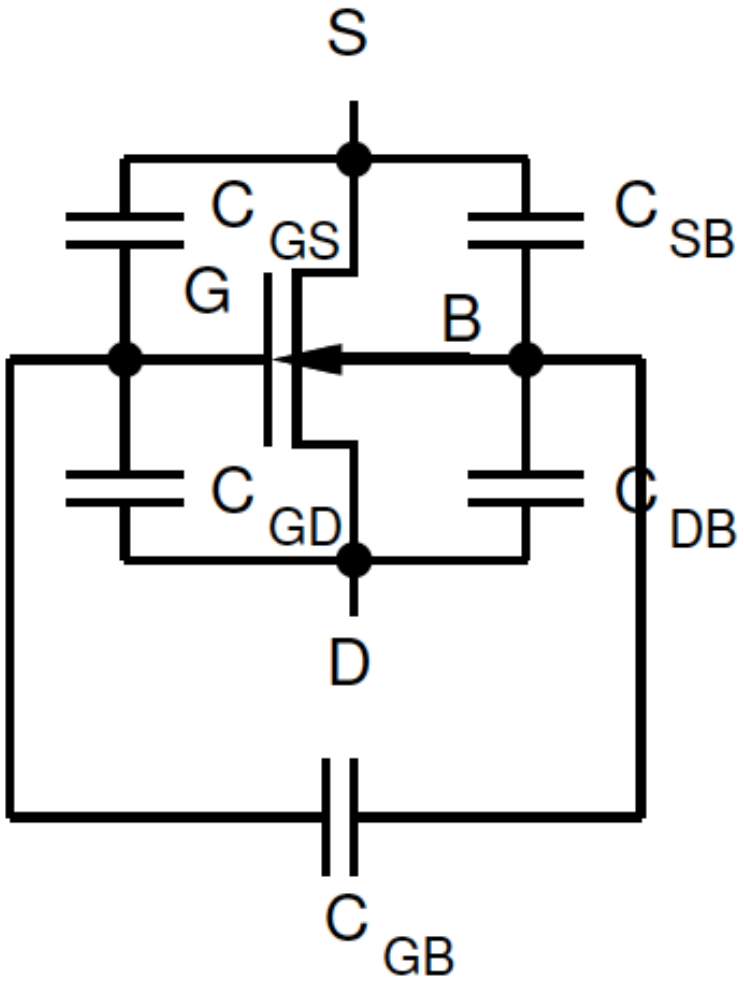
Saturation Capacitance





Capacitance Roundup

- $C_{GS}=C_{GCS}+C_{GSO}$
- $C_{GD}=C_{GCD}+C_{GDO}$
- $C_{GB}=C_{GCB}$
- $C_{SB}=C_{diff}$
- $C_{DB}=C_{diff}$



First Order Capacitance Summary

Operation Region	C_{GCB}	C_{GCS}	C_{GCD}	C_{GC}	C_G
Subthreshold					
Linear					
Saturation					

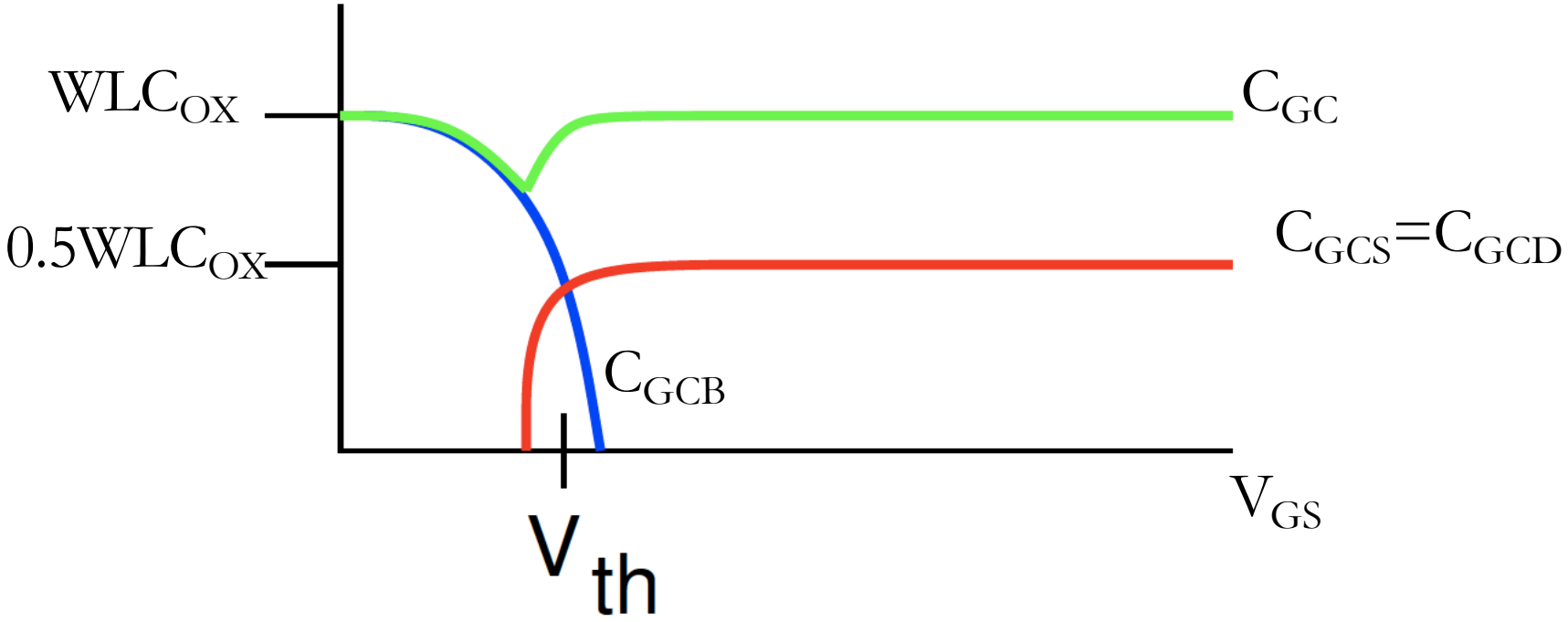
First Order Capacitance Summary

Operation Region	C_{GCB}	C_{GCS}	C_{GCD}	C_{GC}	C_G
Subthreshold					
Linear	0	$C_{OX}WL/2$	$C_{OX}WL/2$		
Saturation					

$$C_{GCS} = C_{GCD} = \frac{1}{2} C_{ox} WL_{effective}$$

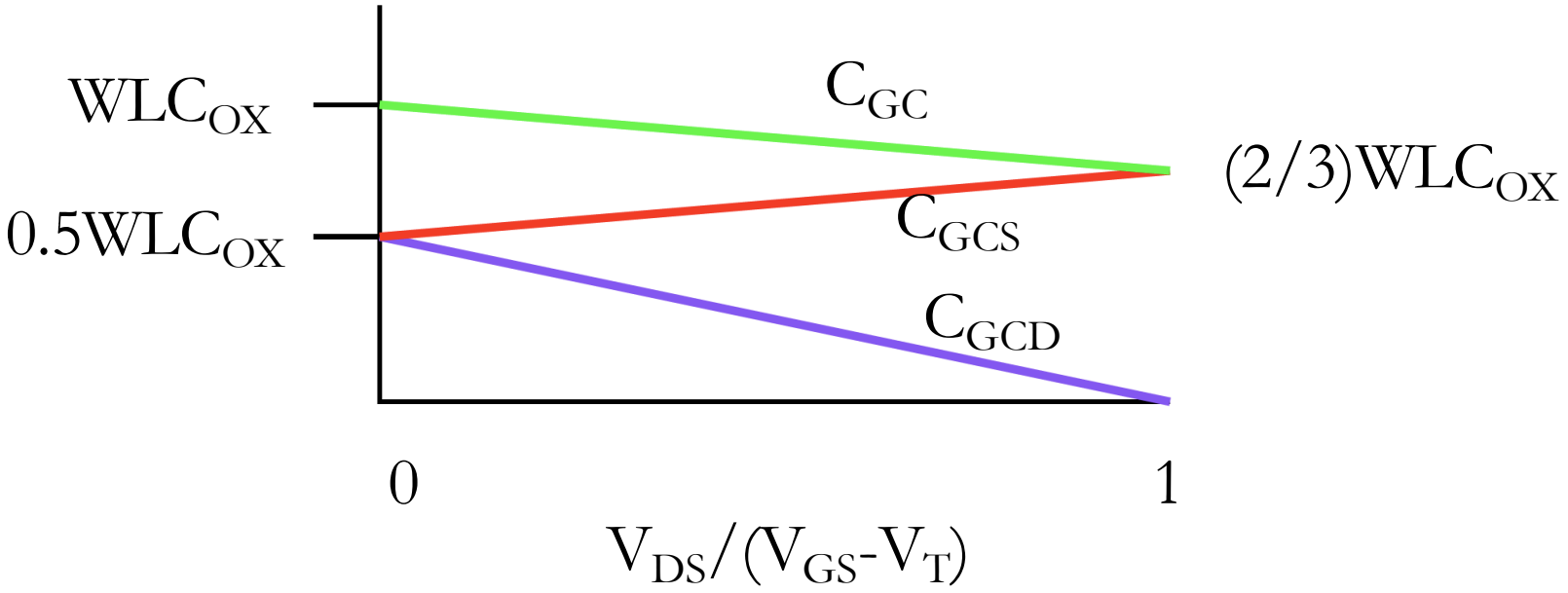
First Order Capacitance Summary

Operation Region	C_{GCB}	C_{GCS}	C_{GCD}	C_{GC}	C_G
Subthreshold	$C_{OX}WL$	0	0		
Linear	0	$C_{OX}WL/2$	$C_{OX}WL/2$		
Saturation					



First Order Capacitance Summary

Operation Region	C_{GCB}	C_{GCS}	C_{GCD}	C_{GC}	C_G
Subthreshold	$C_{OX}WL$	0	0		
Linear	0	$C_{OX}WL/2$	$C_{OX}WL/2$		
Saturation	0	$(2/3)C_{OX}WL$	0		



First Order Capacitance Summary

Operation Region	C_{GCB}	+	C_{GCS}	+	C_{GCD}	=	C_{GC}	C_G
Subthreshold	$C_{OX}WL$		0		0		$C_{OX}WL$	
Linear	0		$C_{OX}WL/2$		$C_{OX}WL/2$		$C_{OX}WL$	
Saturation	0		$(2/3)C_{OX}WL$		0		$(2/3)C_{OX}WL$	

First Order Capacitance Summary

Operation Region	C_{GCB}	C_{GCS}	C_{GCD}	C_{GC}	C_G
Subthreshold	$C_{OX}WL$	0	0	$C_{OX}WL$	$C_{OX}WL+2C_O$
Linear	0	$C_{OX}WL/2$	$C_{OX}WL/2$	$C_{OX}WL$	$C_{OX}WL+2C_O$
Saturation	0	$(2/3)C_{OX}WL$	0	$(2/3)C_{OX}WL$	$(2/3)C_{OX}WL+2C_O$

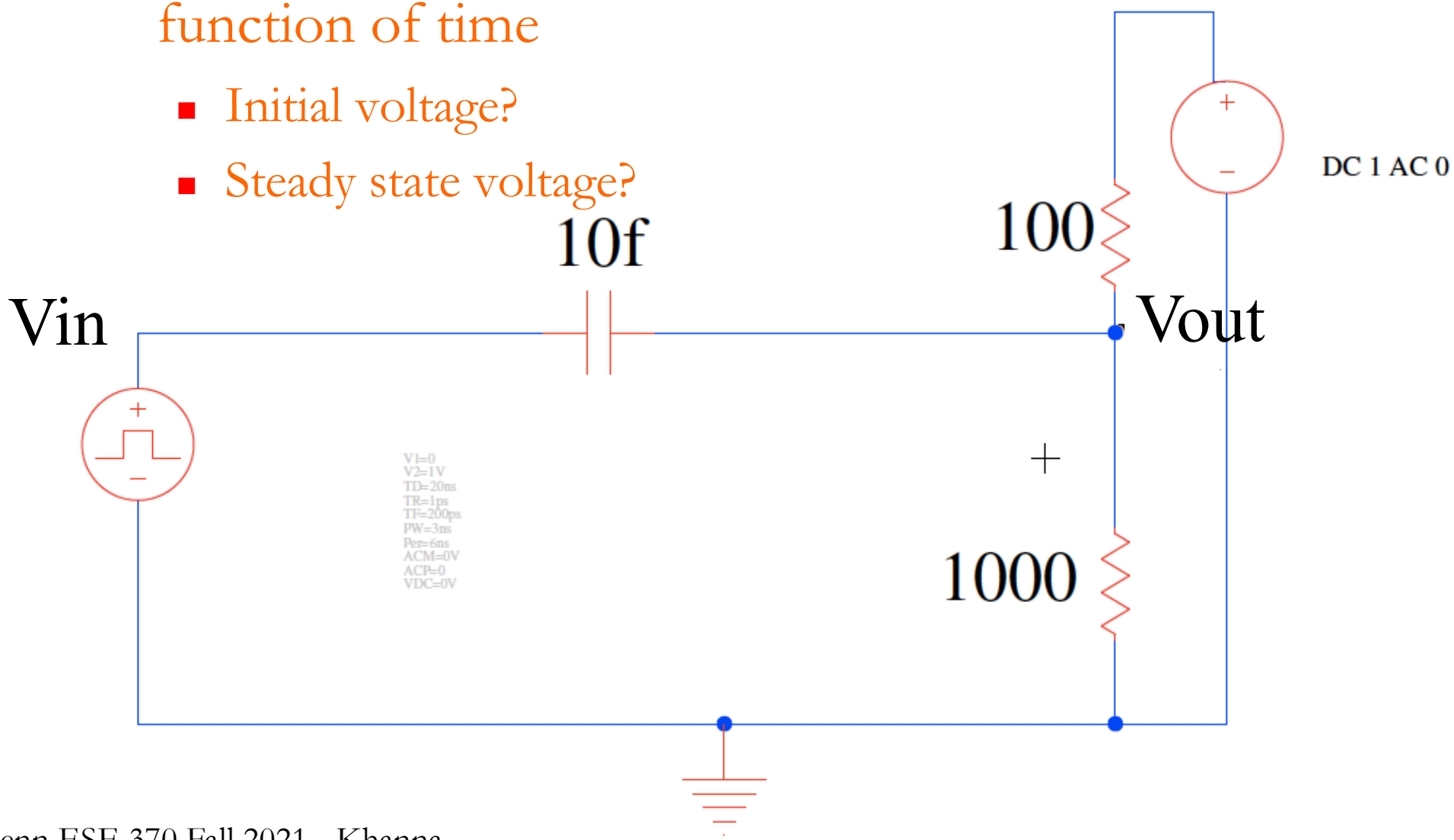
$$C_o = \frac{1}{2} C_{ox} W \left(L_{drawn} - L_{effective} \right) = C_{GSO} = C_{GDO}$$

One Implication

Feedback Capacitance C_{gd}

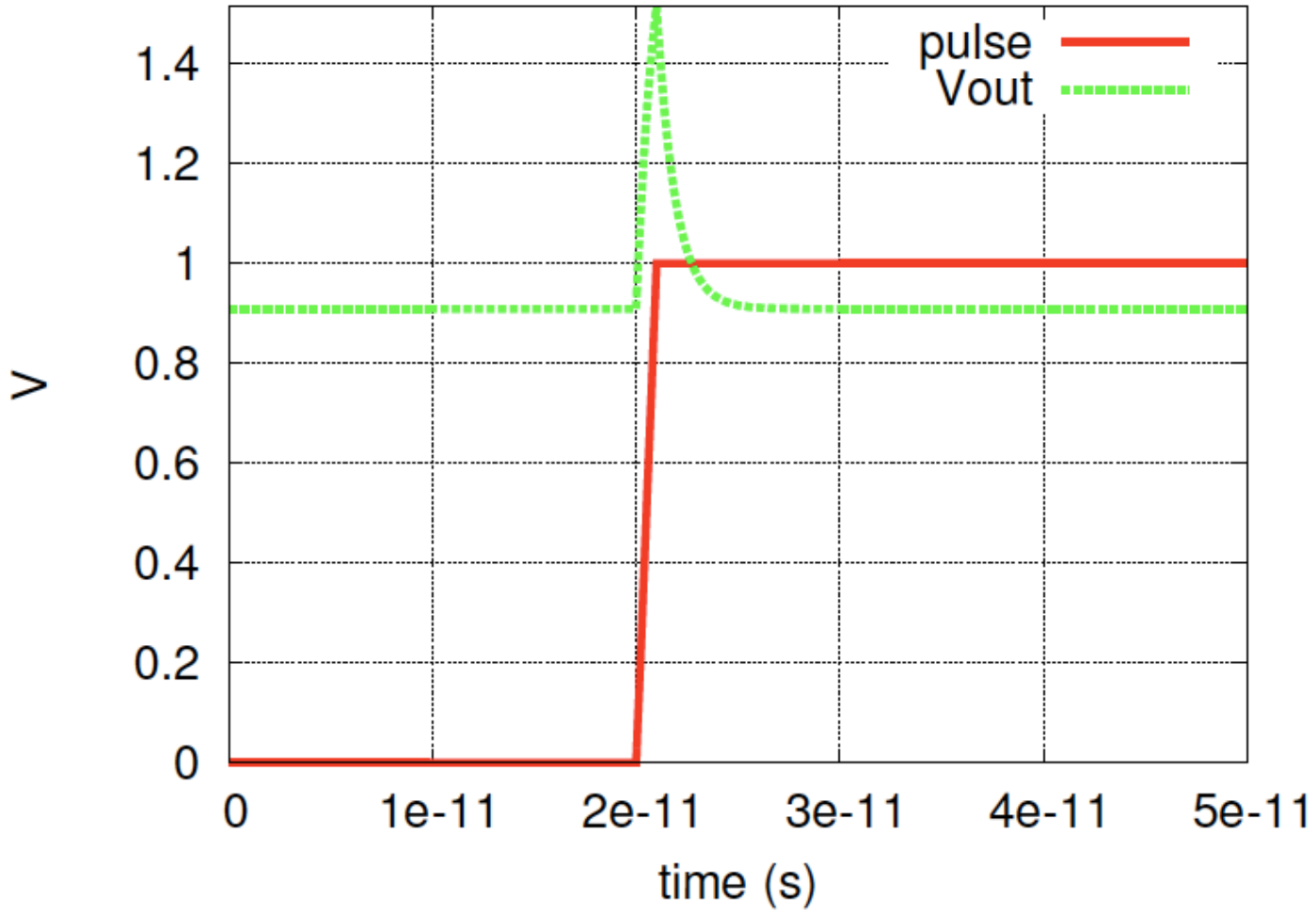
Step Response? (Preclass 2)

- Vin steps from 0 to 1, what does Vout look like as a function of time
  - Initial voltage?
  - Steady state voltage?



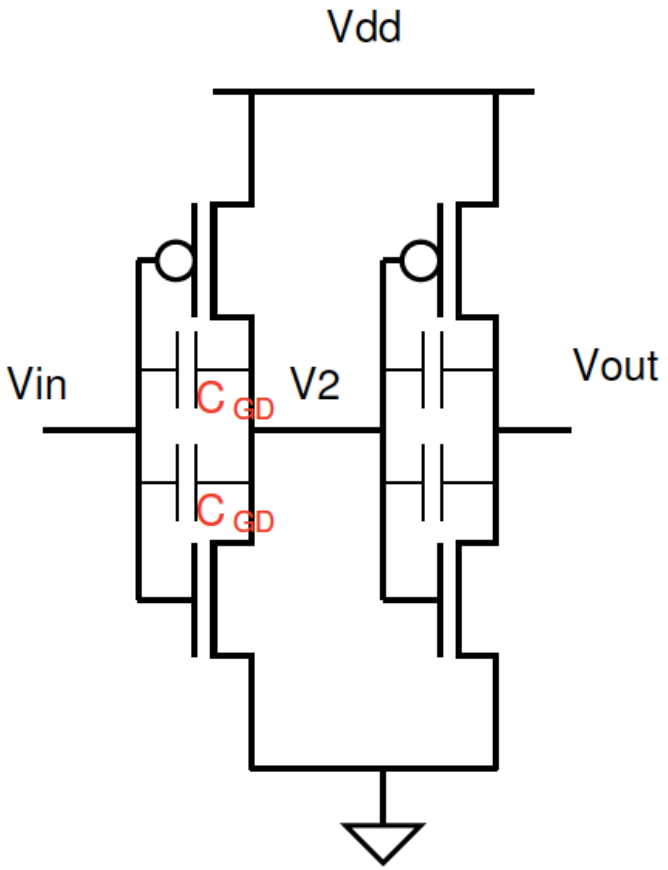
Step Response

Voltage peaking!

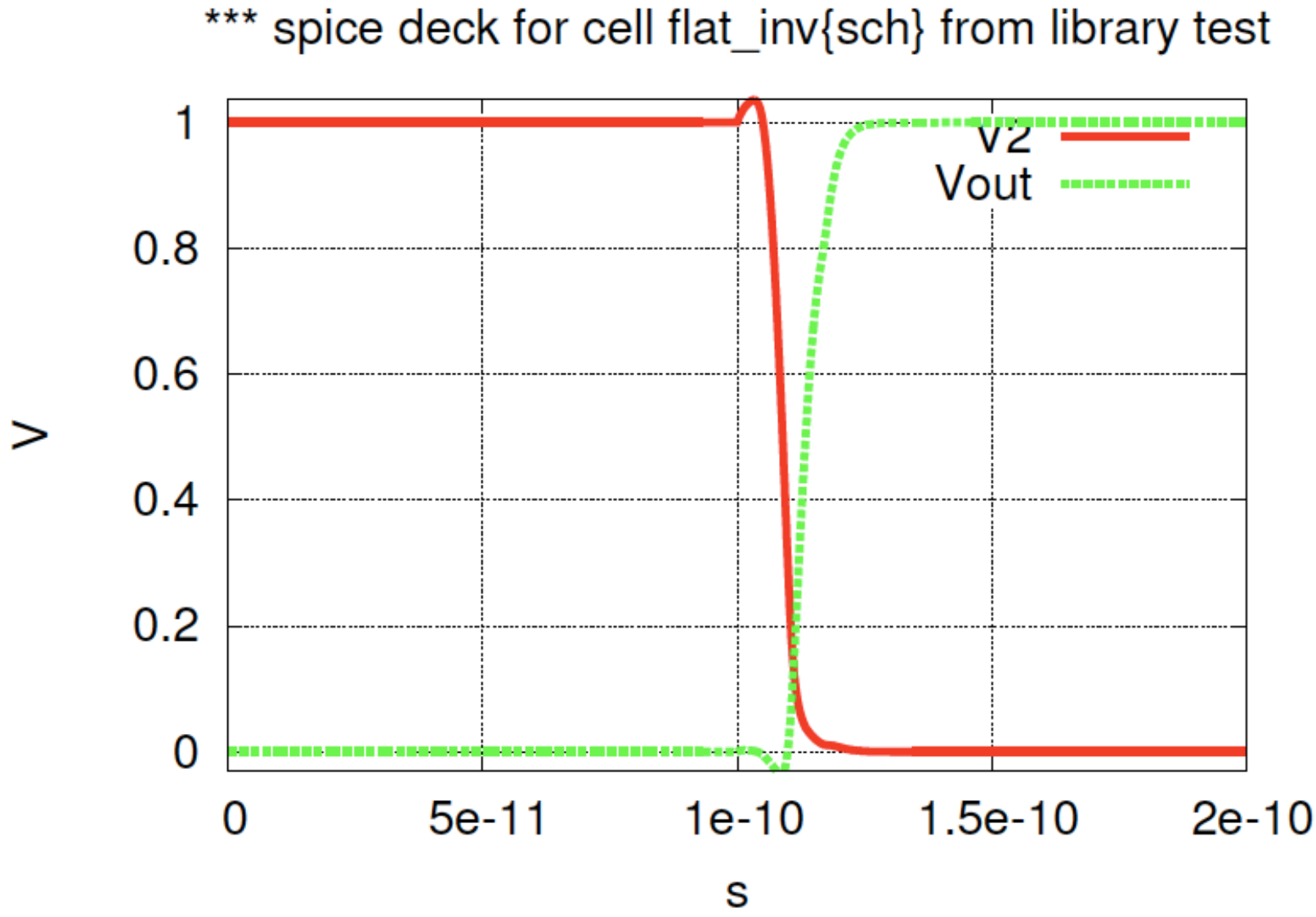


Impact of C_{GD}

- What does C_{GD} do to the switching response here?
  - V_2
  - V_{out}

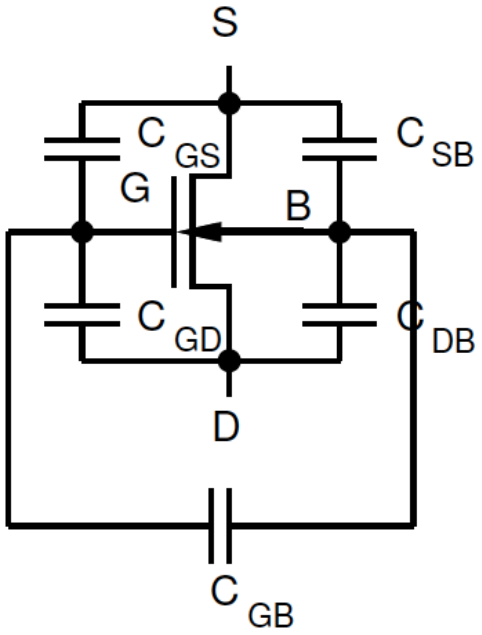


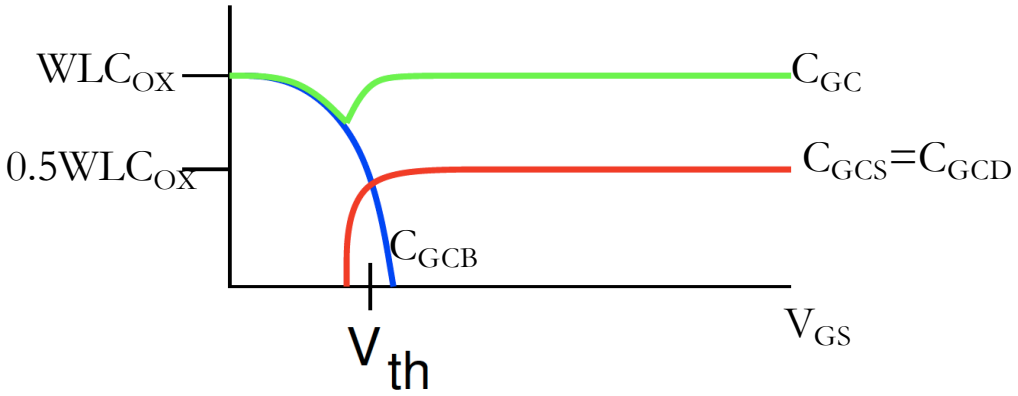
Impact of C_{GD}

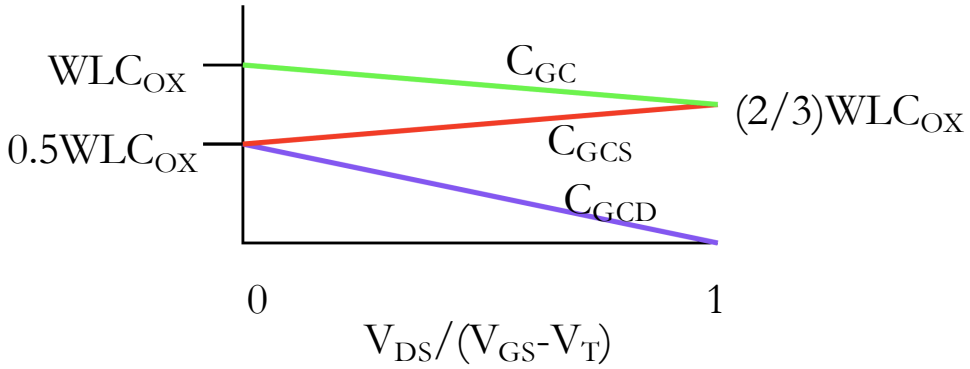


Big Idea

- Capacitance
  - To every terminal
  - Voltage dependent







Admin

- HW 3
  - Due Monday
- Midterm 1 Friday 10/1 (next week)
  - 7-9pm in Towne 309
  - No Lecture, virtual office hours
  - Midterms from 2010-2019 (and Project 1 from 2020)
    - All online with and without answers
  - Midterm 1 Review virtual session next week
    - See Piazza for poll coming soon
  - Conflicts must let me know ASAP

Midterm 1 - Content

- Lec 1 - 9
  - Identify CMOS/non-CMOS
  - Identify CMOS function
  - Any logic function → CMOS gate
  - Noise Margins / Restoration
  - Circuit first order switching rise/fall times
    - Output equivalent resistance
    - Load capacitance
  - MOS Model
  - Identify transistor region of operation
  - Analysis with transistor IV models
  - MOS capacitance models