University of Pennsylvania
Department of Electrical and System Engineering
Circuit-Level Modeling, Design, and Optimization for Digital Systems

ESE370, Fall 2021 Midterm 1 Friday, October 1

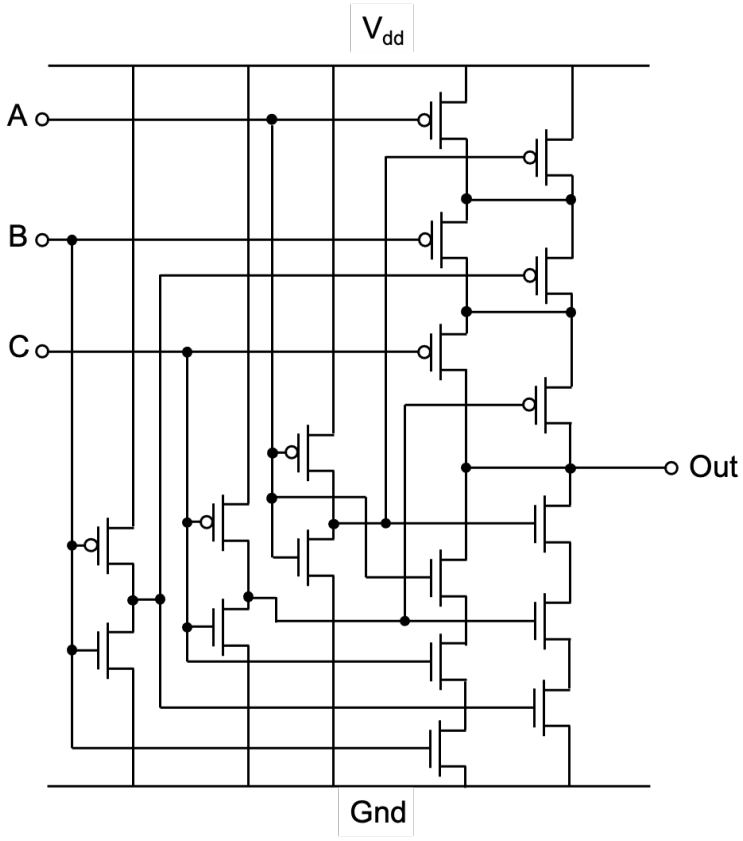
- 4 problems with weights indicated.
- Parts within a problem will not be weighted equally.
- Calculators allowed.
- Closed book = No text or notes allowed.

Name:

Grade:

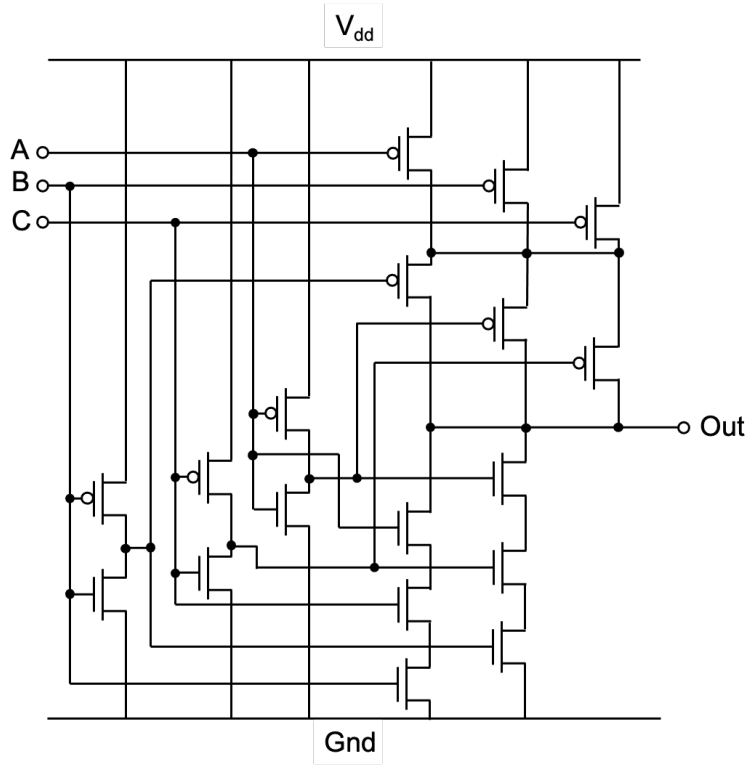
Q1	
Q2	
Q3	
Q4	
Total	

1. (25 points) Identify if the following circuits are CMOS, why or why not, and their functions. [Show your work for partial credit consideration.]



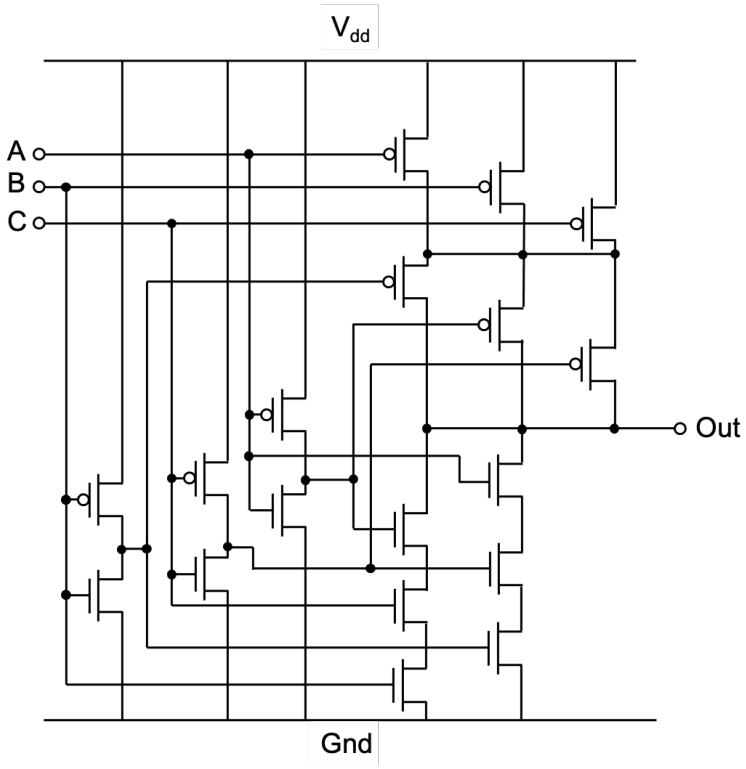
(a)

CMOS? (circle one)	Yes No
(if CMOS) Function (Out)	
(if not CMOS) Why not?	



(b)

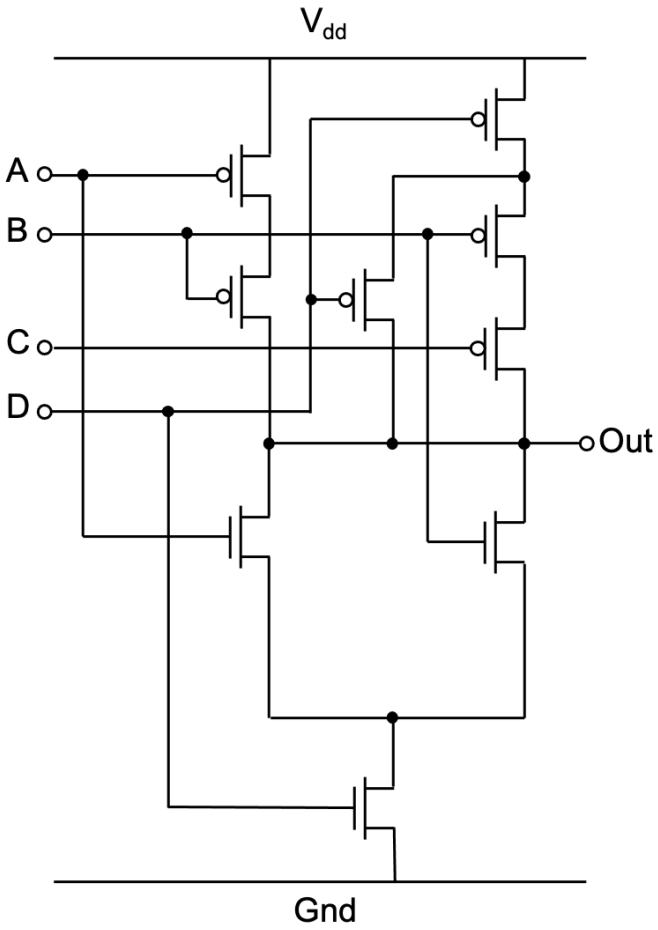
CMOS? (circle one)	Yes No
(if CMOS) Function (Out)	
(if not CMOS) Why not?	



(c)

CMOS? (circle one)	Yes No
(if CMOS) Function (Out)	
(if not CMOS) Why not?	

2. (25 points) Consider the following circuit:



Assume:

- all transistors are same size.
- all on transistors have resitance R_{on}.
- all transistors have total gate capacitance C_g.

(a) Identify the output function.

(b) Lowest resistance driving output?

Case: Resistance:

(c) Highest resistance driving output?

Case: Resistance:

(d) Lowest capacitance of an input?

Which: Capacitance:

(e) Highest capacitance of an input?

Which: Capacitance:

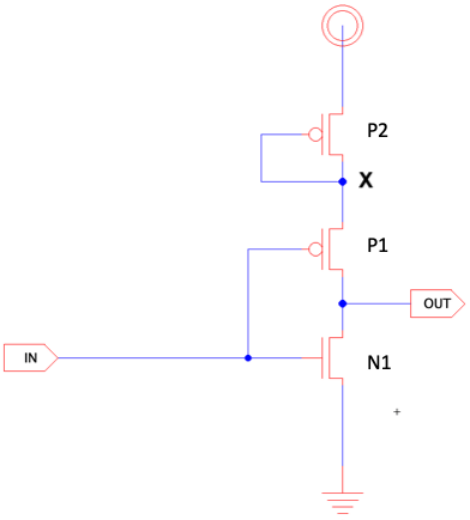
(f) Worst-case 10-90 rise time for one of these gates driving a single input of another of these gates?

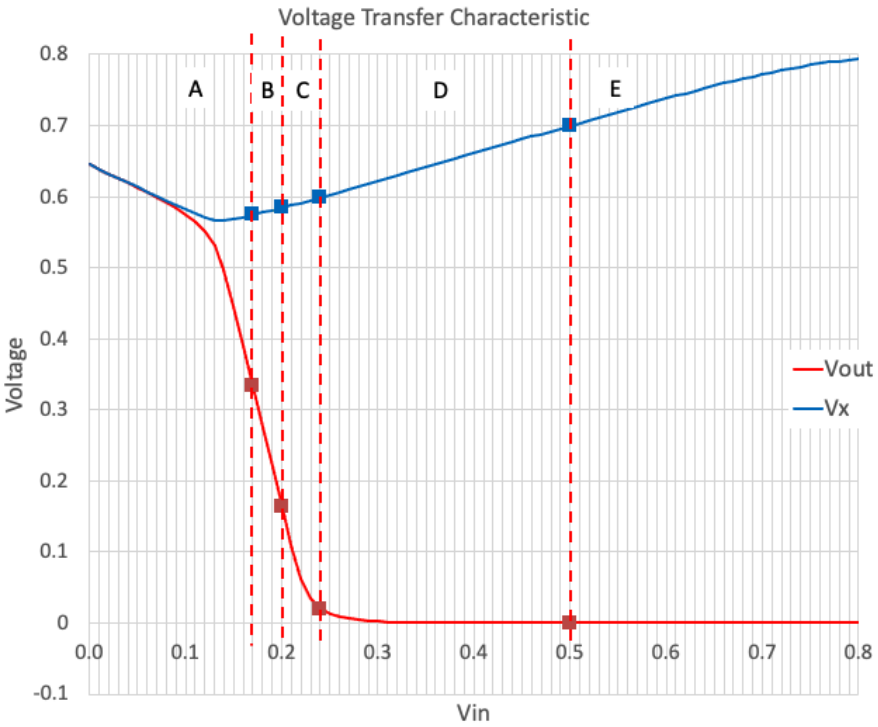
Case:

Rise Time Expression:

[Show calculation for partial credit consideration.]

3. (25 points) Consider the following circuit and its voltage transfer characteristic as well as the voltage at node X. Assume $V_{dd} = 800mV$ and $V_{thn} = -V_{thp} = 200mV$.





For the regions A-E labeled on the transfer function, identify the region of operation of the nMOS and both pMOS devices. Fill out the table below.

	N1	P1	P2
A			
B			
C			
D			
E			

For reference on the next page are the transistor current models and additional work space if needed:

NMOS:

V_{GS}	V_{DS}	Mode	I_{DS}
$\geq V_{thn}$	$< V_{GS} - V_{thn}$	Linear	$\mu_n C_{ox} \frac{W}{L} \cdot \left((V_{GS} - V_{thn}) \cdot V_{DS} - \frac{V_{DS}^2}{2} \right)$
	$\geq V_{GS} - V_{thn}$	Saturation	$\frac{1}{2} \mu_n C_{ox} \frac{W}{L} \cdot (V_{GS} - V_{thn})^2$
$< V_{th}$		Subthreshold	0

PMOS:

V_{GS}	V_{DS}	Mode	I_{DS}
$\leq V_{thp}$	$> V_{GS} - V_{thp}$	Linear	$\mu_p C_{ox} \frac{W}{L} \cdot \left((V_{GS} - V_{thp}) \cdot V_{DS} - \frac{V_{DS}^2}{2} \right)$
	$\leq V_{GS} - V_{thp}$	Saturation	$\frac{1}{2} \mu_n C_{ox} \frac{W}{L} \cdot (V_{GS} - V_{thp})^2$
$> V_{th}$		Subthreshold	0

4. (25 points) For this problem we consider a new technology that is not necessarily MOS. You can assume $V_{dd} = 1V$ We are told there are two "gates" available to us:

   - P-gate: 1-input gate where:

$$V_{out} = \begin{cases} 1 - 0.5V_{in} & V_{in} < 0.3 \\ 1.6 - 2.5V_{in} & 0.3 \leq V_{in} < 0.6 \\ 0.25 - 0.25V_{in} & 0.6 \leq V_{in} \end{cases} \quad (1)$$

   - Q-gate: 2-input gate where: $V_{out} = |V_A - V_B|$

   (a) What logical function does the restoring P-gate perform? Identify the noise margins that will provide restoration for this gate.

   Function:

V_{OH}	
V_{IH}	
V_{IL}	
V_{OL}	
NM_L	
NM_H	

(b) What logical function does the non-restoring Q-gate perform? Draw a combination of P and Q gates that will serve as a restoring gate that performs the same logic function and identify the noise margins that will provide restoration for this new gate.

Function:

V_{OH}	
V_{IH}	
V_{IL}	
V_{OL}	
NM_L	
NM_H	