University of Pennsylvania
Department of Electrical and System Engineering
Circuit-Level Modeling, Design, and Optimization for Digital Systems

ESE370, Fall 2021 Midterm 1 Friday, October 1

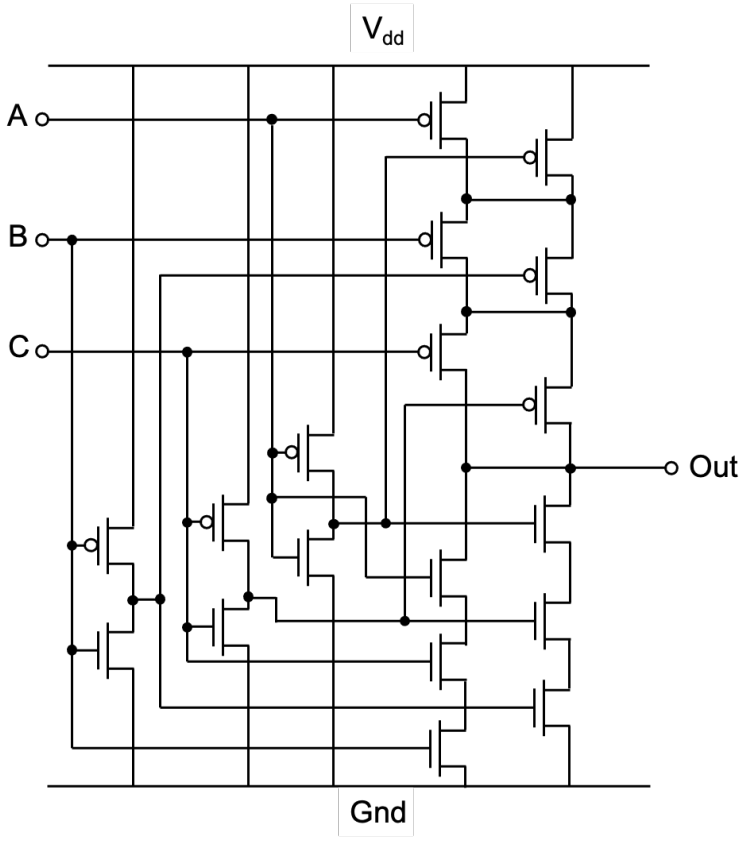
- 4 problems with weights indicated.
- Parts within a problem will not be weighted equally.
- Calculators allowed.
- Closed book = No text or notes allowed.

Name: Answers

Grade:

Q1	
Q2	
Q3	
Q4	
Total	Mean: 92.4, Stdev: 7.2

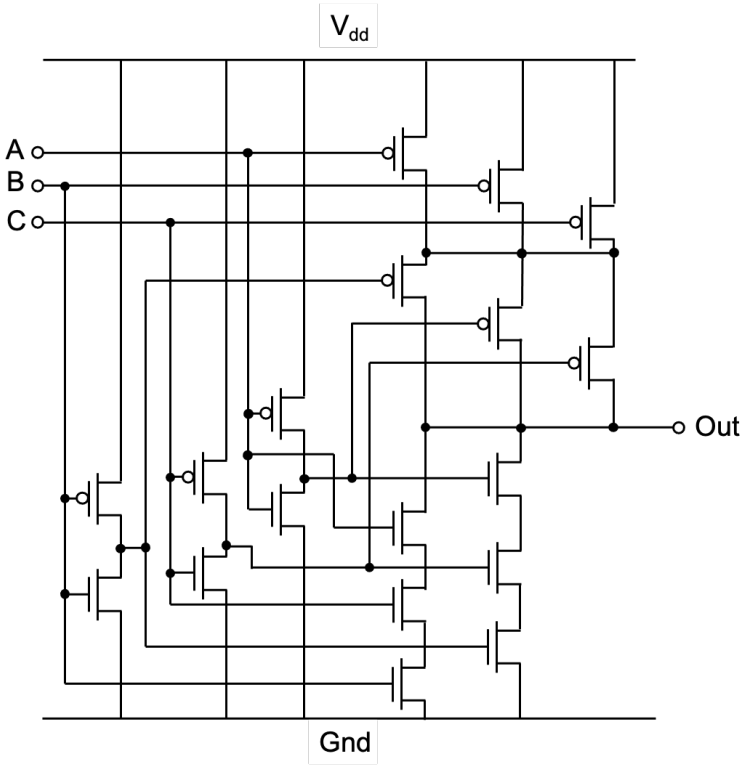
1. (25 points) Identify if the following circuits are CMOS, why or why not, and their functions. [Show your work for partial credit consideration.]



(a)

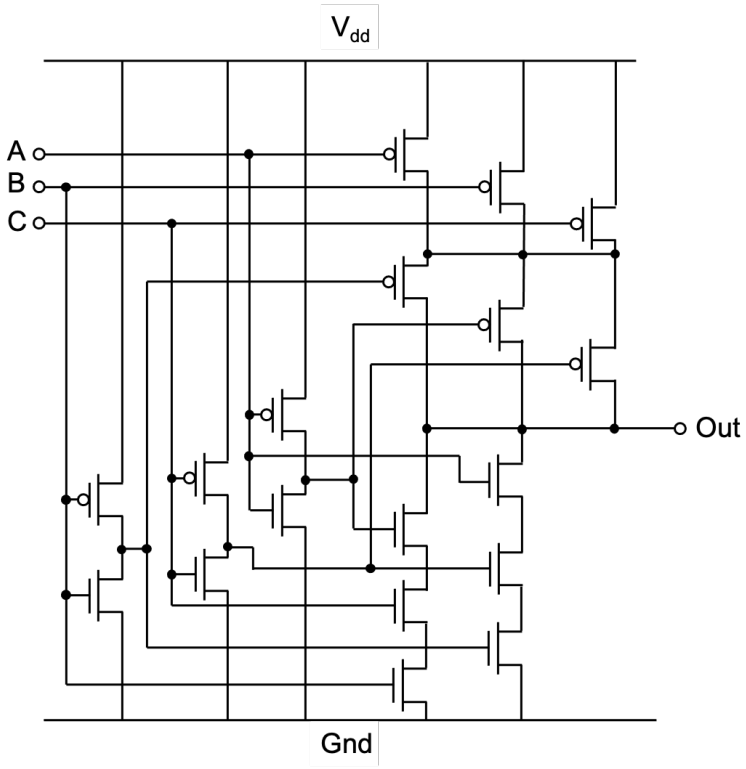
CMOS? (circle one)	Yes No
(if CMOS) Function (Out)	
(if not CMOS) Why not?	Short from Vdd to Gnd for A=B=C=1

(b)



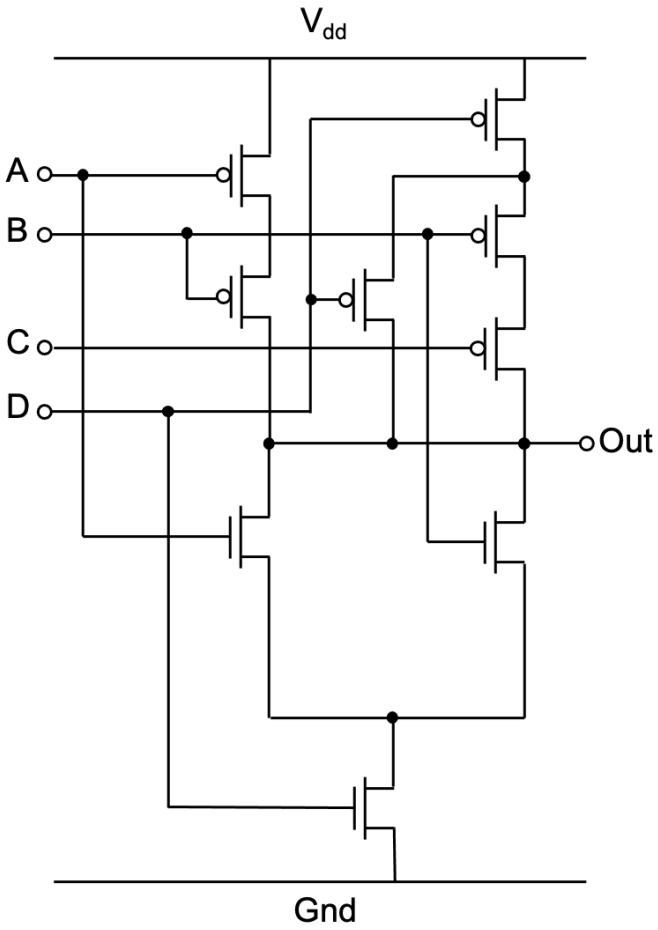
CMOS? (circle one)	Yes No
(if CMOS) Function (Out)	$\overline{Out} = A \cdot B \cdot C + \overline{A} \cdot \overline{B} \cdot \overline{C}$
(if not CMOS) Why not?	

(c)



CMOS? (circle one)	Yes No
(if CMOS) Function (Out)	
(if not CMOS) Why not?	Short from Vdd to Gnd when A=1, B=C=0

2. (25 points) Consider the following circuit:



Assume:

- all transistors are same size.
- all on transistors have resitance R_{on}.
- all transistors have total gate capacitance C_g.

(a) Identify the output function.

$Out = \overline{A} \cdot \overline{B} + \overline{D}$

(b) Lowest resistance driving output?

Case: A=B=C=D=0 Resistance: $\frac{10}{11}R_{on}$

(c) Highest resistance driving output?

Case: A=B=0, C=D=1 Resistance: $2R_{on}$

(d) Lowest capacitance of an input?

Which: C Capacitance: C_g

(e) Highest capacitance of an input?

Which: B, D Capacitance: $3C_g$

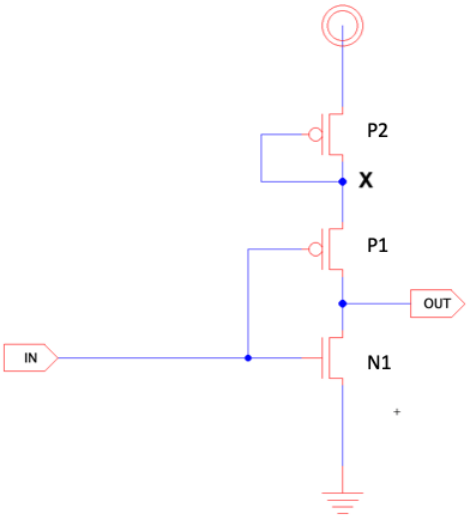
(f) Worst-case 10-90 rise time for one of these gates driving a single input of another of these gates?

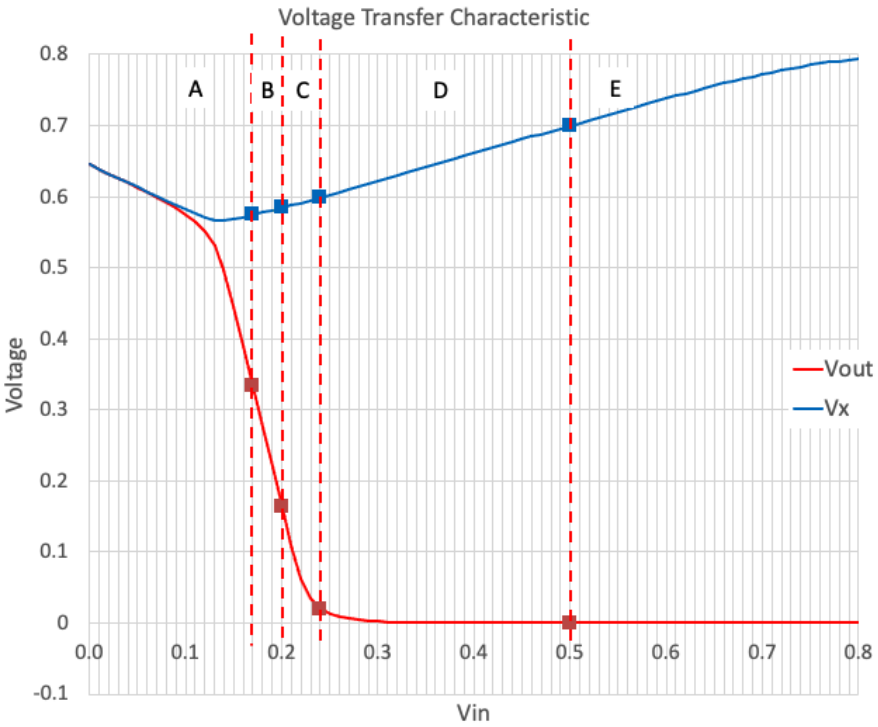
Case: with B=0 ,C=D=1, A:1$\rightarrow$ 0

Rise Time Expression: $2.2 * 2R_{on} * 3C_g = 13.2R_{on}C_g$

[Show calculation for partial credit consideration.]

3. (25 points) Consider the following circuit and its voltage transfer characteristic as well as the voltage at node X. Assume $V_{dd} = 800mV$ and $V_{thn} = -V_{thp} = 200mV$.





For the regions A-E labeled on the transfer function, identify the region of operation of the nMOS and both pMOS devices. Fill out the table below.

	N1	P1	P2
A	Subthreshold	Linear	Saturation*
B	Subthreshold	Saturation	Saturation
C	Saturation	Saturation	Saturation
D	Linear	Saturation	Saturation*
E	Linear	Subthreshold	Saturation*

Subthreshold and Saturation were both accepted.

For reference on the next page are the transistor current models and additional work space if needed:

NMOS:

V_{GS}	V_{DS}	Mode	I_{DS}
$\geq V_{thn}$	$< V_{GS} - V_{thn}$	Linear	$\mu_n C_{ox} \frac{W}{L} \cdot \left((V_{GS} - V_{thn}) \cdot V_{DS} - \frac{V_{DS}^2}{2} \right)$
	$\geq V_{GS} - V_{thn}$	Saturation	$\frac{1}{2} \mu_n C_{ox} \frac{W}{L} \cdot (V_{GS} - V_{thn})^2$
$< V_{th}$		Subthreshold	0

PMOS:

V_{GS}	V_{DS}	Mode	I_{DS}
$\leq V_{thp}$	$> V_{GS} - V_{thp}$	Linear	$\mu_p C_{ox} \frac{W}{L} \cdot \left((V_{GS} - V_{thp}) \cdot V_{DS} - \frac{V_{DS}^2}{2} \right)$
	$\leq V_{GS} - V_{thp}$	Saturation	$\frac{1}{2} \mu_n C_{ox} \frac{W}{L} \cdot (V_{GS} - V_{thp})^2$
$> V_{th}$		Subthreshold	0

4. (25 points) For this problem we consider a new technology that is not necessarily MOS. You can assume $V_{dd} = 1V$ We are told there are two "gates" available to us:

   - P-gate: 1-input gate where:

$$V_{out} = \begin{cases} 1 - 0.5V_{in} & V_{in} < 0.3 \\ 1.6 - 2.5V_{in} & 0.3 \leq V_{in} < 0.6 \\ 0.25 - 0.25V_{in} & 0.6 \leq V_{in} \end{cases} \quad (1)$$

   - Q-gate: 2-input gate where: $V_{out} = |V_A - V_B|$

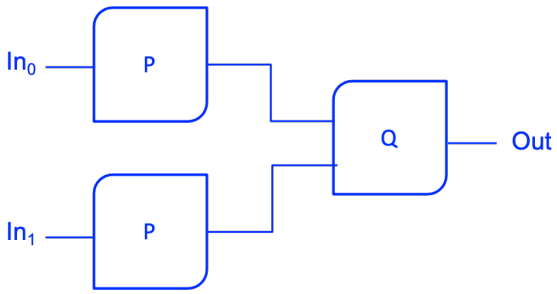
   (a) What logical function does the restoring P-gate perform? Identify the noise margins that will provide restoration for this gate.

   Function: Inverter

V_{OH}	850mV
V_{IH}	600mV
V_{IL}	300mV
V_{OL}	100mV
NM_L	200mV
NM_H	250mV

(b) What logical function does the non-restoring Q-gate perform and is it restoring? Draw a combination of P and Q gates that will serve as a restoring gate that performs the same logic function and identify the noise margins that will provide restoration for this new gate.

Function: XOR



V_{OH}	750mV
V_{IH}	600mV
V_{IL}	300mV
V_{OL}	150mV
NM_L	150mV
NM_H	150mV

V_{IL} and V_{IH} are the inflection points of the P-gates. The outputs of each P-gate will be > 0.85 or < 0.1. The worst-case low output will be when the P-gate outputs are 1 and 0.85, thus $V_{OL} = 0.15$; the worst-case high output will be when the P-gate outputs are 0.1 and 0.85, $V_{OH} = 0.75$