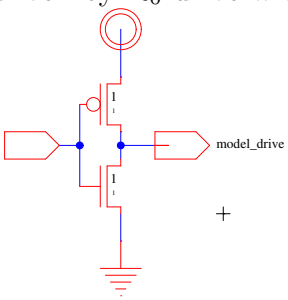
University of Pennsylvania
Department of Electrical and System Engineering
Circuit-Level Modeling, Design, and Optimization for Digital Systems

ESE370, Fall 2021 — Midterm 2 — Wednesday, November 3

- Point values for each problem are denoted in exam. Point breakdown within problems varies.
- Calculators allowed. No smartphones.
- Closed book = No text or notes allowed.
- V_{dd}=1V, $V_{thn} = -V_{thp} = 250$mV, $\mu_n = \mu_p$, $R_{p0} = R_{n0} = R_0$, unless otherwise specified in problem.
- Unless otherwise noted, inputs driven by R_0 drive with self load $2\gamma C_0$.



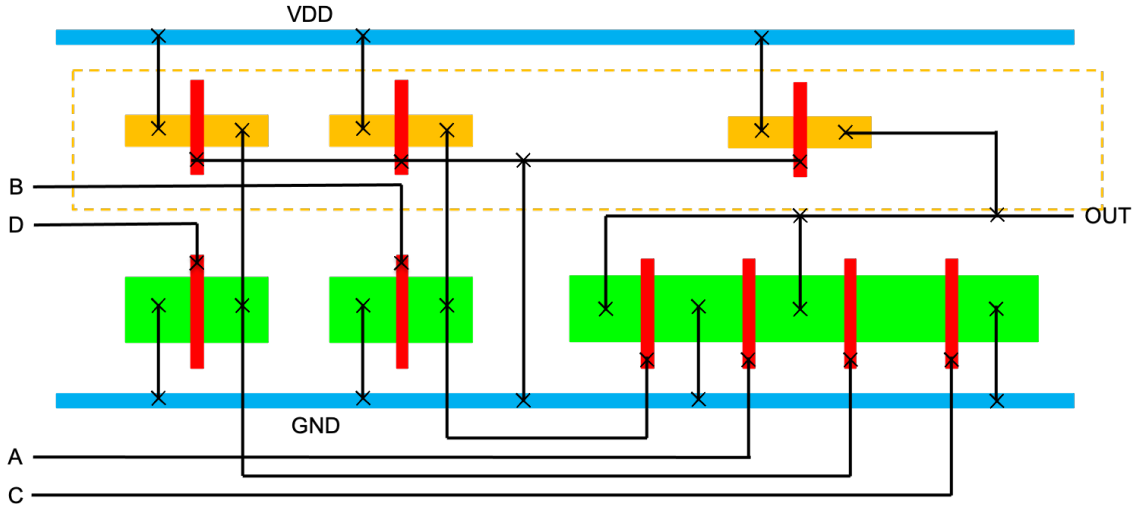
A model for the input driver is:

Name: Answers

Grade:

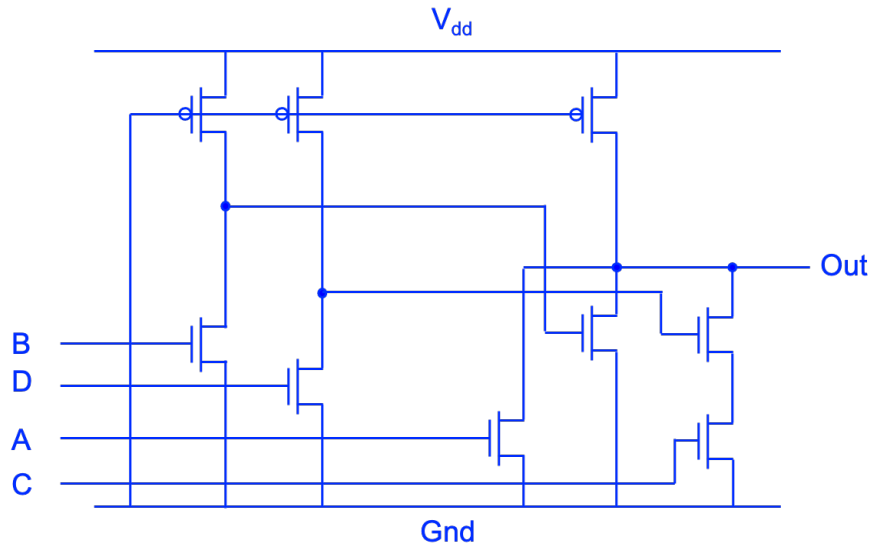
Q1	
Q2	
Q3	
Q4	
Q5	
Total	Mean: 76.5, Stdev: 11.5

1. (10 points) Below is a stick drawing of the layout of a gate. Identify the logic function of the gate and draw the corresponding schematic for this stick diagram. All Xs represent connections between layers or within the same layer



The original stick diagram on the exam had an error on it. Everyone got full credit. Above is the corrected stick diagram.

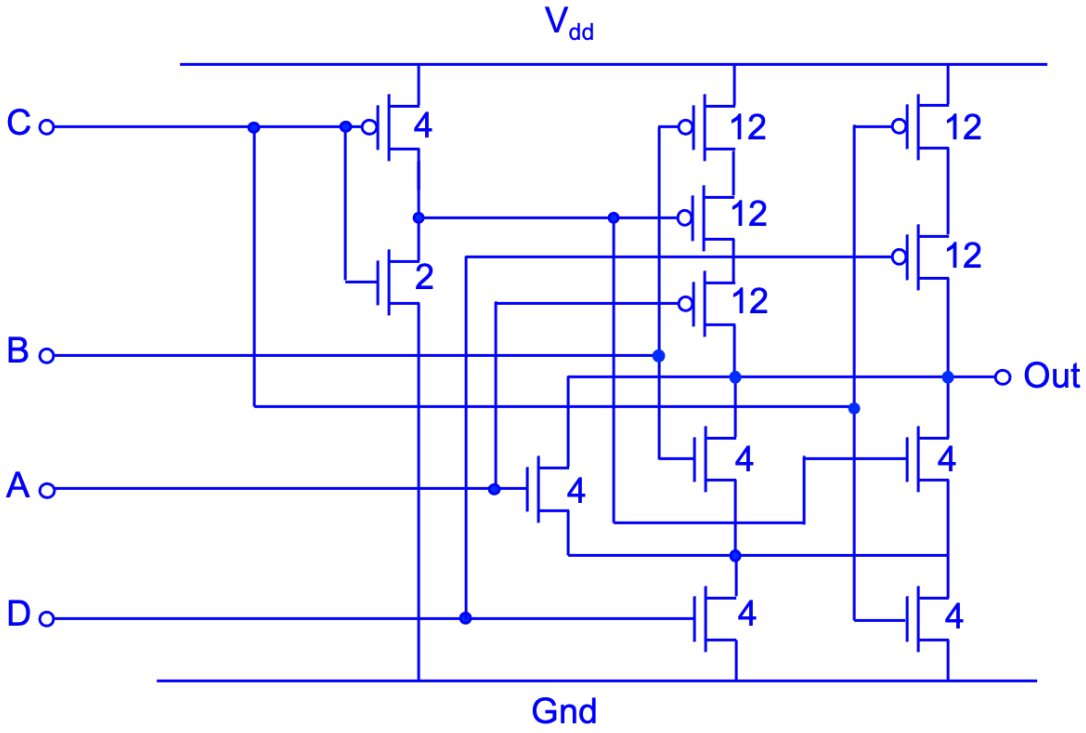
$OUT = B \cdot \overline{A} \cdot (\overline{C} + D)$



2. (20 pts) Assume:

   - $|V_{T_p}| = |V_{T_n}|$
   - R_0=resistance of $W_n = 1$ NMOS transistor
   - μ_n=300 cm$^2/(V \cdot s)$, μ_p=150 cm$^2/(V \cdot s)$ (I.e. $R_{p0} = 2R_{n0}$)
   - C_0 = gate capacitance of $W_n = 1$ transistor
   - C_{diff}=0
   - The output is loaded with a $C_{Load} = 8C_0$
   - All inputs are driven by inverters with an output resistance of $R_0/2$

   Design a CMOS gate for the function $OUT = \overline{A} \cdot \overline{B} \cdot C + \overline{C} \cdot \overline{D}$ with sizes labelled for a worst-case output resistance of $R_0/2$ in each stage. Calculate the worst-case delay in units of τ including driving the inputs and worst case switching energy.



Delay	$(11 + 8 + 4)\tau = 23\tau$
Dynamic Energy	$\frac{1}{2}(6 + 16 \times 5 + 8)C_0V_{dd}^2 = 47C_0$

3. (30pts) Estimate Delay and Switching Energy for the following implementations of a 5-bit priority encoder. An n-bit priority encoder is a circuit with n inputs, A_i, and n outputs, Y_i, where $0 \leq i < n$, such that

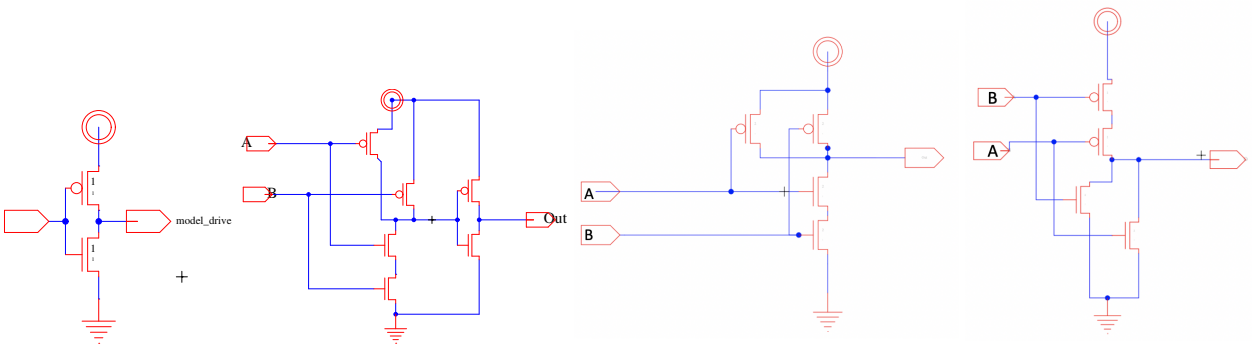
$$Y_i = \begin{cases} 1, & \text{if } A_0 = ... = A_{i-1} = 0 \text{ and } A_i = 1 \\ 0, & \text{otherwise} \end{cases}$$

Informally, a priority encoder identifies the first in the sequence of input bits with value 1. The truth table for a 5-bit priority encoder is given below (for compactness a $*$ indicates either 0 or 1).

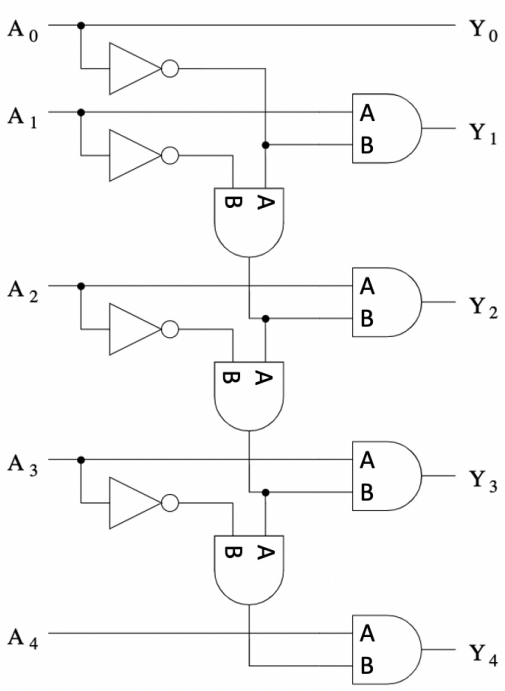
Inputs					Outputs				
A_0	A_1	A_2	A_3	A_4	Y_0	Y_1	Y_2	Y_3	Y_4
0	0	0	0	0	0	0	0	0	0
0	0	0	0	1	0	0	0	0	1
0	0	0	1	$*$	0	0	0	1	0
0	0	1	$*$	$*$	0	0	1	0	0
0	1	$*$	$*$	$*$	0	1	0	0	0
1	$*$	$*$	$*$	$*$	1	0	0	0	0

For the rest of the problem assume:

- Inverter, and2, nand2, and nor2 schematics given below.
- All transistors W=L=1.
- Give answers in terms of τ and γ; $\gamma = C_{diff}/C_{gate}$.
- Assume all inputs arrive at the same time and are driven by R_0 drive with $2\gamma C_0$ self load.
- The load on each of the outputs is $8C_0$.



(a) Below is a daisy chain implementation of the 5-bit priority encoder:



Report worst-case delay for the 5-bit priority encoder from the R_0 input driver driving the inputs through driving the $8C_0$ load on each Y_i in units of τ and the worst-case dynamic switching energy. Show individual stage delays for partial credit.

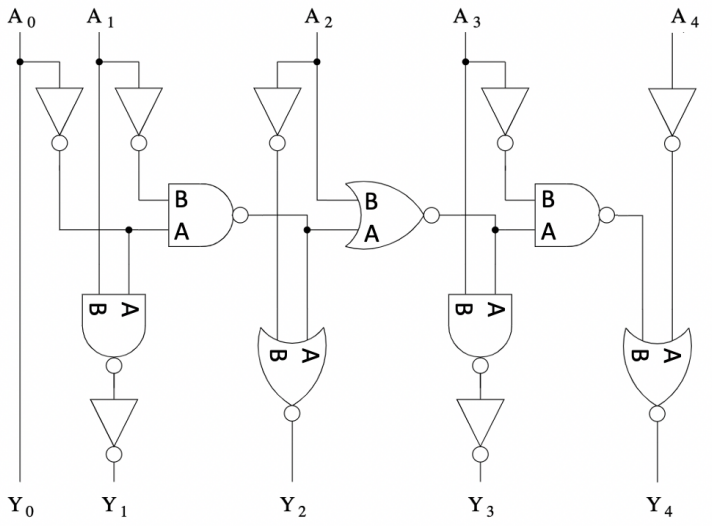
Delay	$(38\gamma + 48)\tau$
Dynamic Energy	$\frac{1}{2}(66 + 57\gamma)C_0V_{dd}^2 = (33 + 35.5)C_0$

Stage	Delay
Driving Input A_0	$R_0(2\gamma + 10)C_0$
A0 Inv	$R_0(2\gamma + 4)C_0$
stg1 And	$2R_0(3\gamma + 2)C_0 + R_0(2\gamma + 4)C_0$ (input B for And discharges 2γ in Nand early)
stg2 And	$2R_0(3\gamma + 2)C_0 + R_0(2\gamma + 4)C_0$ (input B for And discharges 2γ in Nand early)
stg3 And	$2R_0(3\gamma + 2)C_0 + R_0(2\gamma + 2)C_0$ (input B for And discharges 2γ in Nand early)
stg4 And on Y4	$R_0(5\gamma + 2)C_0 + R_0(3\gamma + 2)C_0 + R_0(2\gamma + 8)$ (Must discharge 2γ for this one)
Sum	$(38\gamma + 48)\tau$

including inputs (OK if you didn't), 4 inverters, 7 and gates, and at most 2 outputs switching

$C_{sw} = 5 * 2\gamma + 4 * (2 + 2\gamma)C_0 + 7 * (7\gamma + 6)C_0 + 2 * 8C_0 = (66 + 67\gamma)C_0$

(b) Below is an inverting daisy chain implementation of the 5-bit priority encoder:



Report worst-case delay for the 5-bit priority encoder from the R_0 input driver driving the inputs through driving the $8C_0$ load on each Y_i in units of τ and the worst-case dynamic switching energy. Show individual stage delays for partial credit.

Delay	$(30\gamma + 50)\tau$
Dynamic Energy	$\frac{1}{2}(58 + 59\gamma)C_0V_{dd}^2 = (29 + 29.5)C_0$

Stage	Delay
Driving Input A_0	$R_0(2\gamma + 10)C_0$
A0 Inv	$R_0(2\gamma + 4)C_0$
stg1 Nand	$2R_0(3\gamma + 4)C_0$ (input B discharges 2γ in Nand early)
stg2 Nor	$2R_0(3\gamma + 4)C_0$ (input B charges 2γ in Nor early)
stg3 Nand	$2R_0(3\gamma + 2)C_0$ (input B discharges 2γ in Nand early)
stg4 Nor on Y4	$R_0(5\gamma + 8)C_0 + R_0(3\gamma + 8)C_0$ (Must discharge 2γ for this one)
Sum	$(30\gamma + 50)\tau$

including inputs (OK if you didn't), 7 inverters, 4 nand gates, 3 nor gates, and at most 2 outputs switching

$C_{sw} = 5 * 2\gamma + 7 * (2 + 2\gamma)C_0 + 7 * (5\gamma + 4)C_0 + 2 * 8C_0 = (58 + 59\gamma)C_0$

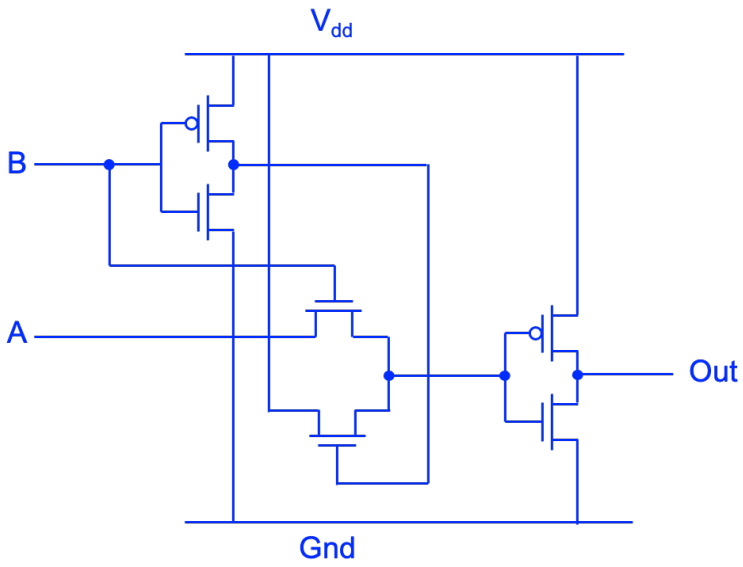
4. (20 points) Pass transistor logic.

   For this problem assume:

   - $|V_{T_p}| = |V_{T_n}|$
   - R_0=resistance of $W_n = 1$ NMOS transistor
   - R_{0p}=R_{0n}=resistance of $W_p = 1$ PMOS transistor
   - C_0 = gate capacitance of $W_n = 1$ transistor
   - C_0 = gate capacitance of $W_p = 1$ transistor
   - $C_{diff} = \frac{1}{2}C_0$
   - All inputs arrive simultaneously

   (a) Design a nor2 gate with restoration using pass transistor logic and CMOS inverters while minimizing area (i.e use as few transistors as possible).

   This was left open-ended and many answers were accepted. Below is just one possibility.



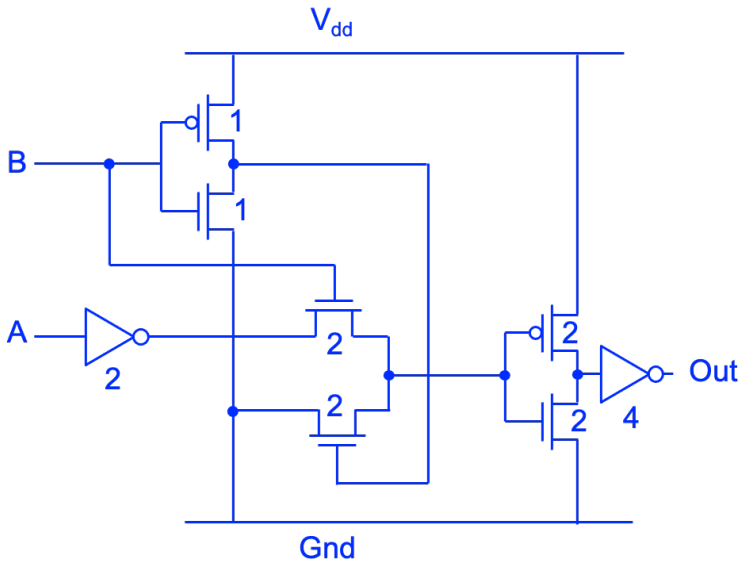
   (b) Assuming all transistors are minimum size, estimate the delay in units of τ of your nor2 gate assuming the inputs are driven by minimum size inverters and your output is loaded by $18C_0$.

$$R_0(2\gamma+3)C_0 + R_0(2\gamma+1)C_0 + R_0(2\gamma+2)C_0 + R_0(2\gamma+18)C_0 \quad (1)$$

$$4\tau + 2\tau + 3\tau + 19\tau = 28\tau \quad (2)$$

(c) Modify your design to reduce the delay (try for 20-50%). Show your new design with transistor sizes specified and report new delay in units of τ.

Looking at the delay equation, we see we need to reduce the load delay. We can do this by sizing the pass transistors and restoring inverter, but the minimum size input driver limits how much delay we can reduce. So we add an inverter on the A input and add an inverter on the output sized as below. We also have to change the bottom pass transistor input to ground for correct logic operation.



$$R_0(2\gamma+4)C_0 + R_0(2\gamma+2)C_0 + \frac{R_0}{2}(4\gamma+4)C_0 + \frac{R_0}{2}(4\gamma+8)C_0 + \frac{R_0}{4}(8\gamma+18)C_0 \quad (3)$$

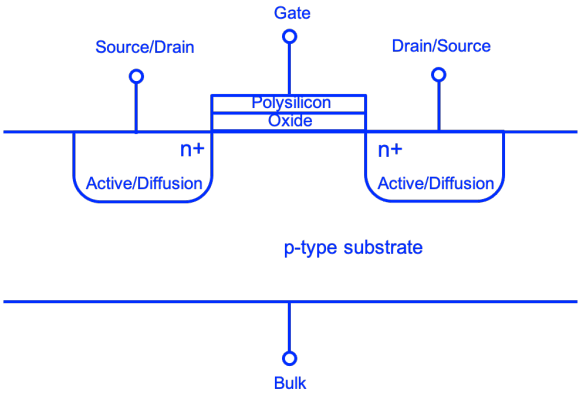
$$\tau(5+3+3+5+5.5) = 21.5\tau \quad (4)$$

5. (20 pts) Short Answer Questions: Answer the questions briefly. Include diagrams and equations as needed. Be clear in your explanation and handwriting.

A What effect does increasing V_{th} have on leakage energy? Explain your answer.

Increasing V_{th} decreases current levels and so there is less leakage current resulting in a lower leakage energy in steady-state.

B Draw the cross section of a fabricated nMOS device. Label all terminals and indicate the different layers.



C A ratioed logic nor2 and nand2 with nMOS PDN and load pMOS device are sized to have the same drive strength. Which one would take more area and why?

The nand2 would take more area because it would have series transistors in the nMOS PDN so they would have to be sized larger to have the same worst case equivalent drive strength as the nor2, which has nMOS devices in series in the PDN.

D What is velocity saturation and when does it occur?

Velocity saturation occurs in a MOSFET device with a small channel length, L, with a large gate voltage creating a large e-field across the oxide layer. This results in an upper bound on velocity or charge particles in the device thus saturating the current level and resulting in a linear dependence between gate voltage and current instead of a quadratic dependence.

E How do you measure propagation delay? Use figures and equations to help explain your answer.

Propagation delay, τ_p, is the average of the τ_{PLH} and τ_{PHL}, which are measured from the 50% point of the input to the 50% point on the output as indicated on the figure below.