ESE370: Circuit-Level Modeling, Design, and Optimization for Digital Systems

Lec 11: March 1, 2023

Ratioed Logic and Design-Space Exploration

Penn

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Today

- Ratioed Logic
  - Break all the rules… (lose our nice properties)
    - Not rail-to-rail signals, steady-state-current…
  - Correctness

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Ratioed Logic

Penn

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Previously

- Restoration and Noise Margins
  - Allows for gate abstraction
- CMOS Gates
  - Drive outputs rail-to-rail
  - Only one PDN/PUN turned on in steady state
    - Only subthreshold leakage current in steady state

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Today

- Ratioed Gates
  - Break all the rules… (nice properties)
    - No rail-to-rail outputs, steady-state-current is not subthreshold…
  - Logic correctness
  - Performance
  - Power implications

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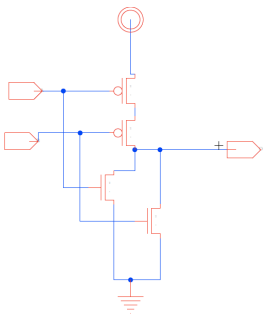
Idea

- Building both pull-up and pull-down can be expensive – many gates
- Seems wasteful to build logic function twice
  - Once in pullup, once in pulldown
  - Large gate capacitance



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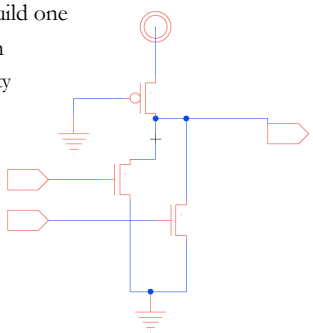
Idea

- Maybe only need to build one
- Build NFET pulldown
  - Exploit high N mobility
    - traditional



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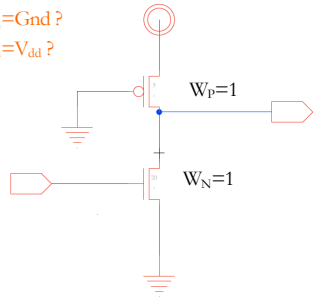
Ratioed Inverter

- Does this work?
  - What is V_{out} for V_{in}=Gnd ?
  - What is V_{out} for V_{in}=V_{dd} ?



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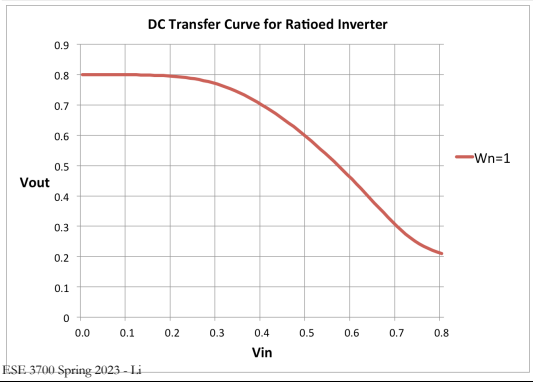
Ratioed Inverter in 22nm



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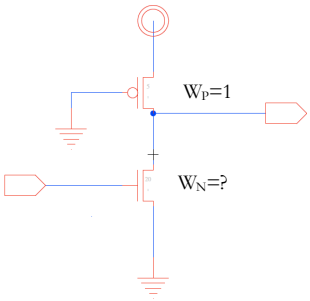
Ratioed Inverter (Preclass 1)

- How do we need to size N to make it "work"?
  - V_{DD}=0.8



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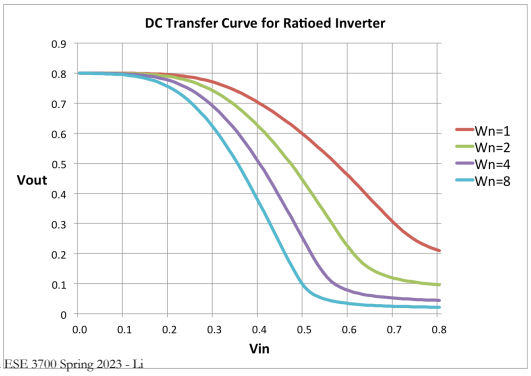
Ratioed Inverter in 22nm



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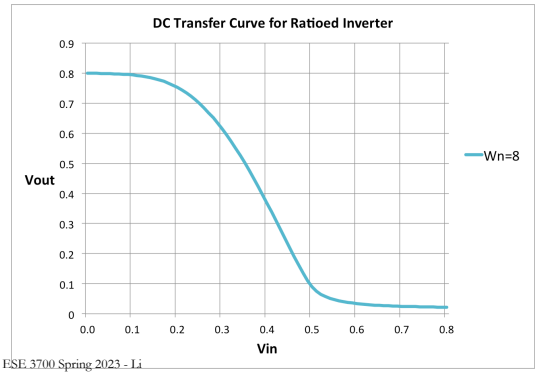
DC Transfer Function



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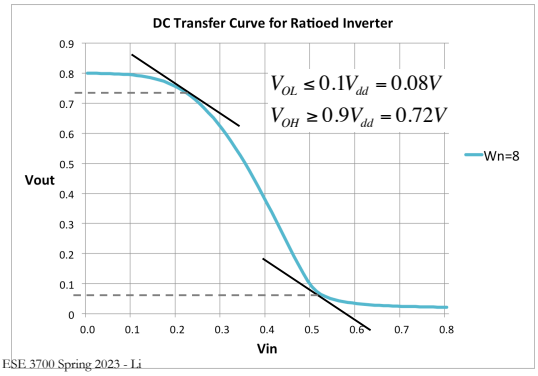
DC Transfer Function



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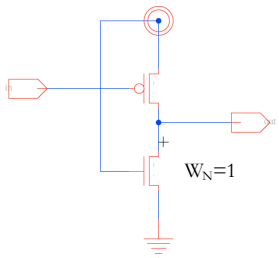
Ratioed Inverter (Preclass 1)

- How do we need to size P to make it work?
  - V_{DD}=0.8



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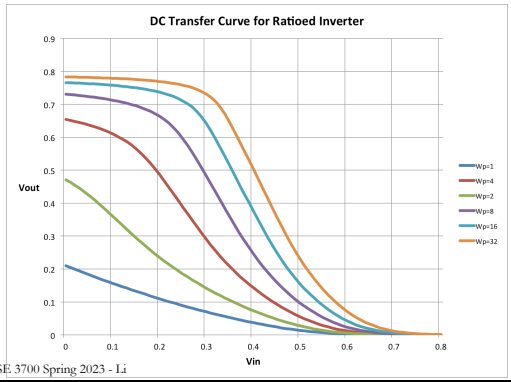
Ratioed Inverter in 22nm



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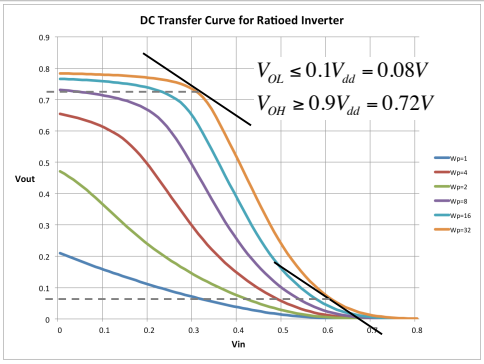
Ratioed Inverter in 22nm



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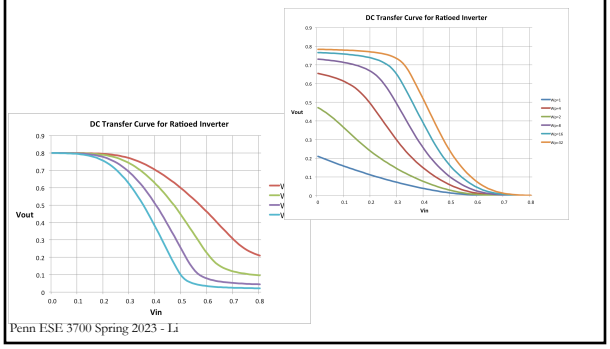
P vs. N

- **Conclude:** still prefer N to P for ratioed logic



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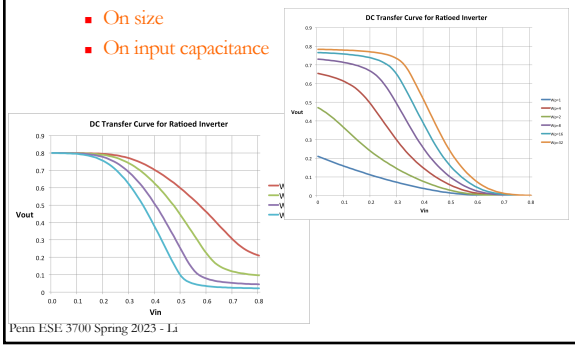
Noise Margin Tradeoff

- What is impact of increasing noise margin?
  - On size
  - On input capacitance



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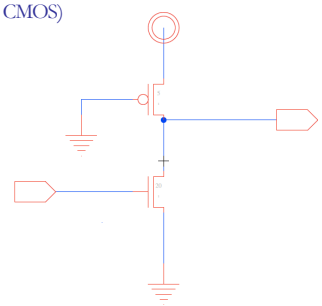
Size for $R_0/2$ drive?

- How do we size for $R_0/2$ drive?
  - (assume $R_{0p}=R_{0n}$ for CMOS)



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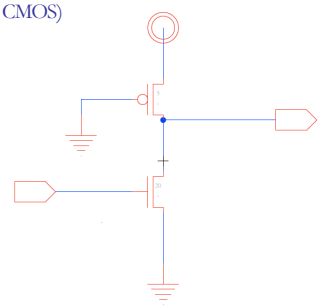
Size for $R_0/2$ drive? (Preclass 2)

- How do we size for $R_0/2$ drive?
  - (assume $R_{0p}=R_{0n}$ for CMOS)

$$R_{drive} = \frac{R_{op}}{W_p} = \frac{R_0}{W_p} = \frac{R_0}{2}$$

$$\Rightarrow W_p = 2$$



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Size for $R_0/2$ drive?

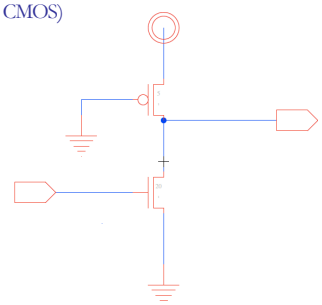
- How do we size for $R_0/2$ drive? What is Cin?
  - (assume $R_{0p}=R_{0n}$ for CMOS)

$$R_{drive} = \frac{R_{op}}{W_p} = \frac{R_0}{W_p} = \frac{R_0}{2}$$

$$\Rightarrow W_p = 2$$

$$W_n > 8W_p$$

$$\Rightarrow W_n = 16$$



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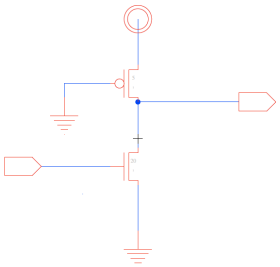
Static Power

- I_{static} ?
- Input low-Output high?
  - I_{leak}
- Input high-Output low?
  - I_{pmos_on}
  - ~$V_{dd}/(R_0/2)$ -- for our sample case



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Total Power

- $P_{tot} \approx a(C_{load} + 2C_{sc})V^2f$

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Total Power

- $P_{tot} \approx a(C_{load} + 2C_{sc})V^2f$
  $+ p(V_{out}=low)V^2/R_{pon}$
  $+ p(V_{out}=high)VI'_s(W/L)e^{-Vt/(nkT/q)}$

$p(V_{out}=low)$ – probability the output is low
$p(V_{out}=high)$ – probability the output is high

$p(V_{out}=high)=1-p(V_{out}=low)$

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Compare Static CMOS

For $R_{drive}=R_0/2$ inverter (assume $R_{0p}=R_{0n}$ for CMOS)

- Total Transistor Width?
- Input capacitance load?

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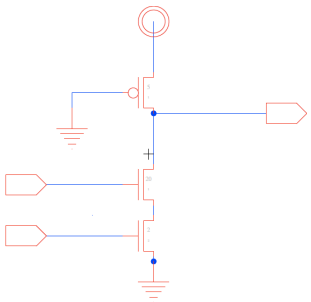
How do we size for $R_0/2$ drive?

- 2-input nand?



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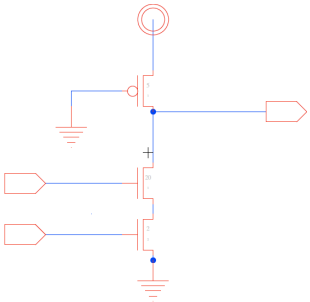
How do we size for $R_0/2$ drive?

- 2-input nand?

$$R_{drive} = \frac{R_{op}}{W_p} = \frac{R_0}{W_p} = \frac{R_0}{2}$$
$$\Rightarrow W_p = 2$$



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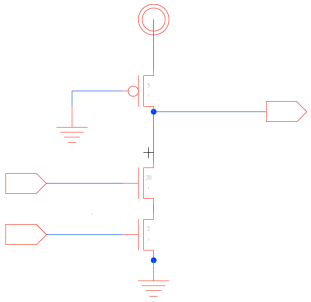
How do we size for $R_0/2$ drive?

- 2-input nand? What is C_{in}?

$$R_{drive} = \frac{R_{op}}{W_p} = \frac{R_0}{W_p} = \frac{R_0}{2}$$
$$\Rightarrow W_p = 2$$

$$R_{drive,pdn} = \frac{2R_0}{W_n} = \frac{R_0}{W_n/2}$$
$$W_n/2 > 8W_p$$
$$\Rightarrow W_n = 32$$



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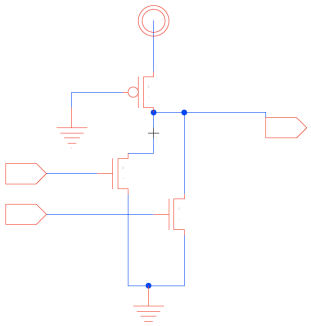
How do we size for $R_0/2$ drive?

- 2-input nor?



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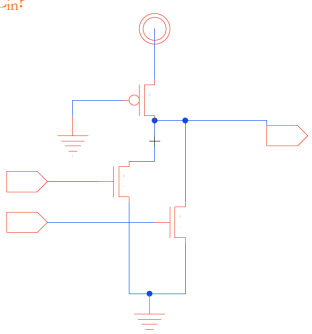
How do we size for $R_0/2$ drive?

- 2-input nor? What is C_{in}?

$$R_{drive} = \frac{R_{op}}{W_p} = \frac{R_o}{W_p} = \frac{R_o}{2}$$
$$\Rightarrow W_p = 2$$

$$W_n > 8W_p$$
$$\Rightarrow W_n = 16$$



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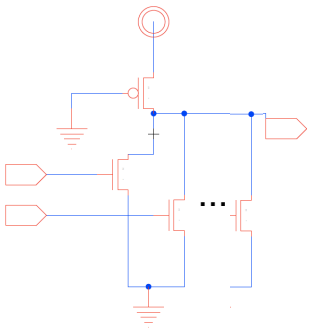
How do we size for $R_0/2$ drive? (Preclass 3)

- k-input nor?
- What is the input capacitance for k-input nor?



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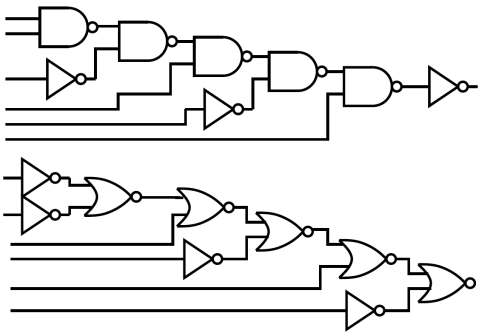
Which Implementation is faster in ratioed logic?



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Design Space Exploration

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Design Problem

- Function: Identify equivalence of two 32bit inputs
- Optimize: Minimize total energy
- Assumptions: Match case uncommon
  - Ie. Most of the time, the inputs won't be matched
- Deliberately focus on Energy to complement project
  - …but will still talk about delay

Last page of preclass

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Idea: Design Space Explore

- Identify options
  - All the knobs you can turn
- Explore space systematically
- Formulate continuum where possible
  - i.e. formulate trends and tradeoffs quantitatively

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Problem Solvable (preclass 4.1)

- Is it feasible?
  - First, make sure we have a solution so we know our main goal is optimization
- How do we decompose the problem?

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Problem Solvable (preclass 4.2)

- Is it feasible?
  - First, make sure we have a solution so we know our main goal is optimization
- How do we decompose the problem?
- What look like built out of nand2 gates and inverters?

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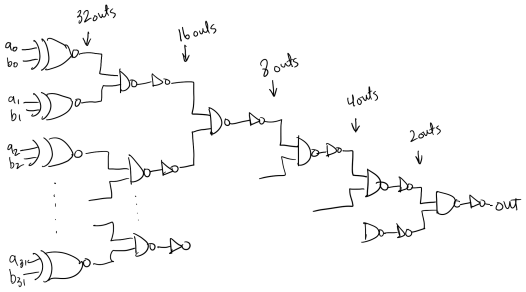
Nand2 and inverter implementation



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Single Gate Match Condition (preclass 4.3)

- Design a single gate for match comparison

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Total Power

- Static CMOS:
  - $P_{tot} \approx a(C_{load}+2C_{sc})V^2f+VI_s(W/L)e^{-Vt/(nkT/q)}$
- Ratioed Logic:
  - $P_{tot} \approx a(C_{load}+2C_{sc})V^2f$
    $+p(V_{out}=low)V^2/R_{pon}$
    $+(1-p(V_{out}=low))VI_s(W/L)e^{-Vt/(nkT/q)}$
- What can we do to reduce power?

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Knobs (preclass 4.4)

- What are the options and knobs we can turn?

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Design Space Dimensions

- Topology
  - (A) Gate choice, logical optimization
  - (B) Fanin, fanout, (C) Serial vs. parallel
- Gate style / logic family
  - (D) CMOS, Ratioed (N load, P load)
- (E) Transistor Sizing
- (F) Vdd
- (G) Vth

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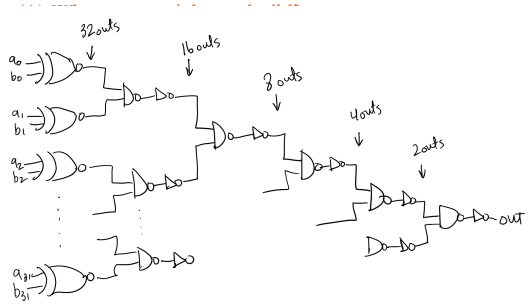
Gate



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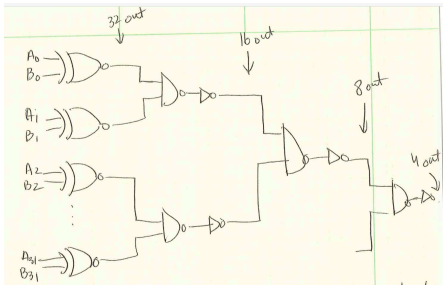
Gate Choice

- (A) What gates might we build?



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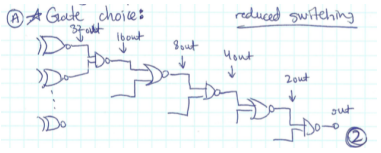
Gate Choice

- (A) What gates might we build?



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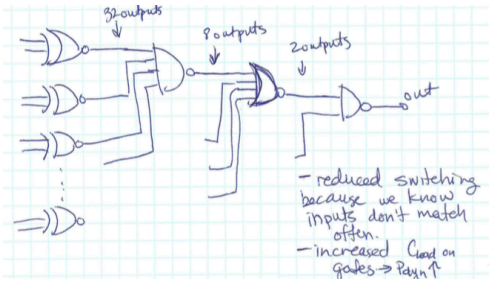
Gate Fan-in

- (B) High fan-in?



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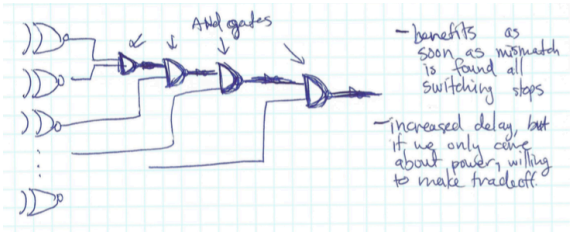
Gate Topology

- (C) Serial-Parallel?



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(D) Logic Family

- Considerations for each logic family?
  - CMOS
  - Ratioed with PMOS load
  - Ratioed with NMOS load
- Ratioed Logic
  - Reduced C_{loads} result in lower switching power (P_{dyn} ↓)
  - Increased static power

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(E) Sizing

- How do we want to size gates?
  - Sizing transistors up will reduce delay →
    - Reduces short circuit power

$$E = V_{dd} \times \left(I_{peak} \times t_{sc} \times \left(\frac{1}{2} \right) \right)$$

    - Increases dynamic power

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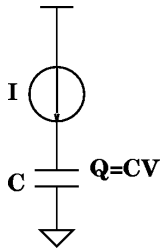
(F) Reduce Vdd

- What happens as reduce V?
  - Energy?
    - Dynamic ↓
    - Static ↓
  - Switching Delay? ↑
- $\tau_{gd}=Q/I=(CV)/I$
- $I_d=(\mu C_{OX}/2)(W/L)(V_{gs}-V_{TH})^2$
- τ_{gd} impact?
- $\tau_{gd} \propto 1/V$
- Limit on Vdd?



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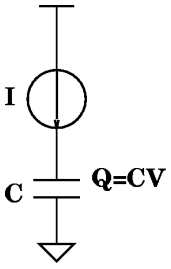
(G) Increase V_{th}?

- What is impact of increasing threshold on
  - Dynamic Energy? ↓
  - Leakage Energy? ↓
  - Delay? ↑
- $\tau_{gd}=Q/I=(CV)/I$
- $I_{ds}=(v_{sat}C_{OX})(W)(V_{gs}-V_{TH}-V_{DSAT}/2)$



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Ideas

- There are other logic disciplines
- You have the tools to analyze
- Ratioed Logic
  - Tradeoff noise margin for
    - Reduced area? Capacitive load?
  - Dissipates non-leakage static power in one input case
- We know many things we can do to our circuits
- Design space is large
- Systematically identify dimensions
- Identify continuum (trends) tuning when possible
- Watch tradeoffs …but don't over-tune

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Admin

- Project 1 out now
  - Design 8-bit ripple-carry adder
    - You already know how to do this
    - Refresh yourself on binary addition of 2 bits
  - Work individually
  - Full Report due F 3/24
- No in-class lecture (3/13)
  - Monday (after spring break)
  - Work on your project

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Acknowledgement

- Prof. André DeHon (University of Pennsylvania)
- Prof. Tania Khanna (University of Pennsylvania)

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