ESE370: Circuit-Level Modeling, Design, and Optimization for Digital Systems

Lec 12: March 15, 2023
Design Space Exploration (con't)
Pass Transistor Logic

Penn

1

Today

- Pass Transistor Logic
- Pass Transistor Circuit
  - $C_{diff}>0$
  - Output levels
  - Cascading
    - Series pass transistors?
    - Delay

2

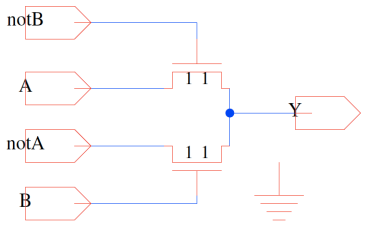
Pass Transistor Logic

Penn

3

Pass Transistor Logic (Preclass 1)

- What does this do?

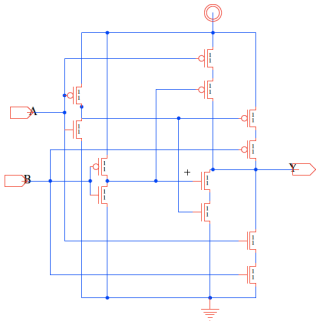


A	B	Y
0	0	
0	1	
1	0	
1	1	

4

Identify Function (Preclass 2)

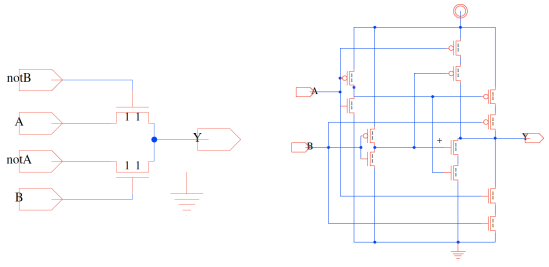
- What function is this?



5

Area

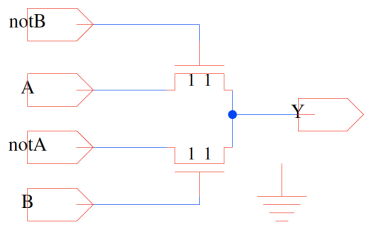
- Compare PT with CMOS circuit?



6

Output

- Is this a regenerating/restoring gate?

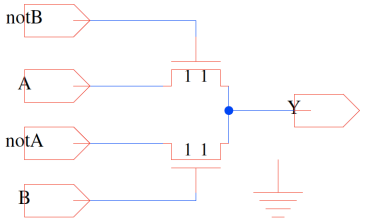


A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

7

Output

- What does output look like (DC transfer)?
  - (B=1, notB=0, sweep A, notA=CMOS inv(A))



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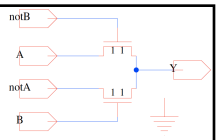
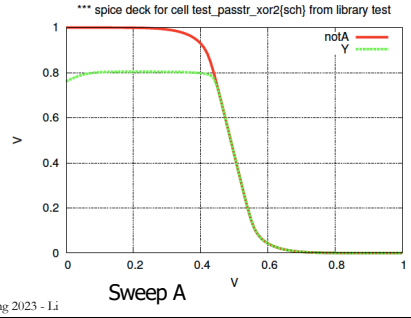
Pass TR transfer (B=1)





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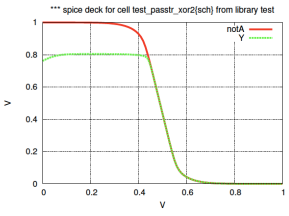
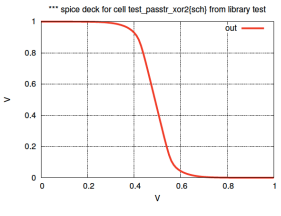
XOR Output

- Reasonable Input to CMOS Inverter?





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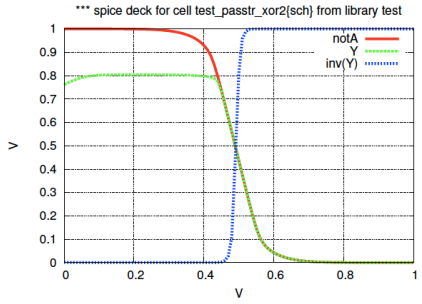
Pass Transistor xor2 with inv restore



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Required to use?

- What should we add to make suitable comparison with CMOS?

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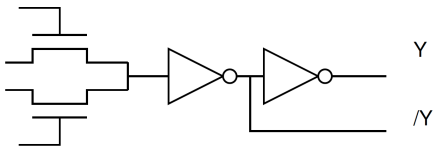
Restore Output

- What should we add to make suitable comparison with CMOS?



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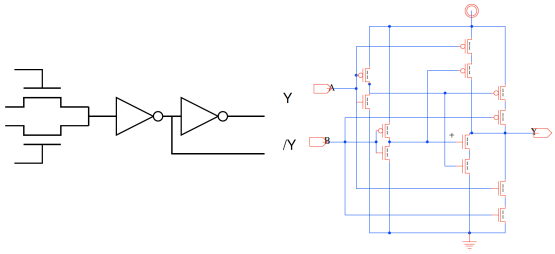
Restore Output

- Area? (compare to CMOS)



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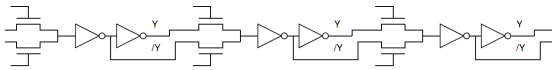
Chain Together



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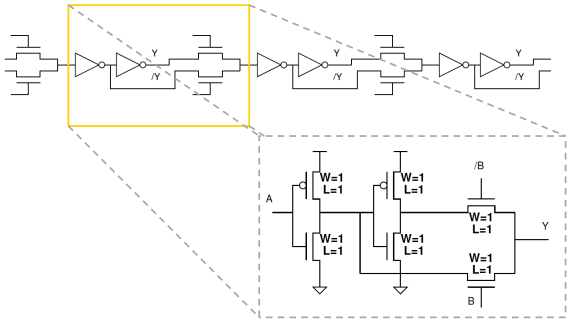
Analyze Stage



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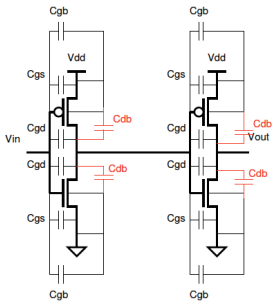
Impact of Capacitance

- $C_{GS}=C_{GCS}+C_{GSO}$
- $C_{GD}=C_{GCD}+C_{GDO}$
- $C_{GB}=C_{GCB}$
- $C_{SB}=C_{diff}$
- $C_{DB}=C_{diff}$



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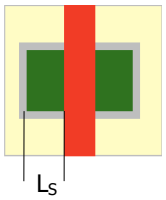
Contact/Diffusion Capacitance

- C_j – diffusion depletion
- C_{jsw} – sidewall capacitance
- L_S – length of diffusion



$$C_{diff} = C_j L_S W + C_{jsw}(2L_S + W)$$

Define: $C_{diff\,0} \approx \gamma C_0$

$$C_{diff} \approx WC_{diff\,0} = W \cdot \gamma C_0$$

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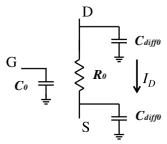
First Order Model



- Switch
  - Loads all terminals capacitively
    - Draw no steady-state current for a CMOS gate
    - Does not impact steady-state output voltage
    - Impacts Settling time/Delay
  - Has finite drive strength
    - Could form voltage divider with resistive load
    - Impacts Settling time/Delay

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First Order Delay

- R_0 = Resistance of minimum size NMOS device
- C_0 = gate capacitance of minimum size NMOS device
- C_{diff0} = diffusion capacitance on minimum size NMOS
  - $C_{diff0} = \gamma C_0$
- $R_{drive} = R_0/W$
- $C_g = WC_0$
- $C_{diff} = WC_{diff0} = \gamma WC_0$

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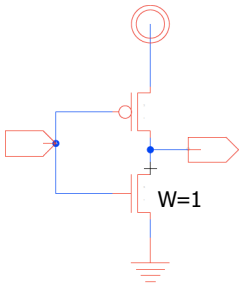
Inverter Delay

- Delay driving another (min size) inverter?
  - Include $C_{diff} = \gamma C_g = \gamma WC_0$



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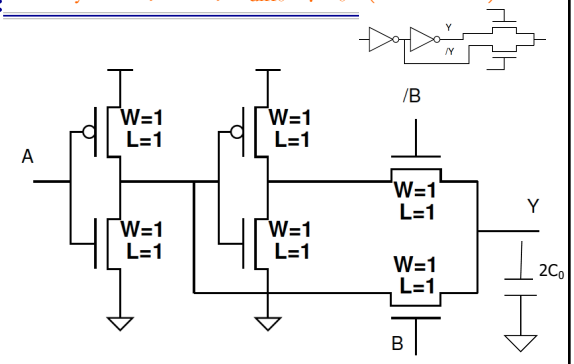
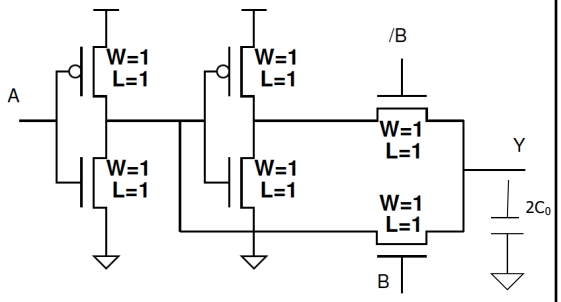
Delay A=1, B=0, $C_{diff0}=\gamma C_0$? (Preclass 3)



22

Delay A=1, B=0, $C_{diff0}=\gamma C_0$? (Preclass 3)

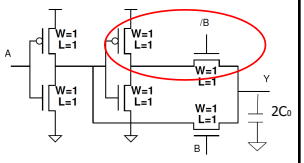
- What's the equivalent RC circuit?



23

Delay A=1, B=0, $C_{diff0}=\gamma C_0$? (Preclass 3)

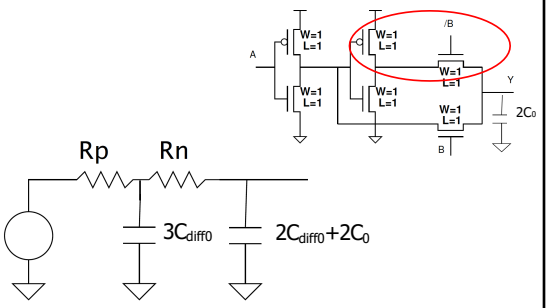
- What's the equivalent RC circuit?



24

Delay A=1, B=0, $C_{diff0}=\gamma C_0$? (Preclass 3)

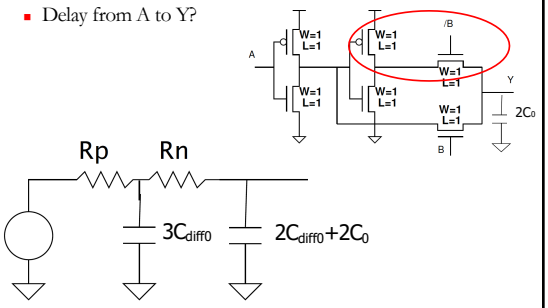
- What's the equivalent RC circuit?



25

Delay A=1, B=0, $C_{diff0}=\gamma C_0$? (Preclass 3)

- What's the equivalent RC circuit?
  - Delay from A to Y?



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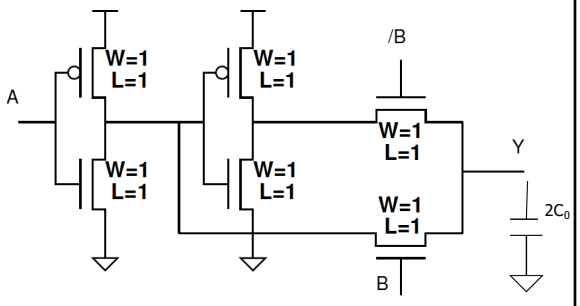
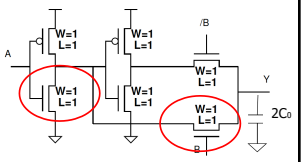
Delay A=1, B=1, $C_{diff0}=\gamma C_0$? (Preclass 3)



27

Delay A=1, B=1, $C_{diff0}=\gamma C_0$? (Preclass 3)

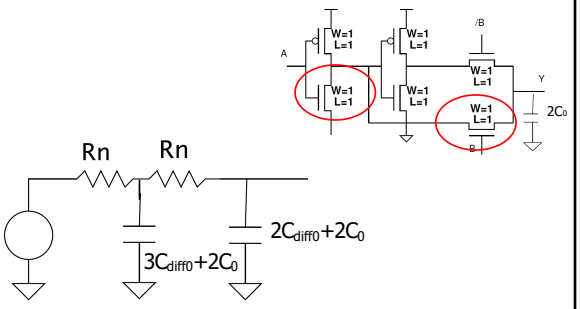
- What's the equivalent RC circuit?



28

Delay A=1, B=1, $C_{diff0}=\gamma C_0$? (Preclass 3)

- What's the equivalent RC circuit?



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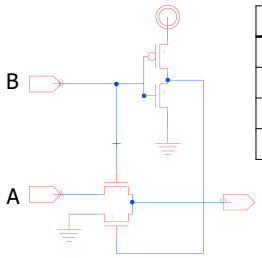
Bonus

- What does this do?



A	B	Y
0	0	
0	1	
1	0	
1	1	

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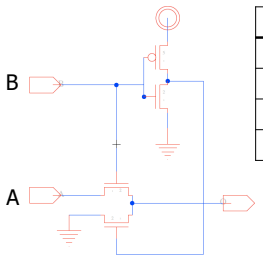
Bonus

- What does this do?



A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

More examples in the text

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Cascading Pass Transistors

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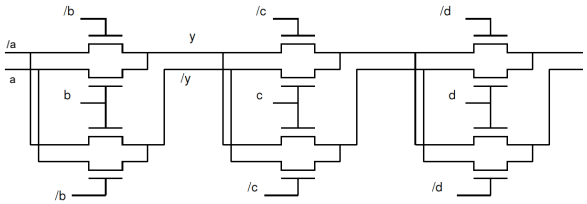
Chain without Inverters

- What if we did this?



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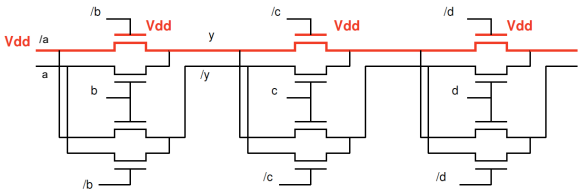
Chain without Inverters

- Extract key path



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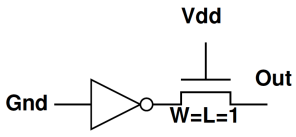
Voltage of Chain (Preclass 4)

- What is voltage at output?

V_{dd}=1V
V_{thn}=-V_{thp}=0.3V



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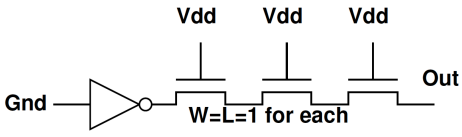
Voltage of Chain (Preclass 4)

- What is voltage at output?

V_{dd}=1V
V_{thn}=-V_{thp}=0.3V



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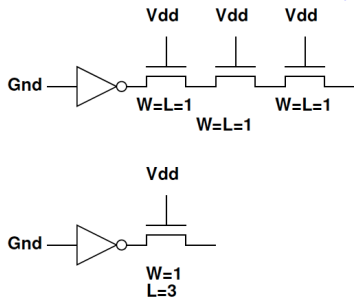
How compare (Preclass 4)

- Compare

V_{dd}=1V
V_{thn}=-V_{thp}=0.3V



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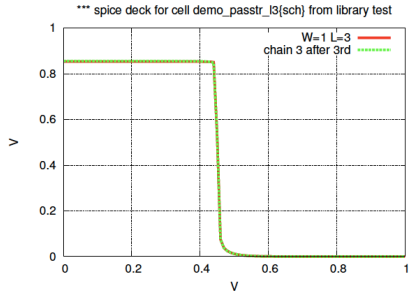
DC Analysis – chain of 3 vs length of 3



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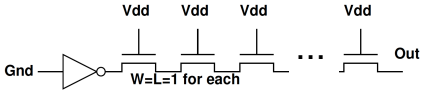
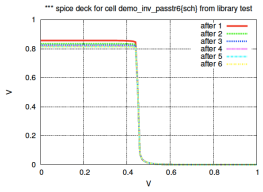
Conclude

- Can chain any number of pass transistors and only drop a single V_{th}





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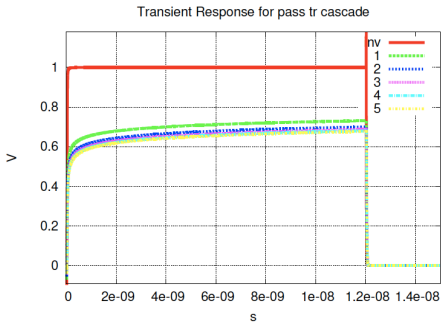
Transient



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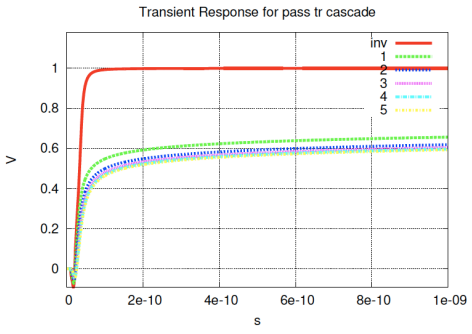
Transient: Zoomed Closeup



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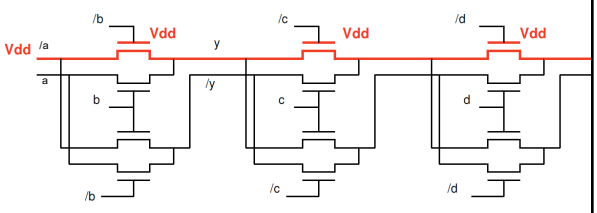
Capacitance

- What is output capacitance per stage?
  - I.e. What is the capacitance at output y?



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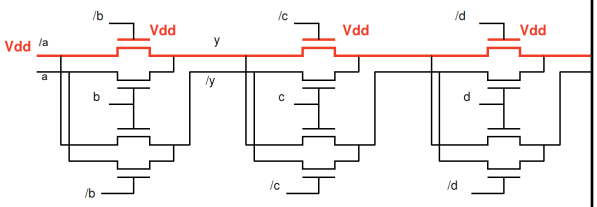
Delay Setup

- What does RC circuit look like?



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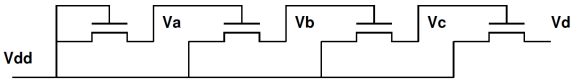
Gate Cascade? (Preclass 5)

- What are the voltages?

V_{dd}=1V
V_{thn}=-V_{thp}=0.3V



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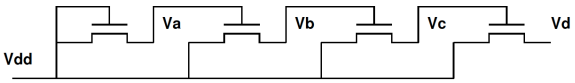
Conclude

- Cannot cascade degraded inputs into **gates**.



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Idea

- There are other circuit disciplines
- Can use pass transistors for logic
  - Even chains of pass transistors
  - Mostly gives area win, sometimes gives delay win
    - Will talk more about delay on Wednesday
- Do not cascade as easily as CMOS

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Admin

- Project 1 out now
  - Design 8-bit ripple-carry adder
    - You already know how to do this
    - Refresh yourself on binary addition of 2 bits
  - Work individually
  - Full Report due F 3/24
  - **Can't pass the class if you don't turn in projects**
    - **Can't do project last minute**

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Logic Types

- CMOS Gates
  - Dual pull-down and pull-up networks, only one enabled at a time
  - Performance of gate is strong function of the fanin of gate
    - Techniques to improve performance include sizing, input reordering, and buffering (staging)
- Ratioed Gates
  - Have active pull-down (-up) network connected to load device
  - Reduced gate complexity at expense of static power asymmetric transfer function
    - Techniques to improve performance include sizing to improve noise margins and reduce static power
- Pass Gates
  - Implement logic gate as switch network for reduced area and load capacitance
  - Long cascades of switches result in quadratic increase in delay
  - Also suffer from reduced noise margins (V_T drop)
    - Use level-restoring buffers to improve noise margins

- Dynamic logic … coming up soon

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Acknowledgement

- Prof. André DeHon (University of Pennsylvania)
- Prof. Tania Khanna (University of Pennsylvania)