ESE370: Circuit-Level Modeling, Design, and Optimization for Digital Systems

Lec 13: March 20, 2023
Distributed RC Wire and Elmore Delay

1

Today

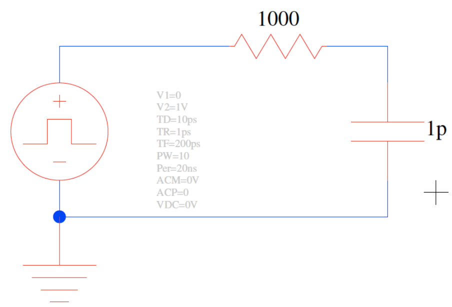
- Estimate delay in RC Network
  - Elmore delay calculation
- Apply to wire delay
- Apply to pass transistor circuits
- Apply to CMOS gates

2

Distributed RC (setup)

3

What is response? (Preclass 1)



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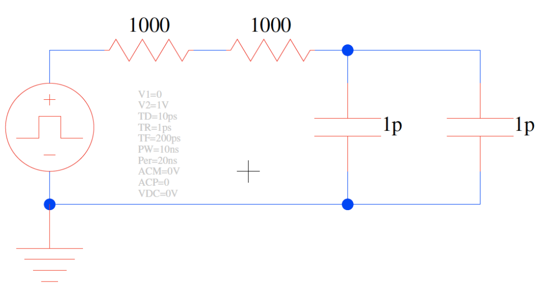

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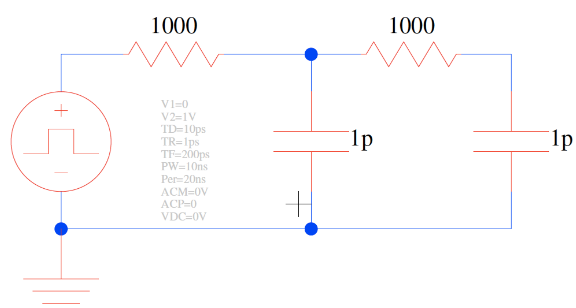

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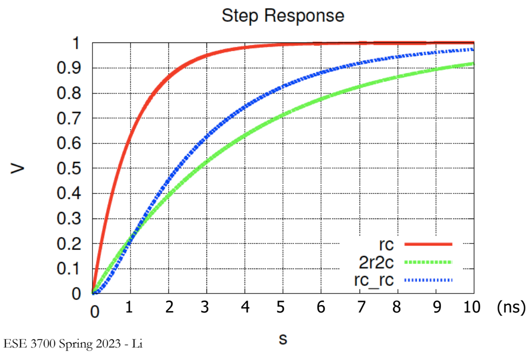
SPICE Response



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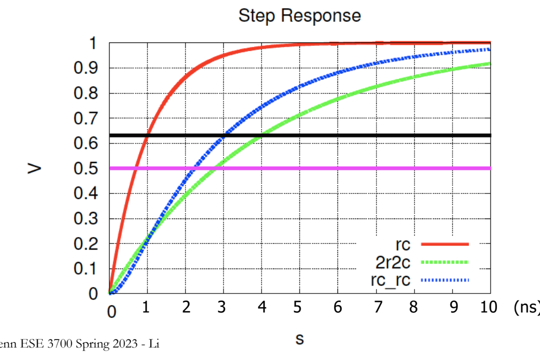
SPICE Response



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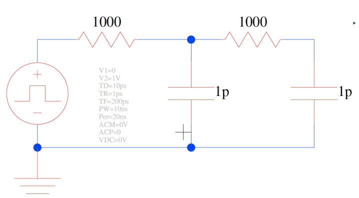
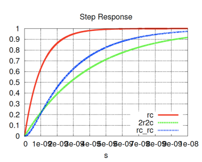
Intuition

- Look at series of R's on path
  - Must move Q=V(ΣC) across each R





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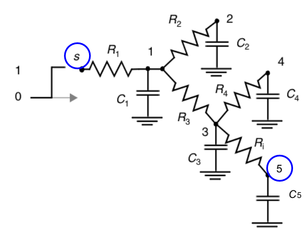
Elmore Delay: Distributed RC network

- The delay from source *s* to node *5*
  - N = number of nodes in circuit



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Elmore Delay: Distributed RC network

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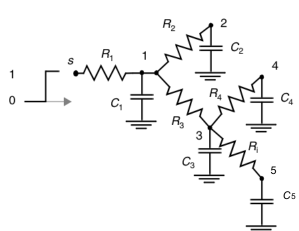
$$R_{5k} = \sum R_j \Rightarrow (R_j \in [path(s \to 5) \cap path(s \to k)])$$

$$\tau_{D5} = \sum_{k=1}^{N} C_k R_{5k}$$



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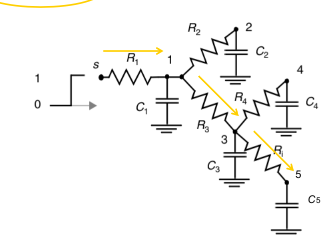

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Elmore Delay: Distributed RC network

- The delay from source *s* to node *5*
  - N = number of nodes in circuit

k=4

$$R_{5k} = \sum R_j \Rightarrow (R_j \in [path(s \to 5) \cap path(s \to k)])$$

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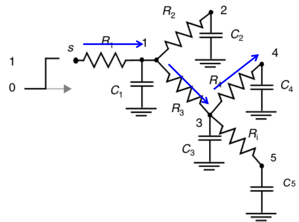

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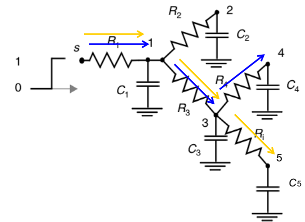

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Elmore Delay: Distributed RC network

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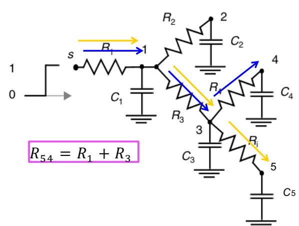

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Elmore Delay: Distributed RC network

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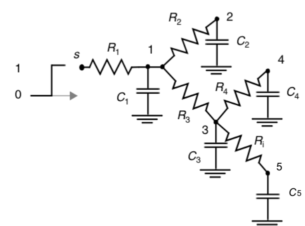

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Elmore Delay: Distributed RC network

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$$R_{5k} = \sum R_j \Rightarrow (R_j \in [path(s \to 5) \cap path(s \to k)])$$

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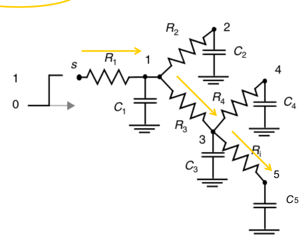

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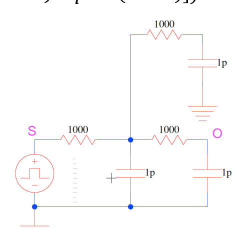
Elmore Delay: Practice

- The delay from source *s* to node *O*
  - N = number of nodes in circuit

$$R_{Ok} = \sum R_j \Rightarrow (R_j \in [path(s \to O) \cap path(s \to k)])$$

$$\tau_{DO} = \sum_{k=1}^{N} C_k R_{Ok} = ?$$



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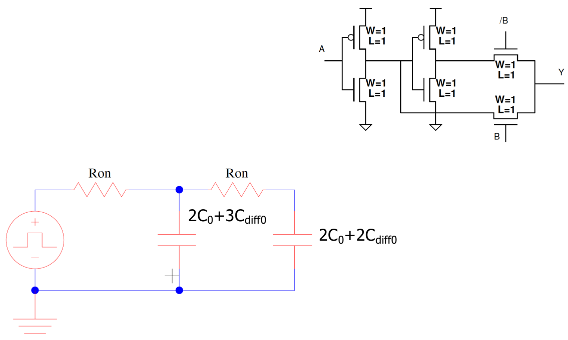
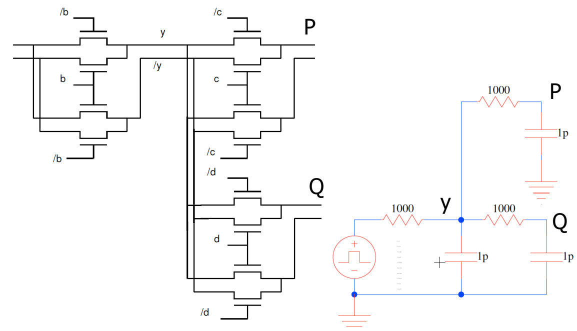
Previously: Equivalent RC



What is response?

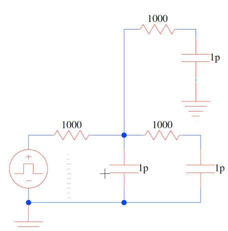


Elmore Delay: Practice (preclass 1)

- The delay from source *s* to node *i*
  - N = number of nodes in circuit

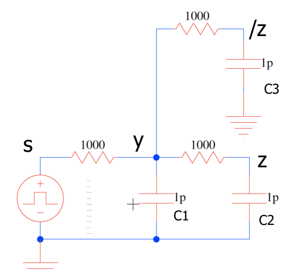
$$R_{ik} = \sum R_j \Rightarrow (R_j \in [path(s \rightarrow i) \cap path(s \rightarrow k)])$$

$$\tau_{Di} = \sum_{k=1}^{N} C_k R_{ik}$$

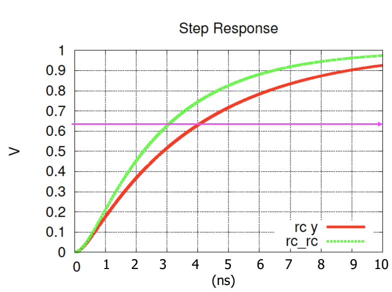


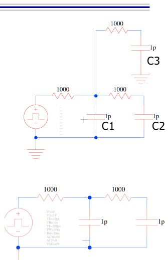
Apply (preclass 1)

- What is Elmore delay?
  - S → Z



SPICE Response

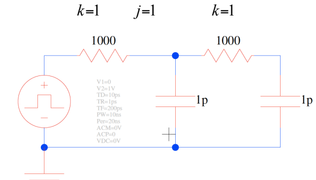




Elmore Delay: Special Ladder Case

- For each resistor C_k in path
  - Compute R_{kk} = sum of all Rs upstream of C_k

$$\tau_{DN} = \sum_{k=1}^{N} C_k \sum_{j=1}^{k} R_j = \sum_{k=1}^{N} C_k R_{kk}$$



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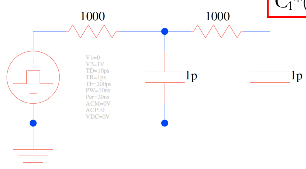
$C_1*(R_1)+C_2*(R_1+R_2)$



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Elmore Delay: Special Ladder Case

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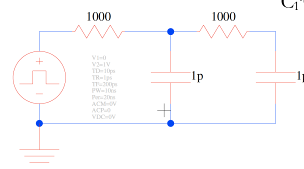

=3RC
=3ns

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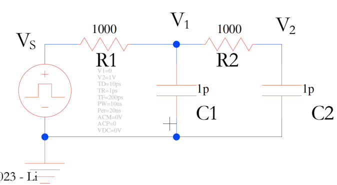
Compare KCL: Setup

- Equations from KCL?

@V1: $\frac{V_S - V_1}{R_1} = \frac{V_1 - V_2}{R_2} + C_1\frac{dV_1}{dt}$

@V2: $\frac{V_1 - V_2}{R_2} = C_2\frac{dV_2}{dt}$



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Compare KCL: Math

@V1:

$$\frac{V_S - V_1}{R_1} = \frac{V_1 - V_2}{R_2} + C_1\frac{dV_1}{dt}$$

$$\frac{V_S}{R_1} = \frac{V_1}{R_1} + \frac{V_1}{R_2} - \frac{V_2}{R_2} + C_1\frac{dV_1}{dt}$$

$$V_S = V_1\left(1+\frac{R_1}{R_2}\right) - \frac{R_1V_2}{R_2} + R_1C_1\frac{dV_1}{dt}$$

@V2:

$$\frac{V_1 - V_2}{R_2} = C_2\frac{dV_2}{dt}$$

$$\frac{V_1}{R_2} = \frac{V_2}{R_2} + C_2\frac{dV_2}{dt}$$

$$V_1 = V_2 + R_2C_2\frac{dV_2}{dt}$$

$$\frac{dV_1}{dt} = \frac{dV_2}{dt} + R_2C_2\frac{d^2V_2}{dt^2}$$

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Compare KCL: Math

$$V_S = V_1\left(1+\frac{R_1}{R_2}\right) - \frac{R_1}{R_2}V_2 + R_1C_1\frac{dV_1}{dt}$$

$$V_S = \left(V_2 + R_2C_2\frac{dV_2}{dt}\right)\left(1+\frac{R_1}{R_2}\right) - \frac{R_1}{R_2}V_2 + R_1C_1\left(\frac{dV_2}{dt} + R_2C_2\frac{d^2V_2}{dt^2}\right)$$

$$V_S = V_2 + \left(R_2C_2\left(1+\frac{R_1}{R_2}\right) + R_1C_1\right)\frac{dV_2}{dt} + R_1C_1R_2C_2\frac{d^2V_2}{dt^2}$$

$$V_S = V_2 + (R_2C_2 + R_1C_2 + R_1C_1)\frac{dV_2}{dt} + R_1C_1R_2C_2\frac{d^2V_2}{dt^2}$$

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Compare KCL: Math

$$R_1 = R_2 = R$$

$$C_1 = C_2 = C$$

$$V_S = V_2 + (R_2C_2 + R_1C_2 + R_1C_1)\frac{dV_2}{dt} + R_1C_1R_2C_2\frac{d^2V_2}{dt^2}$$

$$V_S = V_2 + 3RC\frac{dV_2}{dt} + R^2C^2\frac{d^2V_2}{dt^2}$$

30

Compare KCL: Math

$$R_1 = R_2 = R$$
$$C_1 = C_2 = C$$

$$V_S = V_2 + (R_2C_2 + R_1C_2 + R_1C_1)\frac{dV_2}{dt} + R_1C_1R_2C_2\frac{d^2V_2}{dt^2}$$

$$V_S = V_2 + 3RC\frac{dV_2}{dt} + R^2C^2\frac{d^2V_2}{dt^2}$$

$$\boxed{V_2 = A(1+e^{-\alpha t}) \rightarrow}$$
$$V_S = A(1+e^{-\alpha t}) - 3RC\cdot\alpha Ae^{-\alpha t} + R^2C^2\cdot\alpha^2 Ae^{-\alpha t}$$

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Compare KCL: Math

$$V_2 = A(1+e^{-\alpha t}) \rightarrow$$
$$V_S = A(1+e^{-\alpha t}) - 3RC\cdot\alpha Ae^{-\alpha t} + R^2C^2\cdot\alpha^2 Ae^{-\alpha t}$$
$$\boxed{t = \infty \rightarrow V_2 = V_S = A}$$

32

Compare KCL: Math

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$$\boxed{t = \infty \rightarrow V_2 = V_S = A}$$

$$V_S = V_S(1+e^{-\alpha t}) - 3RC\cdot\alpha V_S e^{-\alpha t} + R^2C^2\cdot\alpha^2 V_S e^{-\alpha t}$$
$$0 = e^{-\alpha t} - 3RC\cdot\alpha e^{-\alpha t} + R^2C^2\cdot\alpha^2 e^{-\alpha t}$$
$$0 = e^{-\alpha t}(1 - 3RC\alpha + R^2C^2\cdot\alpha^2)$$
$$0 = 1 - 3RC\alpha + R^2C^2\cdot\alpha^2$$

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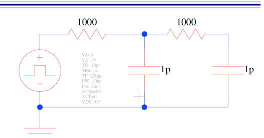
Compare KCL: Math



$$V_2 = V_S(1+e^{-\alpha t})$$

$$0 = 1 - 3RC\alpha + R^2C^2\cdot\alpha^2$$

$$\alpha = \frac{3RC \pm \sqrt{9(RC)^2 - 4(RC)^2}}{2(RC)^2} = \frac{3RC \pm \sqrt{5}RC}{2(RC)^2} = \frac{3 \pm \sqrt{5}}{2RC}$$

$$\rightarrow \tau = \frac{2}{3 \pm \sqrt{5}}RC \approx 2.6RC$$

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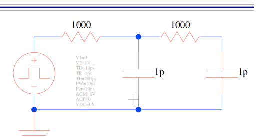
Compare KCL: Math



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=3RC
=3ns

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Elmore Delay: Distributed RC network

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  - N = number of nodes in circuit

$$R_{ik} = \sum R_j \Rightarrow (R_j \in [path(s \rightarrow i) \cap path(s \rightarrow k)])$$

$$\tau_{Di} = \sum_{k=1}^{N} C_k R_{ik}$$

- Special ladder case

$$\tau_{DN} = \sum_{k=1}^{N} C_k \sum_{j=1}^{k} R_j = \sum_{k=1}^{N} C_k R_{kk}$$

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Wire Delay

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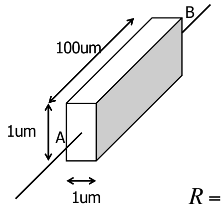
Wire Resistance



$$R = \frac{\rho L}{A}$$

$$R = \frac{10^{-7}\Omega \cdot m \cdot 100\mu m}{1\mu m \cdot 1\mu m} = 10\Omega$$

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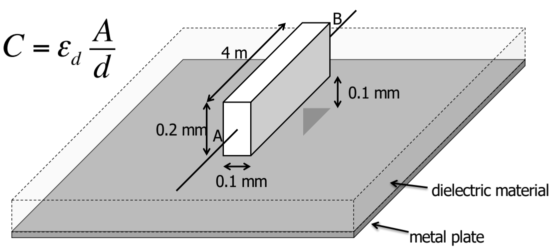
Wire Capacitance

$$C = \varepsilon_d \frac{A}{d}$$



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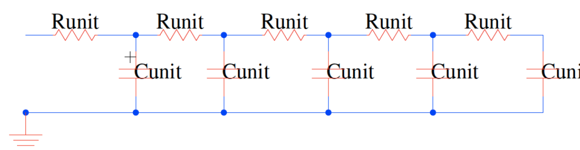
Wire as Distributed RC Ladder

- Measure wire length in units
  - Say λ
  - Each λ unit has C_{unit}, R_{unit}
    - Unit capacitance and resistance of wire of length λ



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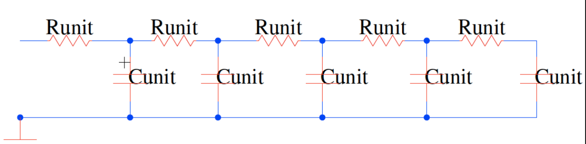
Wire Delay

- Delay of Wire N units long:



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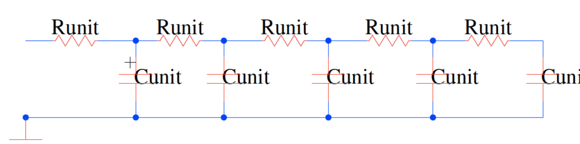
Wire Delay

- Delay of Wire N units long:

  $R_{unit}C_{unit}$



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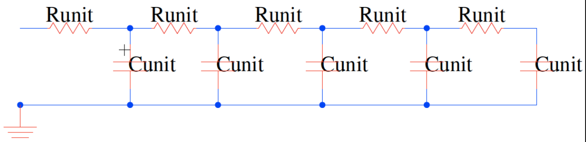
Wire Delay

- Delay of Wire N units long:

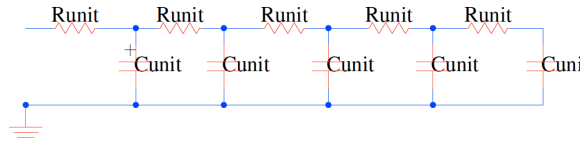
  $R_{unit}C_{unit}$
  $+ 2R_{unit}C_{unit}$



Wire Delay

- Delay of Wire N units long:

  $R_{unit}C_{unit}$
  $+ 2R_{unit}C_{unit}$
  $+ 3R_{unit}*C_{unit} + \ldots + NR_{unit}*C_{unit}$
  $=(R_{unit}*C_{unit})*(N+(N-1)+(N-2)+\ldots 1)$



Sum of integers (preclass 2)

- What's the sum of the integer 1 to N?

$$\sum_{k=0}^{N} k =$$

Sum of integers

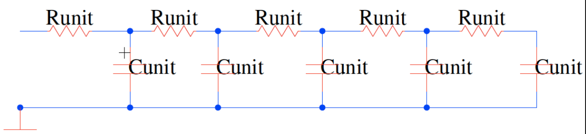
- What's the sum of the integer 1 to N?

$$\sum_{k=0}^{N} k = \frac{N(N+1)}{2} \approx \frac{N^2}{2}$$

Wire Delay (preclass 3)

- Delay of Wire N units long:

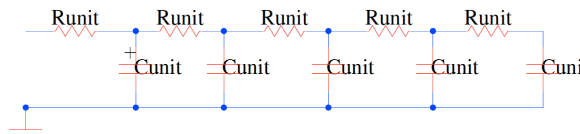
  $R_{unit}*(N*C_{unit})$
  $+ R_{unit}((N-1)*C_{unit}$
  $+ R_{unit}*(N-2)*C_{unit} + \ldots + R_{unit}*C_{unit}$
  $=(R_{unit}*C_{unit})*(N+N-1+N-2+\ldots 1)$
  $\sim=R_{unit}C_{unit}*N^2/2$



Lumped RC Wire? (preclass 4)

- What would the delay be if we treated the wire as lumped R and C?

$R_{wire} = N \times R_{unit}$ $\quad$ $C_{wire} = N \times C_{unit}$



Wire Delay

- $R_{wire} = N*R_{unit}$
- $C_{wire}=N*C_{unit}$
- Lumped RC wire delay = $R_{unit}*C_{unit}*N^2$
- Distributed RC Wire delay = $R_{unit}*C_{unit}*N^2/2$

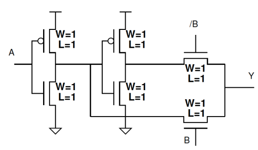
- Distributed has half the delay of lumped RC product
- Delay is quadratic in length of wire in both cases

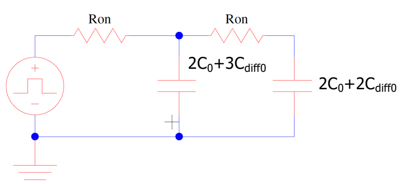
Apply to Gates

Pass Transistor and CMOS

Pass Transistor XOR

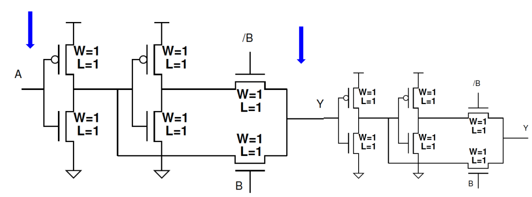
- Delay when A=B=1?





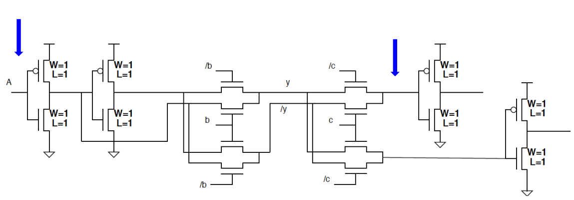
Pass Transistor XOR (preclass 5)

- Delay when A=1, B=0?
  - Start with equivalent RC circuit



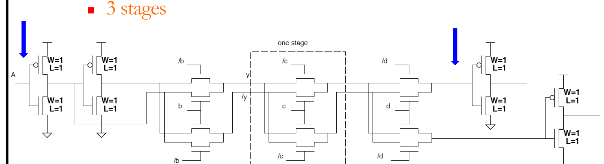
Unbuffered (preclass 6)

- Circuit → Delay?
  - 2 stages



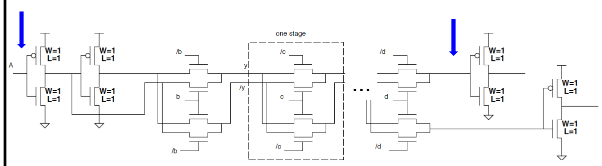
Unbuffered (preclass 7)

- Circuit → Delay?
  - 3 stages



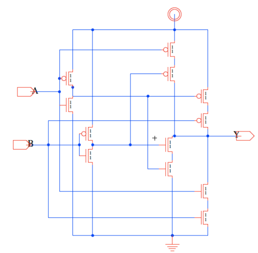
Unbuffered (preclass 8)

- Delay as a function of number of stages, k?

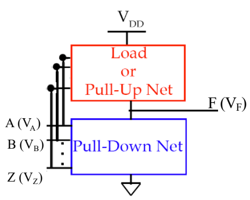


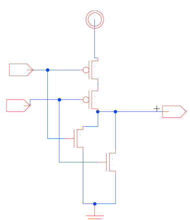
CMOS XOR (preclass 9)

- Delay with Cdiff>0?



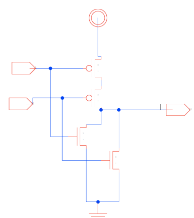
Review: Two-Input NOR Gate (NOR2)

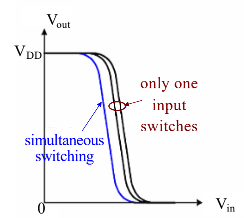




- Worst case delay of NOR2?
  - Minimum size, Loaded with itself

NOR2 Transfer Curve



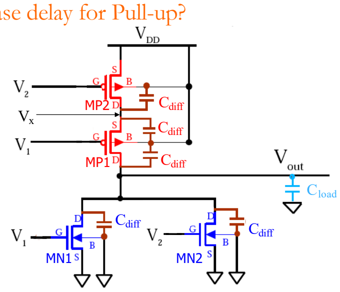


3 VTC Cases
$V_1 = 0$ V; $V_2 = 0 \rightarrow V_{DD}$
$V_1 = 0 \rightarrow V_{DD}$; $V_2 = 0$
V_1 and $V_2 = 0 \rightarrow V_{DD}$ simultaneously

Switching Threshold Voltage:
$V_1 = V_2 = V_{out} = V_t$

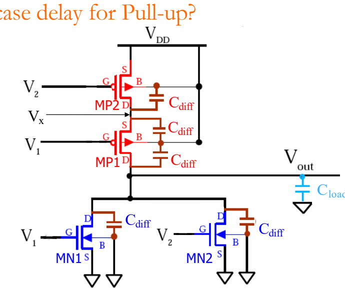
NOR2 Delay (preclass 10)

- Worst case delay for Pull-up?



NOR2 Delay

- Worst case delay for Pull-up?



Worst Case for Pull-up → $V_1 = 0$, $V_2 = V_{DD}$-> 0 @t=0 & $V_x \approx V_{out} = 0$ -> V_{DD}

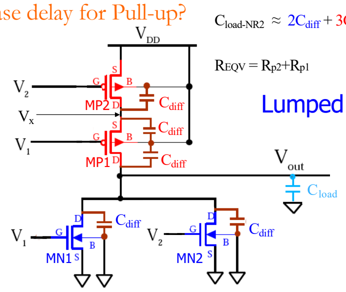
NOR2 Delay

- Worst case delay for Pull-up?

$C_{load\text{-}NR2} \approx 2C_{diff} + 3C_{diff} + C_{load}$

$R_{EQV} = R_{p2}+R_{p1}$

Lumped Model



Worst Case for Pull-up → $V_1 = 0$, $V_2 = V_{DD}$-> 0 @t=0 & $V_x \approx V_{out}$ = 0 -> V_{DD}

61

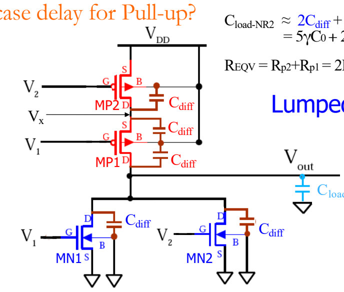
NOR2 Delay

- Worst case delay for Pull-up?

$C_{load\text{-}NR2} \approx 2C_{diff} + 3C_{diff} + C_{load} = 5\gamma C_0 + 2C_0$

$R_{EQV} = R_{p2}+R_{p1} = 2R_0$

Lumped Model



Worst Case for Pull-up → $V_1 = 0$, $V_2 = V_{DD}$-> 0 @t=0 & $V_x \approx V_{out}$ = 0 -> V_{DD}

delay = $(5\gamma C_0 + 2C_0)(2R_0)=(10\gamma+4)\tau$

62

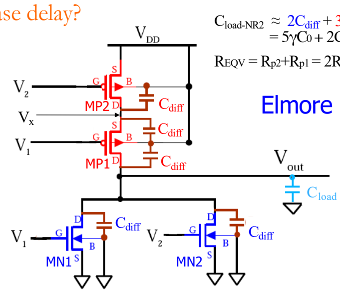
NOR2 Delay

- Worst case delay?

$C_{load\text{-}NR2} \approx 2C_{diff} + 3C_{diff} + C_{load} = 5\gamma C_0 + 2C_0$

$R_{EQV} = R_{p2}+R_{p1} = 2R_0$

Elmore Model?



Worst Case for Pull-up → $V_1 = 0$, $V_2 = V_{DD}$-> 0 @t=0 & $V_x \approx V_{out}$ = 0 -> V_{DD}

63

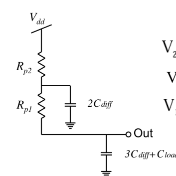
NOR2 Delay

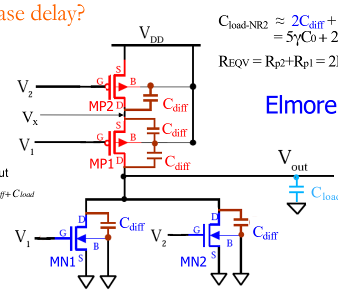
- Worst case delay?

$C_{load\text{-}NR2} \approx 2C_{diff} + 3C_{diff} + C_{load} = 5\gamma C_0 + 2C_0$

$R_{EQV} = R_{p2}+R_{p1} = 2R_0$

Elmore Model?





Worst Case for Pull-up → $V_1 = 0$, $V_2 = V_{DD}$-> 0 @t=0 & $V_x \approx V_{out}$ = 0 -> V_{DD}

64

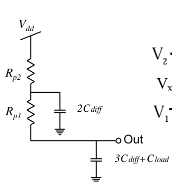
NOR2 Delay

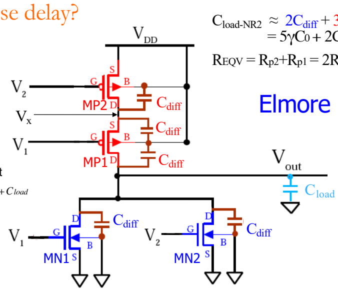
- Worst case delay?

$C_{load\text{-}NR2} \approx 2C_{diff} + 3C_{diff} + C_{load} = 5\gamma C_0 + 2C_0$

$R_{EQV} = R_{p2}+R_{p1} = 2R_0$

Elmore Model?





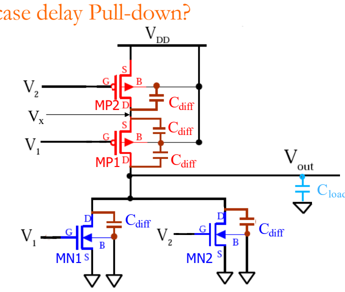
Worst Case for Pull-up → $V_1 = 0$, $V_2 = V_{DD}$-> 0 @t=0 & $V_x \approx V_{out}$ = 0 -> V_{DD}

delay = $(2C_{diff})(R_{p2})+(3C_{diff}+C_{load})(R_{p1}+R_{p2})=(8\gamma+4)\tau$

65

NOR2 Delay

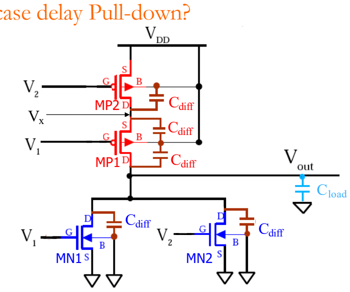
- Worst case delay Pull-down?



66

NOR2 Delay

- Worst case delay Pull-down?

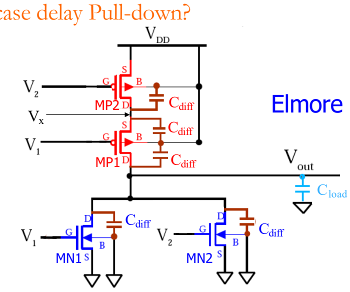


Worst case for Pull-down → $V_1 = 0$, $V_2 = 0 \text{->} V_{DD}$ @t=0 & $V_x \approx V_{out}=V_{DD}\text{->} 0$

67

NOR2 Delay

- Worst case delay Pull-down?



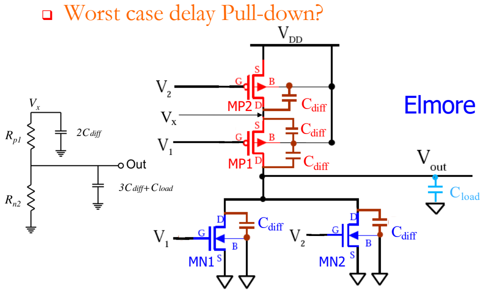
Elmore Model?

Worst case for Pull-down → $V_1 = 0$, $V_2 = 0 \text{->} V_{DD}$ @t=0 & $V_x \approx V_{out}=V_{DD}\text{->} 0$

68

NOR2 Delay

- Worst case delay Pull-down?



Elmore Model?

Worst case for Pull-down → $V_1 = 0$, $V_2 = 0 \text{->} V_{DD}$ @t=0 & $V_x \approx V_{out}=V_{DD}\text{->} 0$

$$\text{delay} = (2C_{diff})(R_{p1}+R_{n2})+(3C_{diff}+C_{load})(R_{n2})=(7\gamma+2)\tau$$

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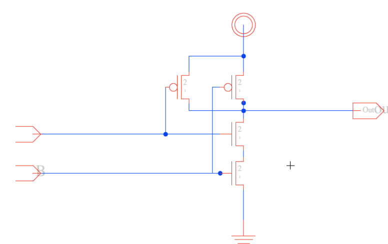
NAND2 Delay (preclass 11)



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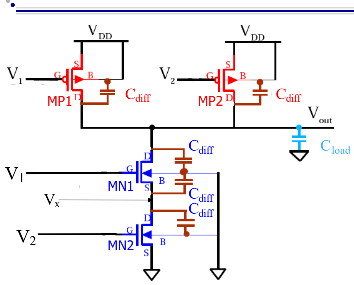
Parasitic Caps for NAND2 (worst case)



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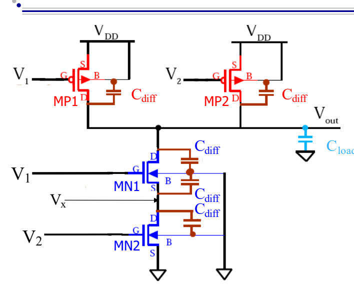
Parasitic Caps for NAND2 (worst case)



Worst case for Pull-up →

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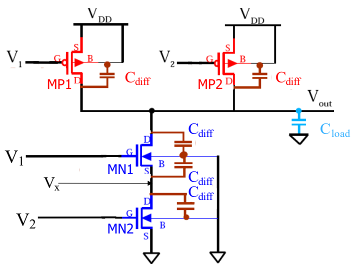
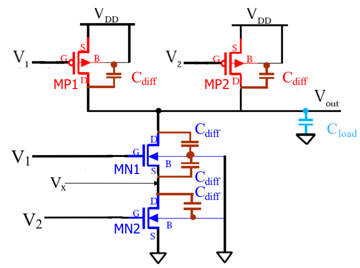
Parasitic Caps for NAND2 (worst case)



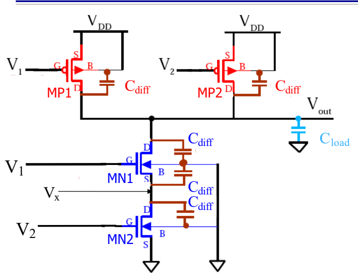
Worst case for Pull-up → $V_1 = V_{DD}$, $V_2 = V_{DD}$-> 0 @t=0 & $V_x \approx V_{out}$= 0 ->V_{DD}

Parasitic Caps for NAND2 (worst case)



Worst case for pull down →

Parasitic Caps for NAND2 (worst case)



Worst case for pull down → $V_1 = V_{DD}$, V_2 = 0 ->V_{DD} @t=0 & $V_x \approx V_{out}$=V_{DD}-> 0

Logic Types

- CMOS Gates
  - Dual pull-down and pull-up networks, only one enabled at a time
  - Performance of gate is strong function of the fanin of gate
    - Techniques to improve performance include sizing, input reordering, and buffering (staging)
- Ratioed Gates
  - Have active pull-down (-up) network connected to load device
  - Reduced gate complexity at expense of static power asymmetric transfer function
    - Techniques to improve performance include sizing to improve noise margins and reduce static power
- Pass Gates
  - Implement logic gate as switch network for area and often delay win
  - Long cascades of switches result in quadratic increase in delay
  - Also suffer from reduced noise margins (V_T drop)
    - Use level-restoring buffers to improve noise margins
- Dynamic logic … next time

Idea

- Elmore delay calculation allows us to estimate delay for distributed RC network
  - Necessary for pass transistors
- Wires are distributed RC
  - Half delay lumped calculation
  - Still quadratic in length

Admin

- Project 1
  - Final report due **Friday 3/24** midnight

Acknowledgement

- Prof. André DeHon (University of Pennsylvania)
- Prof. Tania Khanna (University of Pennsylvania)