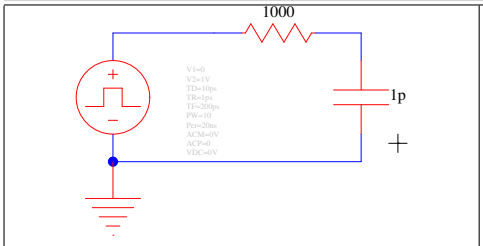
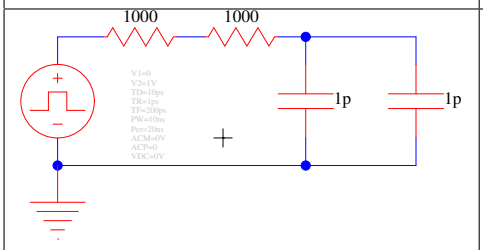
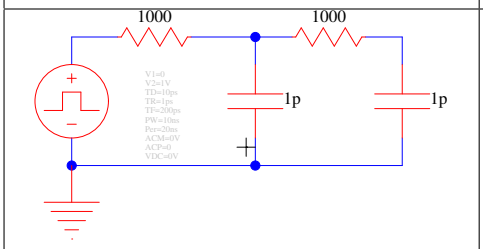
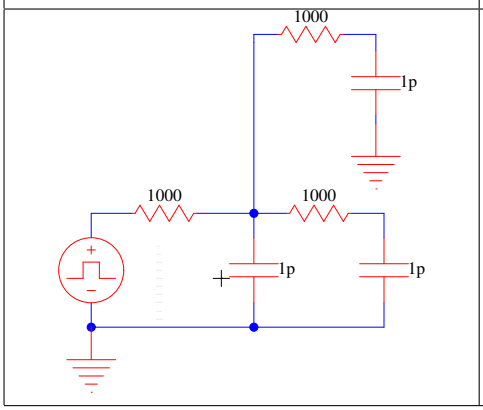
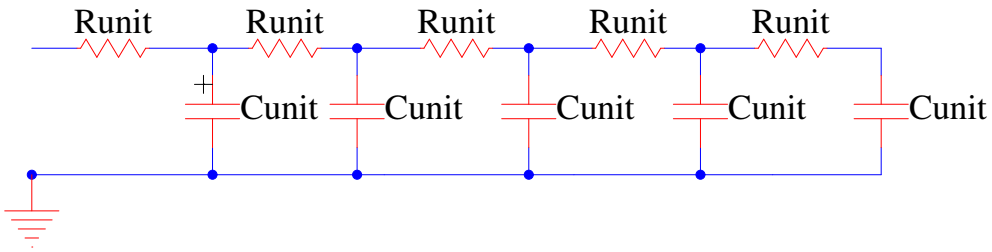
1. What is the delay (time constant) associated with each of the following?

Circuit	Time Constant
	
	
	
	

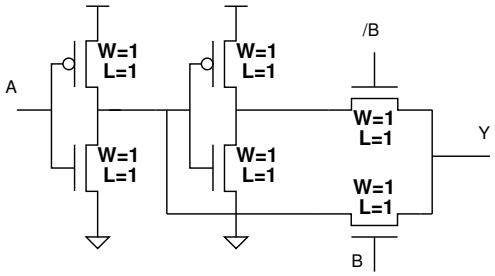
2. What is the sum of the integers 1 to N? ____

3. Delay of length N RC-ladder (length 5 shown) ? ____

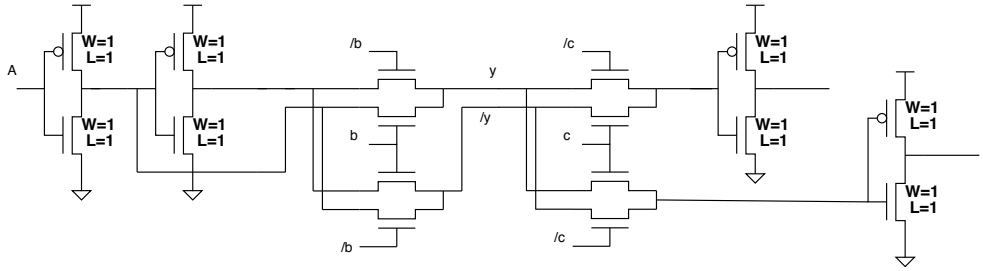


4. How does the above (problem 3) result compare to treating the R's and C's as lumped (all C's following the Rs)?

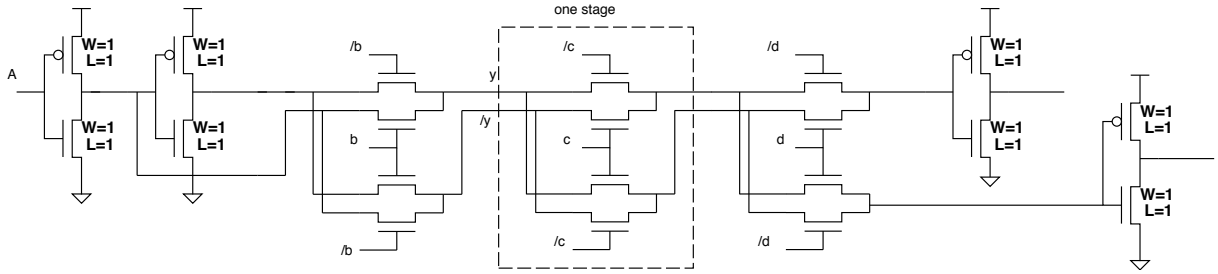
5. Delay driving A input of a copy of itself (A=1, B=0)



6. Delay from inverter shown on left to (but not including) inverter shown on right (A=1, B=C=0)

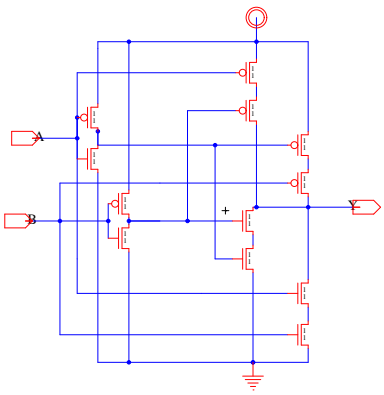


7. Delay from inverter shown on left to (but not including) inverter shown on right (A=1, B=C=D=0)



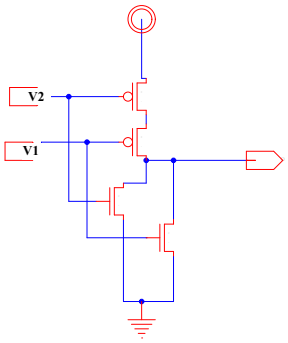
8. Delay above with k stages (previous 2 here $k = 2$, $k = 3$)

9. Delay when loaded by the A input of an identical xor2 gate.



For the remaining preclass we are going to analyze the worst case delays for a nor2 and nand2 gate with $C_{diff} \neq 0$. Assume each gate has minimum size transistors and is loaded with an identical gate.

10. First we will look at the CMOS NOR2 gate.



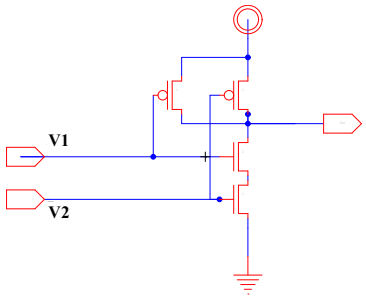
(a) What is the input switching case for the nor2 worst case rise time (i.e. pull-up delay)?

(b) What is the equivalent RC circuit? What is the τ estimate delay?

(c) What is the input switching case for the nor2 worst case fall time (i.e. pull-down delay)?

(d) What is the equivalent RC circuit? What is the τ estimate delay?

11. Next we will look at the CMOS NAND2 gate.



(a) What is the input switching case for the nand2 worst case rise time (i.e. pull-up delay)?

(b) What is the equivalent RC circuit? What is the τ estimate delay?

(c) What is the input switching case for the nand2 worst case fall time (i.e. pull-down delay)?

(d) What is the equivalent RC circuit? What is the τ estimate delay?