ESE370: Circuit-Level Modeling, Design, and Optimization for Digital Systems

Lec 17: April 10, 2023

Memory Overview and Periphery

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Today

- Memory
  - Classification
  - Architecture
  - Periphery
  - Serial Access Memories
- Project 2 is on this

2

Memory Overview

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Semiconductor Memory Classification

RWM		NVRWM	ROM
Random Access	**Non-Random Access**	EPROM E^2PROM FLASH	Mask-Programmed Programmable (PROM)
SRAM DRAM	FIFO LIFO Shift Register CAM		

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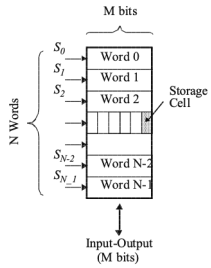
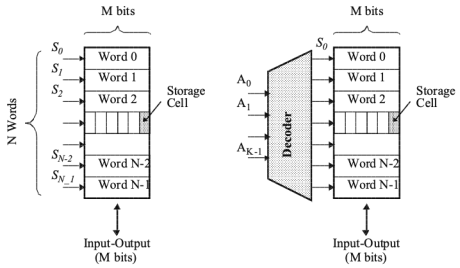
Memory Architecture: Core



N words => N select signals
Too many select signals

5

Memory Architecture: Decoders



N words => N select signals
Too many select signals

Decoder reduces # of select signals
$K = \log_2 N$

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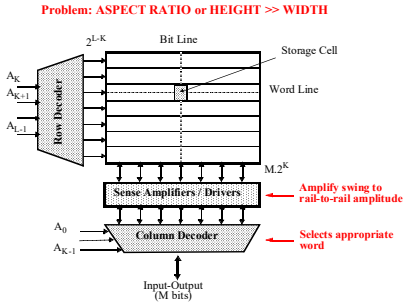
Array-Structured Memory Architecture



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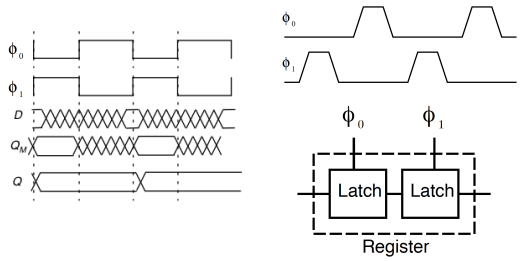
Latches/Register – Can Store a State

- Build register from pair of latches
- Control with non-overlapping clocks



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ROM Memories

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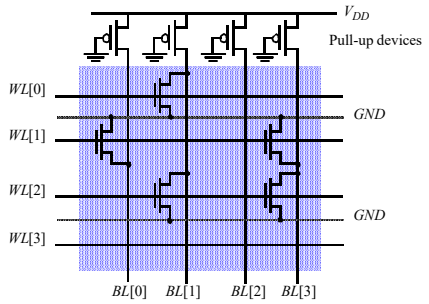
MOS NOR ROM



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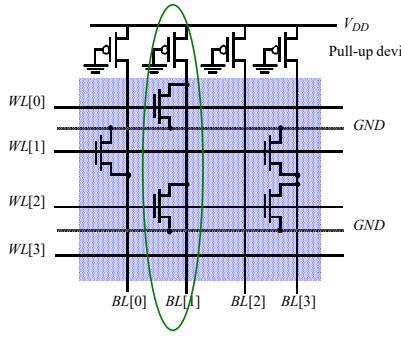
MOS NOR ROM



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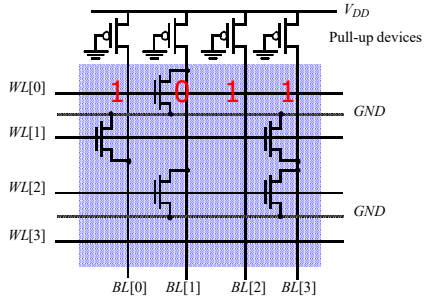
MOS NOR ROM



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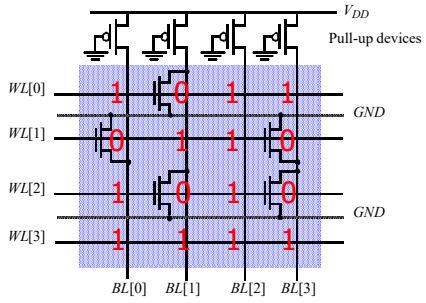
MOS NOR ROM



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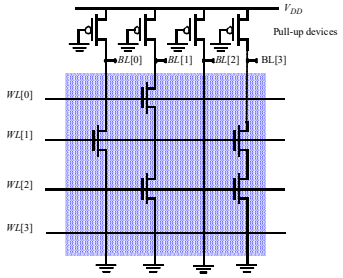
MOS NAND ROM



All word lines high by default with exception of selected row

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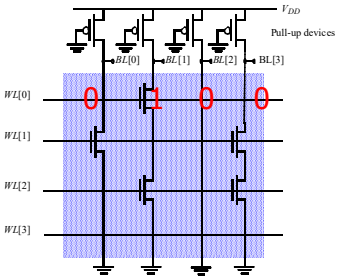
MOS NAND ROM



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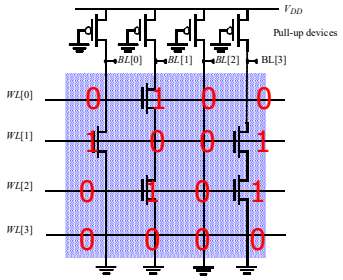
MOS NAND ROM



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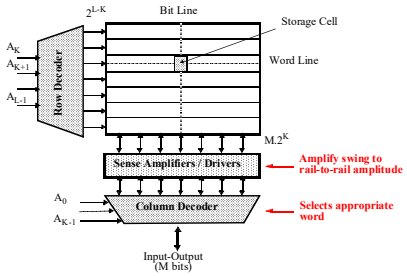
Array-Structured Memory Architecture

Problem: ASPECT RATIO or HEIGHT >> WIDTH



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ROM Memories

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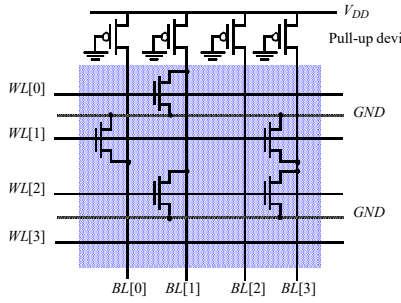
MOS NOR ROM



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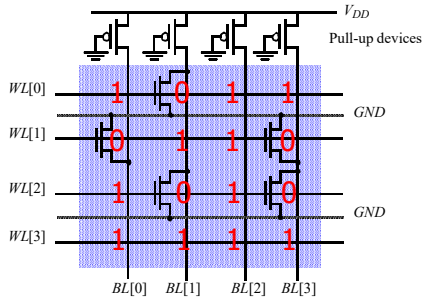
MOS NOR ROM



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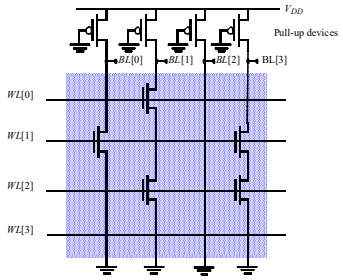
MOS NAND ROM



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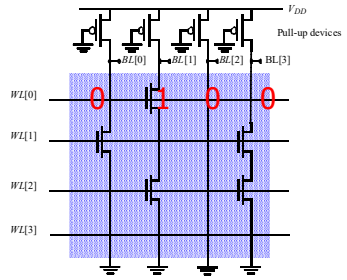
MOS NAND ROM



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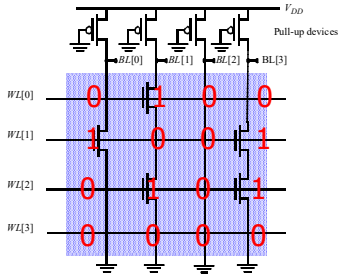

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Memory Periphery

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Periphery

- Decoders
- Column Circuitry
  - Bit-line Conditioning
  - Sense Amplifiers
  - Input/Output Buffers
- Control/Timing Circuitry

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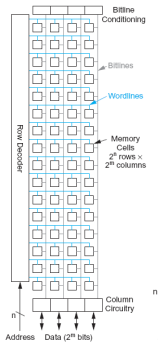
Array Architecture

- 2^n *words* of 2^m *bits* each
- Good regularity – easy to design
- Very high density if good cells are used



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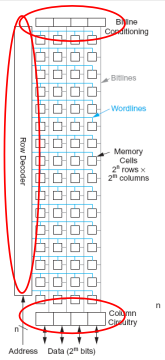

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Decoders

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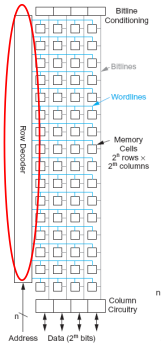

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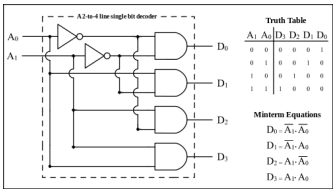
Decoders

- n:2^n decoder consists of 2^n n-input AND gates
  - One needed for each row of memory
  - Build AND from NAND or NOR gates

Static CMOS



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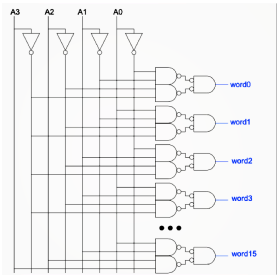
Large Decoders

- For n > 4, NAND gates become slow
  - Break large gates into multiple smaller gates



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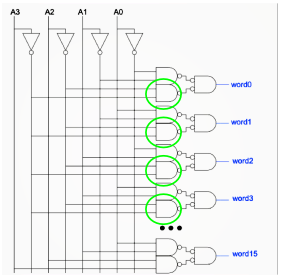

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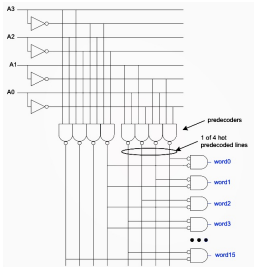
Predecoding

- Many of these gates are redundant
  - Factor out common gates into predecoder
  - Saves area
  - Same path effort



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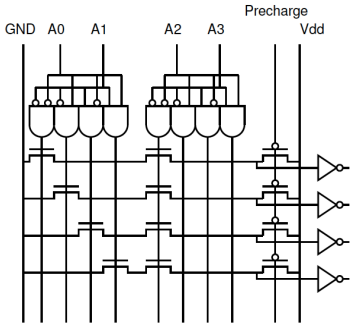
Row Select: Precharge NAND



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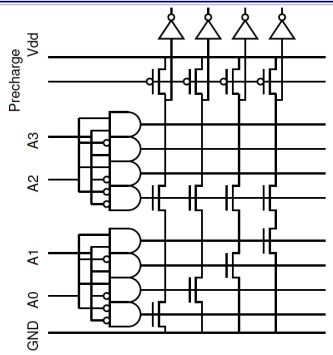
Row Select: Precharge NAND



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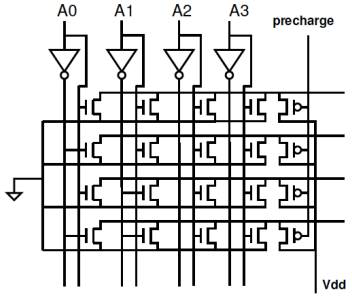
Row Select: Precharge NOR



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Column Circuitry

& Bit-line Conditioning

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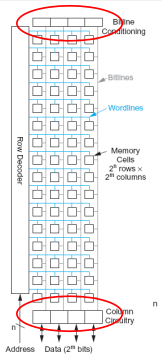

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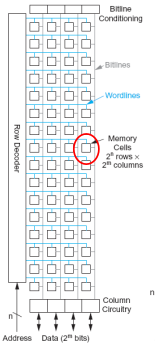

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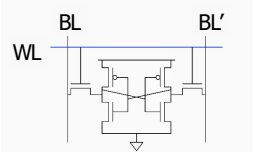
6T SRAM Cell

- Cell size accounts for most of array size
  - Reduce cell size at expense of complexity
- 6T SRAM Cell
  - Used in most commercial chips
  - Data stored in cross-coupled inverters
- Read:
  - Precharge BL, BL'
  - Raise WL
- Write:
  - Drive data onto BL, BL'
  - Raise WL



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Column Circuitry

- Some circuitry is required for each column
  - Required: Bitline conditioning
    - Precharging
    - Driving input data to bitline
  - Increased speed: Sense amplifiers
  - Aspect ratio (square memory): Column multiplexing (AKA Column Decoders)

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Bitline Conditioning

- Precharge bitlines high before read operations

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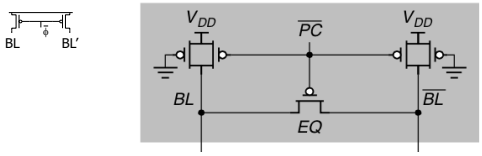
Bitline Conditioning

- Precharge bitlines high before reads



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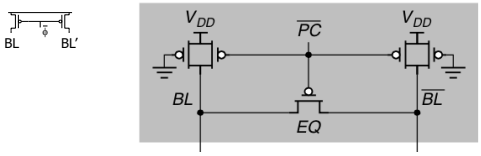
Bitline Conditioning

- Precharge bitlines high before reads



- What if pre-charged to Vdd/2?
  - Pros: reduces read-upset
  - Challenge: generate Vdd/2 voltage on chip

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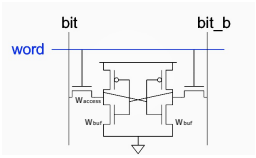
Column Capacitance Consequence

- Preclass1: What is capacitance of a bitline?
  - W_{access} (pass transistor size), d rows, $\gamma=C_{diff0}/C_0$



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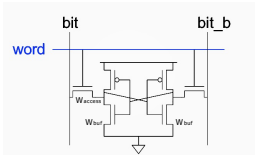
Column Capacitance Consequence

- Preclass1: What is capacitance of a bitline?
  - W_{access} (pass transistor size), d rows, $\gamma=C_{diff0}/C_0$
- Preclass2: What is the delay for the cell to drive the bitline during a read?
  - W_{buf} (inverter size in cell), R_0



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Column Capacitance Consequence

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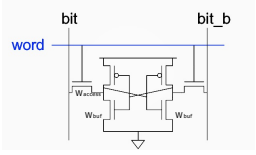
- Preclass2: What is the delay for the cell to drive the bitline during a read?
  - W_{buf} (inverter size in cell), R_0
- Preclass3: Waccess=Wbuf=1, γ=1/2
  - Delay for d=32, 512?



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Column Capacitance Consequence

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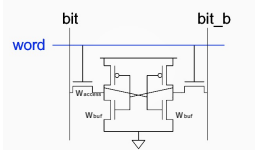
  - W_{access} (pass transistor size), d rows, $\gamma=C_{diff0}/C_0$
- Preclass2: What is the delay for the cell to drive the bitline during a read?
  - W_{buf} (inverter size in cell), R_0
- **Conclude:** Can't size up cell→driving bitline will be slow



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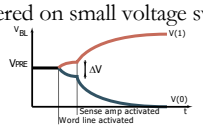
Sense Amplifiers

- Bitlines have many cells attached
  - Ex: 32-kbit SRAM has 128 rows x 256 cols
  - 128 cells on each bitline
- $t_{pd} \propto (C/I)\,\Delta V$
  - Even with shared diffusion contacts, 64C of diffusion capacitance (big C)
  - Discharged slowly through small transistors in each memory cell (small I)
- *Sense amplifiers* are triggered on small voltage swing (ΔV)



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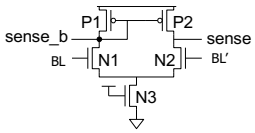
Differential Pair Amp

- Differential pair requires no clock
- But always dissipates static power



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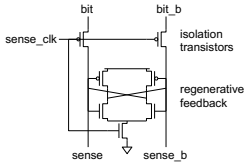
Clocked Sense Amp

- Clocked sense amp saves power
- Requires sense_clk after enough bitline swing
- Isolation transistors cut off large bitline capacitance



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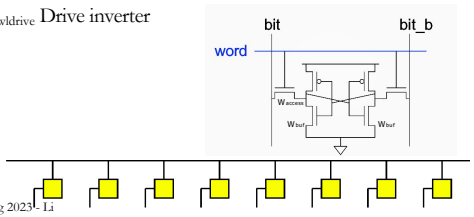
Word Line Capacitance

- Preclass4: What is capacitance of word line (row)?
  - W_{access}– transistor width of column device
  - w columns
  - $\gamma = C_{diff()}/C_0$
- Preclass5: Delay driving word line?
  - $W_{wldrive}$ Drive inverter



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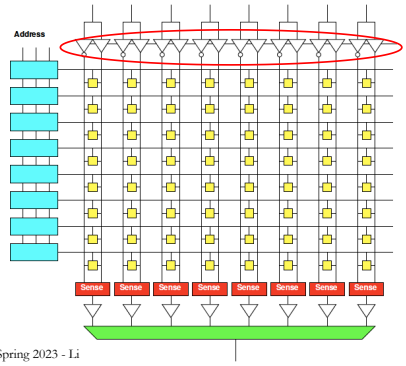
Column Drivers: Memory Bank



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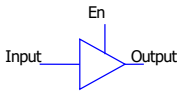
Tristate Buffer

- Typically used for signal traveling, e.g. bus
- Ideally all devices connected to a bus should be disconnected except for active device reading or writing to bus
- Use high-impedance state to simulate disconnecting



Active-high buffer

Input	En	Ouptut
0	0	Z
1	0	Z
0	1	0
1	1	1

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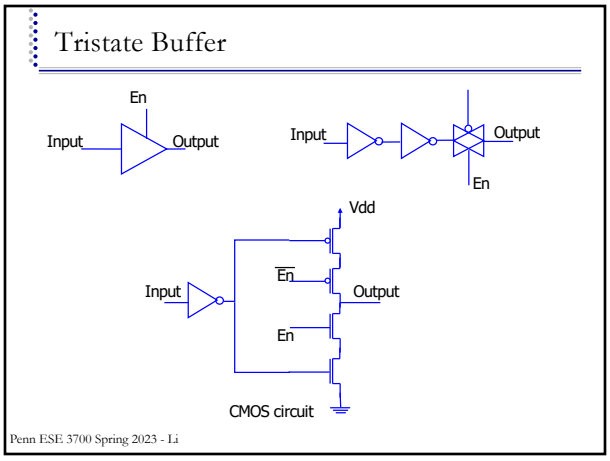

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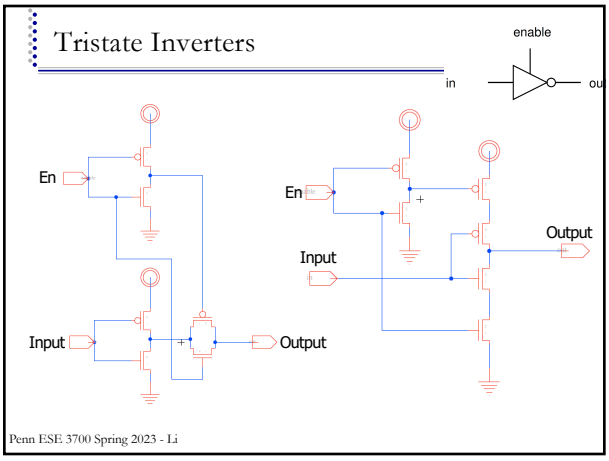

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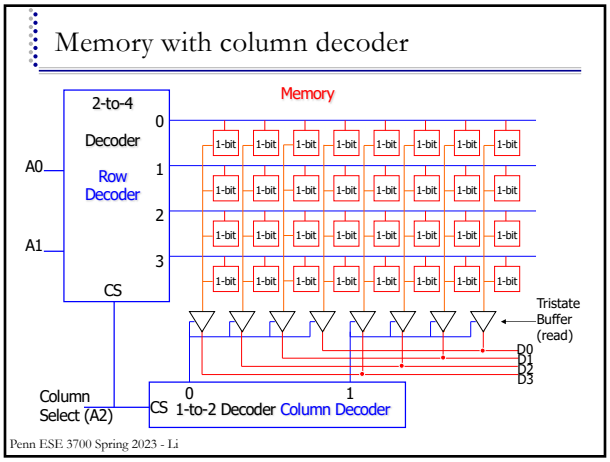

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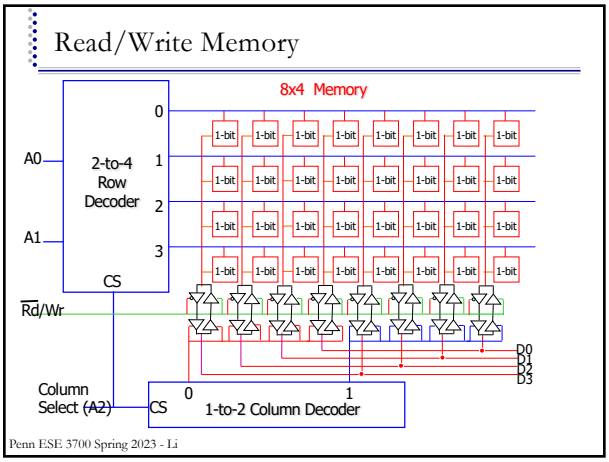

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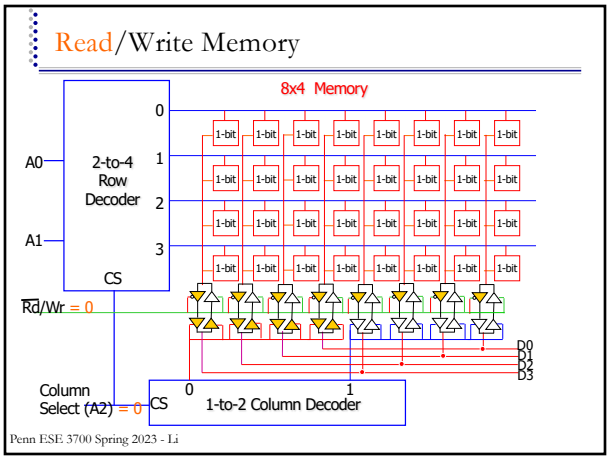

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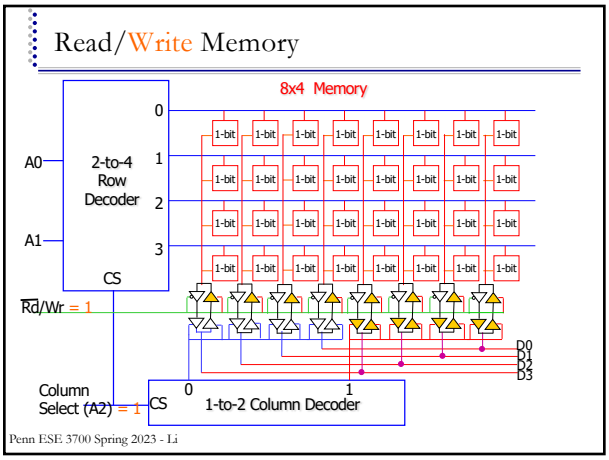

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Serial Access Memories (Optional)

- Serial access memories do not use an address
  - Serial In Parallel Out (SIPO)
  - Parallel In Serial Out (PISO)
  - Shift Registers
  - Queues (FIFO, LIFO)

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Idea

- Memory for compact state storage
- Share circuitry across many bits
  - Minimize area per bit → maximize density
- Aggressively use:
  - Pass transistors, Ratioing
  - Precharge, Amplifiers to keep area down

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Admin

- Homework 6 due **Friday 4/7**
- Project 2 out Friday 4/7
  - Work in teams of up to two
  - Final report due Wednesday 4/26

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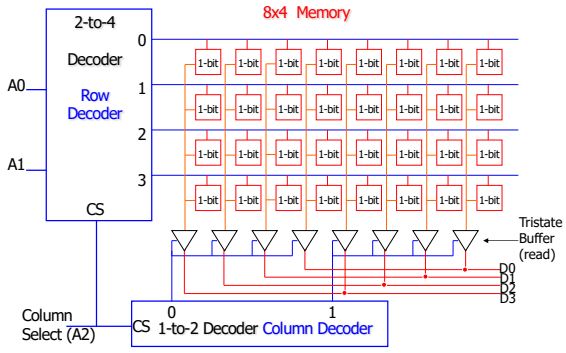
8x4 Memory with column decoder



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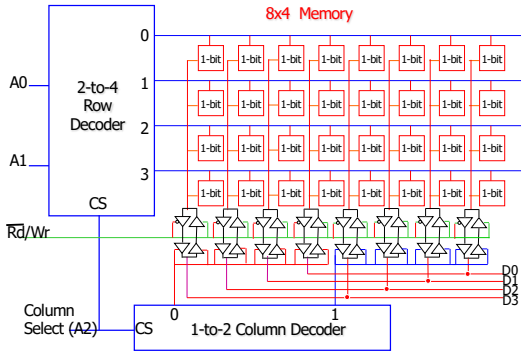
Read/Write Memory



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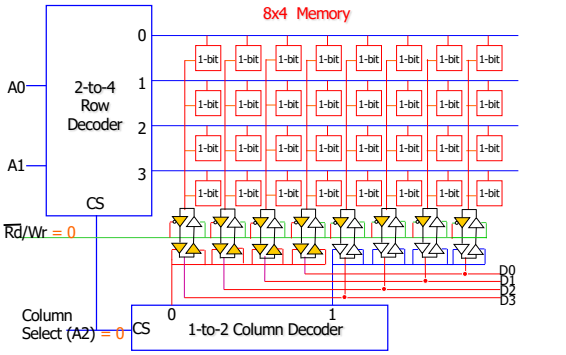
Read/Write Memory



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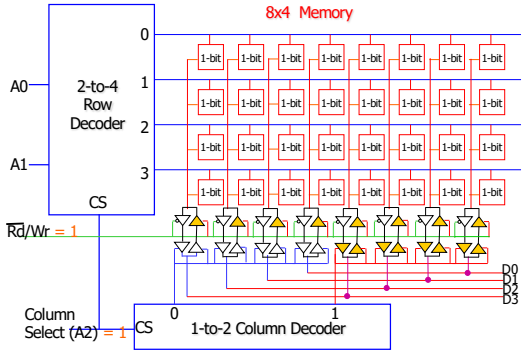
Read/Write Memory



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- Prof. Tania Khanna (University of Pennsylvania)

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