ESE370: Circuit-Level Modeling, Design, and Optimization for Digital Systems

Lec 18: April 12, 2023

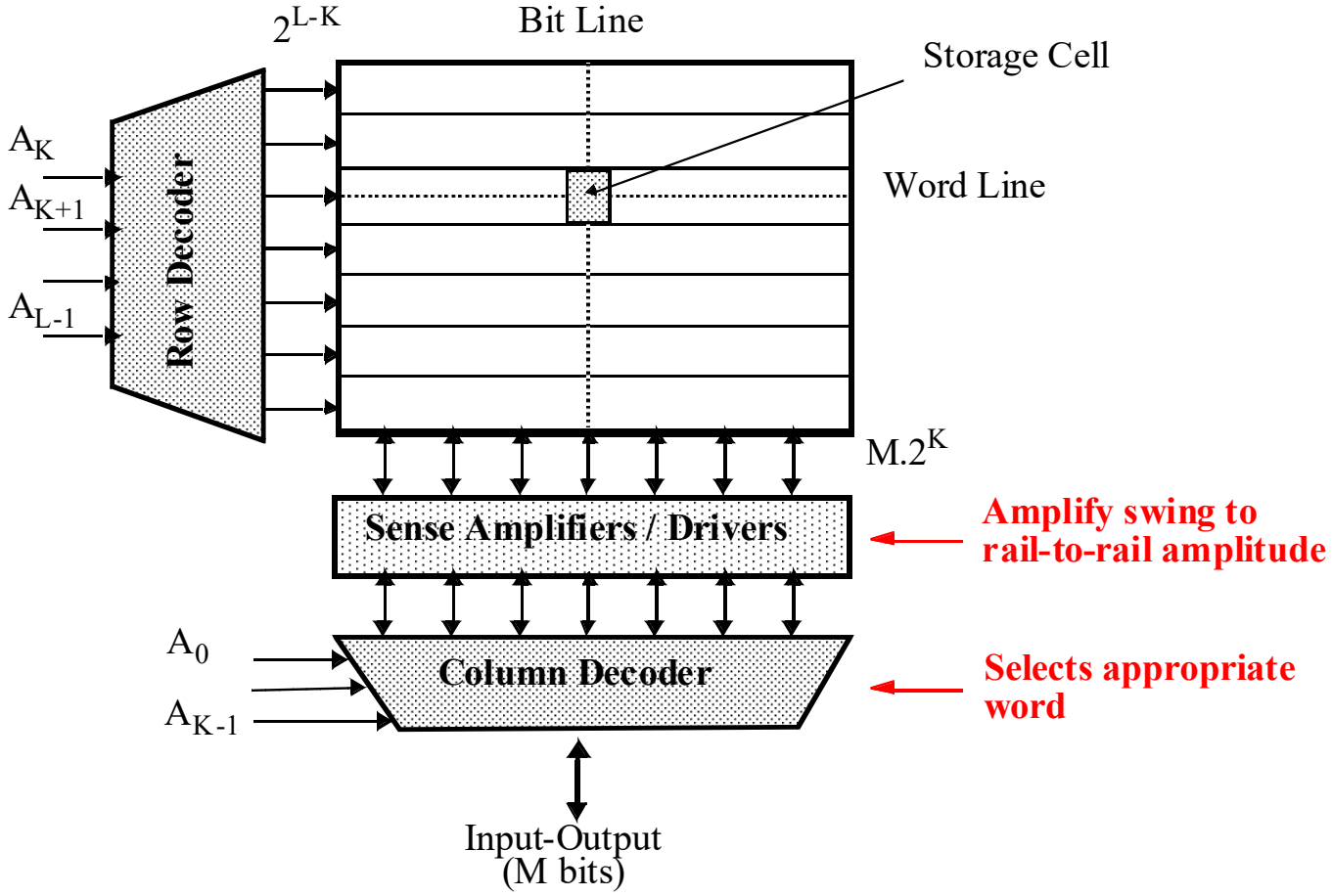
Memory Core

Today

- Memory Array examples
- Memory
  - Memory core
    - 6T SRAM
- Project 2 is on this

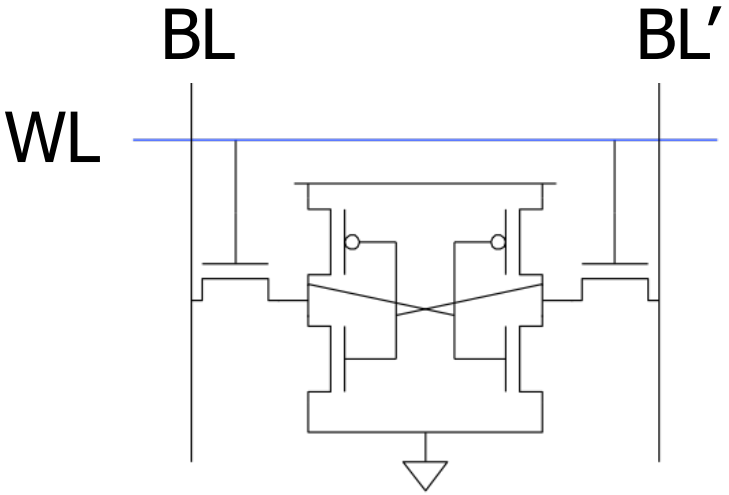
Array-Structured Memory Architecture

Problem: ASPECT RATIO or HEIGHT >> WIDTH

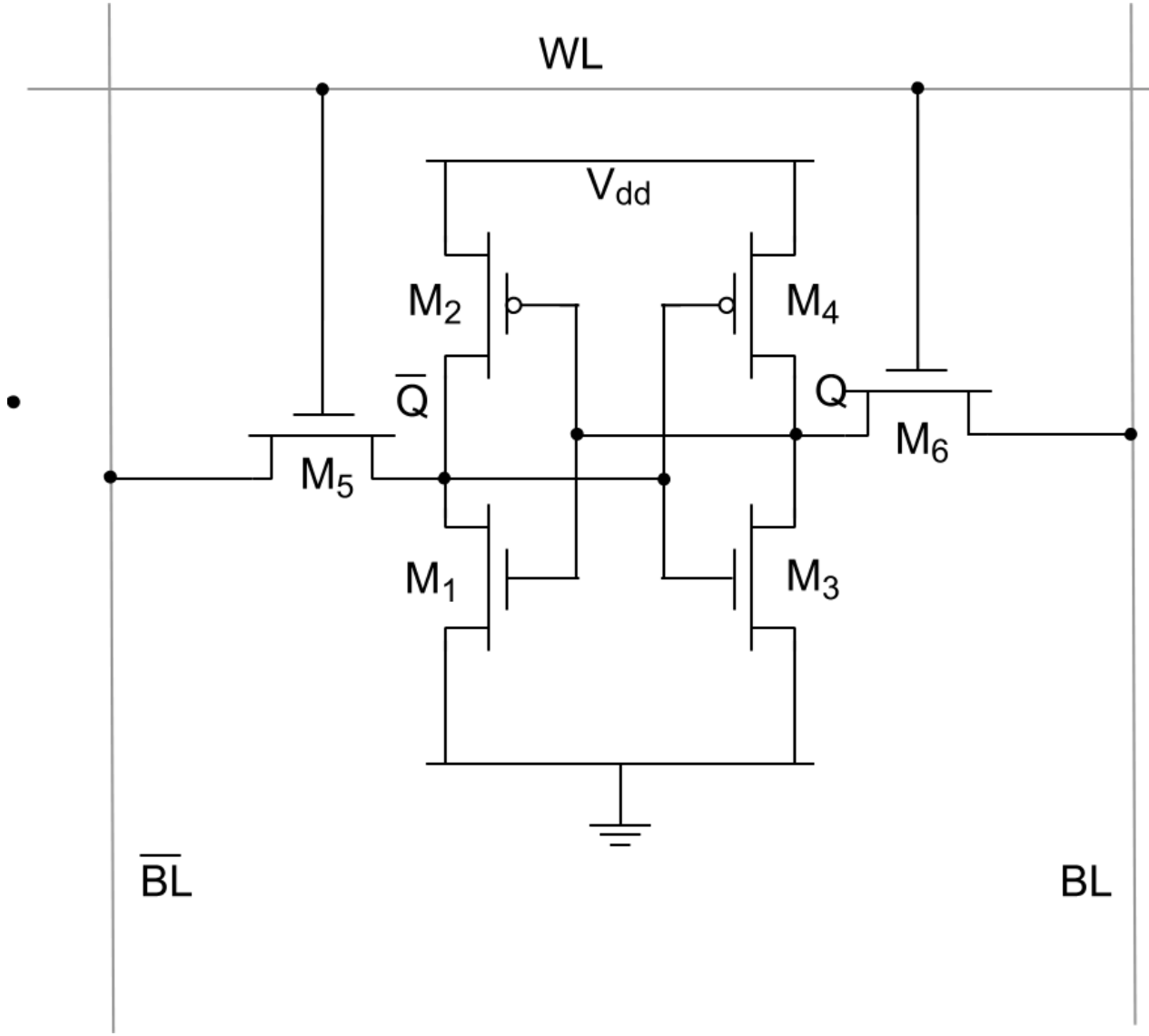


6T SRAM Cell

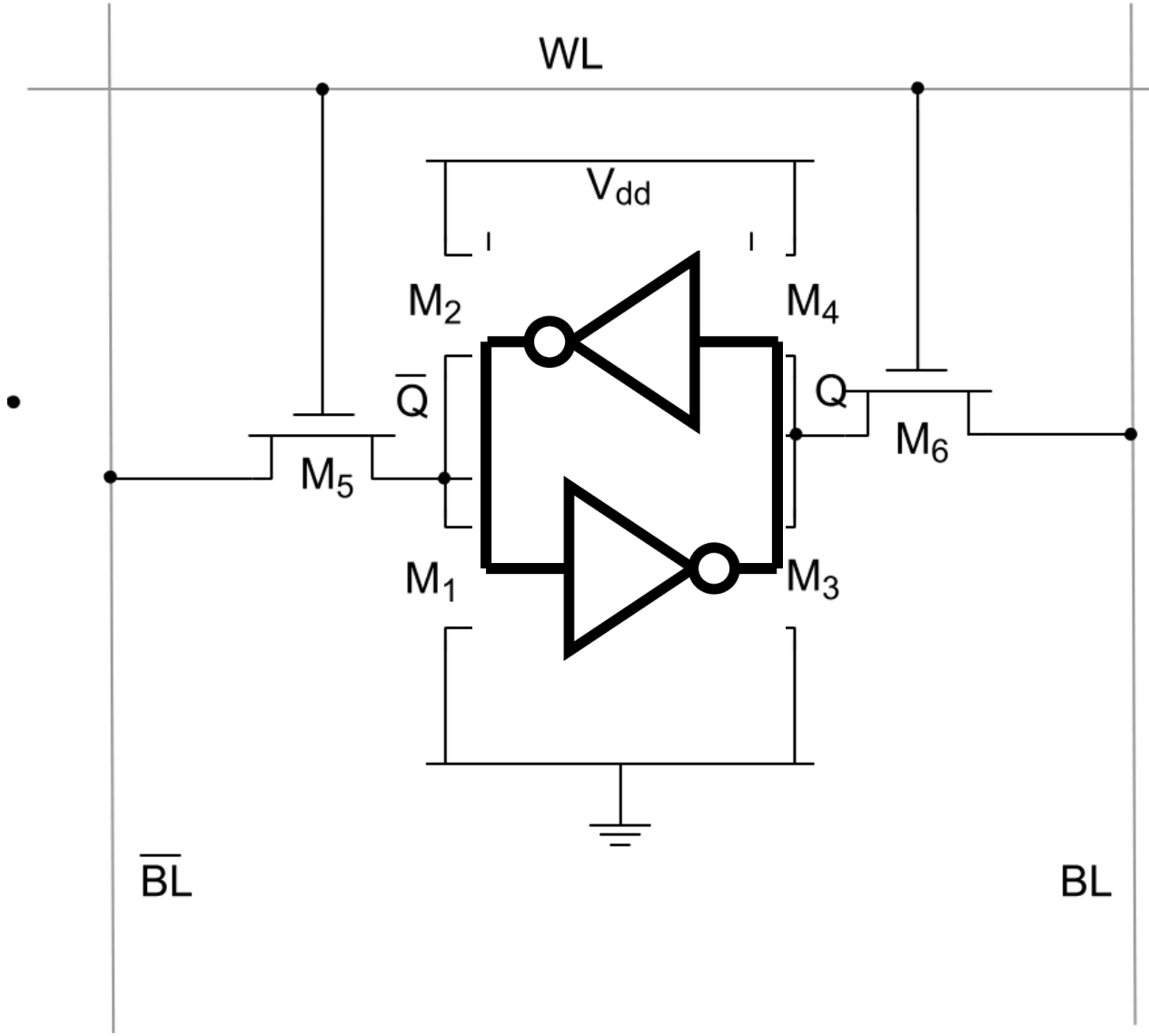
- Cell size accounts for most of array size
  - Reduce cell size at expense of complexity
- 6T SRAM Cell
  - Used in most commercial chips
  - Data stored in cross-coupled inverters
- Read:
  - Precharge BL, BL'
  - Raise WL
- Write:
  - Drive data onto BL, BL'
  - Raise WL



6-transistor CMOS SRAM Cell



6-transistor CMOS SRAM Cell

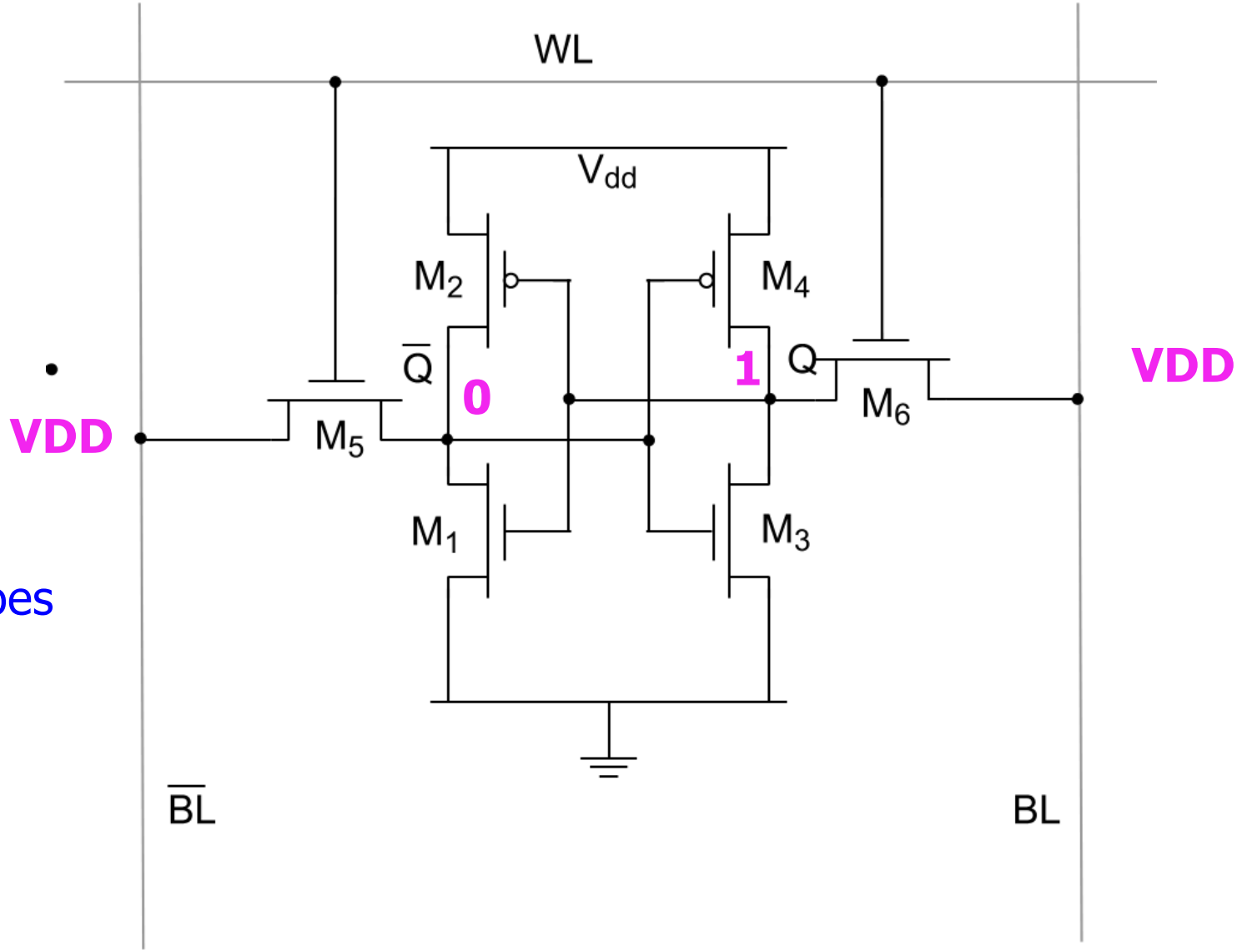


6-transistor CMOS SRAM Cell (preclass 1)

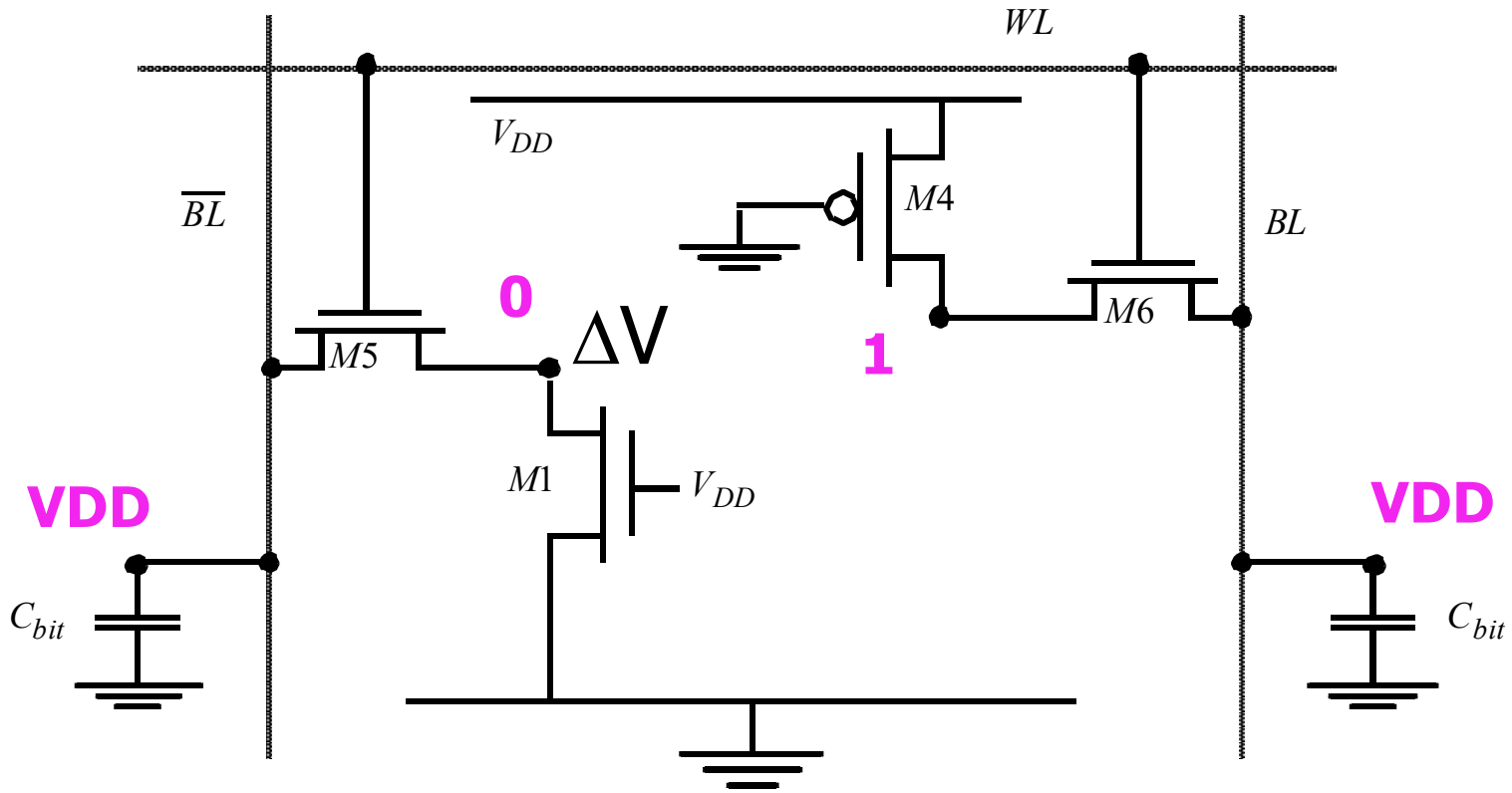
Assume 1 is stored (Q=1)

Read Operation:

- First bitlines get precharged high (Vdd)
- Then wordline goes high (Vdd)
  - Precharge disconnected

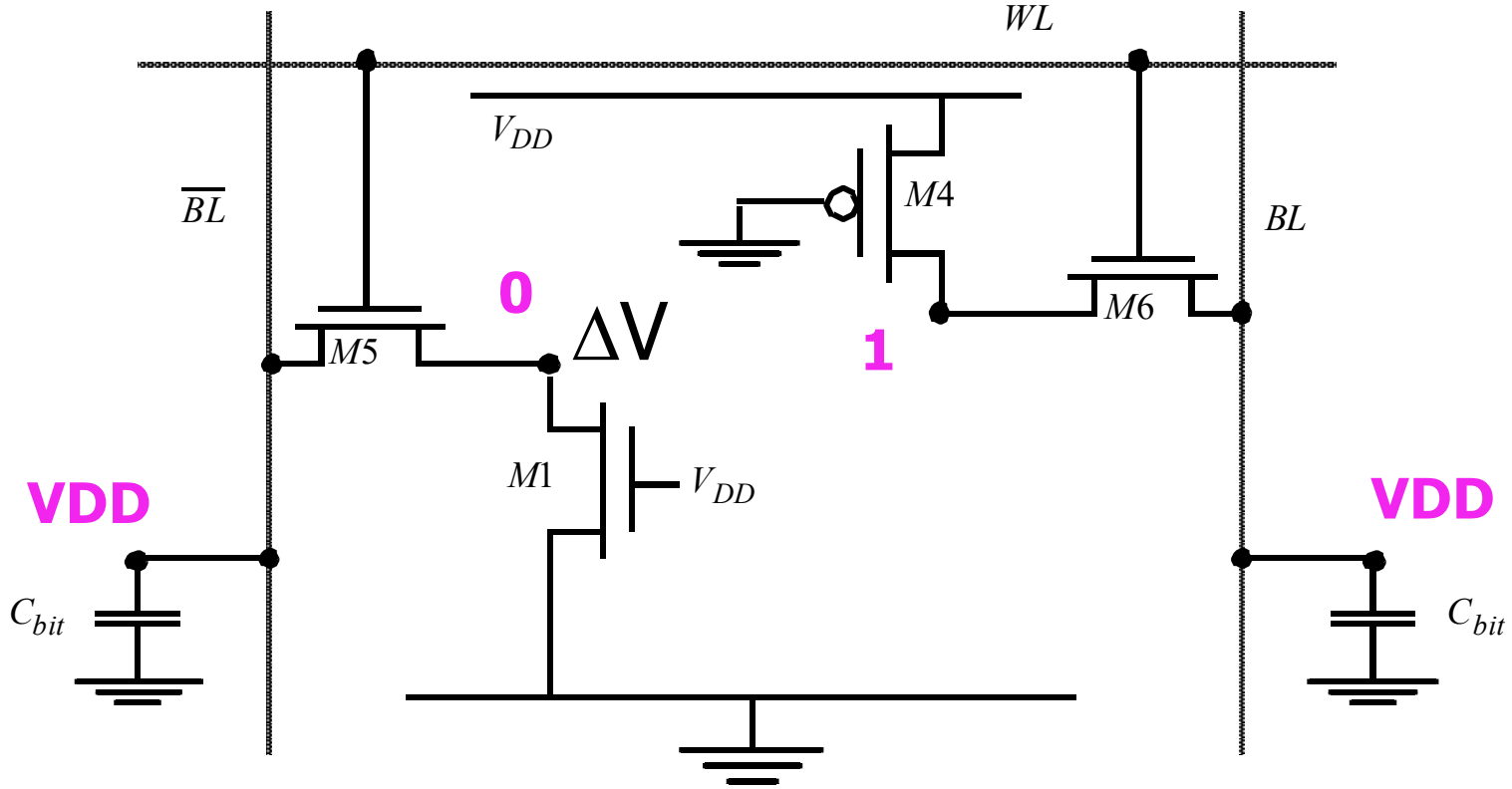


CMOS SRAM Analysis (Read) (preclass 1)



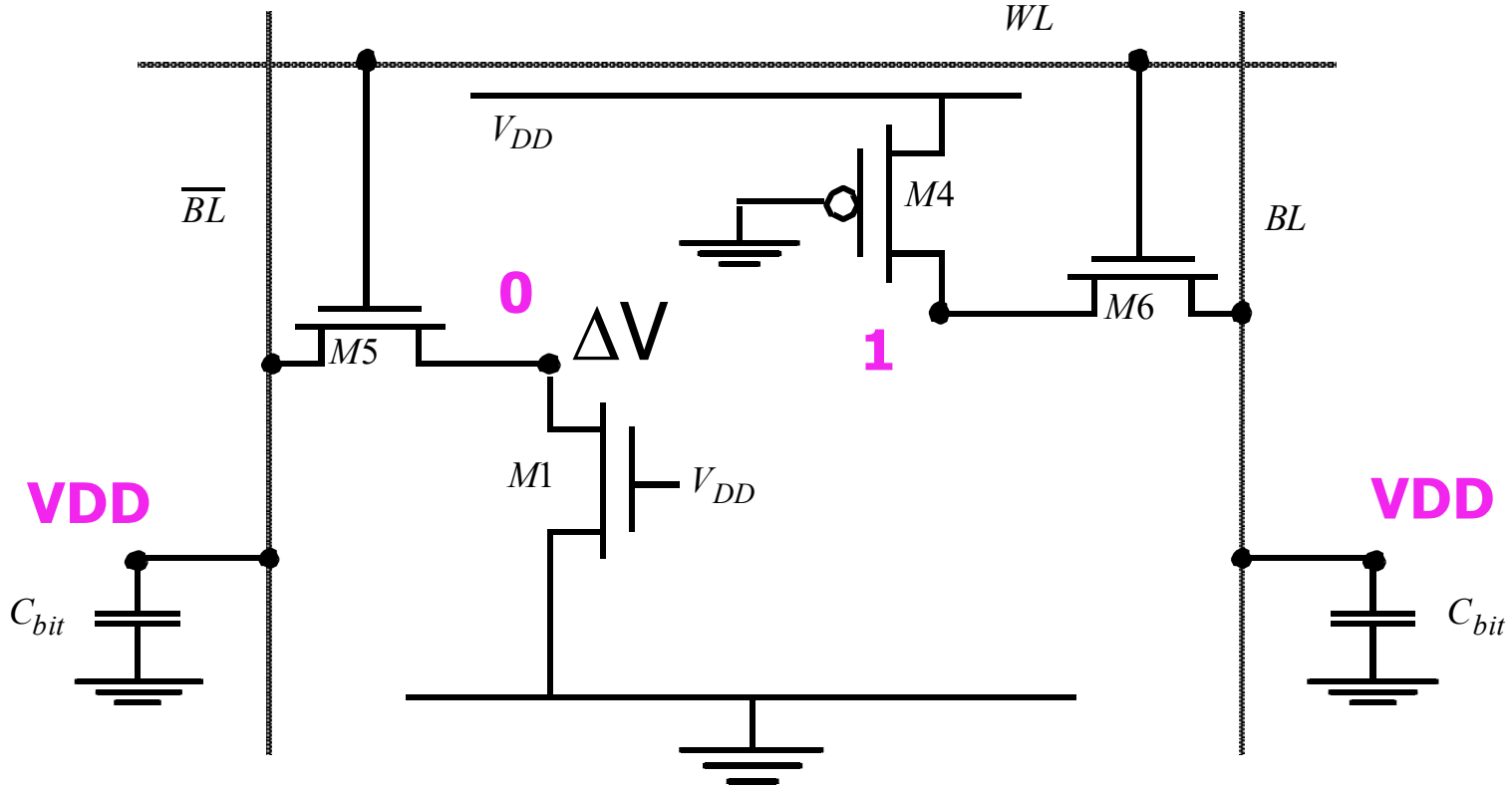
Which two transistors are discharging \BL to Gnd?
What regions of operation are the transistors in?
Write the KCL equation for the two transistors

CMOS SRAM Analysis (Read)



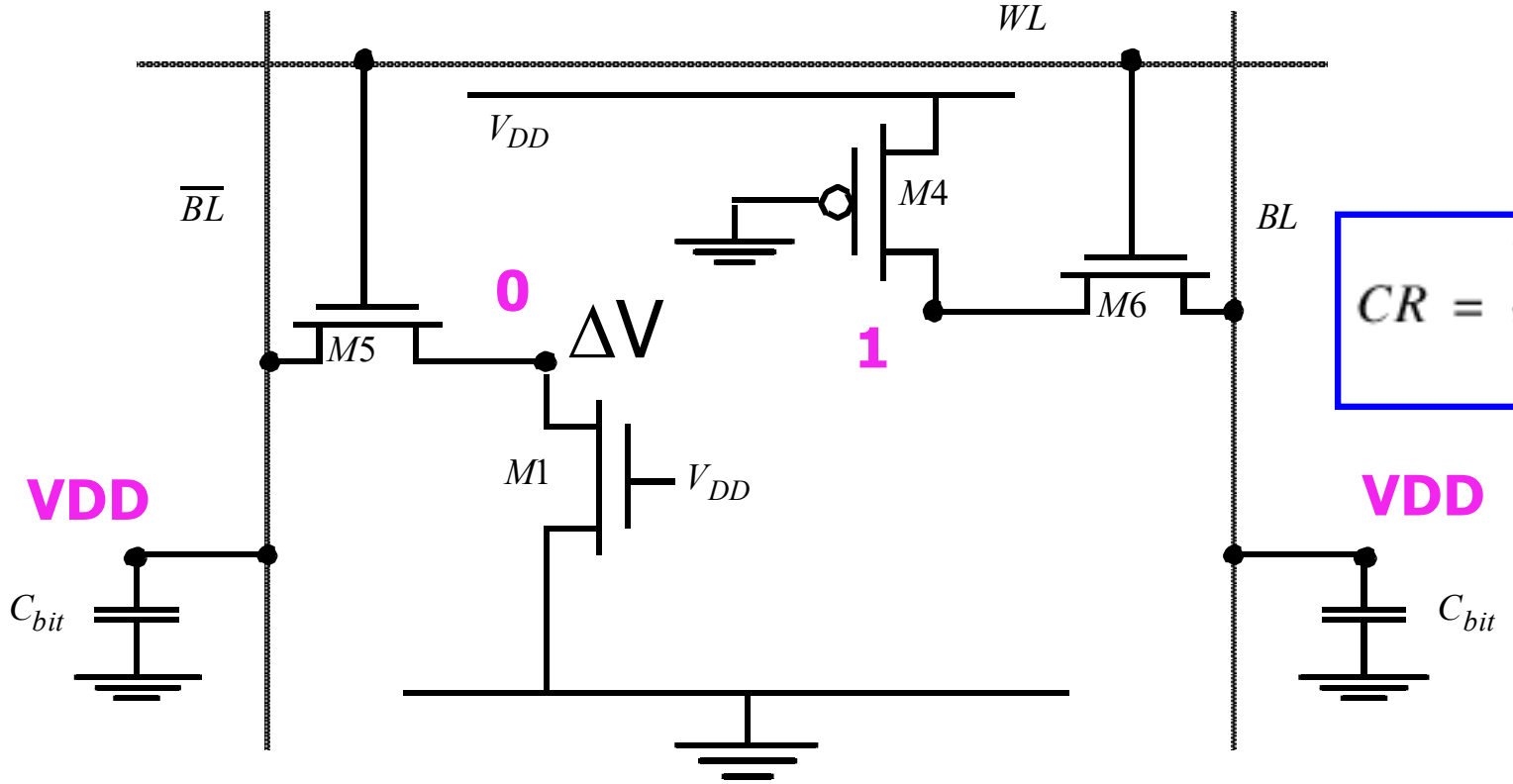
$$k_{n,M5}\left(V_{DD}-\Delta V-V_{Tn}\right)^2 = k_{n,M1}\left((V_{DD}-V_{Tn})\Delta V-\frac{\Delta V^2}{2}\right)$$

CMOS SRAM Analysis (Read)



$$\frac{k_{n,M1}}{k_{n,M5}} = \frac{\left(\frac{W}{L}\right)_1}{\left(\frac{W}{L}\right)_5} = \frac{\left(V_{DD} - \Delta V - V_{Tn}\right)^2}{(V_{DD} - V_{Tn})\Delta V - \frac{\Delta V^2}{2}}$$

CMOS SRAM Analysis (Read)



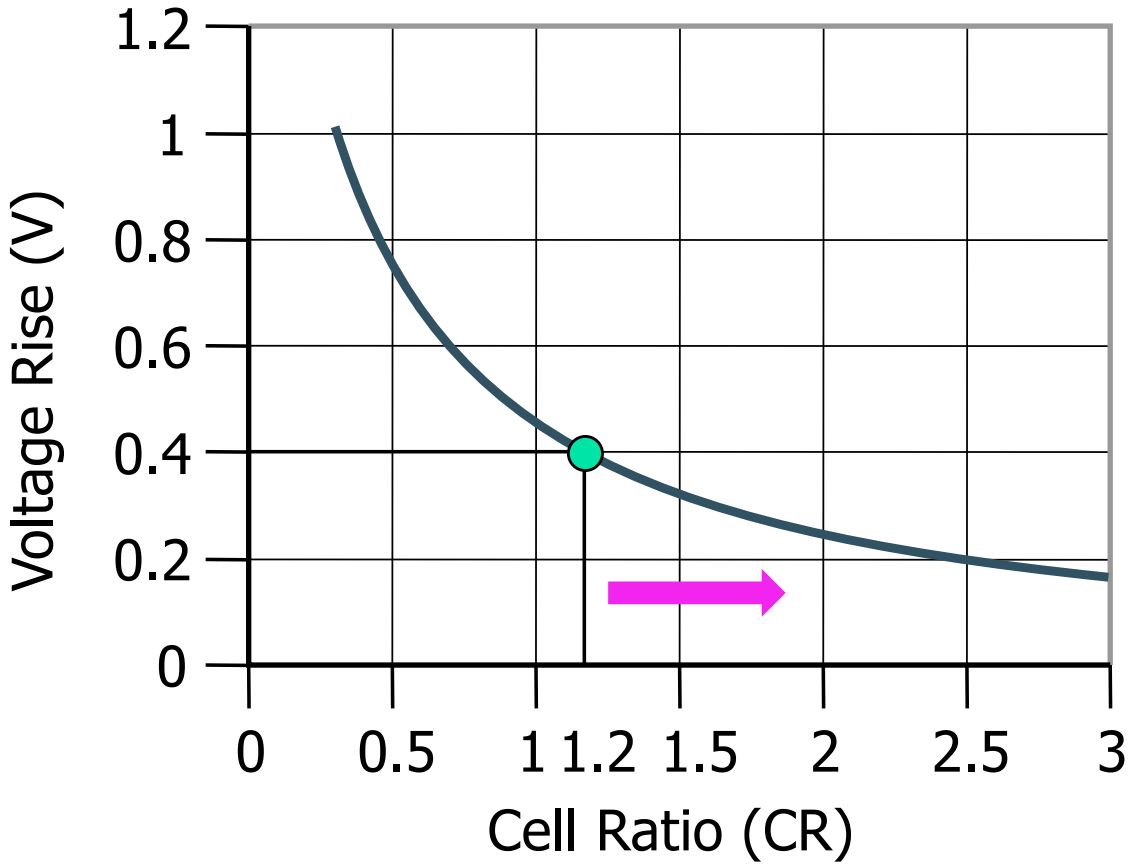
$$CR = \frac{W_1/L_1}{W_5/L_5}$$

$$\frac{k_{n,M1}}{k_{n,M5}} = \frac{\left(\frac{W}{L}\right)_1}{\left(\frac{W}{L}\right)_5} = \frac{\left(V_{DD} - \Delta V - V_{Tn}\right)^2}{(V_{DD} - V_{Tn})\Delta V - \frac{\Delta V^2}{2}}$$

$\Delta V = V_{Tn}$ →

$$\frac{\left(\frac{W}{L}\right)_1}{\left(\frac{W}{L}\right)_5} = \frac{\left(V_{DD} - 2V_{Tn}\right)^2}{(V_{DD} - 1.5V_{Tn})V_{Tn}}$$

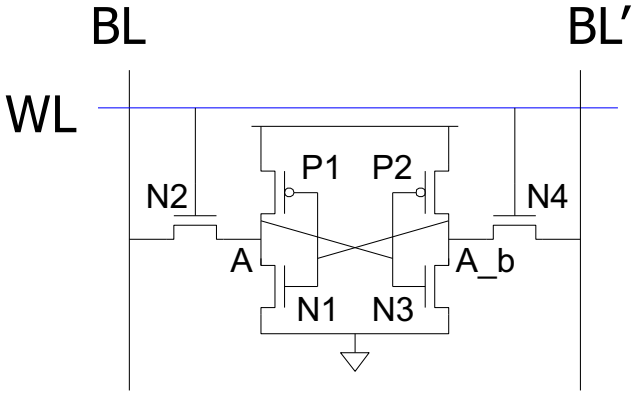
CMOS SRAM Analysis (Read)

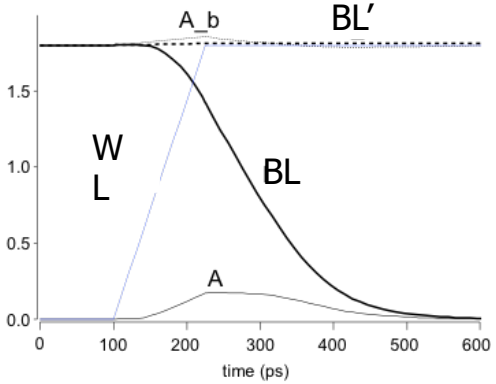


$$CR = \frac{W_1/L_1}{W_5/L_5}$$

SRAM Read

- Precharge both bitlines high
- Then turn on wordline, WL
- One of the two bitlines will be pulled down by the cell
- Ex: A = 0, A_b = 1
  - BL discharges, BL' stays high
  - But A bumps up slightly
- *Read stability*
  - A must not flip
  - N1 > N2



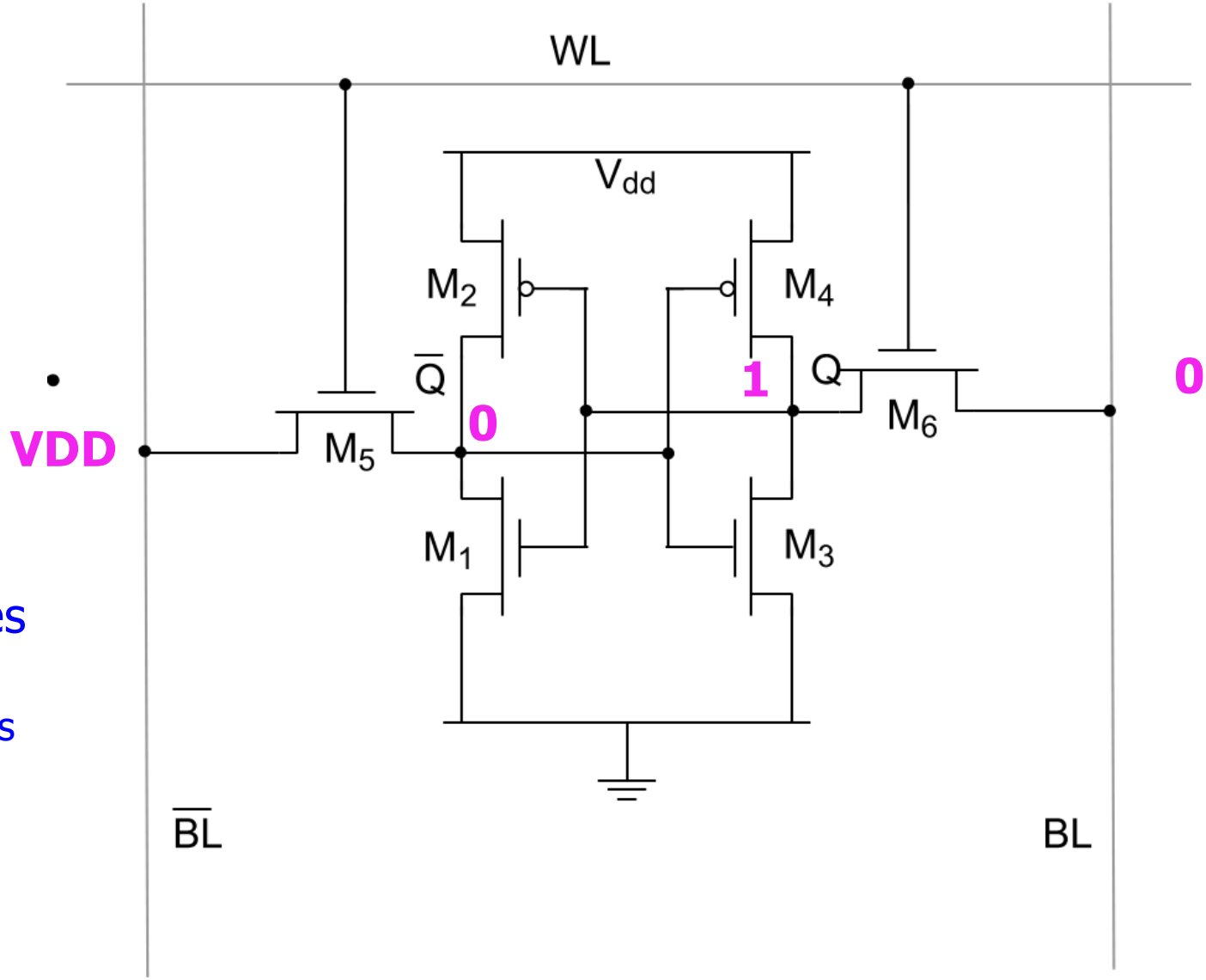


6-transistor CMOS SRAM Cell (preclass 2)

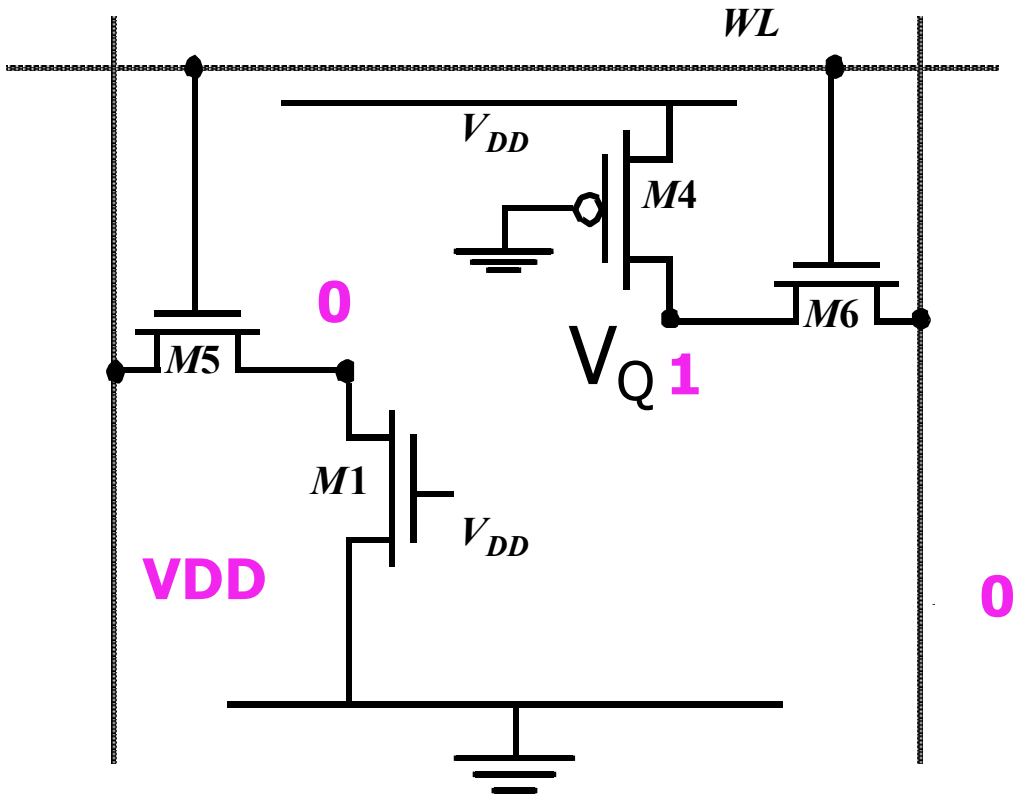
Assume 1 is stored (Q=1)

Write Operation:

- Want to write a 0
- First drive bitlines with input data
- Then wordline goes high (Vdd)
  - Still driving bitlines

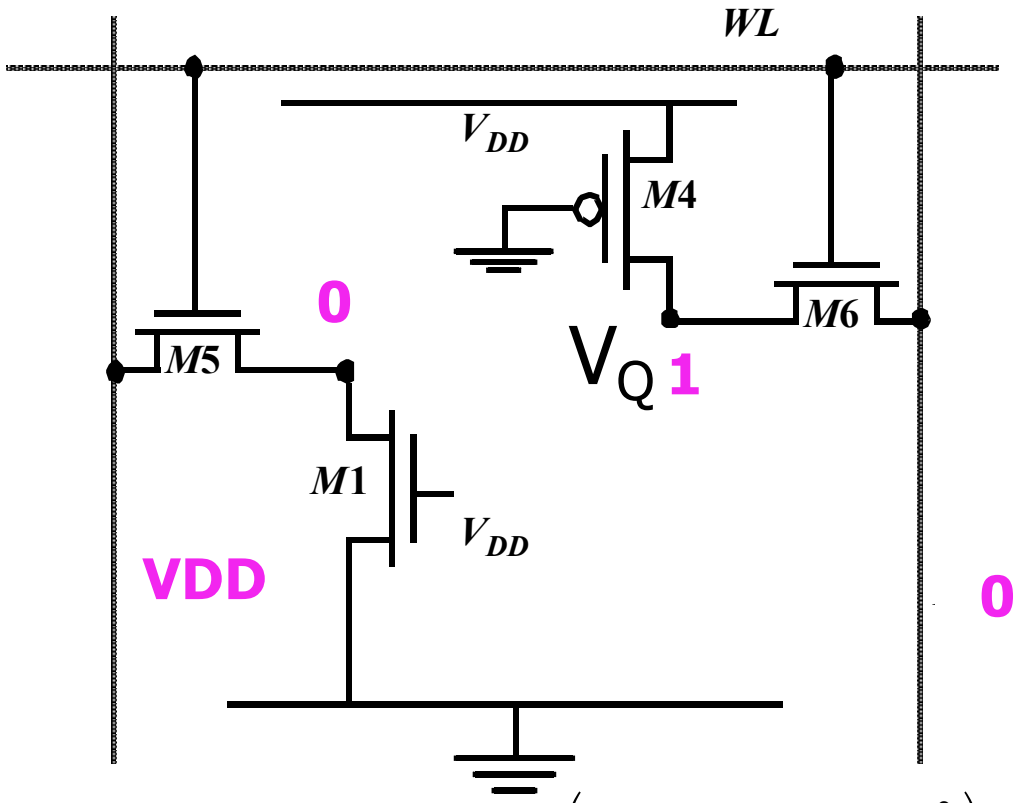


CMOS SRAM Analysis (Write) (preclass 2)



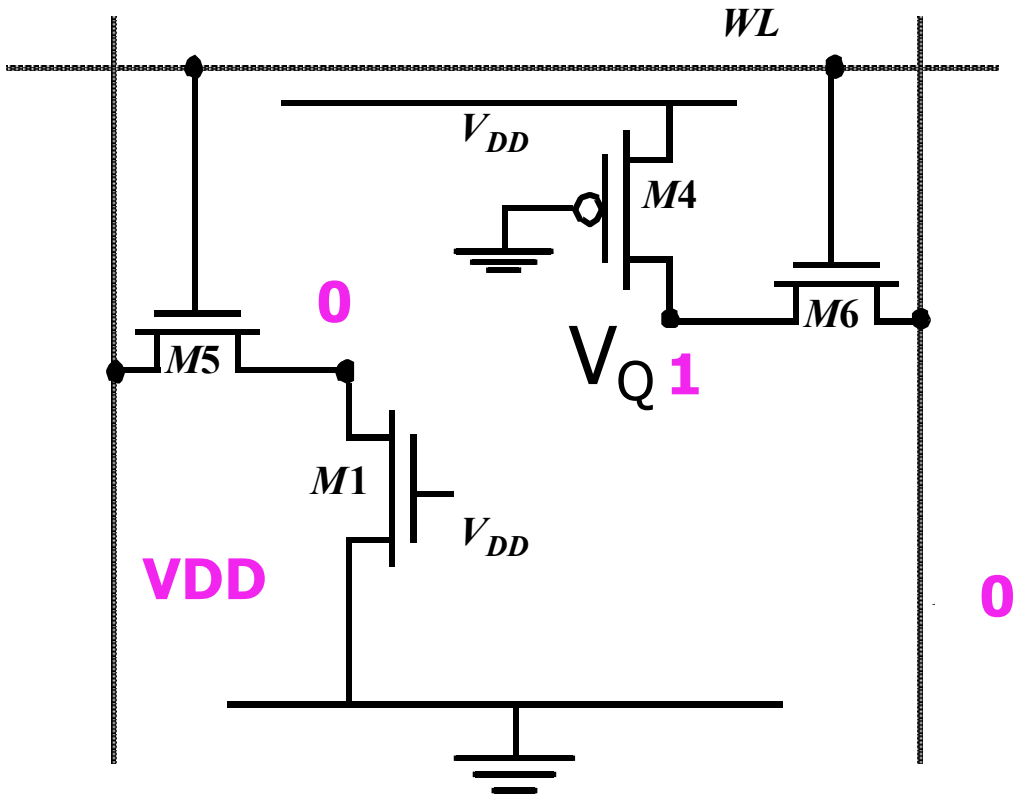
Which transistor discharges Q to Gnd?
Which transistor must it overpower?
What regions of operation are the transistors in?
Write the KCL equation for the two transistors

CMOS SRAM Analysis (Write)



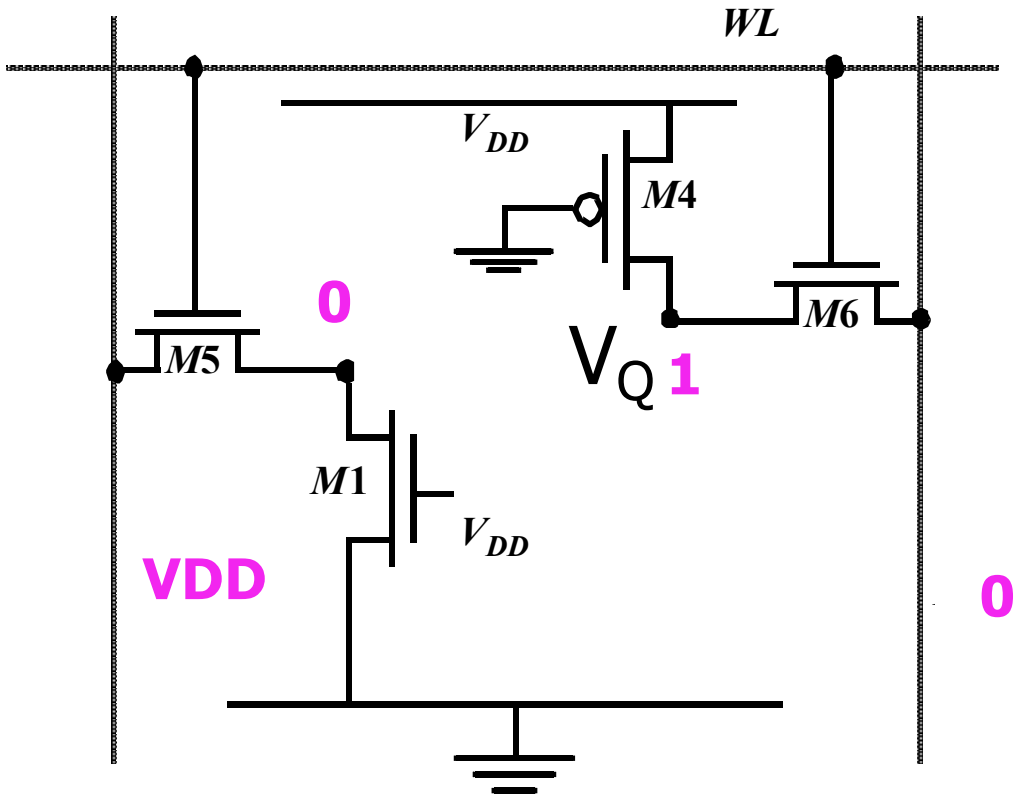
$$k_{p,M4}\left(V_{DD}-\left|V_{Tp}\right|\right)^2 = k_{n,M6}\left((V_{DD}-V_{Tn})V_Q-\frac{V_Q^2}{2}\right)$$

CMOS SRAM Analysis (Write)



$$\frac{k_{p,M4}}{k_{n,M6}} = \frac{(V_{DD} - V_{Tn})V_Q - \frac{V_Q^2}{2}}{\left(V_{DD} - |V_{Tp}|\right)^2}$$

CMOS SRAM Analysis (Write)



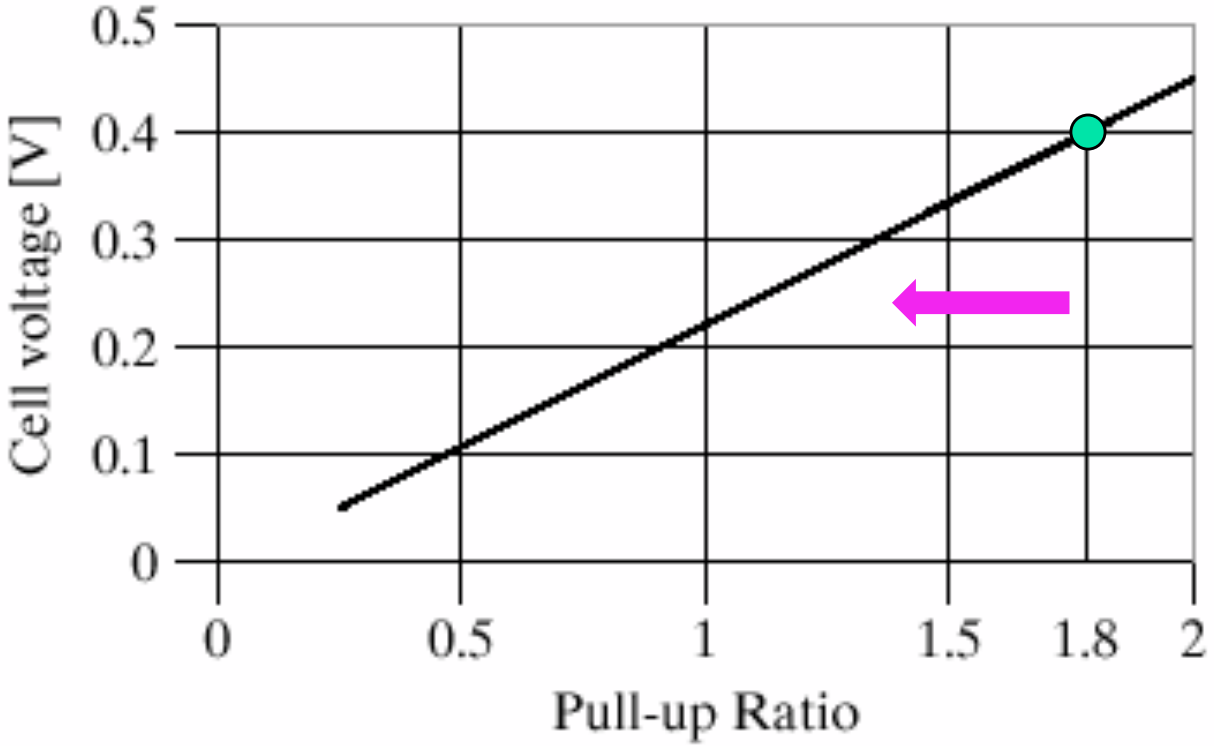
$$PR = \frac{W_4/L_4}{W_6/L_6}$$

$$\frac{k_{p,M4}}{k_{n,M6}} = \frac{(V_{DD} - V_{Tn})V_Q - \frac{V_Q^2}{2}}{\left(V_{DD} - |V_{Tp}|\right)^2}$$

$V_Q = V_{Tn}$

$$\frac{k_{p,M4}}{k_{n,M6}} = \frac{(V_{DD} - V_{Tn})V_{Tn} - \frac{V_{Tn}^2}{2}}{\left(V_{DD} - |V_{Tp}|\right)^2}$$

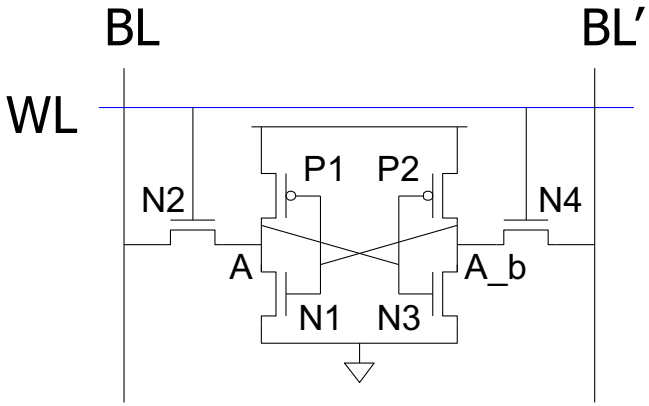
CMOS SRAM Analysis (Write)

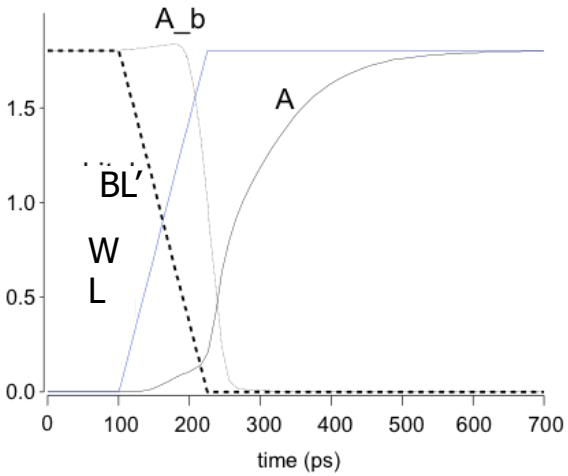


$$PR = \frac{W_4/L_4}{W_6/L_6}$$

SRAM Write

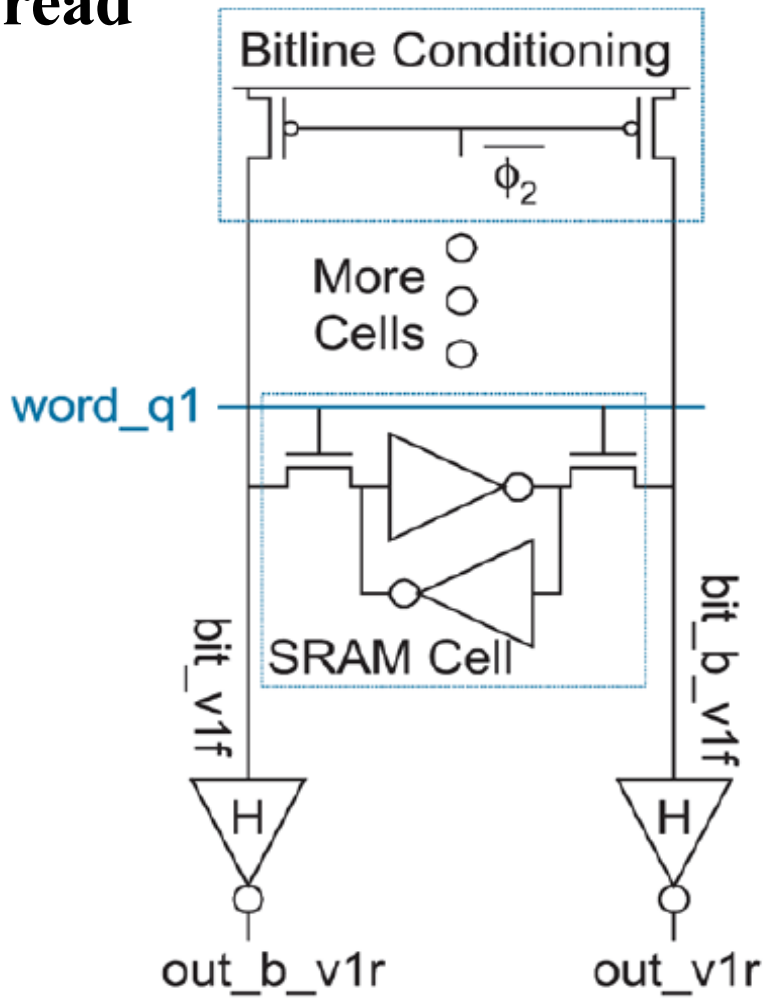
- Drive one bitline high, the other low
  - Depending on write data
- Then turn on wordline, WL
- Bitlines overpower cell with new value
- Ex: A = 0, A_b = 1, BL = 1, BL' = 0
  - Force A_b low, then A charges high
- *Writability*
  - Must overpower feedback inverter
  - N4 >> P2



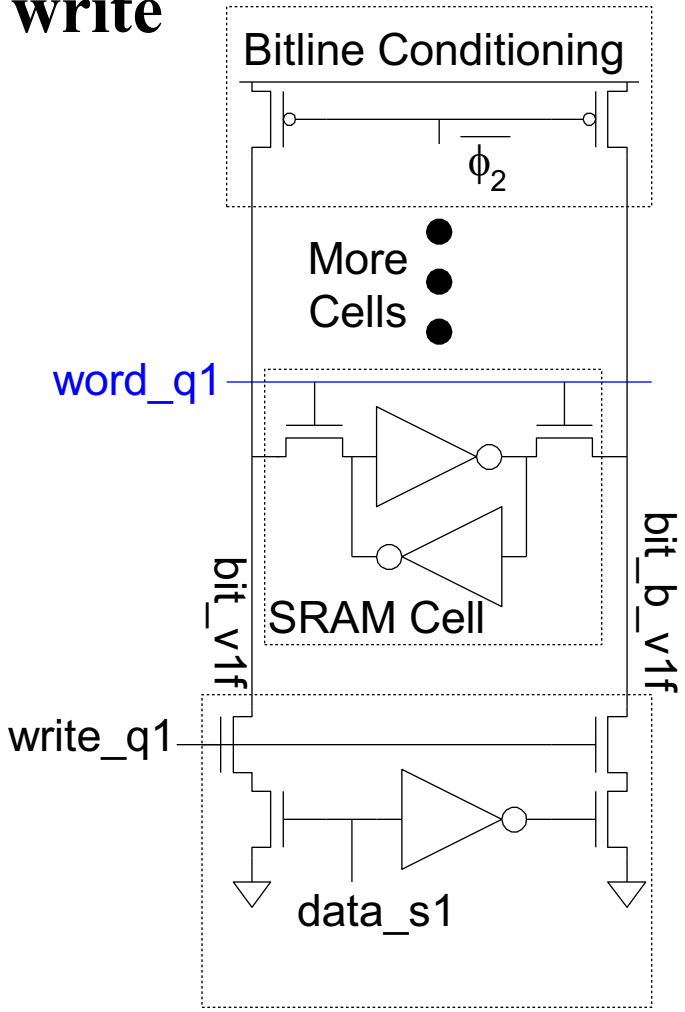


SRAM Column Example

read

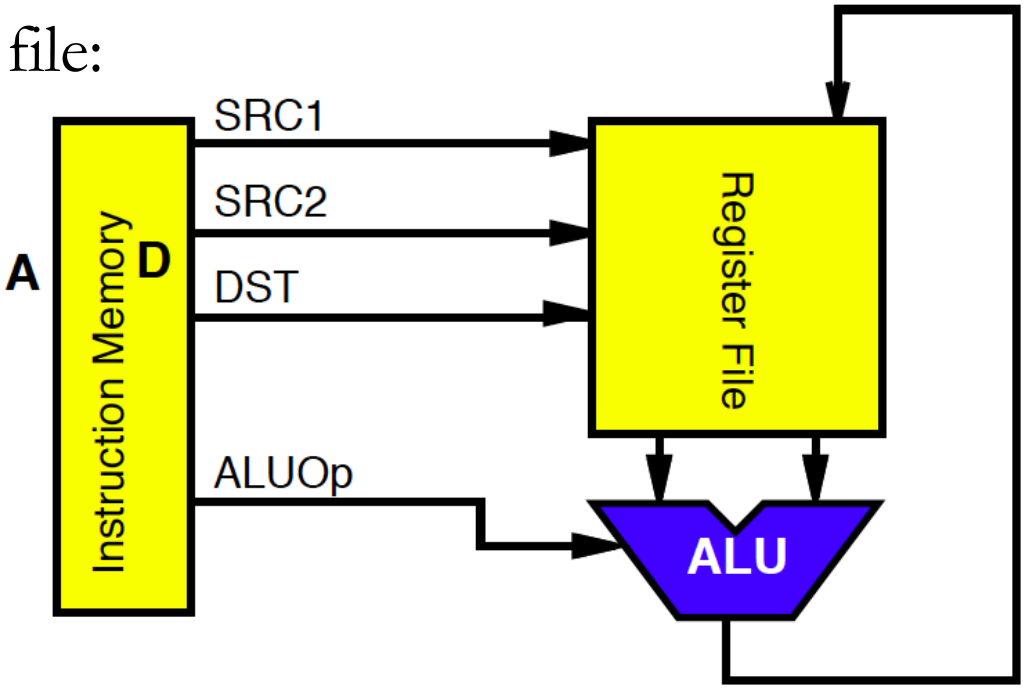


write



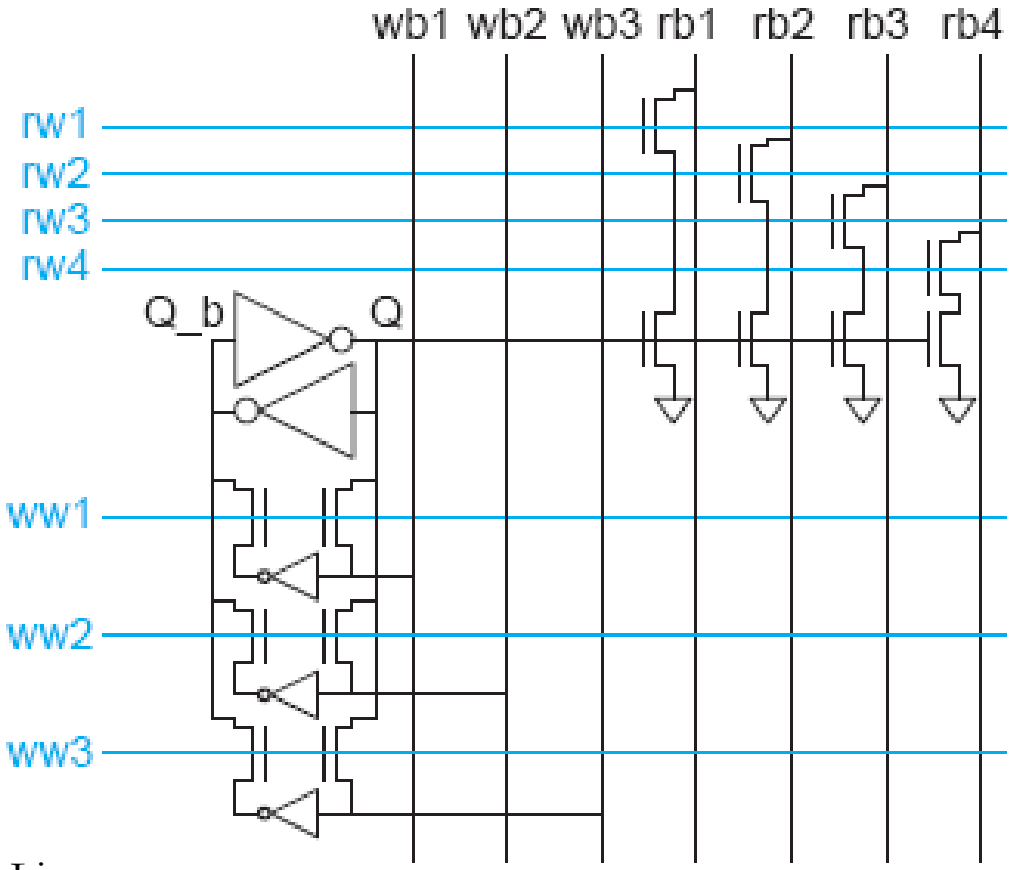
Multiple Ports

- We have considered single-ported SRAM
  - One read or one write on each cycle
- *Multiported* SRAM are needed for register files
- Examples:
  - Pipelined ALU register file:
    - add r1,r2,r3
    - R3←R1+R2
    - Requires two reads and one write



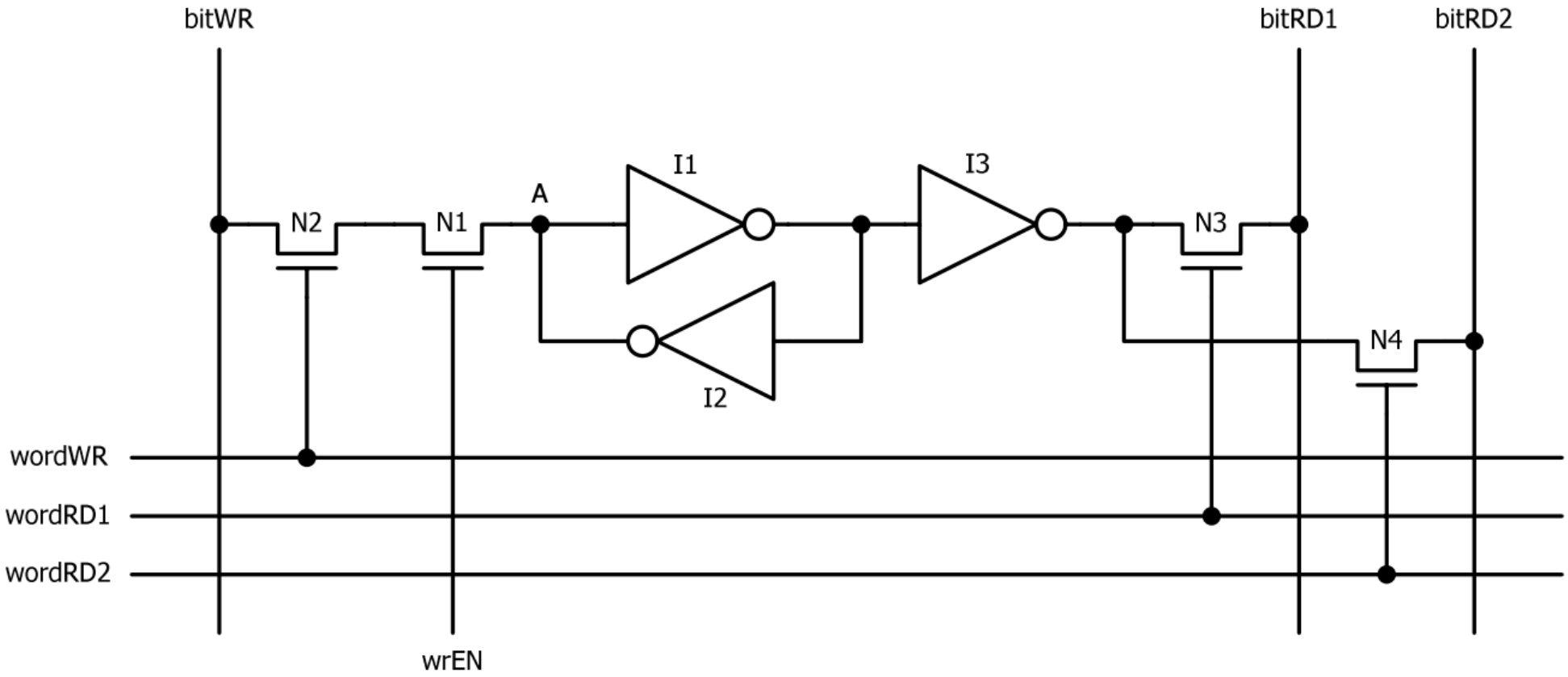
Multi-Ported SRAM

- Adding more access transistors hurts read stability
- Multiported SRAM isolates reads from state node
- Single-ended bitlines save area



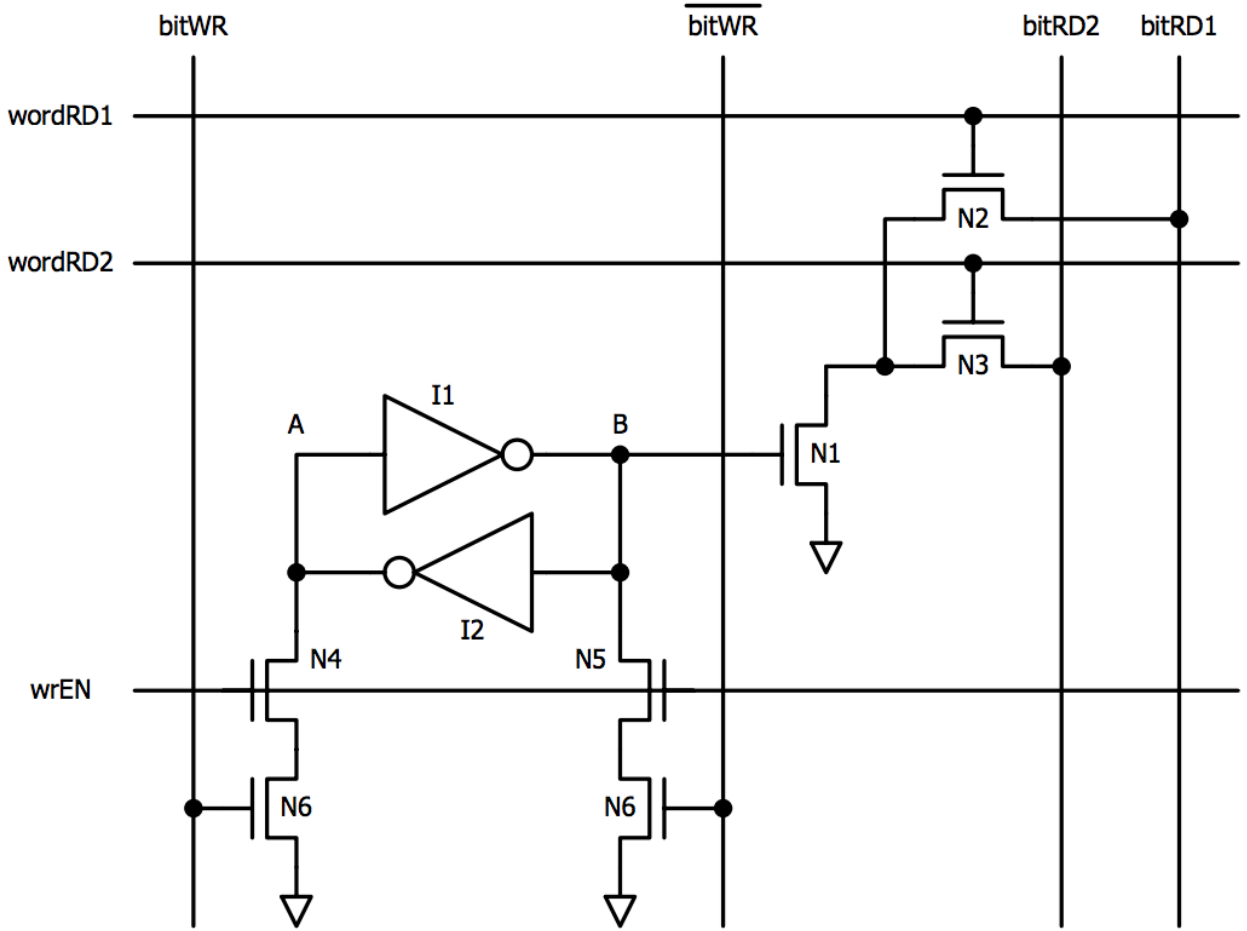
Register File Cell

- Single-ended 2-read/1-write ports (Slow-write)



Register File Cell

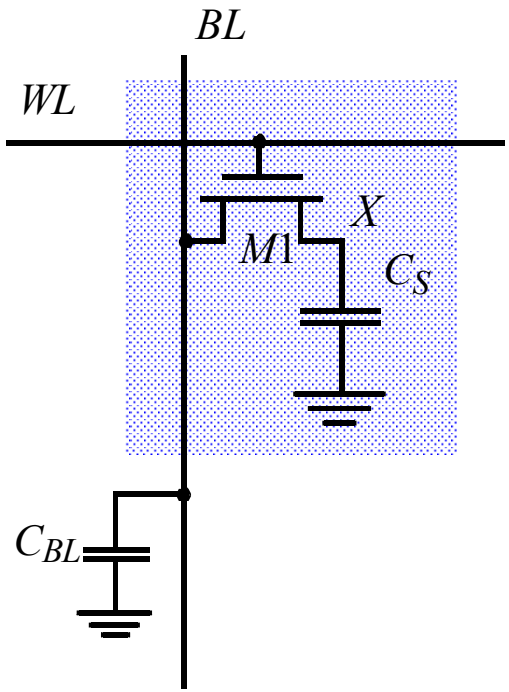
- Single-ended Read/Dual-ended Write



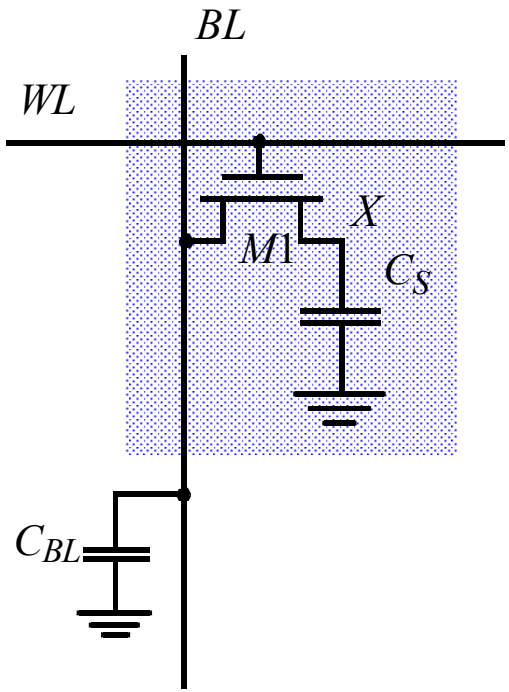
DRAM

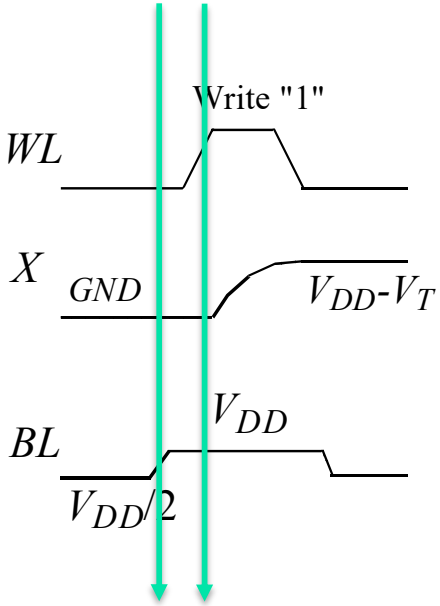
- Smaller than SRAM
- Require data refresh to compensate for leakage

1-Transistor DRAM Cell



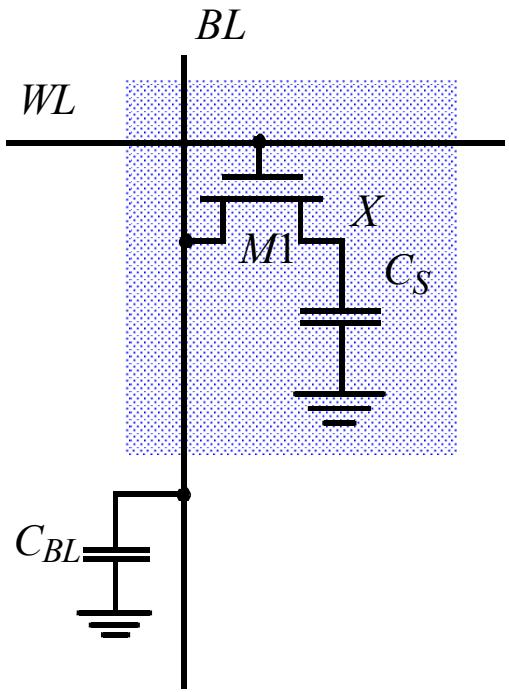
1-Transistor DRAM Cell

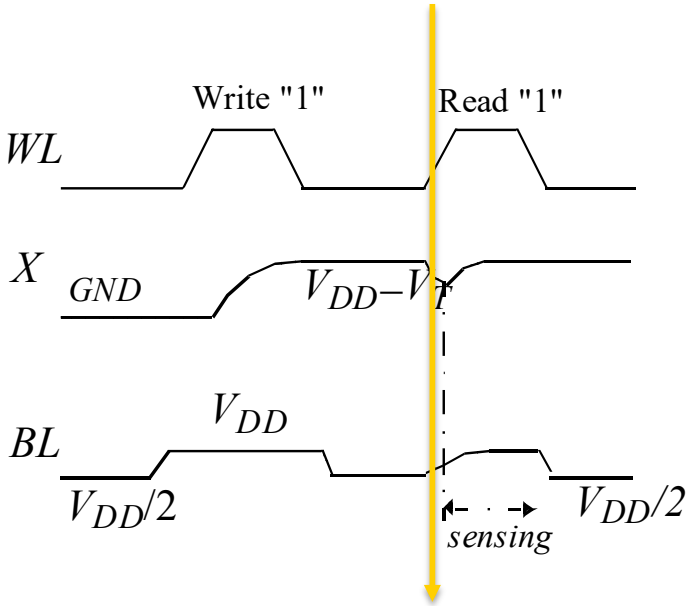




Write: C_S is charged or discharged by asserting WL and BL.

1-Transistor DRAM Cell



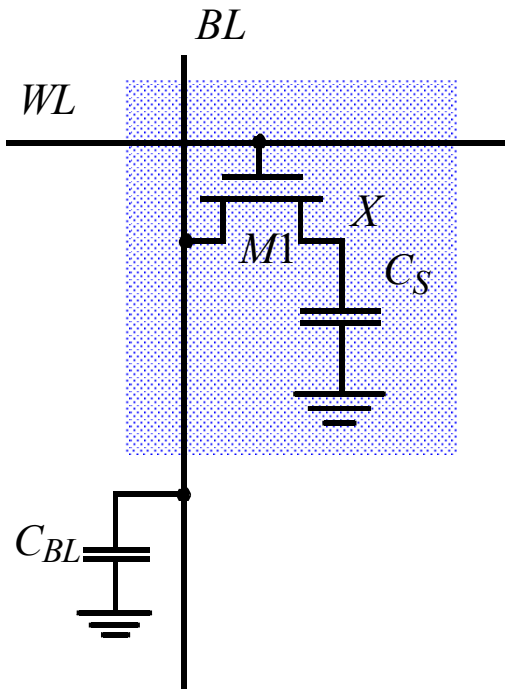


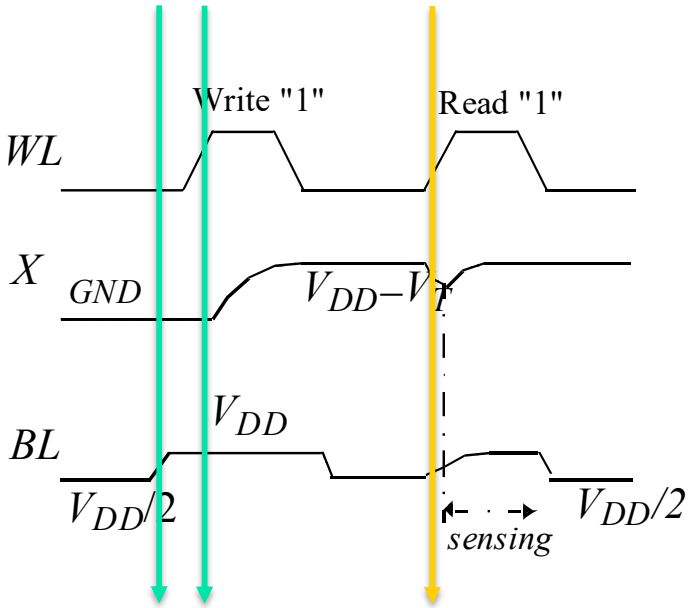
Write: C_S is charged or discharged by asserting WL and BL.
Read: Charge redistribution takes places between bit line and storage capacitance

$$\Delta V = V_{BL} - V_{PRE} = (V_{BIT} - V_{PRE})\frac{C_S}{C_S + C_{BL}}$$

Voltage swing is small; typically around 250 mV.

1-Transistor DRAM Cell





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Voltage swing is small; typically around 250 mV.

DRAM Cell Observations

- 1T DRAM requires a sense amplifier for each bit line, due to charge redistribution read-out
- DRAM memory cells are single ended in contrast to SRAM cells
- The read-out of the 1T DRAM cell is destructive; read and refresh operation are necessary for correct operation
- 1T cell requires presence of an extra capacitance that must be explicitly included in the design
- When writing a "1" into a DRAM cell, a threshold voltage is lost. This loss can be circumvented by bootstrapping the word lines to a higher value than V_{DD}.

Big Idea

- 6T SRAM
  - Robust cell when sized carefully
- 5T SRAM
  - More sensitive to sizing than 6T SRAM
- Minimize area of repeated cell
  - 6T/5T SRAM
  - Mulitport trade off area for function
  - 1T/3T DRAM helps but slower
- Compensate with periphery
  - Decoders
  - Bitline (column) drivers
  - Sensing/Amplification (regeneration/restoration)

Admin

- Project 2 out - START NOW!
  - Work in teams up to 2
  - Final report due 4/26

Acknowledgement

- Prof. André DeHon (University of Pennsylvania)
- Prof. Tania Khanna (University of Pennsylvania)