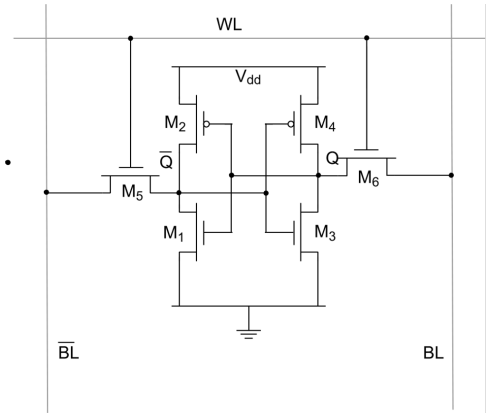
Below is the 6T SRAM cell. We will look at the operation of this cell through a read operation and then a write operation to change the bit value stored in the cell.



1. Assume the cell has a 1 stored ($Q = 1$, $\overline{Q} = 0$). During the read operation the bitlines (BL & $\overline{BL}$) are precharged high, and then the wordline (WL) goes high.

   (a) Which two transistors are discharging $\overline{BL}$ to Gnd?

   (b) What regions of operation are the transistors in?

   (c) Assuming the node between the two transistors has a peak voltage of ΔV, write the KCL equation for the two transistors.

2. Again assume the cell has a 1 stored ($Q = 1$, $\overline{Q} = 0$). During the write operation the bitlines (BL & $\overline{BL}$) are driven with the write data such that $BL = 0$ and $\overline{BL} = V_{dd}$, and then the wordline (WL) goes high.

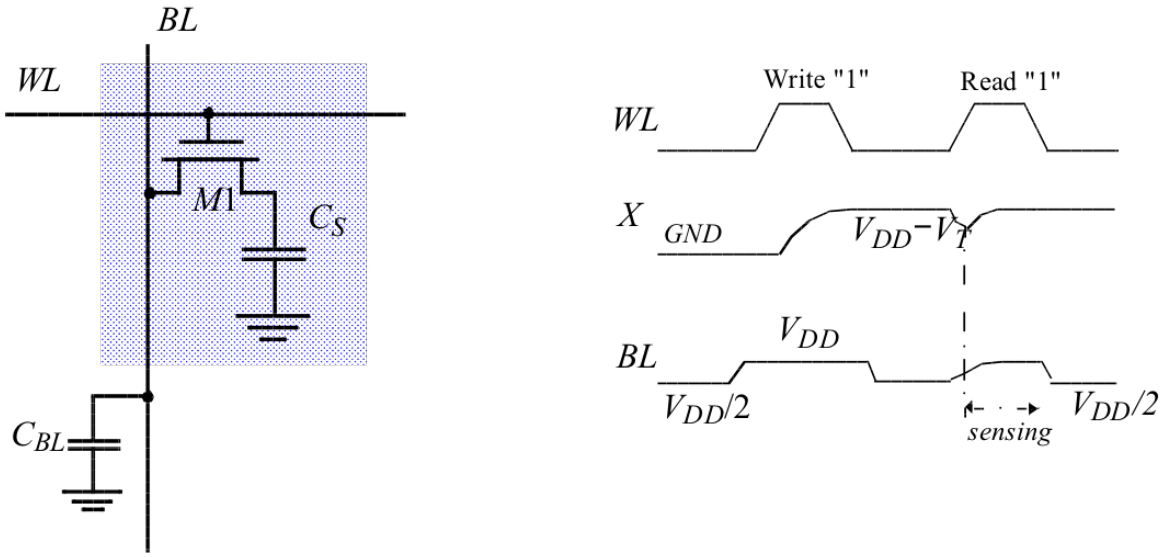
   (a) Which transistor discharges Q to Gnd?

   (b) Which transistor must it overpower to discharge Q?

   (c) What regions of operation are the transistors in?

   (d) Assuming the voltage at Q is V_Q, write the KCL equation for the two transistors.

3. Below is the 1T DRAM cell with waveform for writing a '1' into the cell and then reading the cell.



4. What are some differences between DRAM and SRAM cells?