Course Webpage

Circuit-Level Modeling, Design, and Optimization for Digital Systems

Course: ESE370

Units: 1.0 CU
Term: Spring 2022
When: MW 8:30-10am EST (all times below are EST)
Where: Towne 303
Instructor: Jing (Jane) Li (Levine 274, seas: janeli)
Instructor Office Hours: W 2-3pm (via Zoom, see Piazza for link), or by appointment
TA: Aaron Shurberg (seas: aaronshu) (office hours: TBA)
TA: Neil Chitalia (seas: nchitali) (office hours: TBA)

Prerequisites: ESE 150, ESE 215, CIS 240 is also highly recommended. Roundup of topics you should be familiar with.
URL: <http://www.seas.upenn.edu/~ese370/>

Quick Links: [Course Objectives] [Grading] [Policies] [Fall 2021 Calendar] [Reading] [Student Advice] [Piazza] [Tool Guides]

Catalog Level Description: Circuit-level design and modeling of gates, storage, and interconnect. Emphasis on understanding physical aspects which drive energy, delay, area, and noise in digital circuits. Impact of physical effects on design and achievable performance.

Role and Objectives

The goal of this course is to teach students what they need to know about the physical aspects (area, delay, energy, noise) of electronic circuits to support high-speed, low-energy, area-efficient design of robust digital and computer systems. Students will learn:

- disciplines for robust digital logic and signaling (e.g., restoration, clocking, handshaking)
- where delay, energy, area, and noise arises in gates, memory, and interconnect
- how to model these physical effects both for back-of-the-envelope design (e.g. RC and Elmore delay) and detailed simulation (e.g., SPICE)
- the nature of tradeoffs in optimization
- how to design and optimize logic, memory, and interconnect structures at the gate, transistor, and wire level
- how technology scales and its impact on digital circuits and computer systems

https://www.seas.upenn.edu/~ese370/

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ESE370: Circuit-Level Modeling, Design, and Optimization for Digital Systems

Lec 1: January 12, 2022
Introduction and Overview

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Your First Priority

- Your first priority is your health
  - You should abide by all health guidelines
    - Wear a mask
    - Wash your hands
    - Don't touch your face
    - Maintain ~~social~~ physical distancing
      - Careful and thoughtful social interaction is encouraged!
    - Stay home if you're sick
    - Complete PennOpen Pass daily
  - Part of your health is your mental and emotional health
    - See https://caps.wellness.upenn.edu/selfhelp/ for help
  - For more: https://coronavirus.upenn.edu/

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I want to hear from you…

- Accessibility Survey in Canvas
  - Submit by Saturday (1/22/2022) for full HW credit
- Are there any other accessibility issues I should know about?
- Let me know any concerns -- I will do everything I can to ensure you achieve the learning objectives

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Course Structure: Staff

- Course Staff (complete info on course website)
- Instructor: Jing (Jane) Li (she/her)
  - Virtual OH: W 2-3pm
  - Or by appointment
  - Email: janeli@seas.upenn.edu
    - Best way to reach me
- Website: https://li.seas.upenn.edu/

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TA: Aaron Shurberg

- About me: I am a senior in CMPE. ESE370 was one of my favorite courses. It was a very demanding yet rewarding course. Outside of class I enjoy watching basketball.
- OH:
  - TBD

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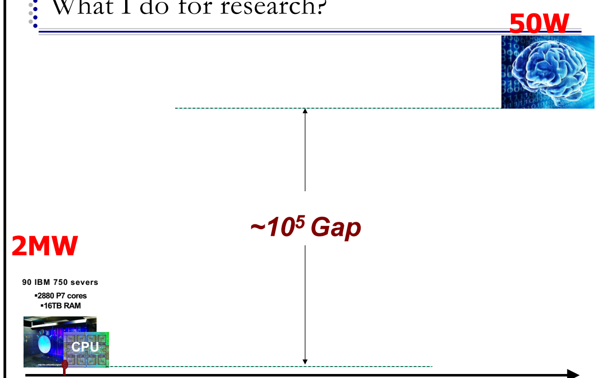
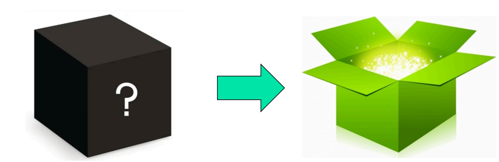
TA: Neil Chitalia

- About me: I am a Senior studying Computer Engineering and Business from Bloomfield Hills, Michigan. Outside the classroom, I play and watch basketball and football and participate in FPGA research in the ESE department.
- OH:
  - TBD

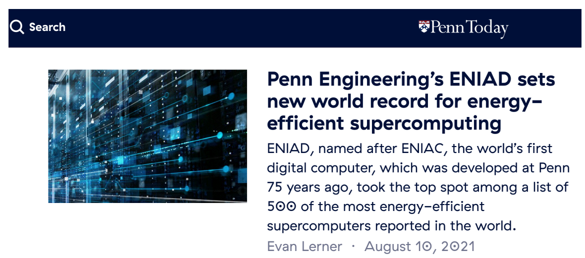
What I do for research?



What I do for research?



What I do for research? (a recent highlight)

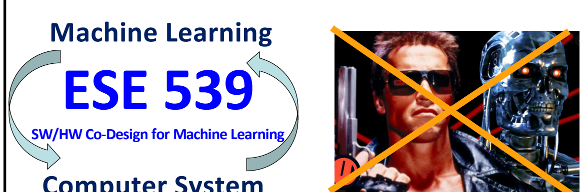


https://penntoday.upenn.edu/news/penn-engineerings-eniad-sets-new-world-record-energy-efficient-supercomputing

What I do for research? (a vision on memory)

https://www.youtube.com/watch?time_continue=3&v=67VKORQX4T4&feature=emb_logo

What I do for research/teaching?



SysML: The New Frontier of Machine Learning Systems

Alexander Ratner, Dan Alistarh, Gustavo Alonso, Peter Bailis, Sarah Bird, Nicholas Carlini, Bryan Catanzaro, Eric Chung, Bill Dally, Jeff Dean, Inderjit S. Dhillon, Alexandros Dimakis, Pradeep Dubey, Charles Elkan, Grigori Fursin, Gregory R. Ganger, Lise Getoor, Phillip B. Gibbons, Garth A. Gibson, Joseph E. Gonzalez, Justin Gottschlich, Song Han, Kim Hazelwood, Furong Huang, Martin Jaggi, Kevin Jamieson, Michael I. Jordan, Gauri Joshi, Rania Khalaf, Jason Knight, Jakub Konečný, Tim Kraska, Arun Kumar, Anastasios Kyrillidis, Jing Li, Samuel Madden, H. Brendan McMahan, Erik Meijer, Ioannis Mitliagkas, Rajat Monga, Derek Murray, Dimitris Papailiopoulos, Gennady Pekhimenko, Theodoros Rekatsinas, Afshin Rostamizadeh, Christopher Ré, Christopher De Sa, Hanie Sedghi, Siddhartha Sen, Virginia Smith, Alex Smola, Dawn Song, Evan Sparks, Ion Stoica, Vivienne Sze, Madeleine Udell, Joaquin Vanschoren, Shivaram Venkataraman, Rashmi Vinayak, Markus Weimer, Andrew Gordon Wilson, Eric Xing, Matei Zaharia, Ce Zhang, Ameet Talwalkar

White Paper: https://arxiv.org/abs/1904.03257

Algorithm/Theory — CIS 419/519/421/521/520/522 /526/620/625……

Software — ESE539 HW/SW ML — **CIS**

Embedded Sys: ESE350/519 — **ESE**

Systems — SoC Arch: ESE 532

Processors — Processor Arch: CIS 371/501 (CIS240) — Mixed Signal: ESE 568 — ADC, DAC Switched Capacitors

Gates, Memories Circuits/VLSI — Digital: ESE370/570 — Analog: ESE419/572 — Amplifier, Compare Voltage/Current Ref.

Transistors — Devices: ESE521 (ESE218)

Adapted from Prof. Andre DeHon's slides

Penn — Hardware/Software Co-Design for Machine Learning — Li Fall 2021 © Penn — 13

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Lecture Outline

- Course Overview
  - Motivating questions
  - What this course is about
  - Learning objectives
  - What you need to know
- Course Details
  - Course structure
  - Course policies
  - Course content

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Virtually all apps will become AI centric

Ion Stoica, SIGMOD'20

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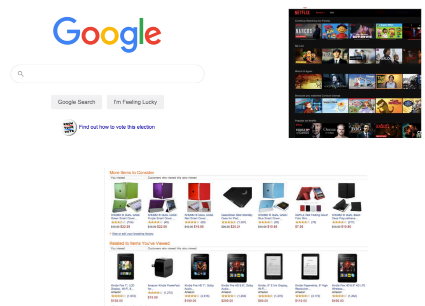

Image source: google

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Image source: google

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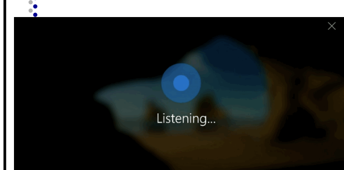
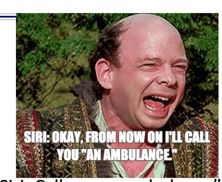
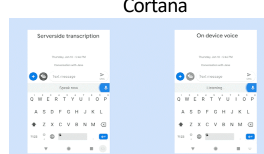


Cortana



"Siri, Call me an ambulance"



Speech To Text

"Remember when people typed with two fingers? My voice is faster."

Source of Gifs: http://www.impactlab.net/2016/10/26/microsofts-speech-recognition-is-now-as-accurate-as-a-humans/; https://www.nextbigfuture.com/2019/04/google-has-80-mb-speech-recognizer-that-can-work-offline-on-your-smartphone.html; https://media.giphy.com/media/LYIgUG96n20h2/giphy.gif

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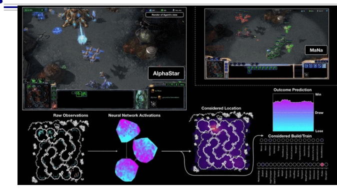
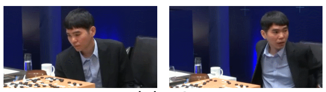



AlphaStar : StarCraft II



Alpha Go

Source of Gifs: https://www.techspot.com/news/78431-human-player-finally-beat-deepmind-alphastar-ai-starcraft.html; https://imgur.com/gallery/aPw2D; Matthew Inkawhich's RT meeting Slides

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"Behind the Scene": Machine Learning System

Harry Potter Movie

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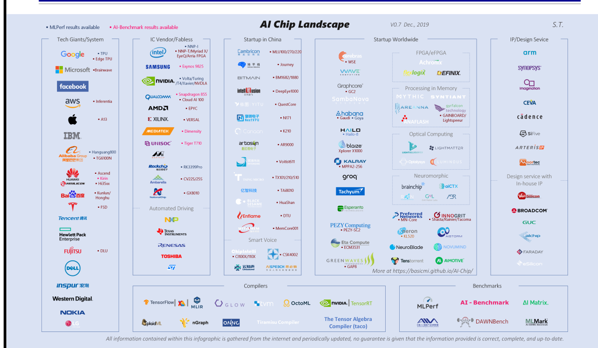
AI Chip Landscape: More Demand



https://github.com/basicmi/AI-Chip

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Ubiquitous Supercomputer: Smaller Scale, Heavily Integrated

Cray 2, 1985	iPhone 4, 2010	Apple Watch, 2015	**~ 2B FLOPs**
CM-5, 1991	2x Samsung S6	1 Haswell Core	**~100B FLOPs**
IBM ASCI Red, 2000	Playstation 4, 2013	32-core Haswell	**~3,000B FLOPs**

https://pages.experts-exchange.com/processing-power-compared


https://www.datacenterknowledge.com/supercomputers/

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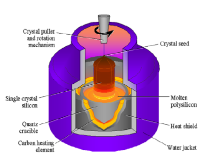
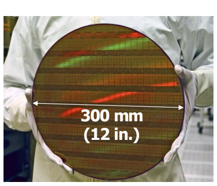
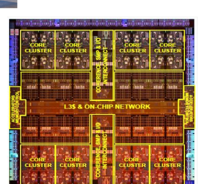
VLSI Design









Oracle SPARC M7 Processor

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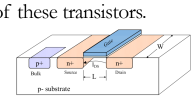
What this course about?

To build something you have to understand what building blocks you have available to you.

To build something really cool you need to have a fairly intimate understanding of how those building blocks work.

In VLSI our two primary building blocks are the NMOS and PMOS transistors. This is not a device physics course, but we will have to dive a bit into the workings of these transistors.



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Motivating Questions

- How fast can my computer run?
  - What limits this speed?
  - What can I do to make it run faster?
- How can I extend the battery life on my gadget?
  - How much energy must my computation take?
- How small can I make a memory?
  - What is SRAM? DRAM? Or Storage Class Memory (SCM)
  - Why does DRAM need to be refreshed? …

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Motivating Questions (con't)

- How many bits/second can I send over a communication link?
  - What limits this?
  - How do I maximize my data rate?
- How does technology scaling change these answers?
  - What can I rely on technology to deliver?

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Motivating Questions (con't)

- How many bits/second can I send over a communication link?
  - What limits this?
  - How do I maximize my data rate?
- How does technology scaling change these answers?
  - What can I rely on technology to deliver?
- How does my application change these answers?
  - Is fastest best? Is lowest energy best? Is smallest best?

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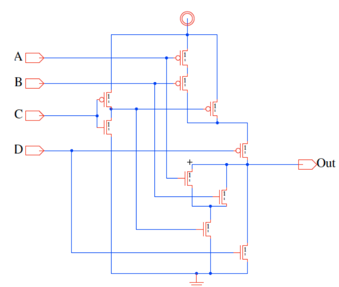
Sample Problems

- What does this circuit do?



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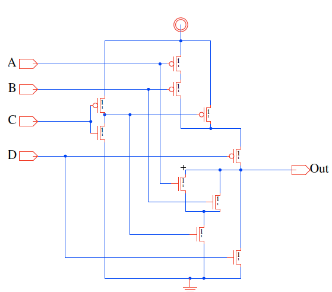
Sample Problems

- What does this circuit do? How fast does it operate?



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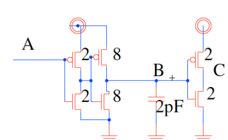
Sample Problems (con't)

- What does this circuit do? How are A, B, C related?



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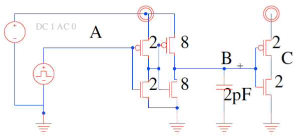
Sample Problems (con't)

- What does this circuit do? How are A, B, C related?



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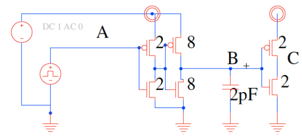
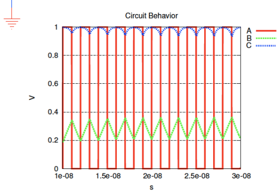
Sample Problems (con't)

- What's wrong here? How do we fix it?





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Limits?

- Consider a 22nm technology
- Typical gate with W=3, 2-input NOR
- Use chip in cell phone
- What prevents us from running 1 billion transistor chip at 10GHz?

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Impact of Voltage?

- If we have a chip running at 1GHz with a 1V power supply dissipating 1W.
- What happens to performance if we cut the power supply to 500mV?
  - Speed?
  - Power?

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What this course is about

- Modeling and abstraction
  - Predict circuit behavior
  - …well enough to know your design will work
  - …with given performance spec(ification)s
    - Speed, energy, size, etc.
  - …well enough to reason about design and optimization
    - What knob can I turn to make faster?
    - How much faster can I expect to make it?

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What this course is about (con't)

- Modeling and abstraction
  - Back-of-the-envelope calculations
    - Simple enough to reason about and estimate
      - …without a calculator
  - Sensitive to phenomena
    - Able to think through the details
  - With computer assistance
    - …understanding even that is a simplified approximation of phenomenology

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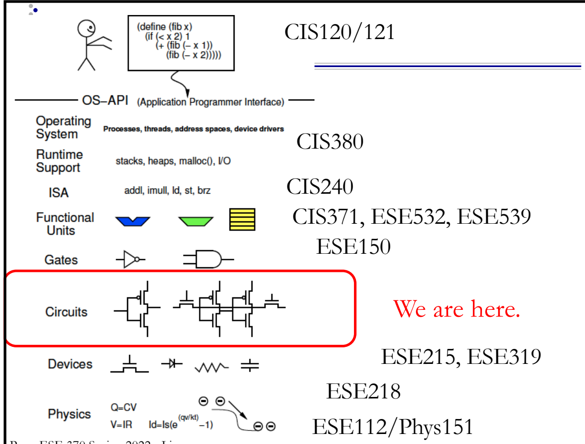

Learning Objectives

- Disciplines for robust digital logic and signaling
  - (*e.g.*, regeneration, clocking)
- Where delay, energy, area, and noise arise in gates, memory, and interconnect
- Modeling these physical effects
  - back-of-the-envelope design
    - (*e.g.* RC and Elmore delay)
  - detailed simulation (*e.g.* SPICE)

Learning Objectives (con't)

- Tradeoffs in performance specs
  - Among delay, energy, area, noise
- How to design and optimize
  - logic, memory, and interconnect structures
  - at the gate, transistor, and wire level
- How technology scales
  - impact on digital circuits and computer systems

What you need to know

- See "knowledge roundup" topics page linked from course webpage
- ESE 150 (CIS 240)
  - Gates, Boolean logic, DeMorgan's, gate optimization, K-maps
  - Review: book chapter in Canvas
- ESE 215
  - RLC circuit analysis
  - Review: 215 lectures posted in Canvas
- Diagnostic Quiz on Canvas
  - Not graded, weighted as a homework assignment
  - Complete by Friday 1/21 midnight
  - 150 and 215 review materials in Canvas Files section
  - TA review video posted early next week

Course Structure: Websites

- Website (http://www.seas.upenn.edu/~ese370/)
  - Course calendar is used for all handouts (preclass, lecture slides, assignments, and readings)
  - Canvas used for assignment submission, grades and lecture recordings
  - Piazza used for announcements and discussions
    - Use for Zoom links for OHs

Course Structure: Lectures

- MW 8:30am-10am Lecture in Towne 303
  - Lecture recordings will be posted on Canvas
- Preclass and lecture slides posted online before class
- Readings from textbook
- 3 lecture periods → Labs in Detkin

ESE370 Spring 2022 Working Schedule

Wk	Lect.	Date		Lecture	Slides	Due	Reading
1	1	1/12	W	Intro/Overview			1 through 1.2; review course web page completely
2		1/17	M	MLK Jr. Day (no class)			
	2	1/19	W	Transistor Introduction (basics) and Gates from Transistors			review ESE215; 6.2 through static properties in 6.2.1
		1/21	F			Diagnostic Quiz (canvas)	
		1/22	Sa			Access Survey (canvas)	
3		1/24	M	Lab 1 (Ketterer): Gate from Discrete Transistors			
		1/25	T			ADD DATE	
	3	1/26	W	Transistor Introduction (first order), Delay and RC Response			3.1, 1.3.3
		1/28	F			HW1	
4	4	1/31	M	Regenerative Property			1.3.2
	5	2/2	W	MOS Intro, Transistor Operating Regions Part 1			2.1-2.3, 3.3.1-3.3.2 (page 92)

Course Structure: Lectures (Physical)

- Mask required
  - Will be asked to leave and reported to OSC if no compliance
- Statistically and empirically speaking, you will do better if you come to lecture
- Better if interactive, **everyone** engaged
  - Asking and answering questions
  - Actively thinking about material every day
- Two things
  - Preclass worksheet exercises
    - Work during ~5 minutes before lecture starts
    - Primes you for topic of the day
    - Will be addressed during lecture
  - Ask questions of individuals

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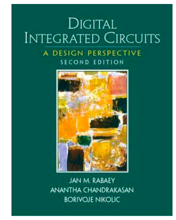
Course Structure: Textbook

- Textbook
  - *Digital Integrated Circuits, A Design Perspective*, Jan M. Rabaey, Anantha Chandrakasan, and Borivoje Nikolic, 2^{nd} edition
    - Great reference text with great detail
    - REALLY!! useful for projects



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Course Structure: SPICE

- Simulation Program with Integrated Circuit Emphasis
  - Industry standard analog circuit simulator
  - Non-linear, differential equation solver specialized for circuits
- Integrated circuits – simply impractical to build to debug
  - Must simulate to optimize/validate design

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Course Structure: Assignments/Exams

- Homework – week long (7 total) [25%]
  - Due (mostly) F at midnight
  - Submit in Canvas
- Projects – 1-3 weeks long (2 total) [30%]
  - Design/Simulation oriented
  - On three main topics
    - 1: Computation - Individual
    - 2: Memory - Team
- Midterms [20%] (2 total)
- Final exam [25%]

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Course Structure: Admin

- Use course calendar
  - Lectures and preclass online before class
    - Will post night before class
    - Reserve the right to change them (usually minor)
  - Homework/projects linked
    - Homework 1 out now
  - Reading for whole term specified
- Take notes!
  - Especially on the examples we do in class
  - Slides have a lot of questions – not a lot of answers

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Course Policies

See course web page for full details

- Turn assignments in on Canvas
  - Anything handwritten/drawn must be clearly legible
    - No handwritten work allowed on projects
  - Submit CAD generated figures, graphs, results when specified
  - Late Policy – allowed 5 late days for whole semester
    - Can only use a max of one day on projects
- Individual work (HW & Project*)
  - CAD drawings, simulations, analysis, writeups
  - May discuss strategies, but acknowledge help

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Course Content

- Logic (Computation) [10 weeks]
  - Combinational logic
  - Sequential logic
- Memory/Storage [2 weeks]
- Communication/Interconnect [3 weeks]

Course Content (con't)

- Logic
  - Transistors → Gates
  - **Lab:** build gate, measure delay
  - Regeneration (noise margins)
  - Delay
  - Area (no layout → ESE370)
  - Energy
  - Synchronous (flip-flops, clocking, dynamic)
  - **Project 1:** fast ripple-carry adder

Course Content (con't)

- Memory/Storage
  - No Lab component
  - RAM Organization
    - Memory cells and periphery circuits
  - Driving Large Capacitances
  - Signal amplification/regeneration
  - **Project 2:** design a SRAM

Course Content (con't)

- Communication/Interconnect
  - Repeaters in wiring
  - **Lab:** Cable noise
    - Measure inductive ground bounce, crosstalk
    - Experiment with PCB transmissions lines, termination
  - Noise
    - Crosstalk
    - Inductive
    - Ionizing particles, shot
  - **Lab:** PCB trace T-line behavior
  - Transmission Lines

Advice

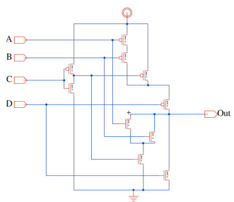
- Course is hard (but valuable)
- Should be thinking about this material every day
- Go to office hours
- MUST READ TEXT!
- Learning is spread over all components
  - Lecture, reading, **homework, projects**, exams
- Cannot pass the class if you don't turn in projects
  - Give yourself enough time. They will take you longer than you think

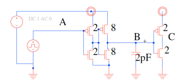
Advice from your fellow students:

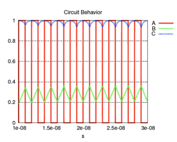
- Q: As a current or former student that did very well in ESE 370, what advice do you have for future students to be successful in ESE 370?
  - "The most important thing for me was to **attend lecture**"
  - "make sure you **start early** on the projects"
  - "ESE 370 is a class that **moves quickly**… best ways to stay abreast of the material was to engage with it … **ask questions and engage** in conversation in class (or in office hours) regularly"
  - "ESE 370 is a very **rewarding class, but not an easy class**. The biggest advice I can offer is to **stay on top of the work**."
  - "will be both very **challenging and rewarding**, and quite **unique compared to other classes at Penn**"
- See course webpage for full answers

Big Ideas

- Model (a.k.a. analysis and simulation) to enable real-life robust design and optimization







Admin

- Find web, get text, assigned reading…
  - http://www.seas.upenn.edu/~ese370
  - piazza.com/upenn/spring2022/srs_ese3700012022a
  - https://canvas.upenn.edu/courses/
- To do:
  - Submit Accessibility Survey (in canvas) – due Sa 1/22
    - Required/Recommended technology
  - Diagnostic Quiz (in Canvas) – due by F 1/21
    - Review as needed
  - HW 1 out now – due F 1/28
    - Need lab and future lectures to finish

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