ESE370: Circuit-Level Modeling, Design, and Optimization for Digital Systems

Lec 2: January 18, 2023
Transistor Introduction and
Gates from Transistors

1

Today

- Transistors – MOSFET
- Zero-th order transistor model
  - Good enough for [what?]
- Basic Digital Gates
- Boolean Logic
  - Basic Algebra
  - Minimum Sum of Products/K-maps
- How to construct static CMOS gates
  - Gate function identification (preclass)
  - CMOS gate structure
    - Pullup/pulldown networks

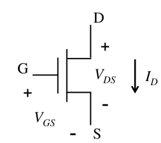
2

Transistor

- Electrical switch to conduct electricity
  - Instead of physically connecting conducting materials to conduct electricity, apply a voltage to conduct

3

MOSFET



$V_{GS} = V_G - V_S$

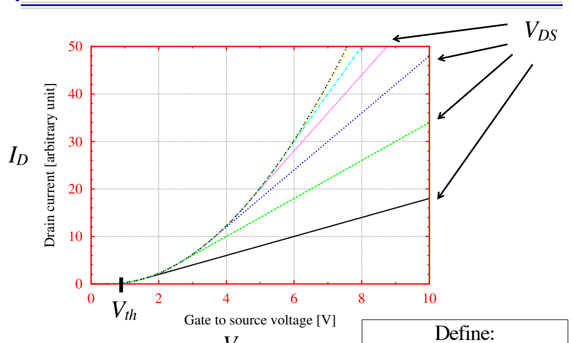
$V_{DS} = V_D - V_S$

$I_D = f(V_{DS}, V_{GS})$

- Metal Oxide Semiconductor Field Effect Transistor
  - Primary **active** component for the term
  - Three terminal device
    - Voltage at gate controls conduction between two other terminals (source, drain)

4

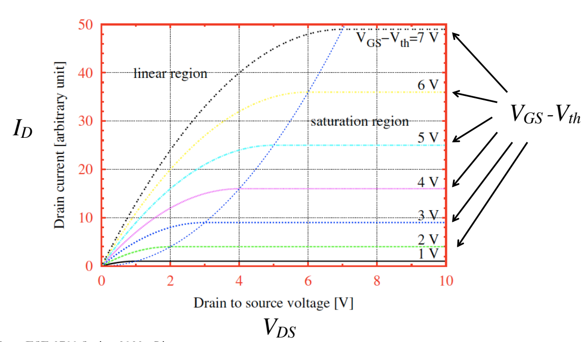
MOSFET – IV Characteristics



Define:
V_{th} = Threshold Voltage

5

MOSFET – IV Characteristics



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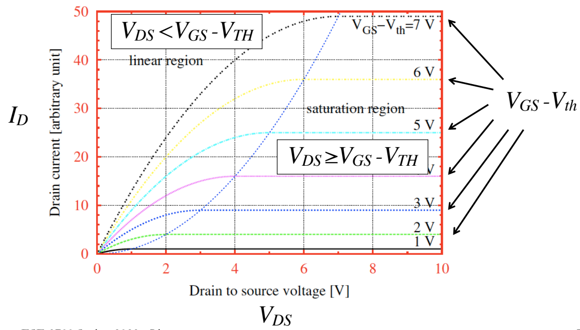
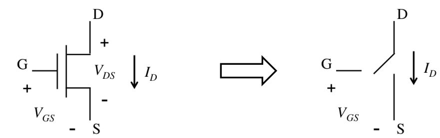
MOSFET – IV Characteristics

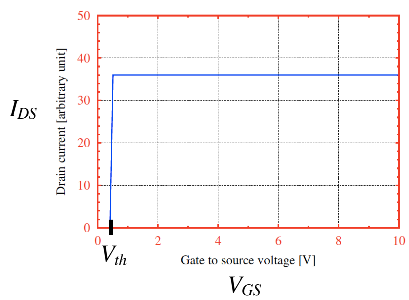


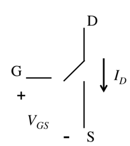
MOSFET – Zeroeth Order Model



- Ideal Switch
  - $V_{GS} > V_{th}$ → switch is closed, conducts
  - $V_{GS} < V_{th}$ → switch is open, does not conduct
- Gate draws no current from input
  - Loads input capacitively (gate capacitance)

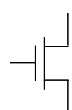
MOSFET – Zeroeth Order Model





MOSFET - Symmetric

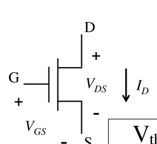
- Switch turned on for positive V_{GS}
  - Which side is drain or source?



MOSFET – N-Type

- Switch turned on for positive V_{GS}

$V_D > V_S$



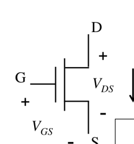
$V_{th,n} > 0$
$V_{GS} > V_{th,n}$
to conduct

MOSFET – N-Type, P-Type

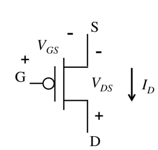
- Switch turned on for positive V_{GS}
- Switch turned on for negative V_{GS}

$V_D > V_S$

$V_S > V_D$



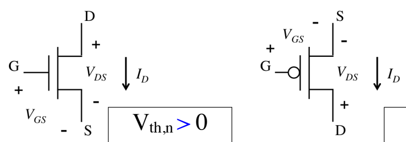
$V_{th,n} > 0$
$V_{GS} > V_{th,n}$
to conduct



MOSFET – N-Type, P-Type

- Switch turned on for positive V_{GS}
- Switch turned on for negative V_{GS}

$V_D > V_S$ $\quad$ $V_S > V_D$



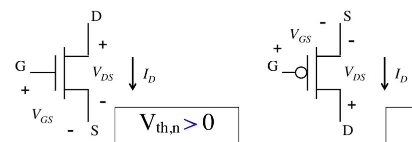
$V_{th,n} > 0$
$V_{GS} > V_{th,n}$
to conduct

$V_{th,p} < 0$
$V_{GS} < V_{th,p}$
to conduct

MOSFET – N-Type, P-Type

- Switch turned on for positive V_{GS}
- Switch turned on for negative V_{GS}

$V_D > V_S$ $\quad$ $V_S > V_D$

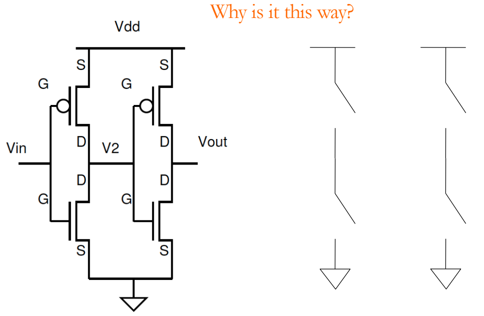


$V_{th,n} > 0$
$V_{GS} > V_{th,n}$
to conduct

$|V_{th,p}| > 0$
$|V_{GS}| > |V_{th,p}|$
to conduct

Apply zero-order model

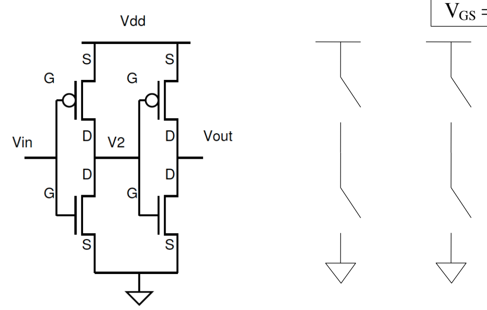
Note S, D annotation on this slide (won't be labeled in future)
Why is it this way?



Apply zero-order model?

What happens when $V_{in} = V_{dd} > V_{thn}$?

$V_{th,p} = -V_{th,n}$
$V_{GS} = V_G - V_S$



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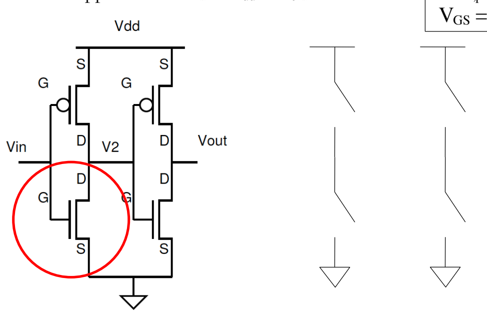

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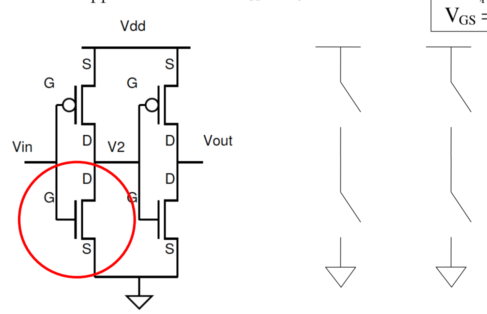

$V_{GS} = V_G - V_S = V_{dd} > V_{th,n}$

Apply zero-order model?

What happens when $V_{in} = V_{dd} > V_{thn}$?

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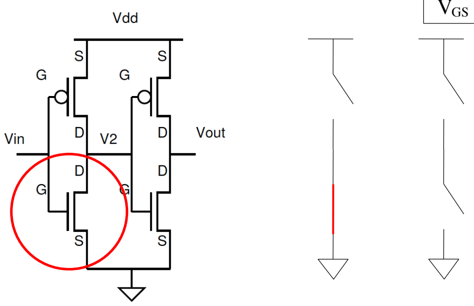

$V_{GS} = V_G - V_S = V_{dd} > V_{th,n}$

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Apply zero-order model?

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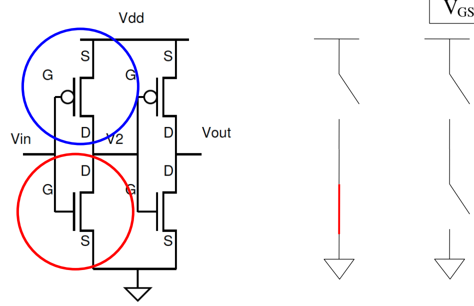
$V_{th,p} = -V_{th,n}$
$V_{GS} = V_G - V_S$



$V_{GS} = V_G - V_S = V_{dd} > V_{th,n}$

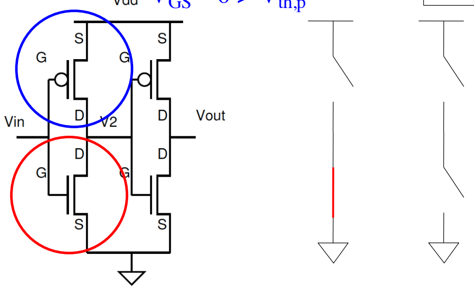
20

Apply zero-order model?

What happens when $V_{in} = V_{dd} > V_{thn}$?

$V_{th,p} = -V_{th,n}$
$V_{GS} = V_G - V_S$

$V_{GS} = 0 > V_{th,p}$



$V_{GS} = V_G - V_S = V_{dd} > V_{th,n}$

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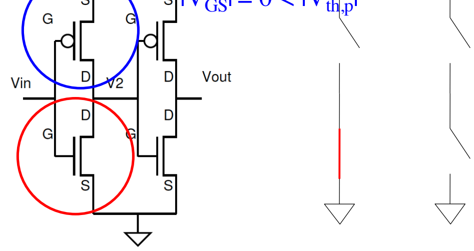
Apply zero-order model?

What happens when $V_{in} = V_{dd} > V_{thn}$?

$V_{th,p} = -V_{th,n}$
$V_{GS} = V_G - V_S$

$V_{GS} = 0 > V_{th,p}$

$|V_{GS}| = 0 < |V_{th,p}|$



$V_{GS} = V_G - V_S = V_{dd} > V_{th,n}$

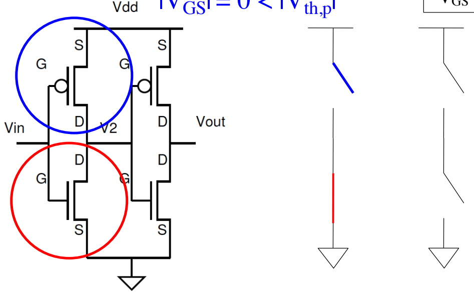
22

Apply zero-order model?

What happens when $V_{in} = V_{dd} > V_{thn}$?

$V_{th,p} = -V_{th,n}$
$V_{GS} = V_G - V_S$

$|V_{GS}| = 0 < |V_{th,p}|$



$V_{GS} = V_G - V_S = V_{dd} > V_{th,n}$

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Apply zero-order model?

What happens when $V_{in} = V_{dd} > V_{thn}$?

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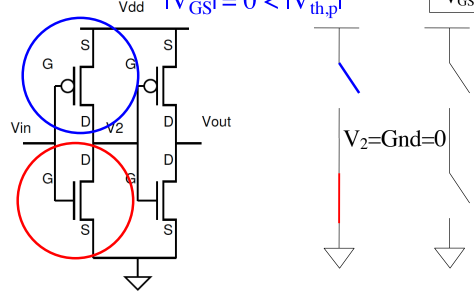
$V_{GS} = V_G - V_S$

$|V_{GS}| = 0 < |V_{th,p}|$



$V_{GS} = V_G - V_S = V_{dd} > V_{th,n}$

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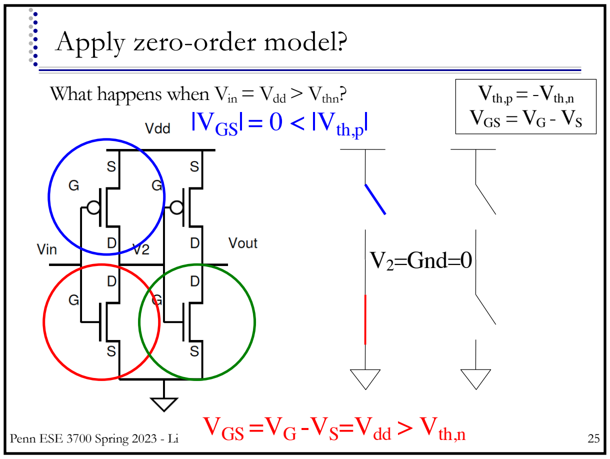

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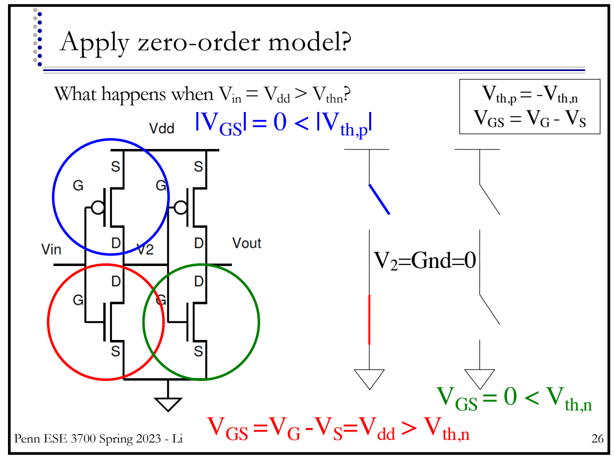

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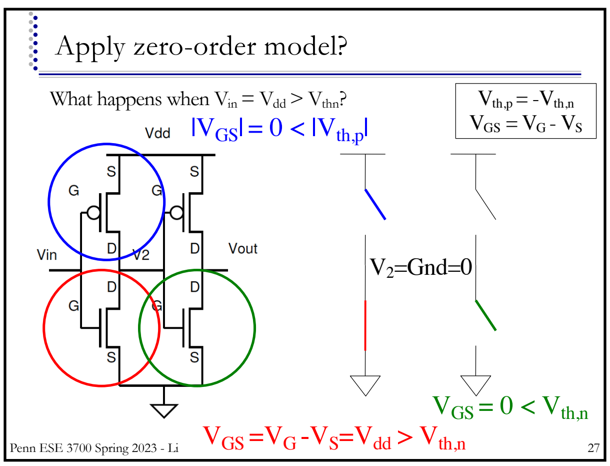

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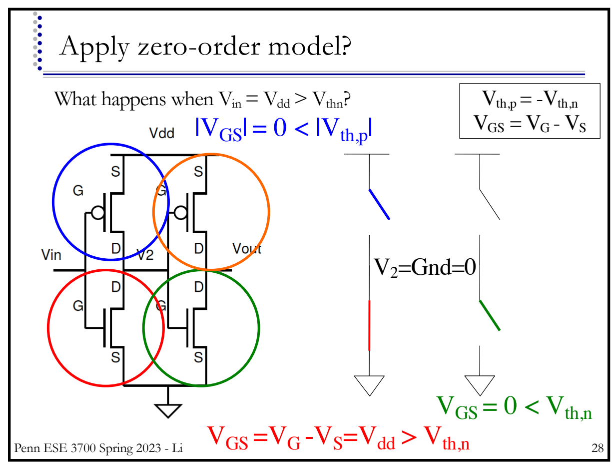

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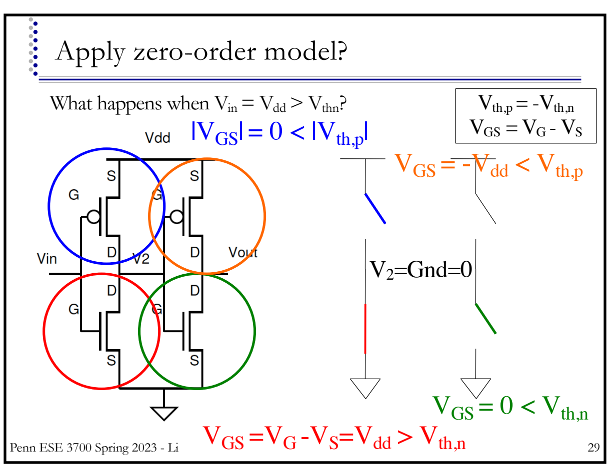

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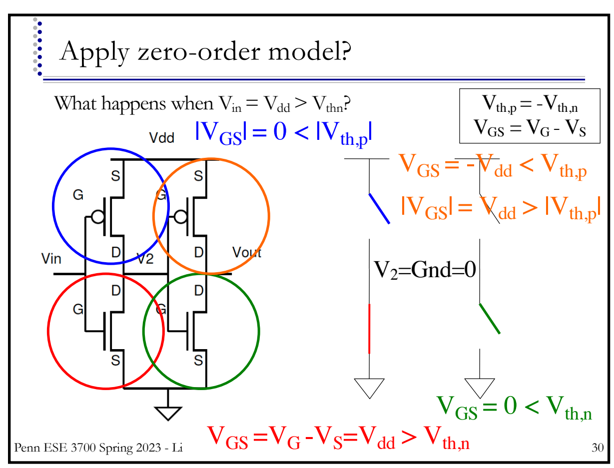

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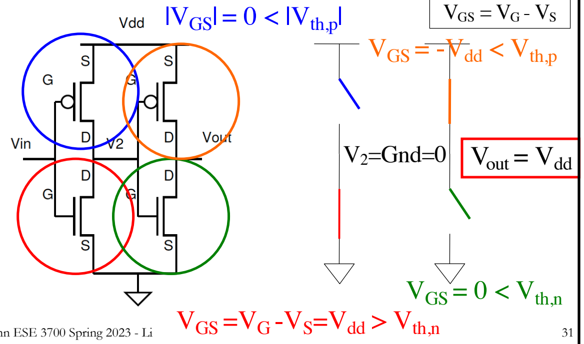
Apply zero-order model?

What happens when $V_{in} = V_{dd} > V_{thn}$?

$V_{th,p} = -V_{th,n}$
$V_{GS} = V_G - V_S$



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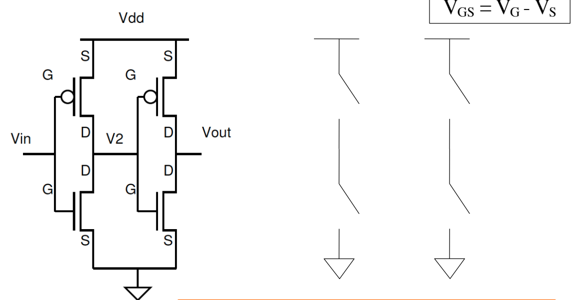
Apply zero-order model?

What happens when $V_{in} = 0$?

$V_{th,p} = -V_{th,n}$
$V_{GS} = V_G - V_S$



Convince yourself that $V_{out} = 0$.

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Zeroeth Order Model

- Allows us to reason (mostly) at logic level about steady-state functionality of typical gate circuits before worrying about performance (speed, power, etc.) details

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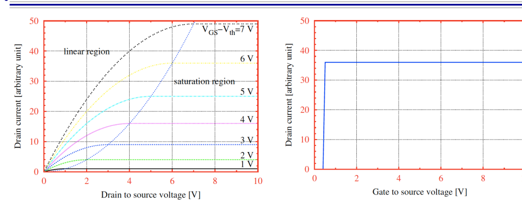
What is missing in Zeroeth Order Model?



- Delay
  - Parasitic capacitances and resistances
- Dynamics
- Zeroeth Order captures behaviour if our circuit is not:
  - Capacitively loaded, acyclic (if there are Loops)

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Digital Logic

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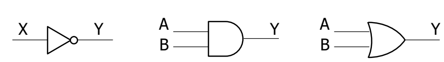
Basic Digital Gates

NOT $Y = \overline{X}$ | AND $Y = A \bullet B$ | OR $Y = A+B$



X	Y
0	1
1	0

A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

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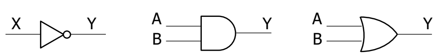
Basic Digital Gates

NOT $Y = \overline{X}$ | AND $Y = A \bullet B$ | OR $Y = A + B$

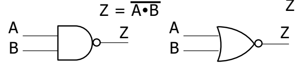


X	Y
0	1
1	0

A	B	Y	Z
0	0	0	1
0	1	0	1
1	0	0	1
1	1	1	0

A	B	Y	Z
0	0	0	1
0	1	1	0
1	0	1	0
1	1	1	0

NAND $Z = \overline{A \bullet B}$ | NOR $Z = \overline{A + B}$



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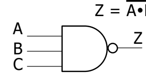
Basic Digital Gates

NAND $Z = \overline{A \bullet B \bullet C}$



A	B	C	Z
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

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Boolean Algebra

TABLE 2-3
Basic Identities of Boolean Algebra

1.	$X + 0 = X$	2.	$X \cdot 1 = X$	
3.	$X + 1 = 1$	4.	$X \cdot 0 = 0$	
5.	$X + X = X$	6.	$X \cdot X = X$	
7.	$X + \overline{X} = 1$	8.	$X \cdot \overline{X} = 0$	
9.	$\overline{\overline{X}} = X$			
10.	$X + Y = Y + X$	11.	$XY = YX$	Commutative
12.	$X + (Y + Z) = (X + Y) + Z$	13.	$X(YZ) = (XY)Z$	Associative
14.	$X(Y + Z) = XY + XZ$	15.	$X + YZ = (X + Y)(X + Z)$	Distributive
16.	$\overline{X + Y} = \overline{X} \cdot \overline{Y}$	17.	$\overline{X \cdot Y} = \overline{X} + \overline{Y}$	DeMorgan's

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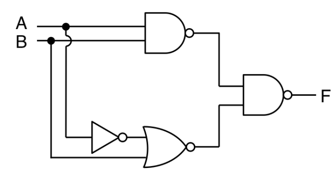
Combination



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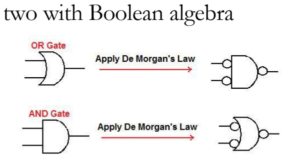
Boolean Expressions

- Sum-of-products form (SOP)
  - Eg. ABC+DEF+GHI
- Product-of-sums form (POS)
  - Eg. (A+B+C)(D+E+F)(G+H+I)
- Convert between the two with Boolean algebra
  - DeMorgan's Law

$$A + B = \overline{\overline{A} \cdot \overline{B}}$$
$$A \cdot B = \overline{\overline{A} + \overline{B}}$$



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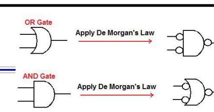
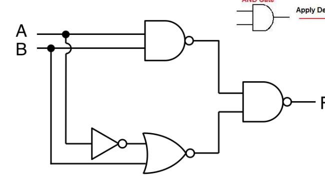
Combination





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Canonical Form

- Every minterm in your expression has every variable

Row Number	A	B	C	f
0	0	0	0	0
1	0	0	1	0
2	0	1	0	0
3	0	1	1	1
4	1	0	0	0
5	1	0	1	0
6	1	1	0	1
7	1	1	1	1

Canonical Form

- Every minterm in your expression has every variable

Row Number	A	B	C	f
0	0	0	0	0
1	0	0	1	0
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5	1	0	1	0
6	1	1	0	1
7	1	1	1	1

$$f(A,B,C) = ABC + AB\overline{C} + \overline{A}BC$$

What is a K(arnaugh)-map?

- A grid of squares (representing truth table)
- Each square represents one minterm
- The minterms are ordered according to **Gray code**
  - Only one variable changes between adjacent squares
- Squares on edges are considered adjacent to squares on opposite edges
  - I.e Table wraps around
- K-maps are clumsy with more than 4 variables

A \ B	0	1
0		
1		

A \ BC	00	01	11	10
0				
1				

K-map Examples (Preclass 1)

- 2-variable

A \ B	0	1
0		
1		

Eg: Z = A'B' + AB' + A'B

- 3-variable

A \ BC	00	01	11	10
0				
1				

K-map Examples (Preclass 2)

- 2-variable

A \ B	0	1
0		
1		

Eg: Z = A'B' + AB' + A'B

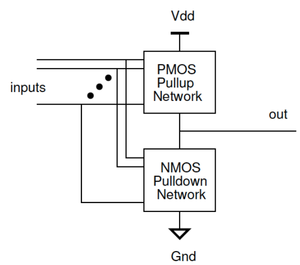
- 3-variable

A \ BC	00	01	11	10
0				
1				

Eg: Z = A'B'C' + A'B + ABC' + AC

CMOS Gates

How to construct static CMOS gates



- Complementary Metal Oxide Semiconductor

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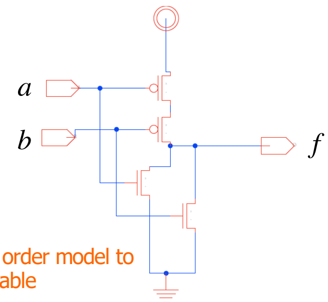
What gate is this? Preclass 3



Hint: use zero order model to make a truth table

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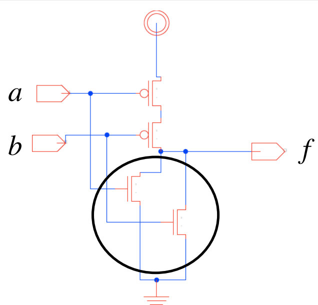
What gate is this?



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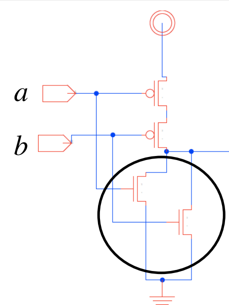
What gate is this? Preclass 4



$\overline{f} = a + b$

What is f in minimum-sum-of-products form?

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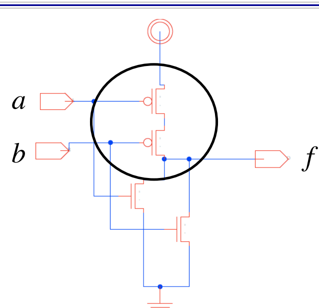
What gate is this?



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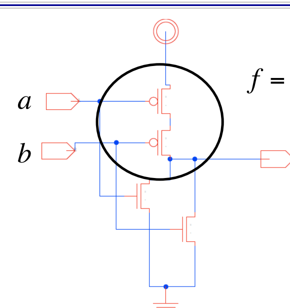
What gate is this?

$f = \overline{a} \cdot \overline{b}$



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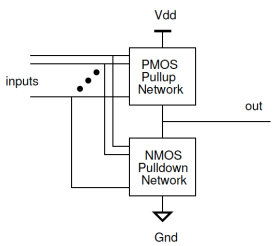
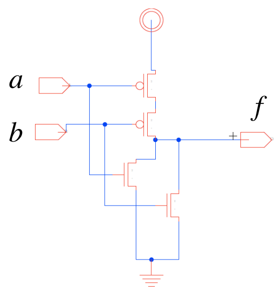
Static CMOS Gate Structure





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CMOS

- Complementary Metal Oxide Semicondutor
- Uses *complementary* transistors
  - NMOS, PMOS
- Pull-down and pull-up networks are *complements* of each other
  - Only one network active (on) at a time to charge or discharge output to V_{dd} or Gnd respectively

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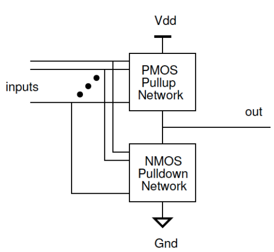
Static CMOS Gate Structure



- Drives rail-to-rail
  - Power rails are V_{dd} and Gnd
  - output is V_{dd} or Gnd
- Input connects to gates
  → load is capacitive
- Once output node is charged doesn't use energy (no static current)
- Output actively driven

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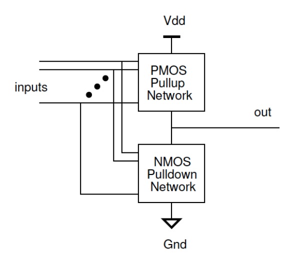
Gate Design Example Preclass 5

- Design gate to perform: $f = (\overline{a} + \overline{b}) \cdot \overline{c}$
- Strategy:
  1. Use static CMOS structure
  2. Design PMOS pullup for *f*
  3. Use DeMorgan's Law to determine *f'*
  4. Design NMOS pulldown for *f'*



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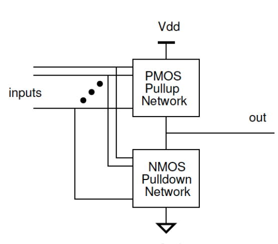
Gate Design Example

- Design gate to perform: $f = (\overline{a} + \overline{b}) \cdot \overline{c}$
- PMOS Pullup for *f*?



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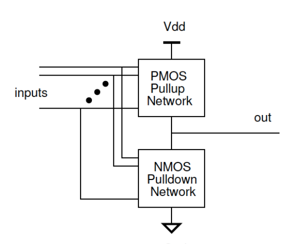
Gate Design Example

- Design gate to perform: $f = (\overline{a} + \overline{b}) \cdot \overline{c}$
- What is *f'*?
  - DeMorgan's Law



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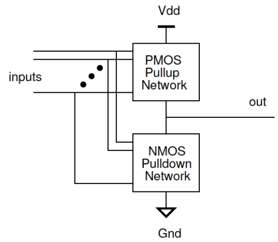
Gate Design Example

- Design gate to perform: $f = (\overline{a} + \overline{b}) \cdot \overline{c}$
- Design NMOS pulldown for f'



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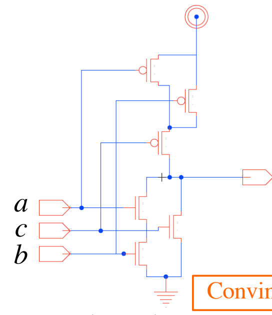
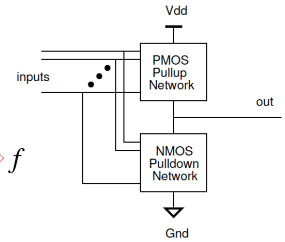
Gate Design Example

- Design gate to perform: $f = (\overline{a} + \overline{b}) \cdot \overline{c}$





Convince yourself with a truth table.

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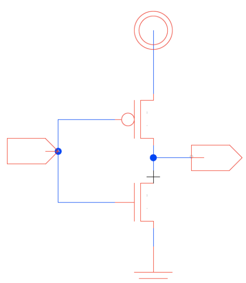
Inverting Stage

- Each stage of Static CMOS gate is inherently inverting



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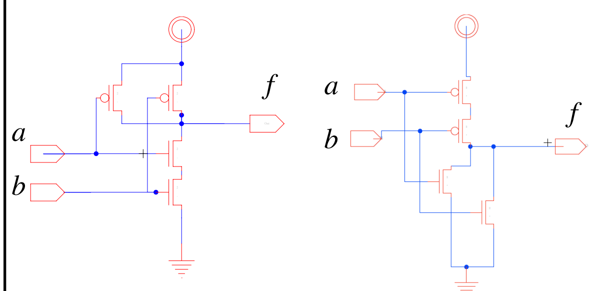
NAND/NOR Fundamental Gates



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How implement OR?

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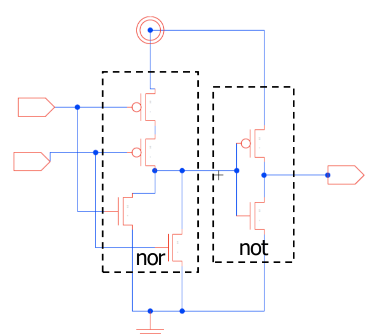
How implement OR?



Cascading Stages

- Can always cascade "stages" to build more complex gates
- Could simply build nor2 or nand2 at circuit level and assemble arbitrary logic by combining – universality
  - but may not be smallest/fastest/least power

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Implement: $f = a \cdot \overline{b}$

- Pullup?
- Pulldown?

Hint: use cascading stages

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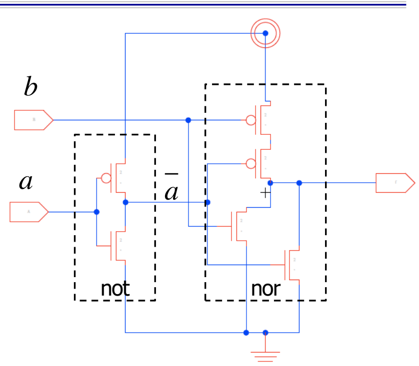
Implement: $f = a \cdot \overline{b}$

- Pullup?
- Pulldown?



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Big Idea

- MOSFET Transistor as switch
- Functionality-driven simplified modeling (Zero order)
  - Aid reasoning
  - Sanity check
  - Simplify design
- CMOS Gate Design
  - Complementary pull-up and pull-down networks

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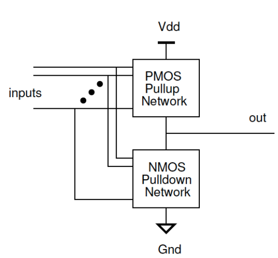
Big Idea

- Systematic construction of any gate from transistors
  1. Use static CMOS structure
  2. Design PMOS pullup for f
  3. Use DeMorgan's Law to determine f'
  4. Design NMOS pulldown for f'



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Admin

- HW 1 out – due 1/27
  - Will take time to learn Electric CAD tool, start early
- Monday (1/23) – no lecture, Lab in Detkin
- Wednesday (1/25) regular physical lecture in LRSM 112B
- TA office hours announced on Ed Discussion (Mon- Friday)

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Acknowledgement

- Prof. André DeHon (University of Pennsylvania)
- Prof. Tania Khanna (University of Pennsylvania)