

ESE370: Circuit-Level Modeling, Design, and Optimization for Digital Systems

Lec 3: January 25, 2023

Transistor First Order Model, Delay, and RC
Response





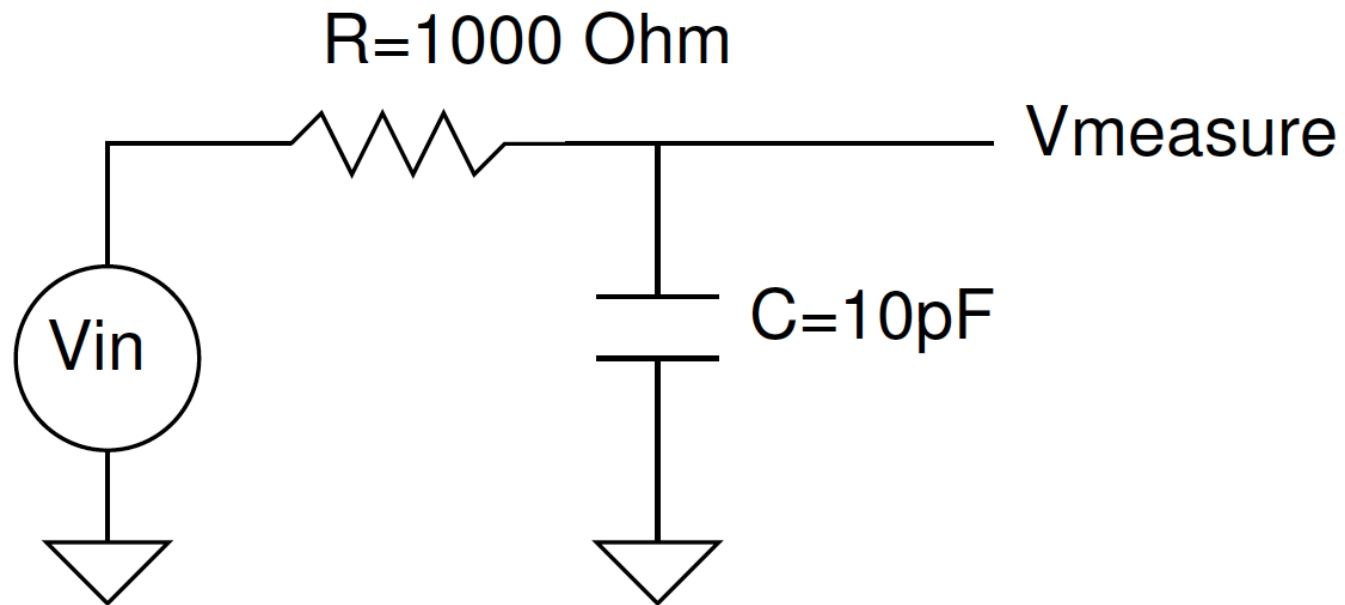
Today

- ❑ Transistor First-Order Model
- ❑ RC Charging
 - RC Step Response Curve
- ❑ What is the C?
 - Capacitive **load** on logic gate output node
- ❑ What is the R?
 - Equivalent **output resistance** on the current path **driving** the output node
- ❑ Approximating and Measuring Delay
 - Tau estimate!

Final Voltage? (Preclass 1)

Assume V_{in} is 0 for $t < 0$ and steps to 1V at $t = 0$.

What value does $V_{measure}$ take on as $t \rightarrow \infty$?

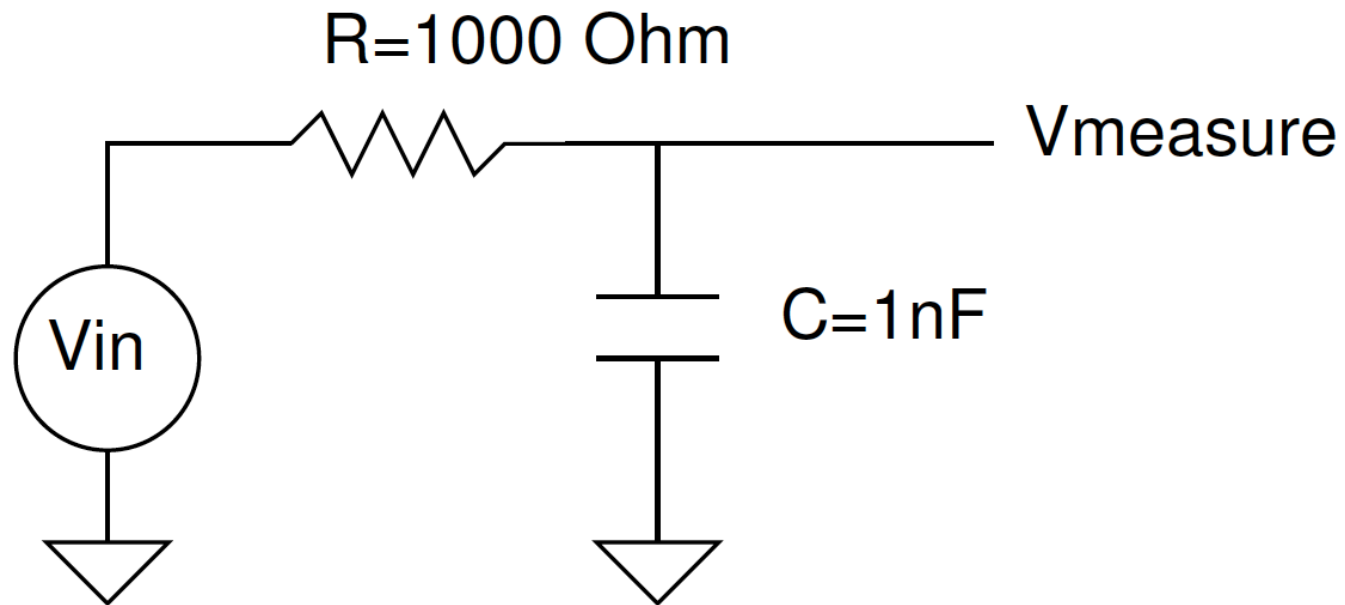




Final Voltage?

Assume V_{in} is 0 for $t < 0$ and steps to 1V at $t = 0$.

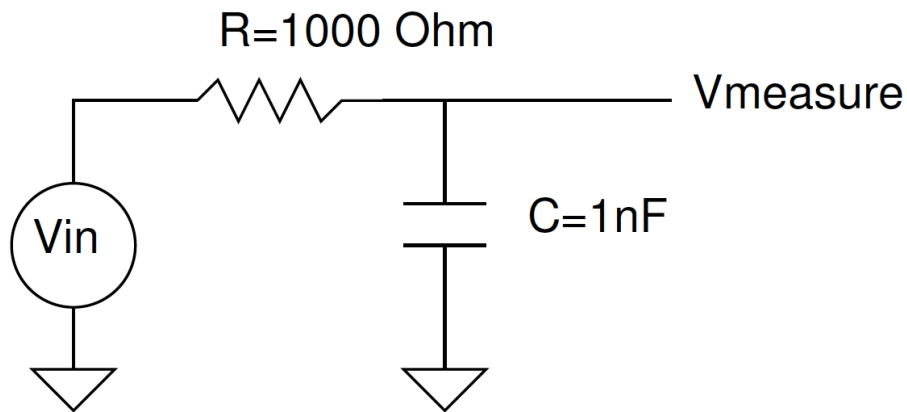
What value does $V_{measure}$ take on as $t \rightarrow \infty$?



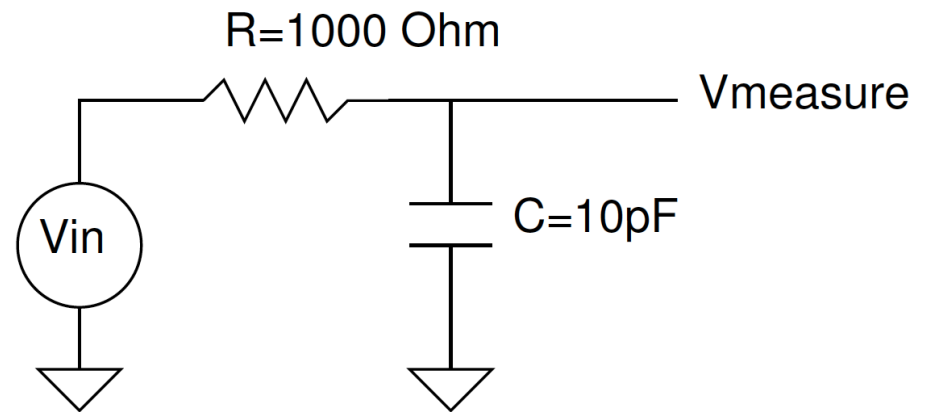


Final Voltage?

□ Bonus question: Which one will settle faster?



A



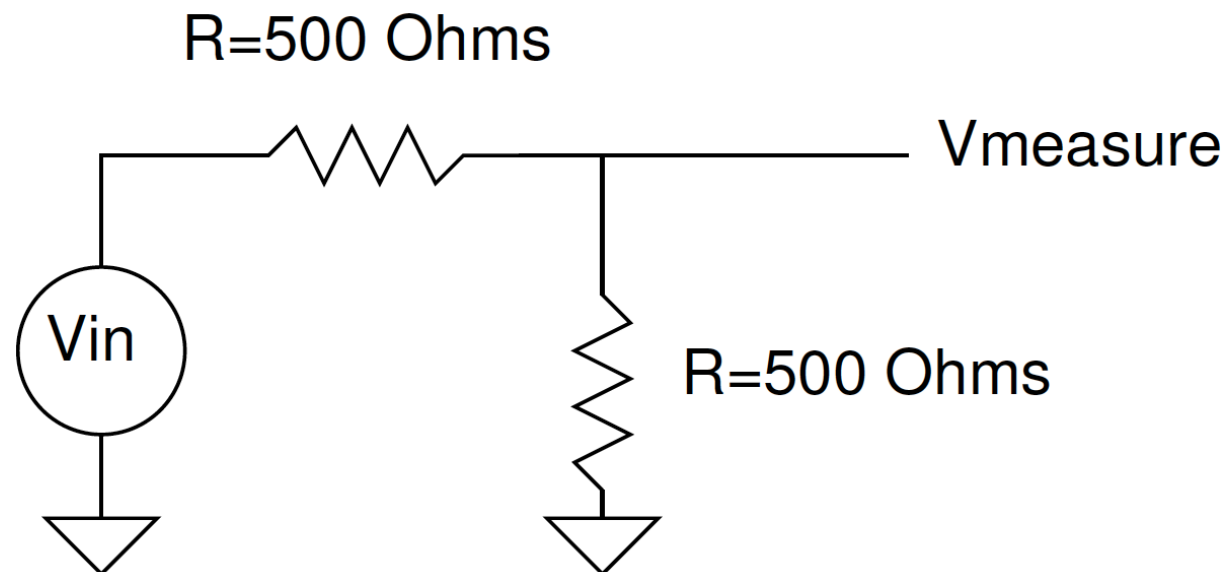
B



Final Voltage?

Assume V_{in} is 0 for $t < 0$ and steps to 1V at $t = 0$.

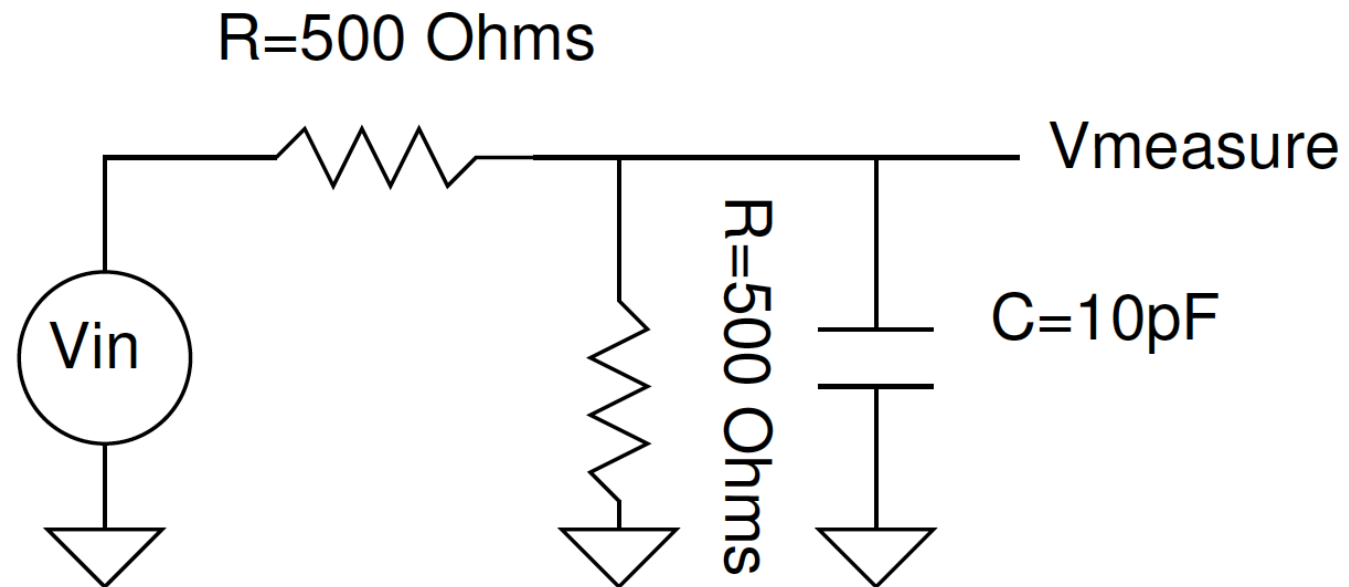
What value does $V_{measure}$ take on as $t \rightarrow \infty$?



Final Voltage?

Assume V_{in} is 0 for $t < 0$ and steps to 1V at $t = 0$.

What value does $V_{measure}$ take on as $t \rightarrow \infty$?

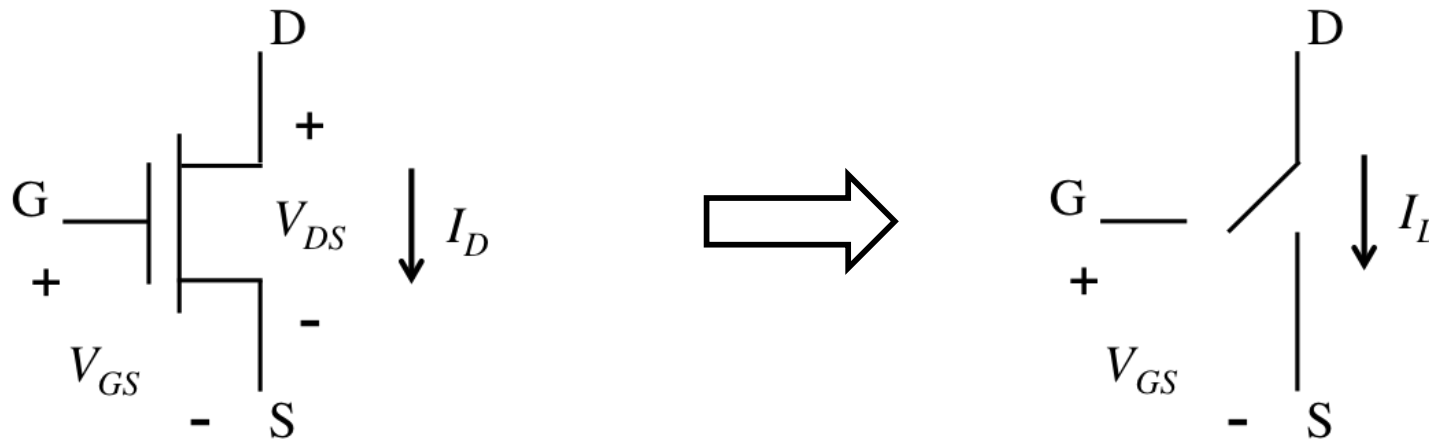




Conclude?

- DC/*Steady-State*
 - Ignore the capacitors
 - Look like “open circuit”

MOSFET – Zeroeth Order Model



□ Ideal Switch

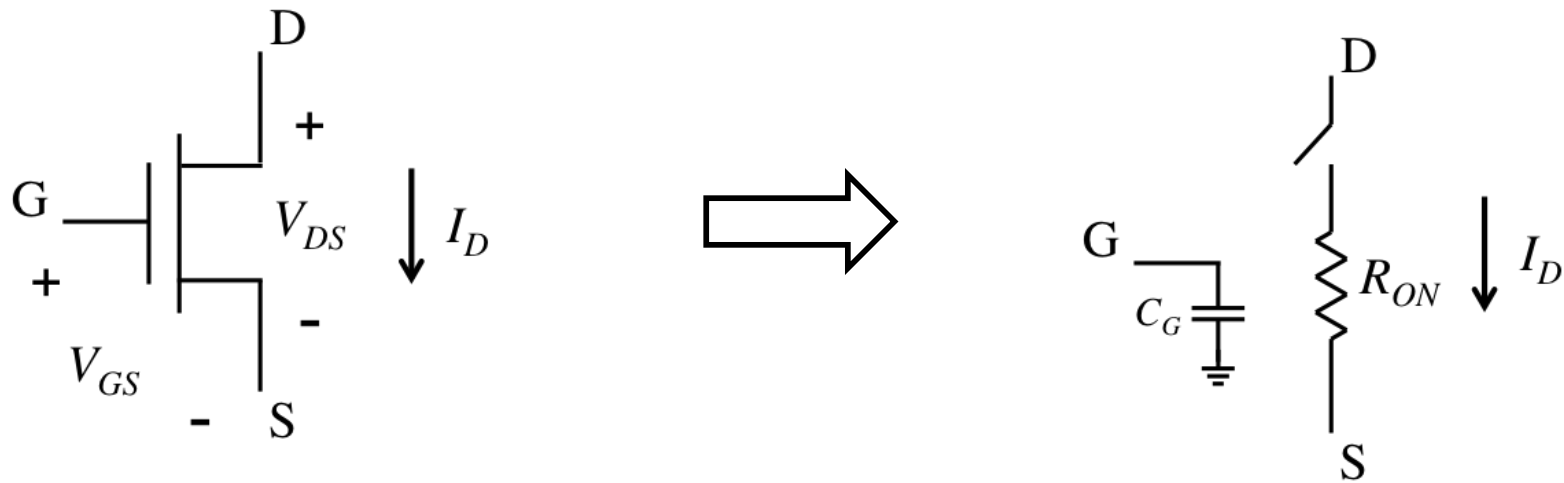
$V_{GS} > V_{th} \rightarrow$ switch is closed, conducts

$V_{GS} < V_{th} \rightarrow$ switch is open, does not conduct

□ Gate draws no current from input

- Loads input capacitively (gate capacitance)

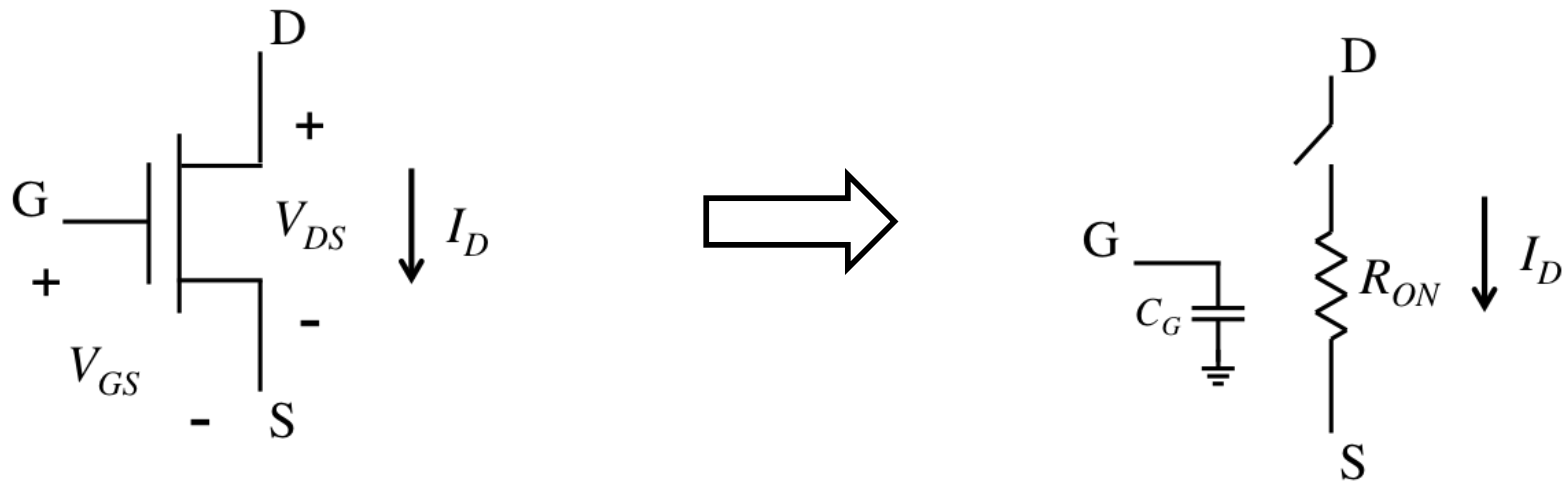
First Order Model



□ Switch

- Loads gate input capacitively
 - C_g
- Has finite drive strength
 - R_{on}

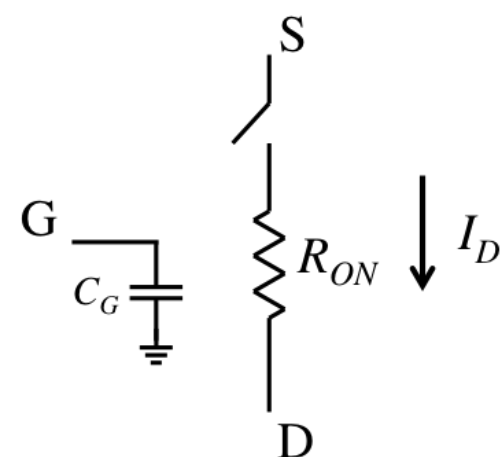
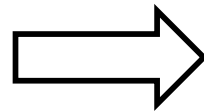
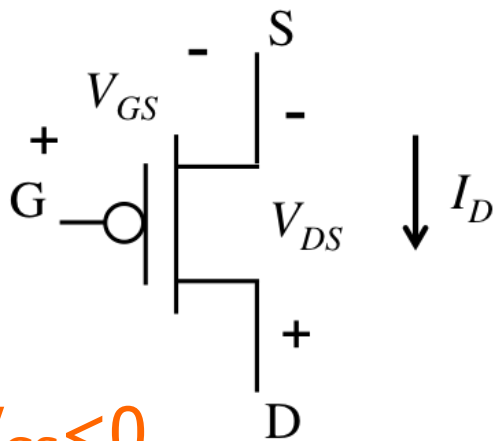
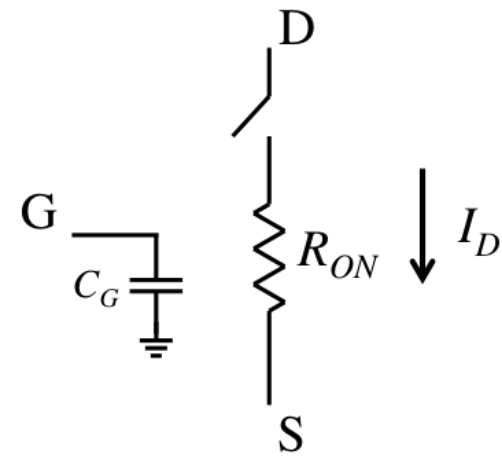
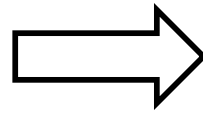
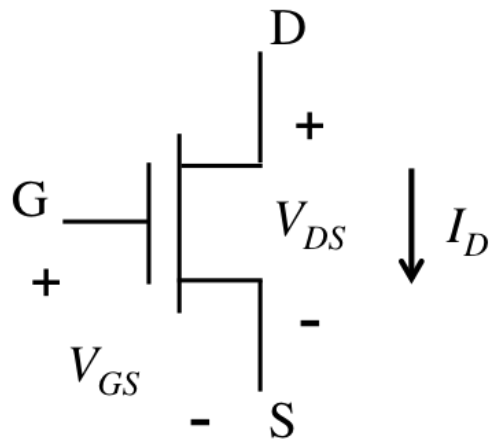
First Order Model



□ Switch

- Loads gate input capacitively
 - C_g
- Has finite drive strength
 - R_{on}

First Order Model - PMOS

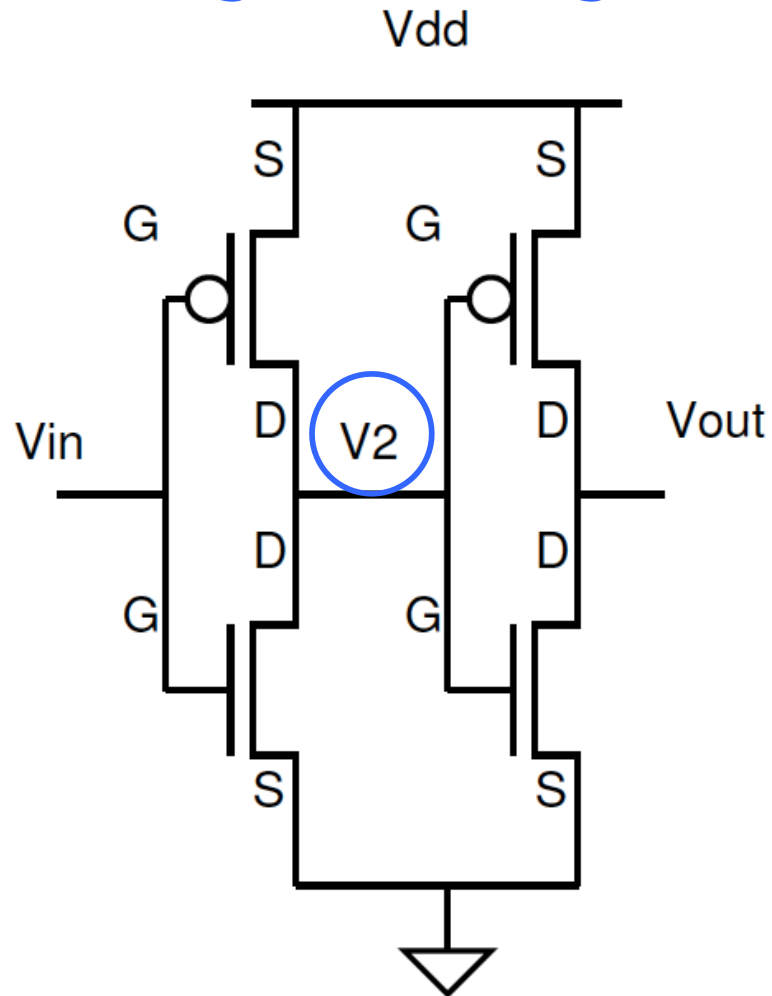


$V_{DS}, V_{GS} < 0$



CMOS Buffer Gate

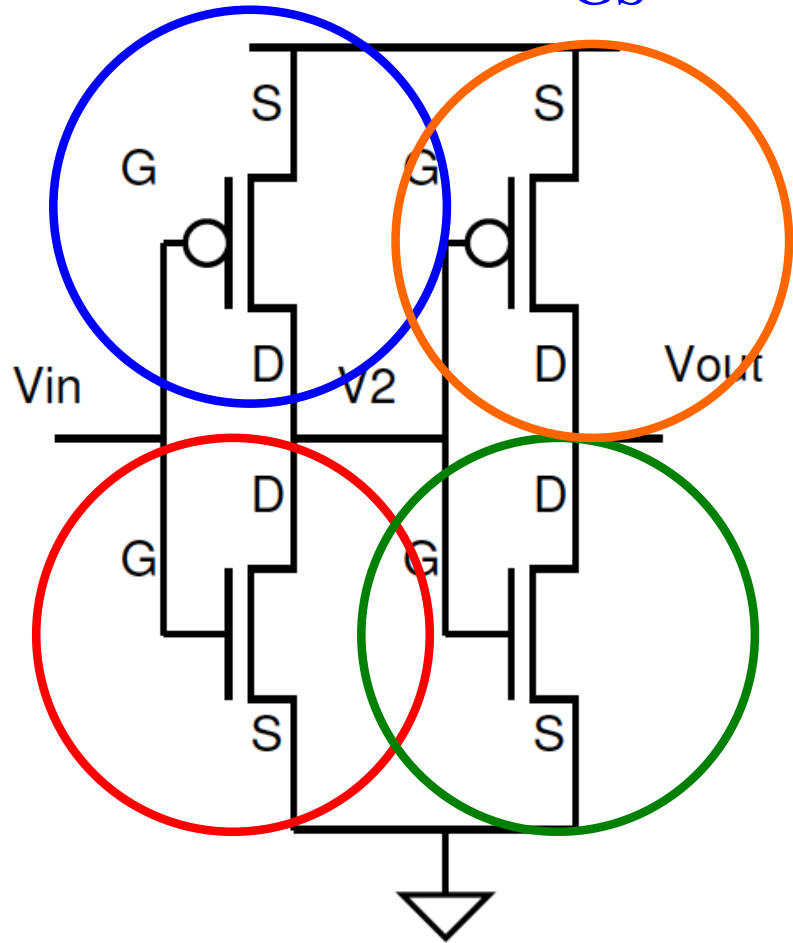
Stage 1 Stage 2



Reminder: Zero-Order Model?

What happens when $V_{in} = V_{dd} > V_{thn}$?

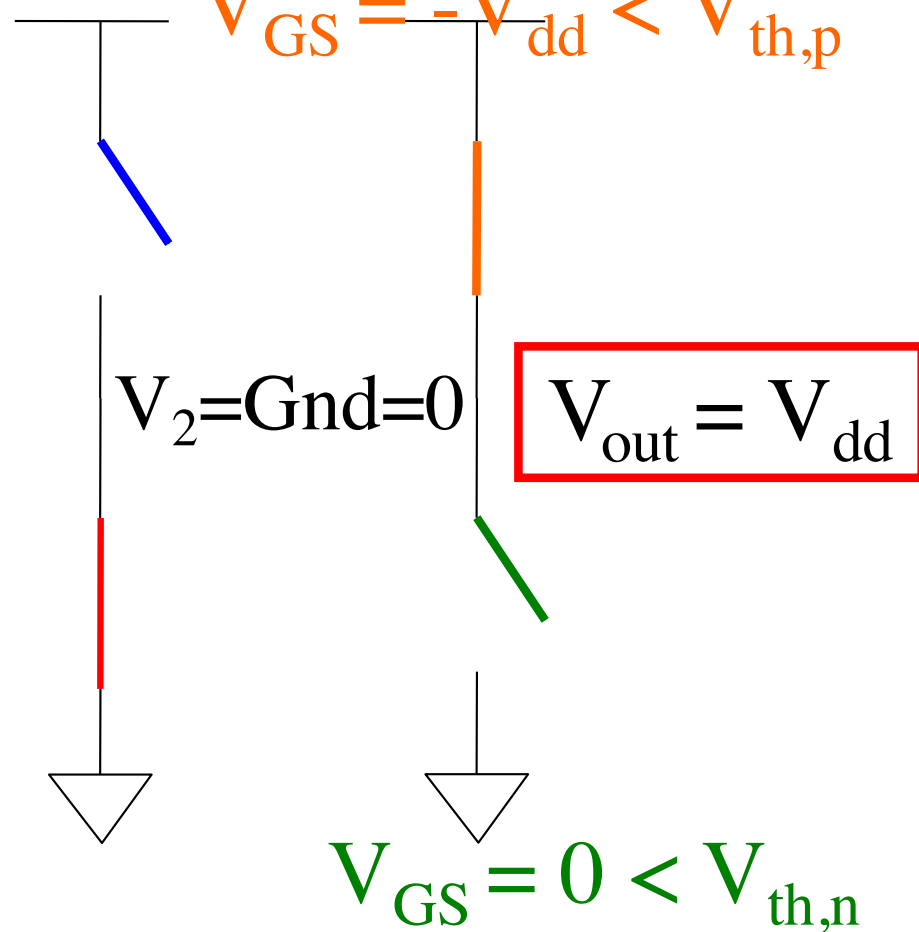
$$V_{GS} = 0 > V_{th,p}$$



$$V_{th,p} = -V_{th,n}$$

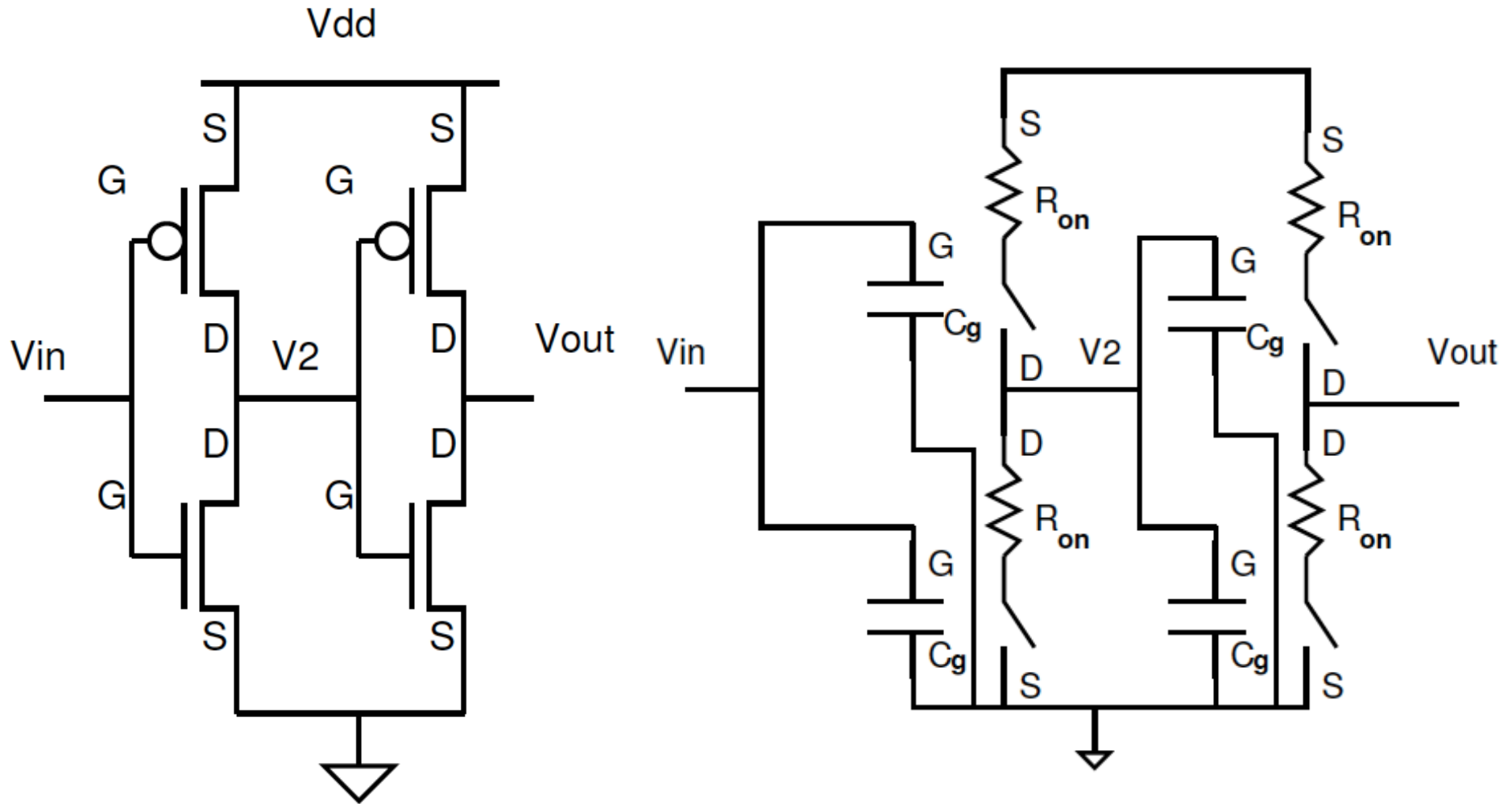
$$V_{GS} = V_G - V_S$$

$$V_{GS} = -V_{dd} < V_{th,p}$$

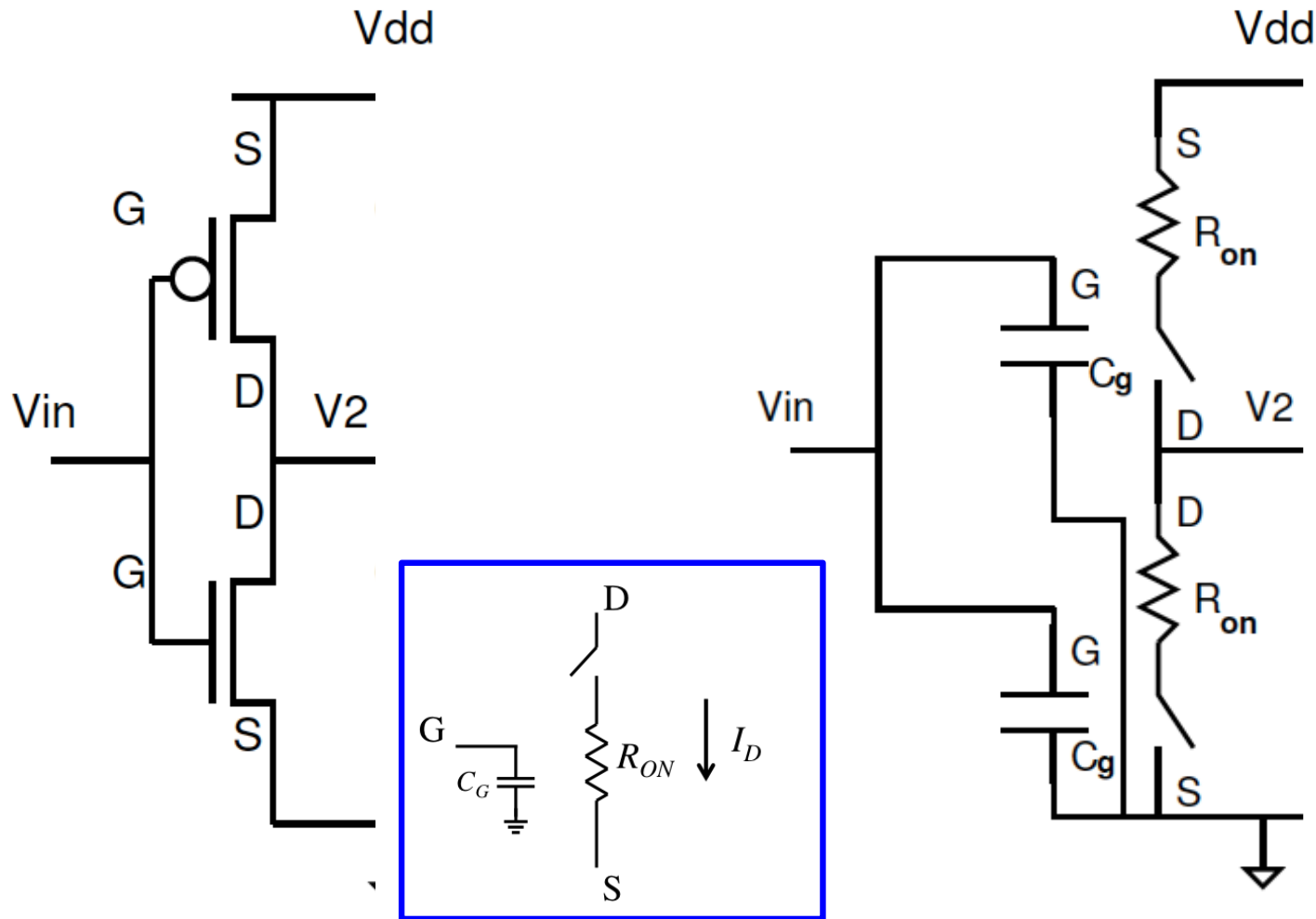


$$V_{GS} = V_G - V_S = V_{dd} > V_{th,n}$$

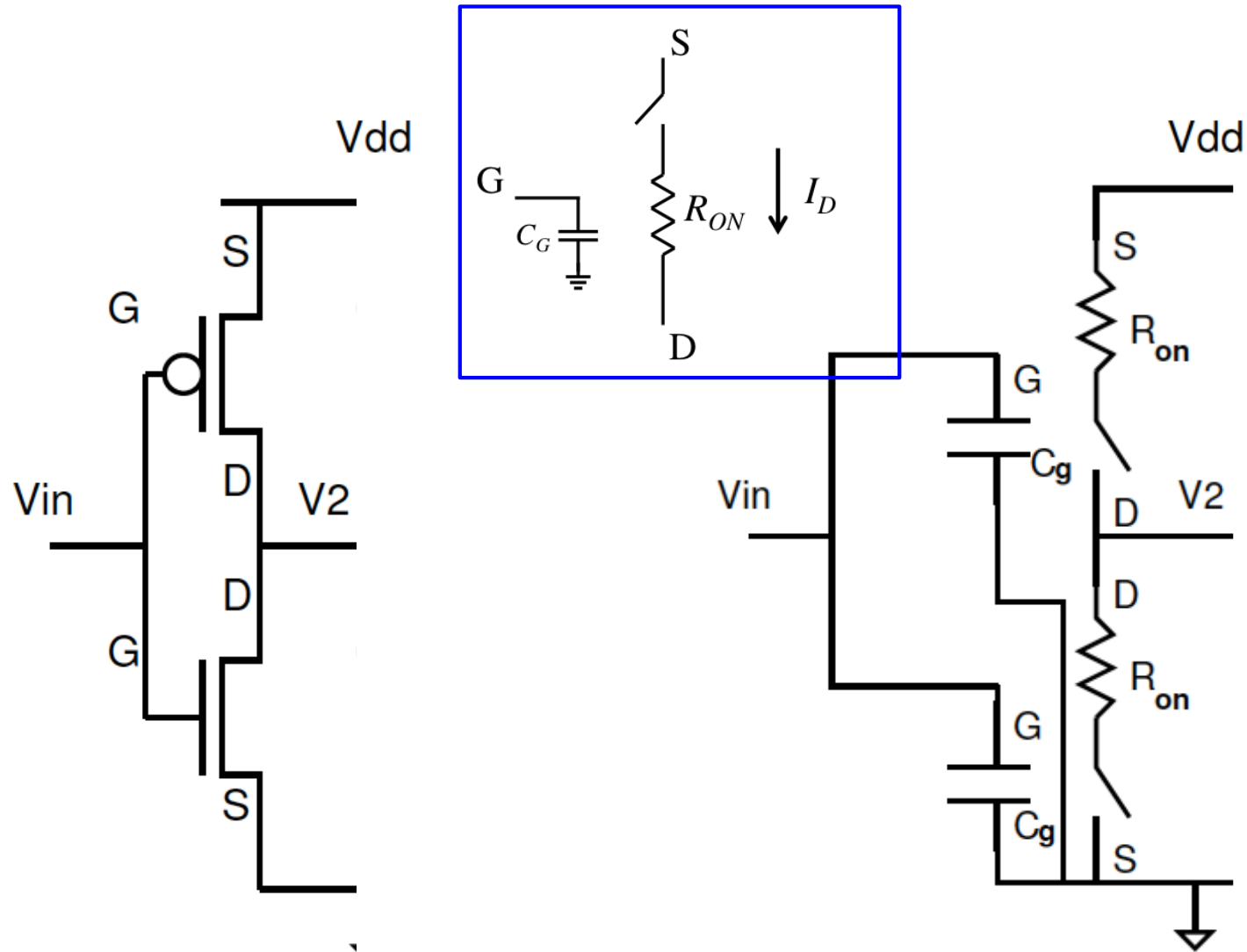
CMOS Buffer Gate - First Order



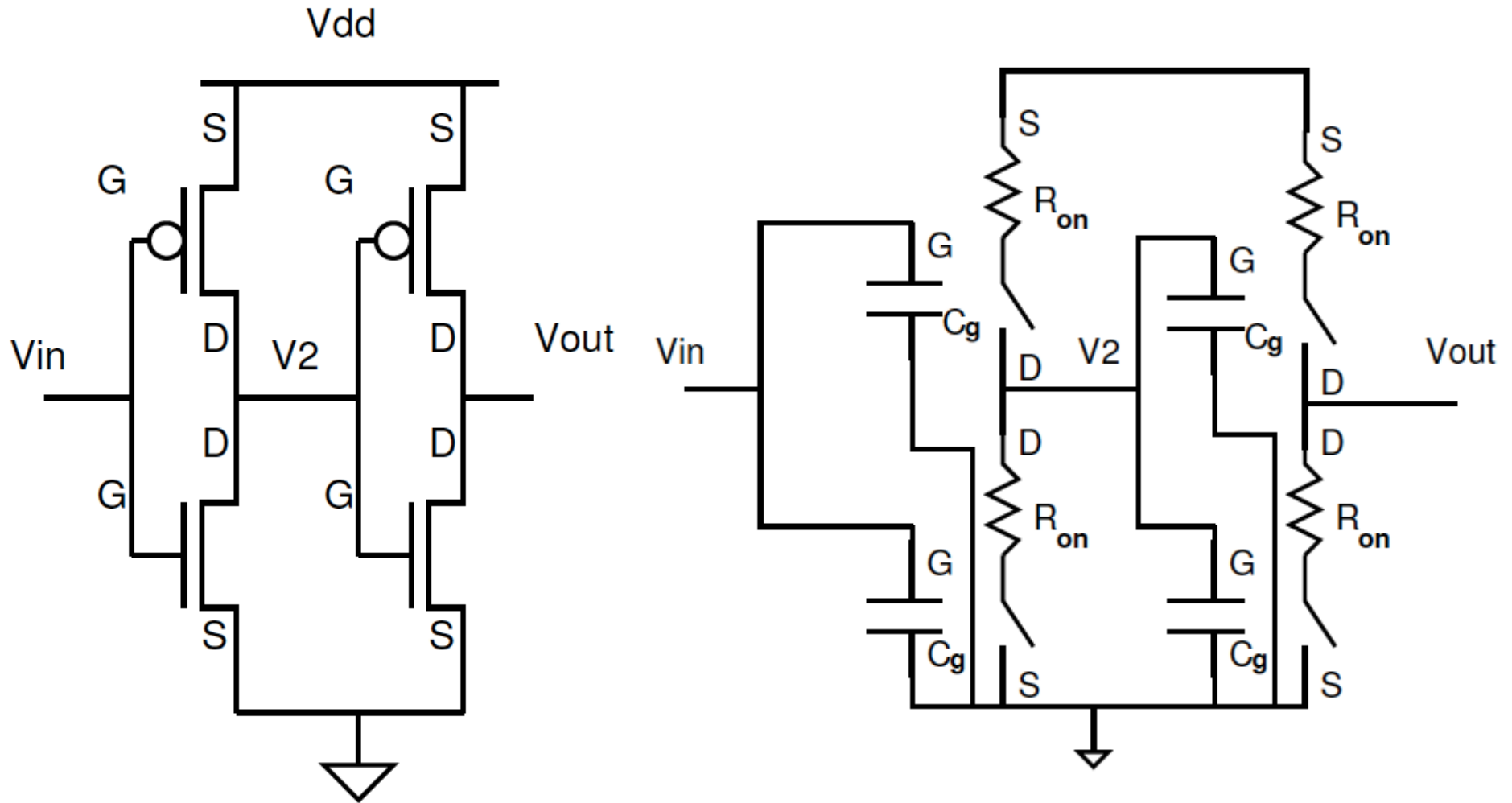
CMOS Buffer Gate - First Order



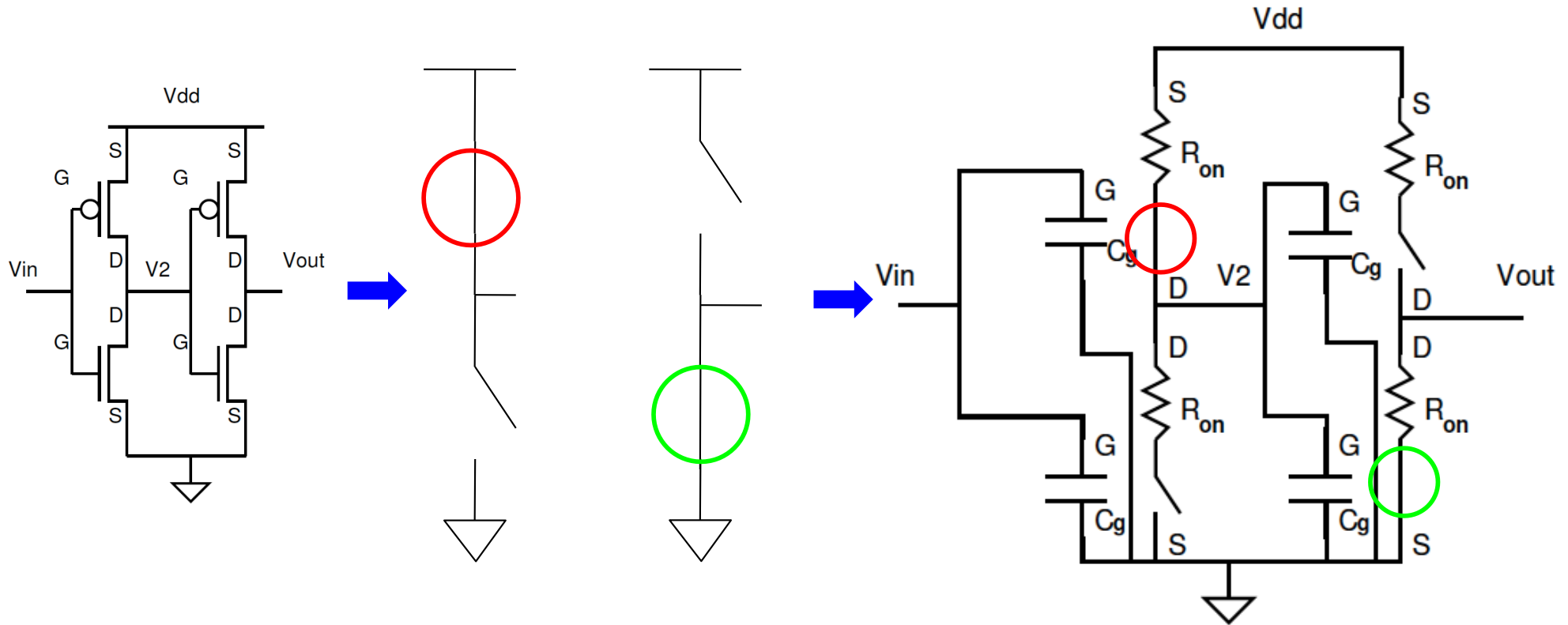
CMOS Buffer Gate - First Order



CMOS Buffer Gate - First Order

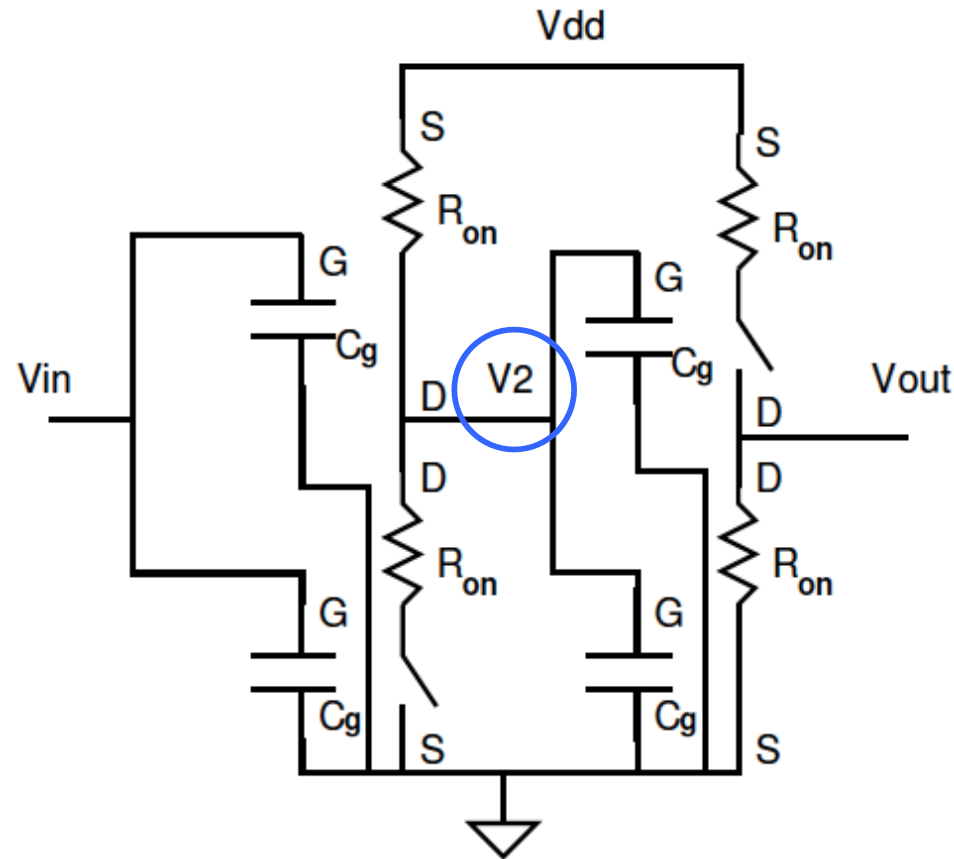


Zero-Order Model to Set Switches



□ What is V_{IN} for this switch pattern?

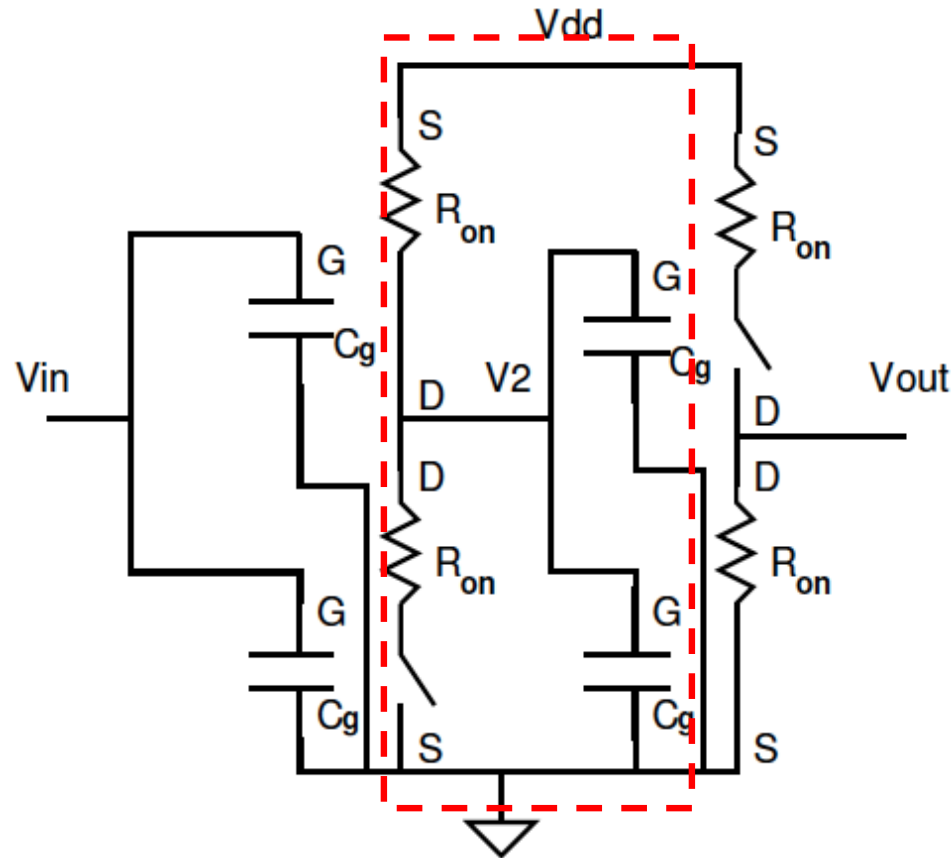
CMOS Buffer Gate - First Order



ESE215 problem

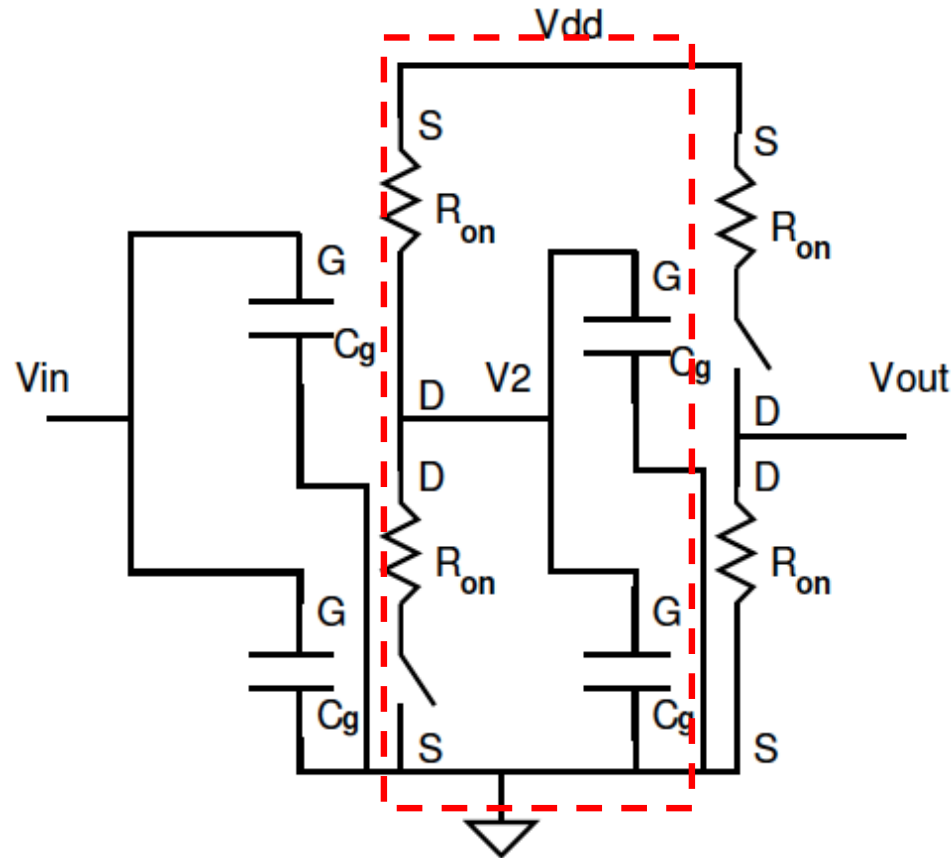
- Leaves an RC Circuit we can analyze

CMOS Buffer Gate - First Order



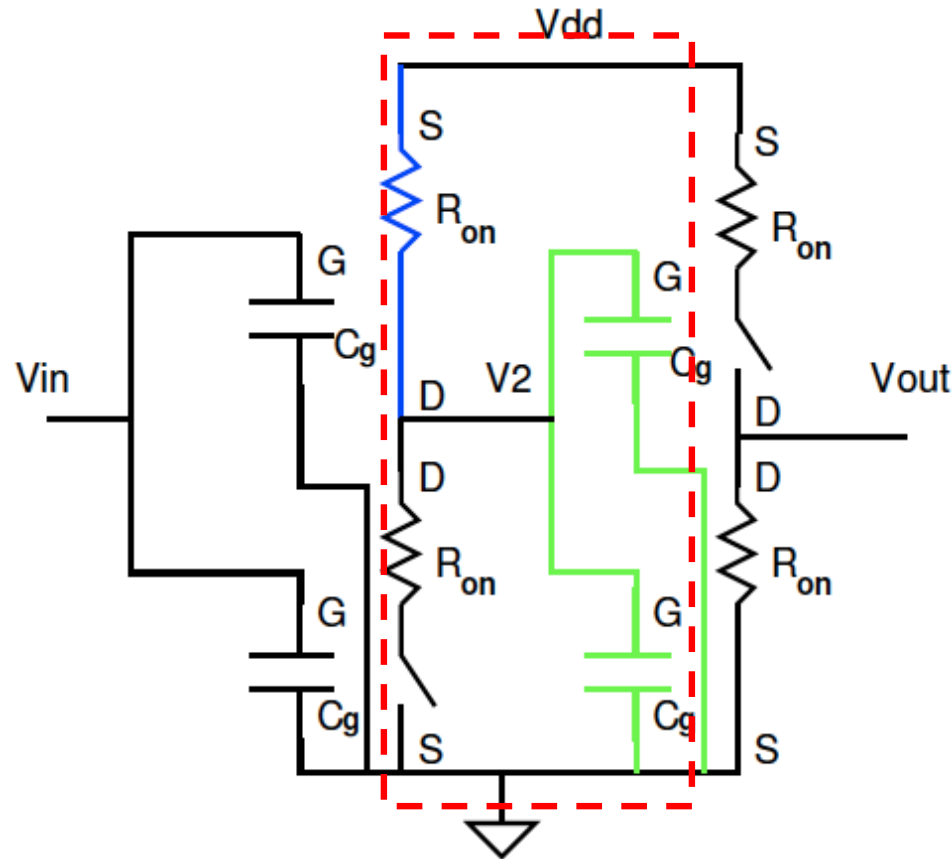
- Look at intermediary node V_2
 - Connected to output of stage 1 and input of stage 2

CMOS Buffer Gate - First Order



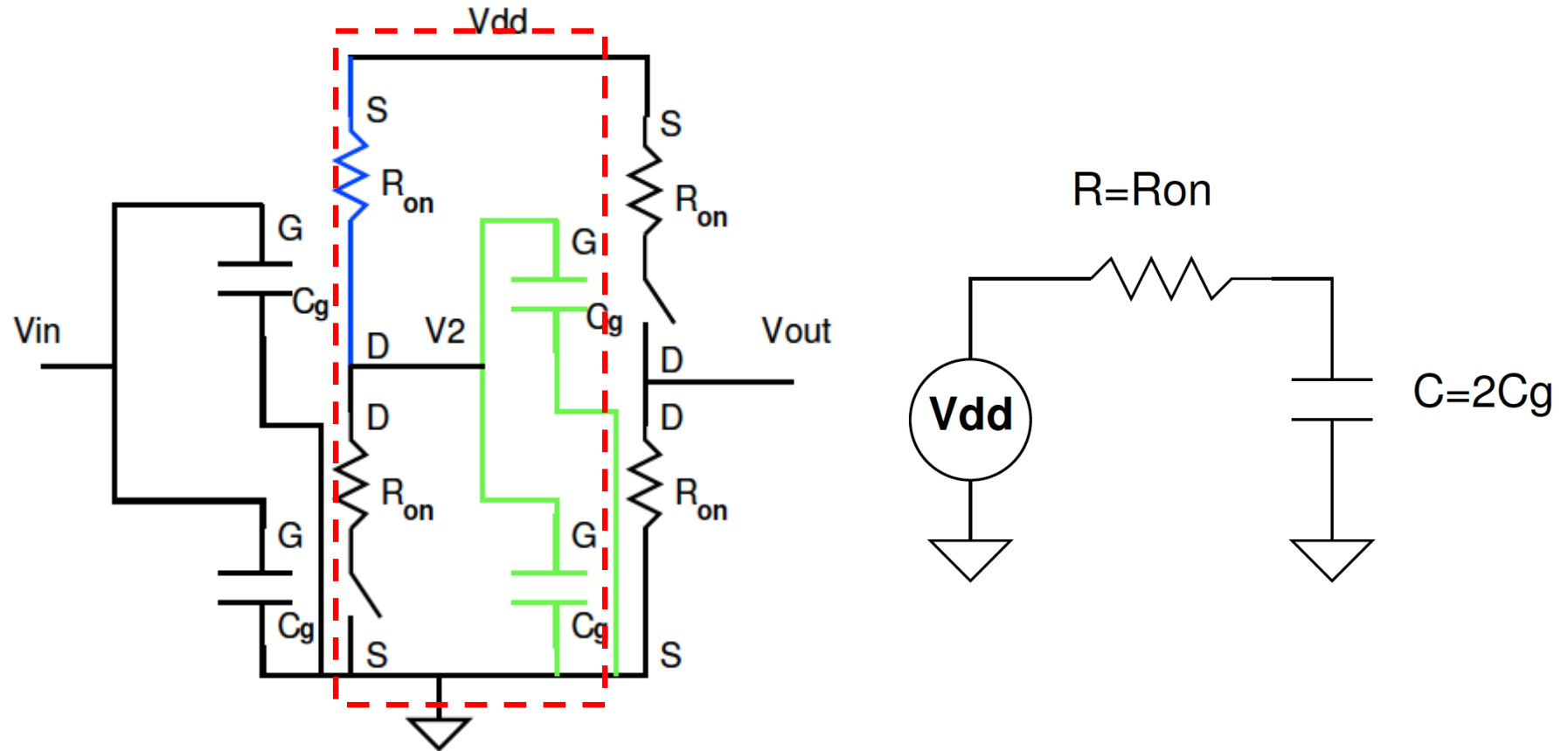
- What is equivalent circuit for the gate output of stage 1 driving V_2 ? What is load on the output of stage 1?

CMOS Buffer Gate - First Order



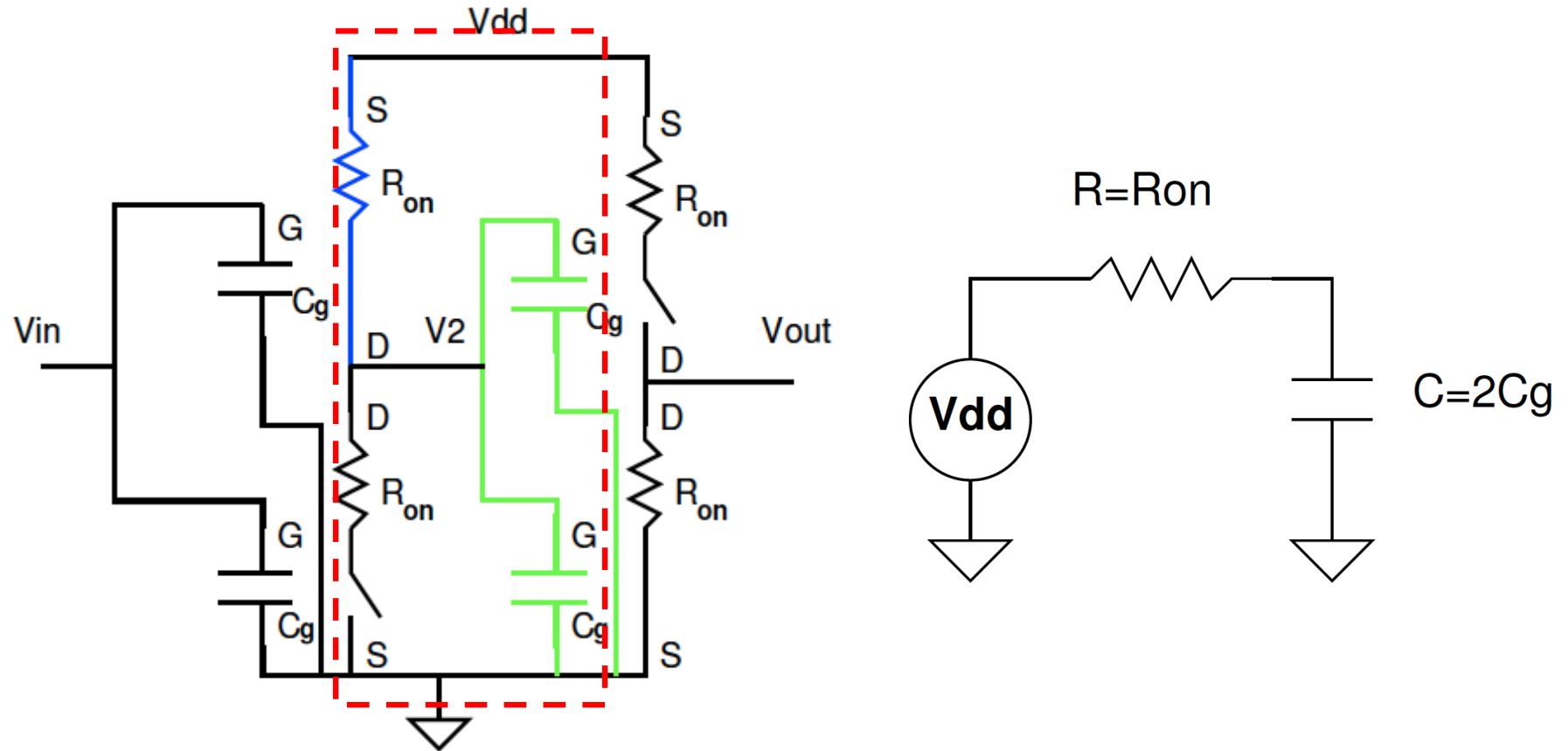
- ❑ Stage 1 equivalent circuit for the gate output
- ❑ Load on V_2
 - Capacitive, input of stage 2

CMOS Buffer Gate - First Order



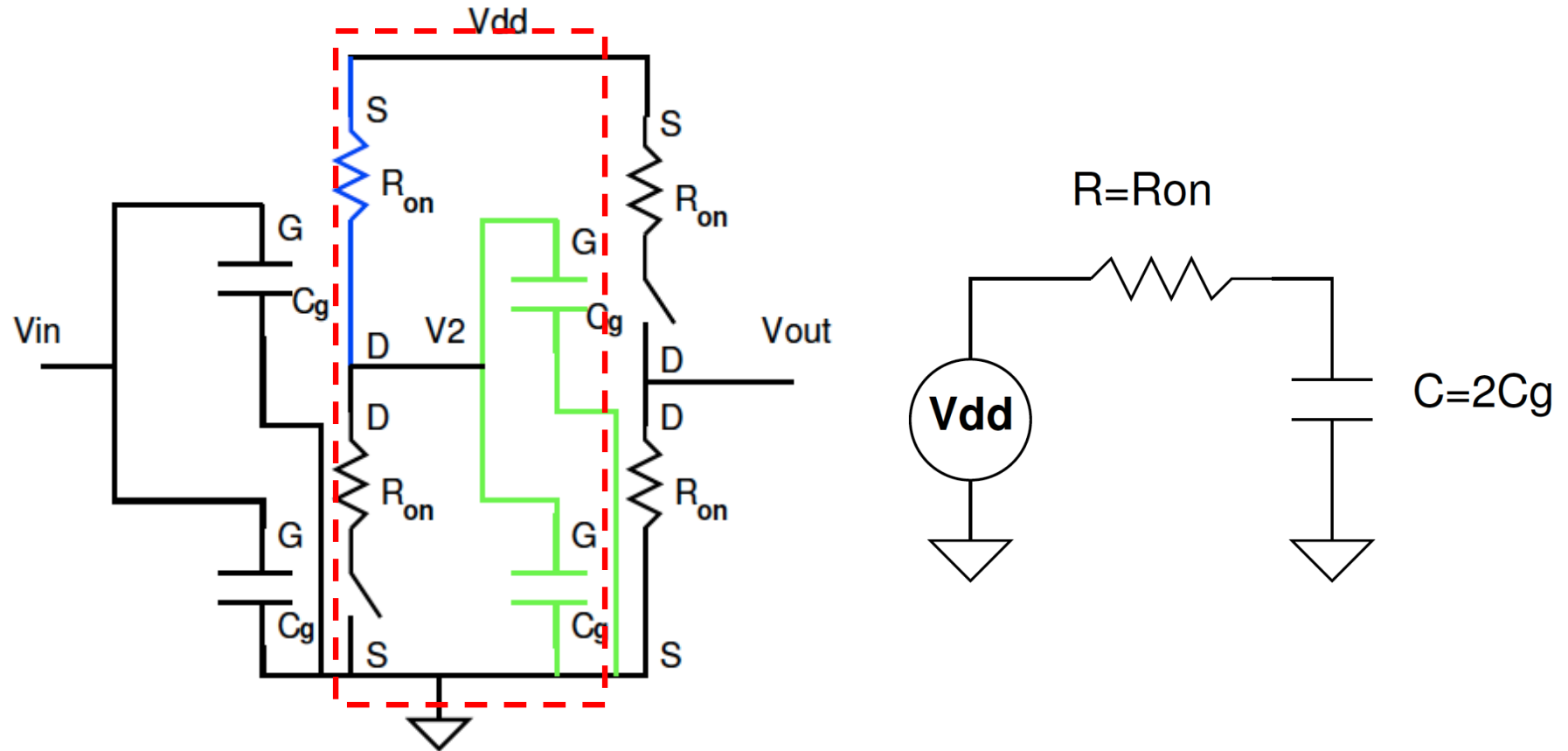
- ❑ Stage 1 equivalent circuit for the gate output
- ❑ Load on V_2
 - Capacitive, input of stage 2

CMOS Buffer Gate - First Order



- What is time constant of V_2 when V_{in} switches from V_{DD} to 0?

CMOS Buffer Gate - First Order



- What is time constant of V_2 when V_{in} switches from V_{DD} to 0?
 - $\tau = 2R_{on}C_g$



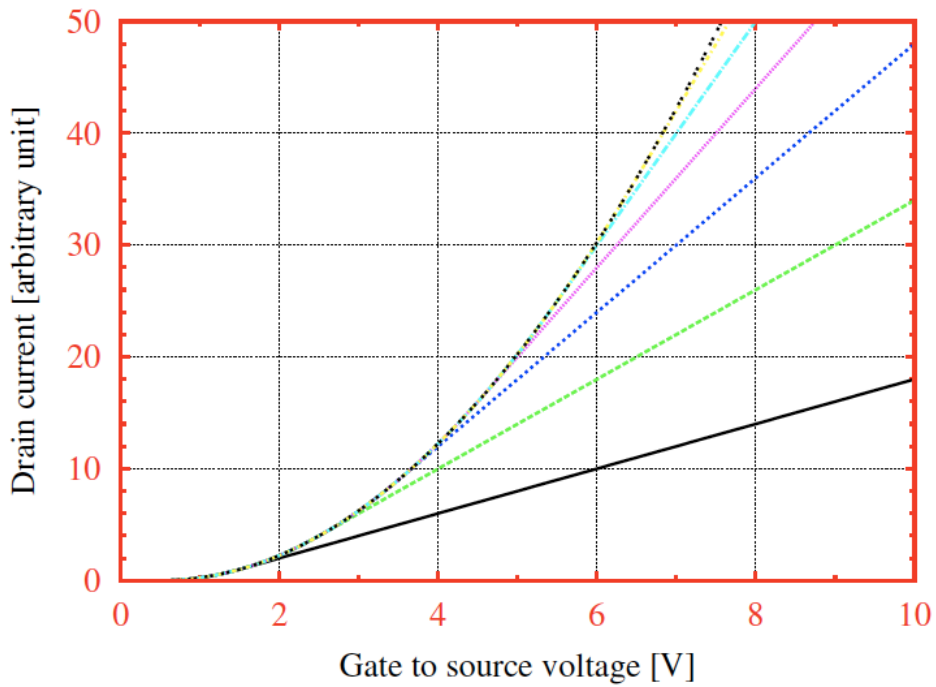
First-Order Model

- ❑ Includes settling times/delay
- ❑ Voltage settling with capacitive loads
 - At least some basis for reasoning about delay

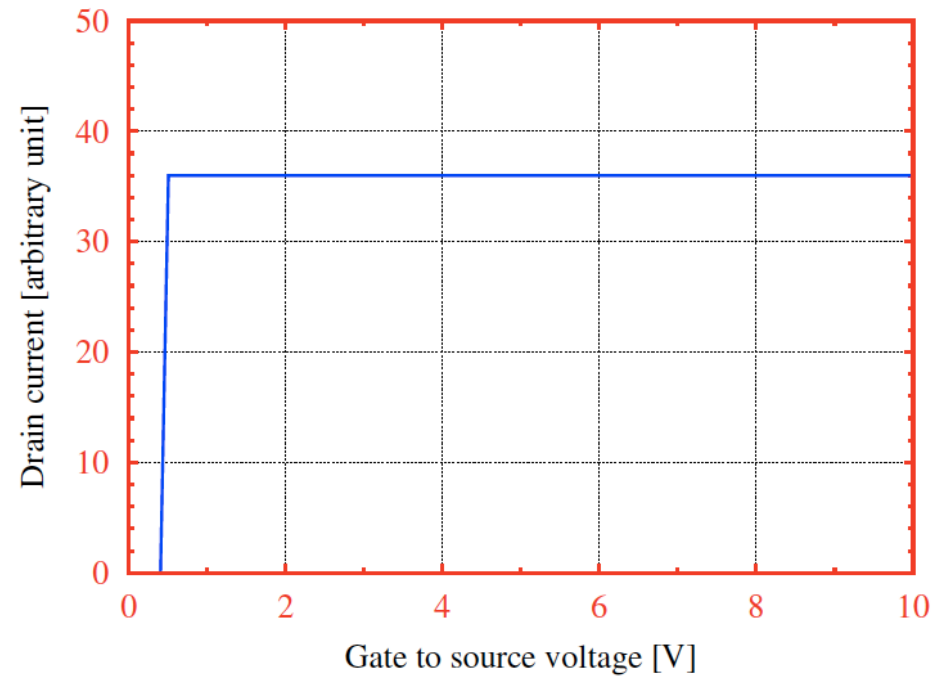


What is still missing?

IV curve



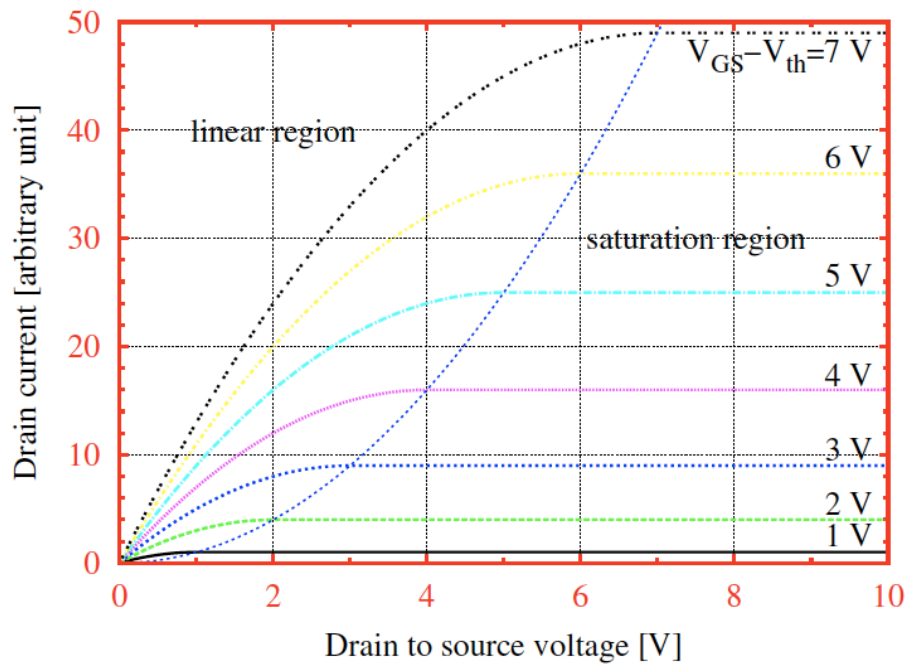
1st Order



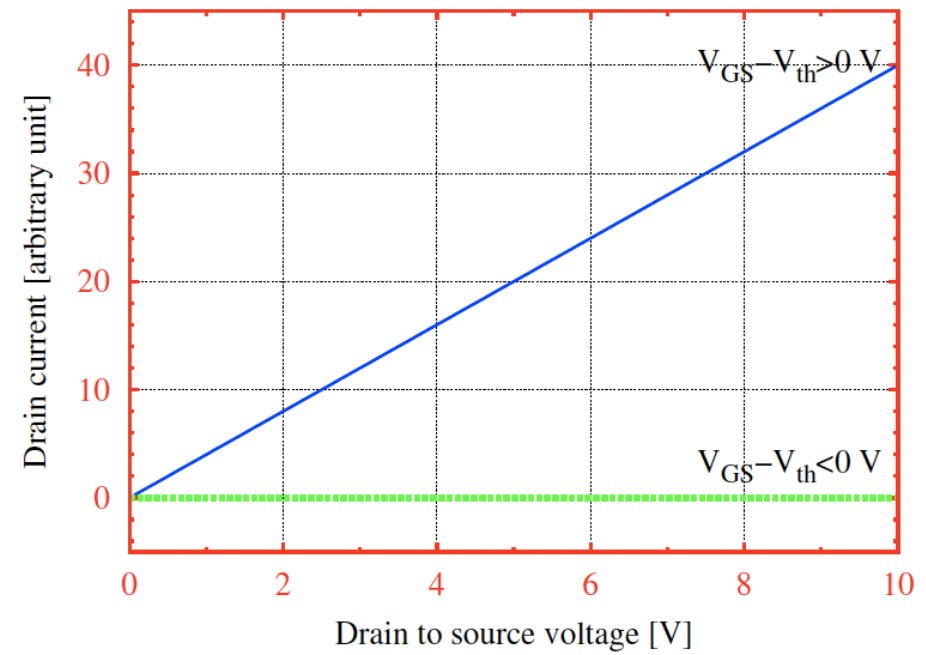


What is still missing?

IV curve



1st Order





What is still missing?

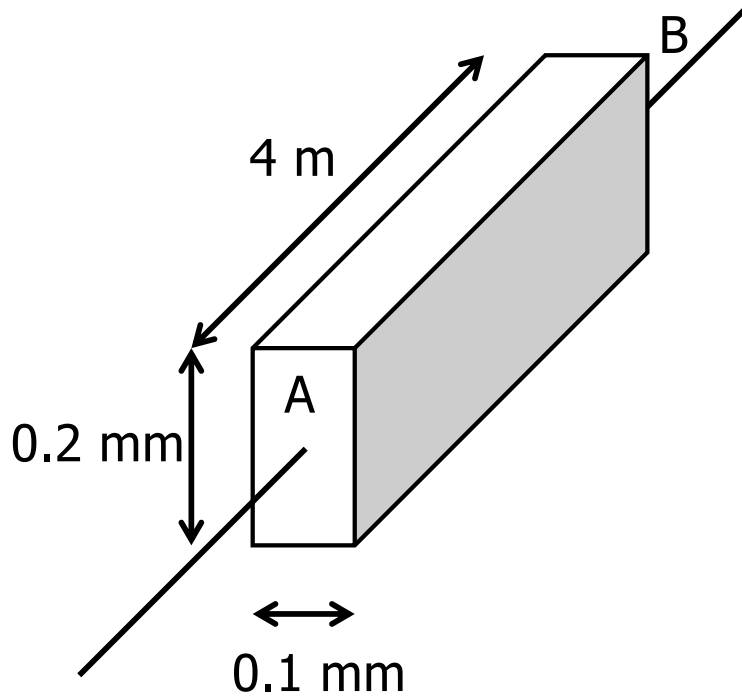
- ❑ What happens at intermediate voltages?
 - When the input is not rail-to-rail (not just gnd or V_{dd} inputs)
- ❑ Details of dynamics, including...
 - Input transition is not an ideal step
 - Intermediate drive strengths change with V_{GS}
 - Drain resistance changes
- ❑ Sub-threshold operation
 - When $V_{gs} < V_{th}$



Design: Engineering Control

- V_{th}
 - Process engineer
- Drive strength (R_{on})
 - Circuit engineer
 - Control with sizing transistors
- Supply voltages (V_{dd})
 - Range set by process engineer
 - Detail use by circuit engineer

Wire Resistance



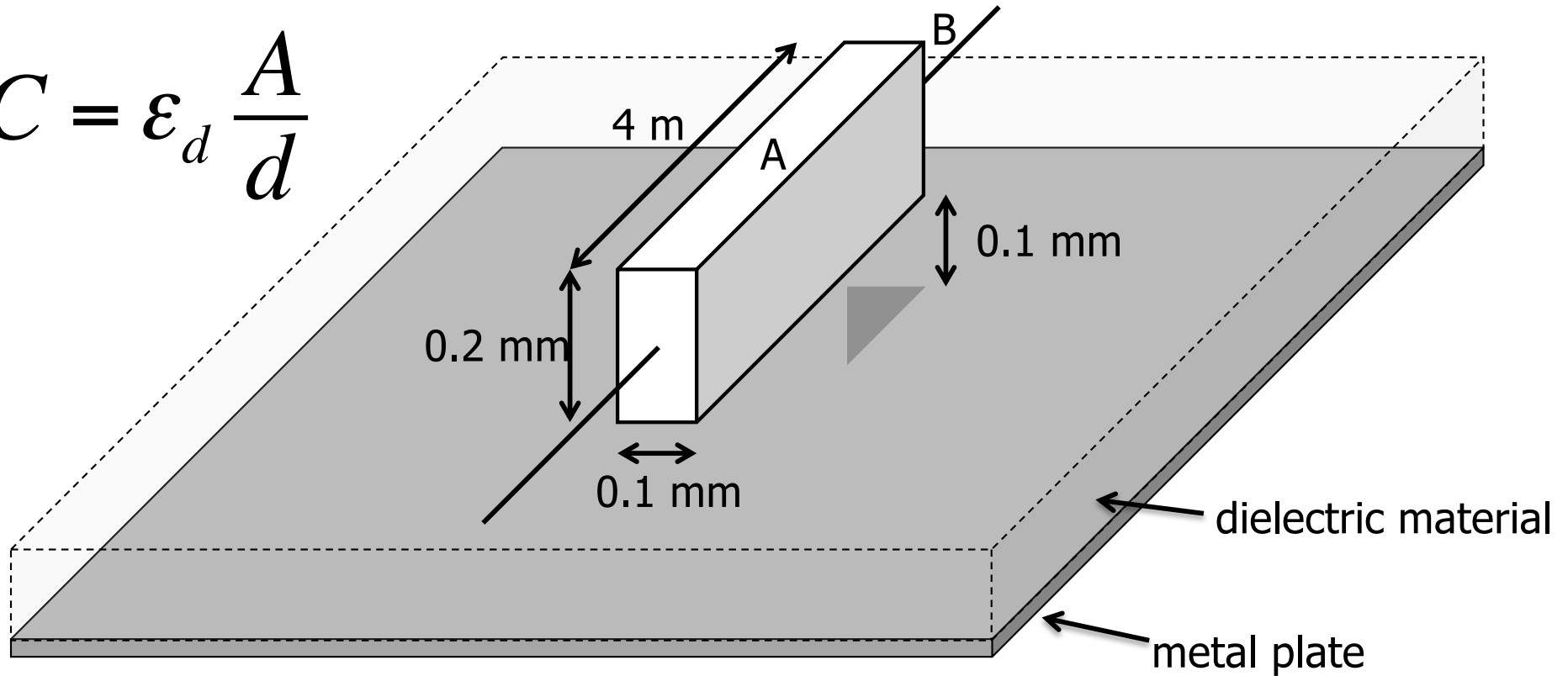
$$R = \frac{\rho L}{A}$$

□ Sanity check

- Wire twice as long = resistors in series
- Wire twice as wide = resistors in parallel

Wire Capacitance

$$C = \epsilon_d \frac{A}{d}$$



□ Sanity check

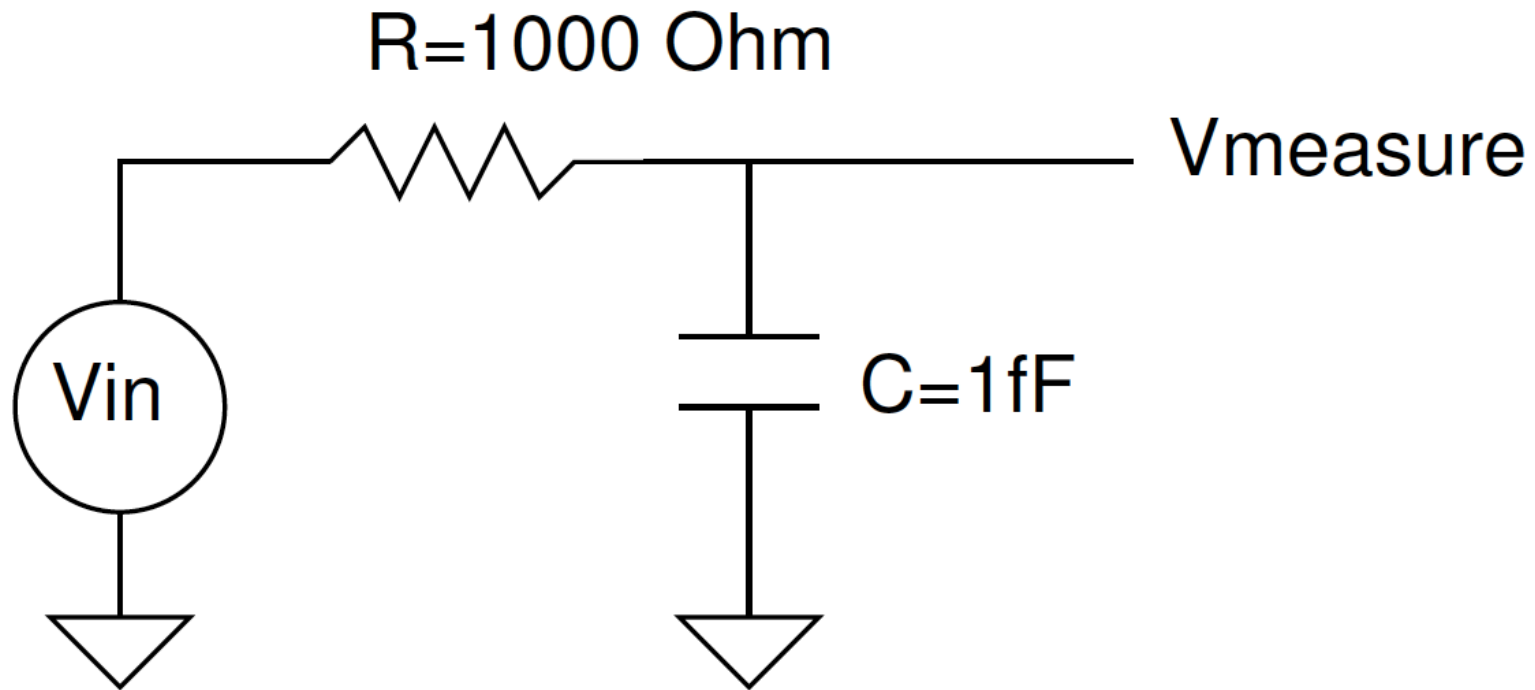
- Wire twice as long = capacitors in parallel
- Wire twice as wide = capacitors in parallel



There are always Rs and Cs

- ❑ Every wire (connection) has resistance
- ❑ Every wire has capacitance
- ❑ (Every wire has inductance)
 - More later
- ❑ Dominant effects
 - $R_{\text{big}} + R_{\text{small}} \approx R_{\text{big}}$ ($R_{\text{wire}} \ll R_{\text{on}})$?
 - $C_{\text{big}} || C_{\text{small}} \approx C_{\text{big}}$ ($C_{\text{wire}} \ll C_{\text{g}}$) ?
 - Today more likely ($C_{\text{wire}} \gg C_{\text{g}}$)

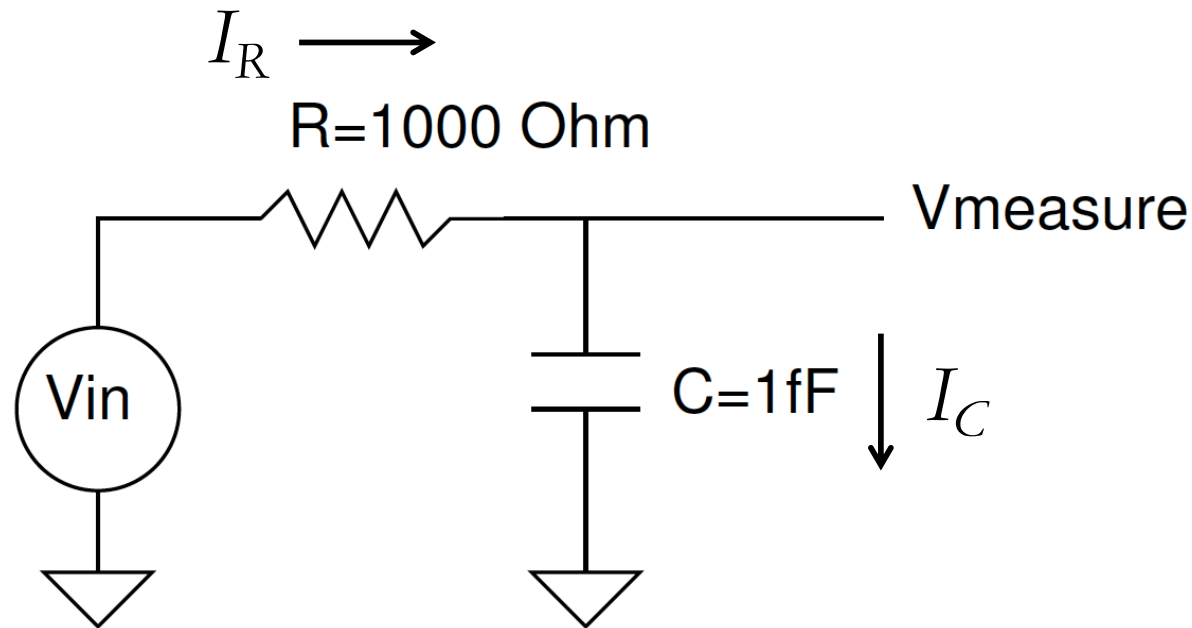
90% Rise Time? (preclass 2a)



What is final $V_{measure}$?

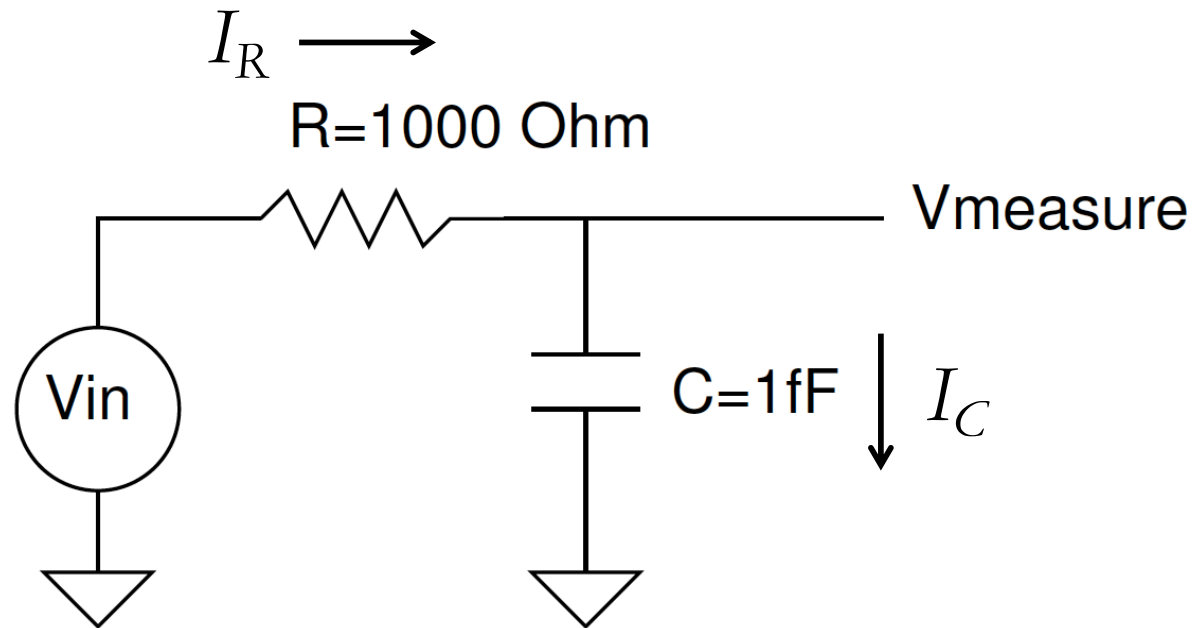
What is time constant, τ ?

Governing Equations? (KCL)



- KCL @ $V_{measure}$
 - Kirchoff's Current Law
 - Sum of all currents into a node = 0
 - Current entering a node = current exiting a node
 - $I_R = I_C$

Governing Equations? (KCL)

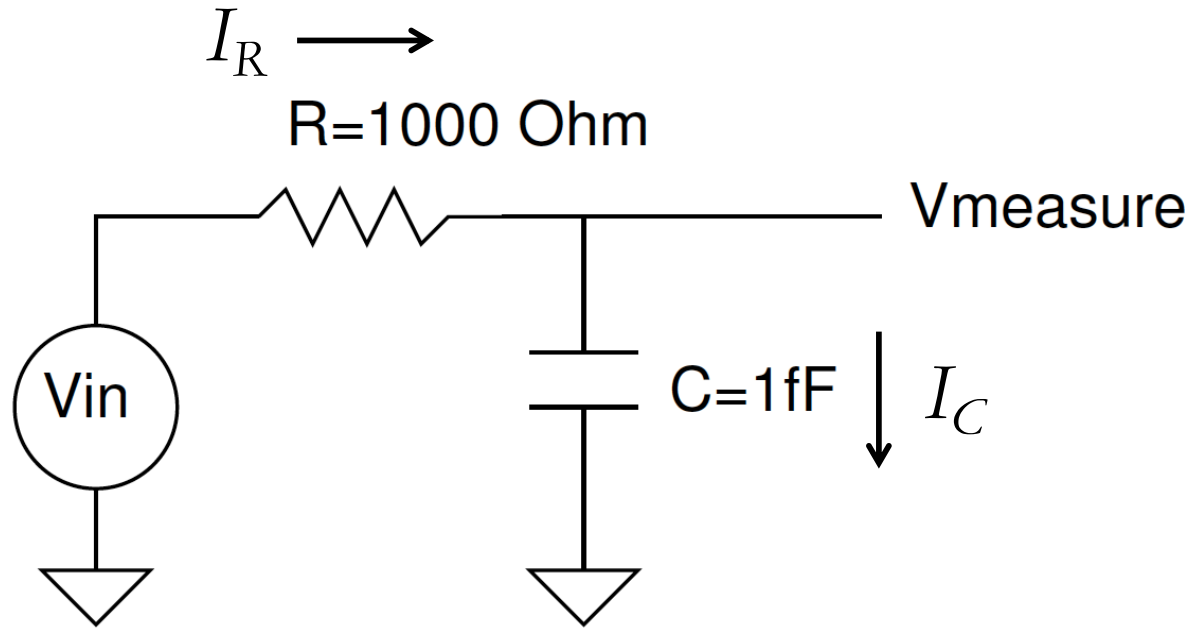


$$I_R = I_C$$

$$\frac{V_R}{R} = C \frac{dV_C}{dt}$$

$$\frac{V_{in} - V_{measure}}{R} = C \frac{dV_{measure}}{dt}$$

Governing Equations? (KCL)



$$I_R = I_C$$

$$\frac{V_R}{R} = C \frac{dV_C}{dt}$$

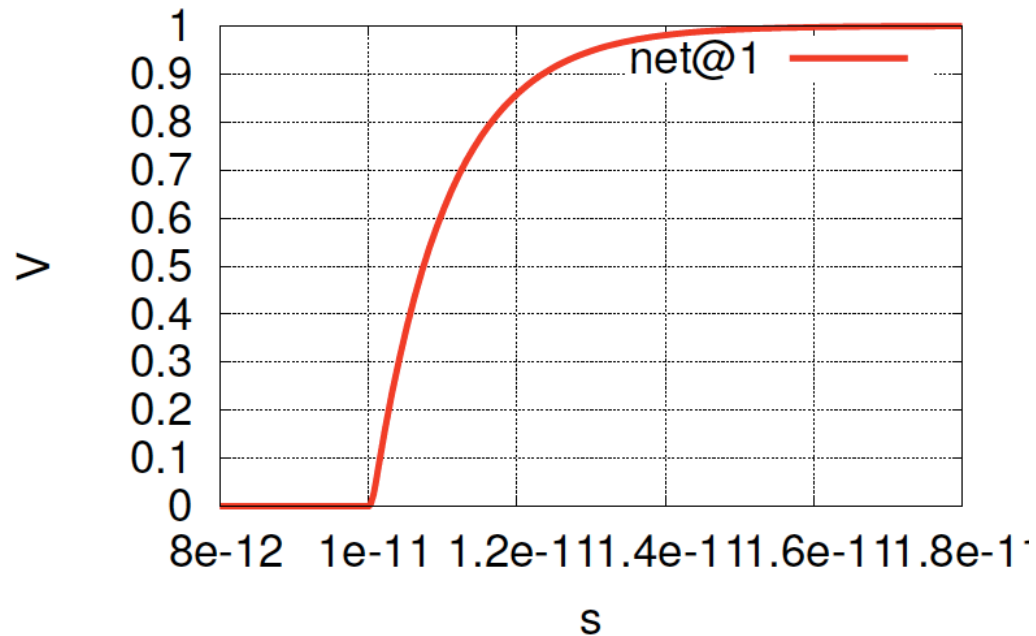
$$\frac{V_{in} - V_{measure}}{R} = C \frac{dV_{measure}}{dt}$$

$$0 = \frac{dV_{measure}}{dt} + \frac{1}{RC} V_{measure} - \frac{V_{in}}{RC}$$

$$V_{measure} = V_{in} \left(1 - \left(e^{-t/RC} \right) \right)$$
$$\tau = RC$$

What does look like?

*** spice deck for cell test_rc{sch} from library t



$$V_{measure} = V_{in} \left(1 - \left(e^{-t/RC} \right) \right)$$

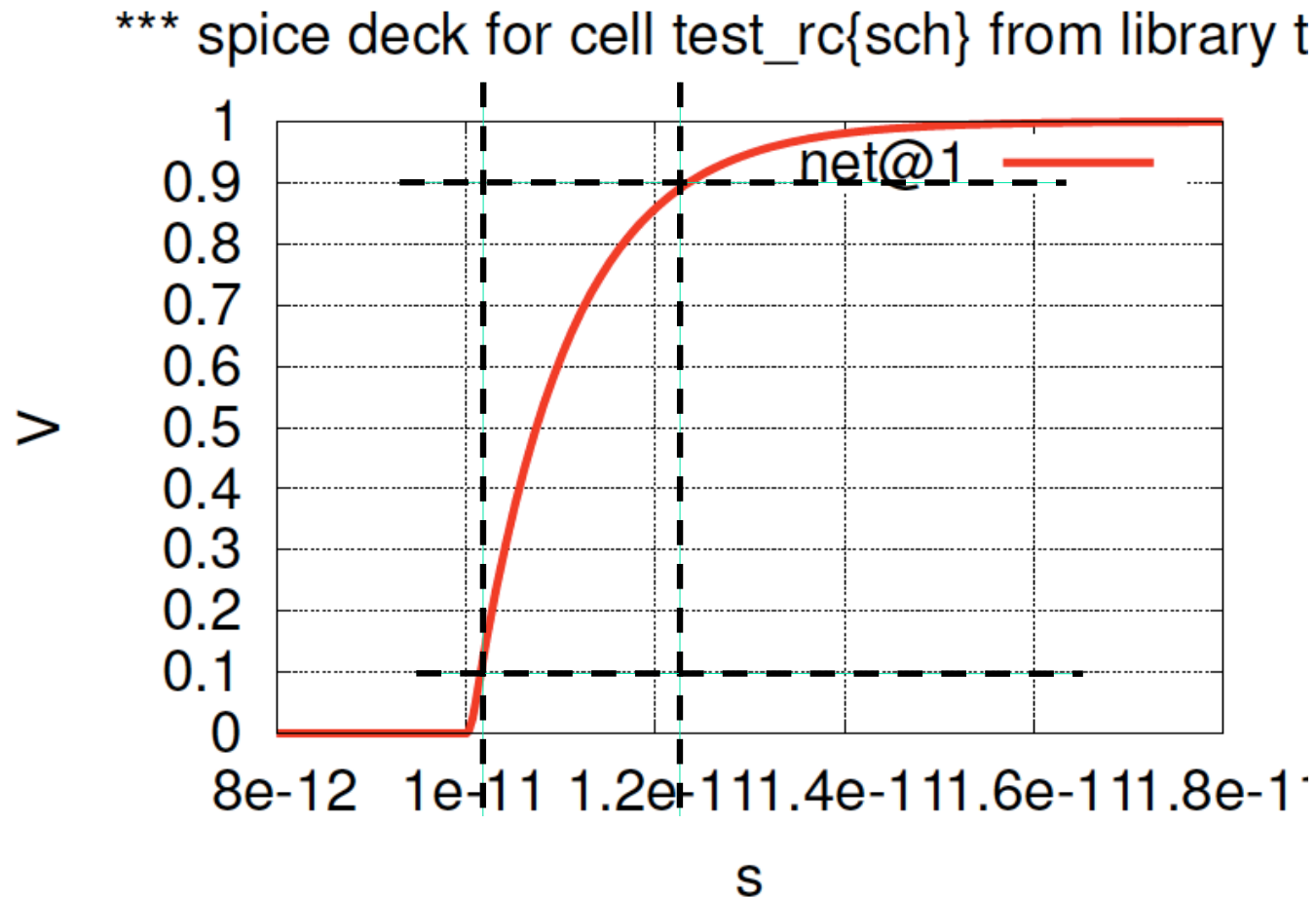
Shape of Curve (preclass 1b)

t (in ps)	$e^{-t/RC}$	$1-e^{-t/RC}$
0		
0.1		
1		
2		
2.3		

$$V_{in} = 1$$

$$V_{measure} = V_{in} \left(1 - \left(e^{-t/RC} \right) \right)$$

Rise Time: 10—90%



$$t_{\text{rise}} \approx 2.2\text{ps} \approx 2.2\tau$$

Shape of Curve (preclass 2c)

t (in ps)	$e^{-t/RC}$	$1-e^{-t/RC}$
0	1	0
0.1	0.9	0.1 10%
1	$1/e = 0.37$	0.66
2	$1/e^2 = 0.14$	0.86
2.3	0.1	0.9 90%

$$V_{in} = 1$$

$$V_{measure} = V_{in} \left(1 - \left(e^{-t/RC} \right) \right)$$

At what time is $V_{measure}$ 50% of its value?

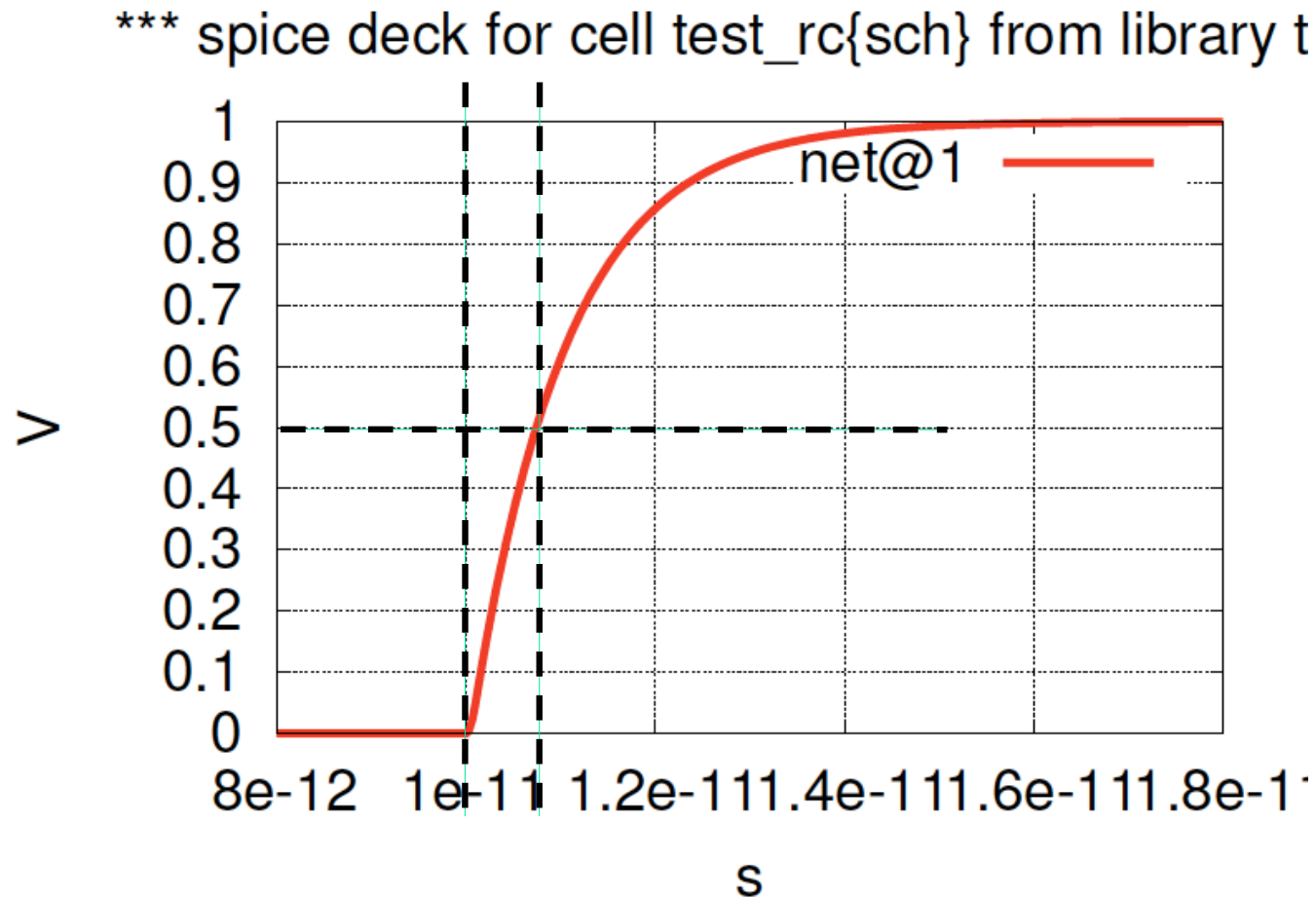
Shape of Curve (preclass 2c)

t (in ps)	$e^{-t/RC}$	$1-e^{-t/RC}$
0	1	0
0.1	0.9	0.1 10%
0.69	0.5	0.5 50%
1	$1/e = 0.37$	0.66
2	$1/e^2 = 0.14$	0.86 90%
2.3	0.1	0.9

$$V_{in} = 1$$

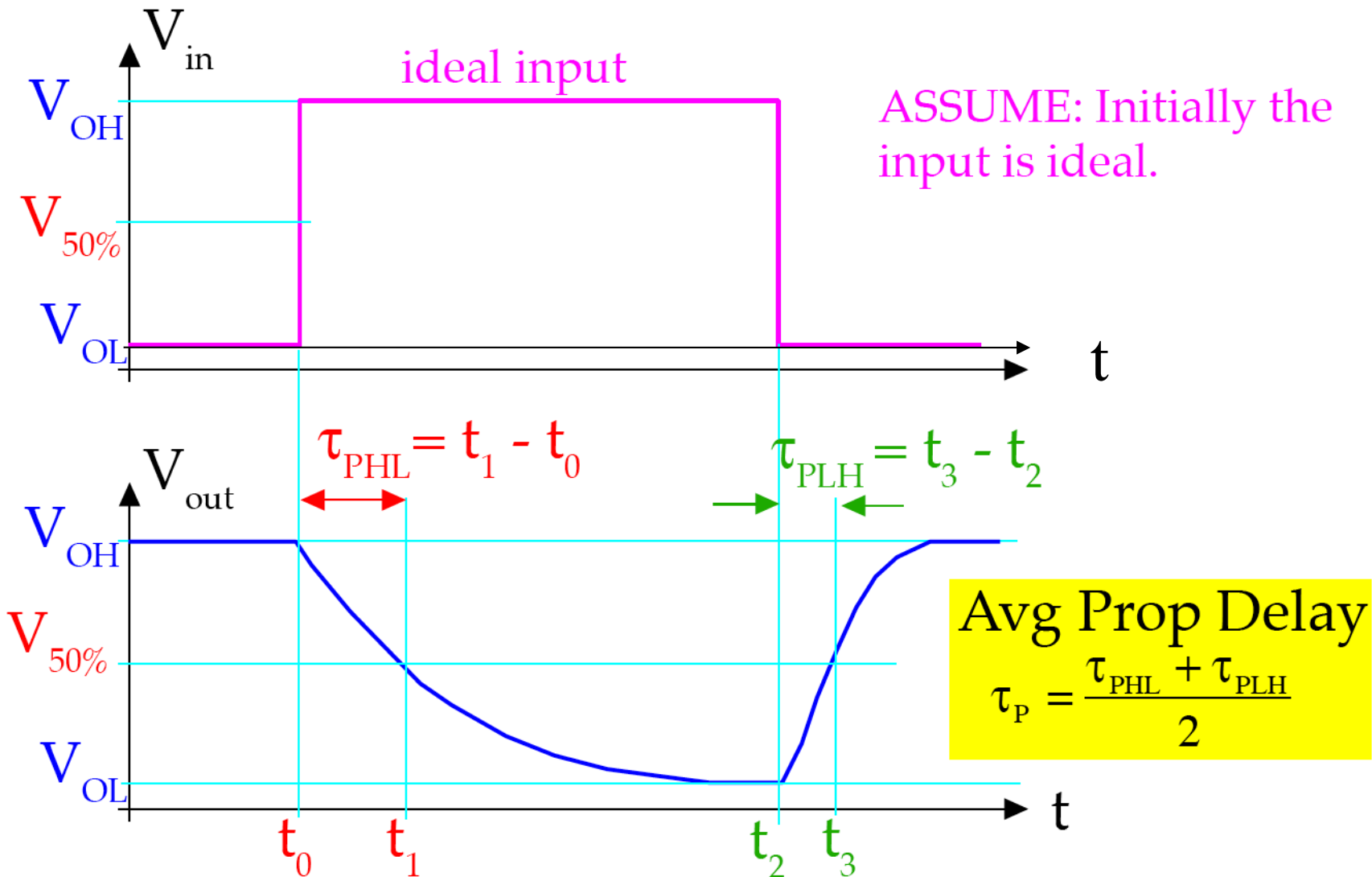
$$V_{measure} = V_{in} \left(1 - \left(e^{-t/RC} \right) \right)$$

Delay Time: 50% (in)—50% (out)



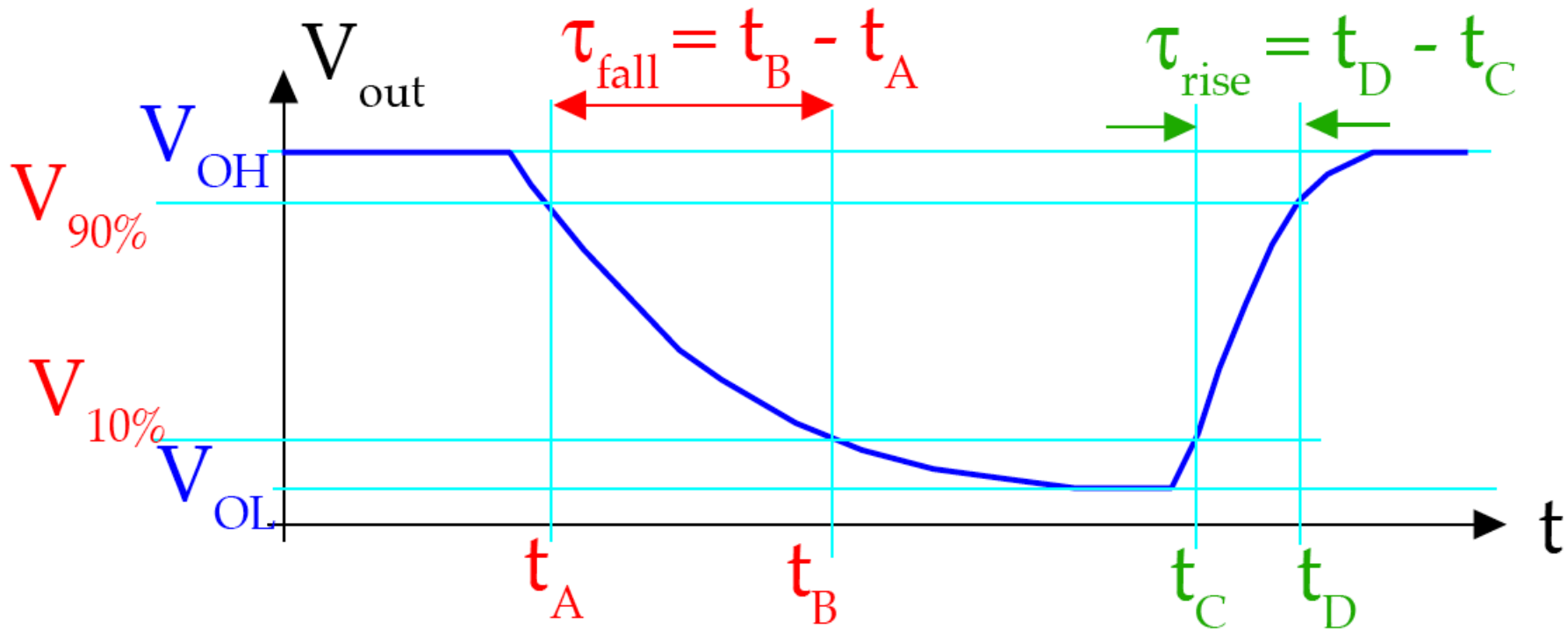
$$t_{\text{PLH}} \approx .69\text{ps} \approx .69\tau$$

Propagation Delay Definitions



$$V_{50\%} = V_{OL} + 0.5 [V_{OH} - V_{OL}] = 0.5 [V_{OL} + V_{OH}]$$

Rise/Fall Times

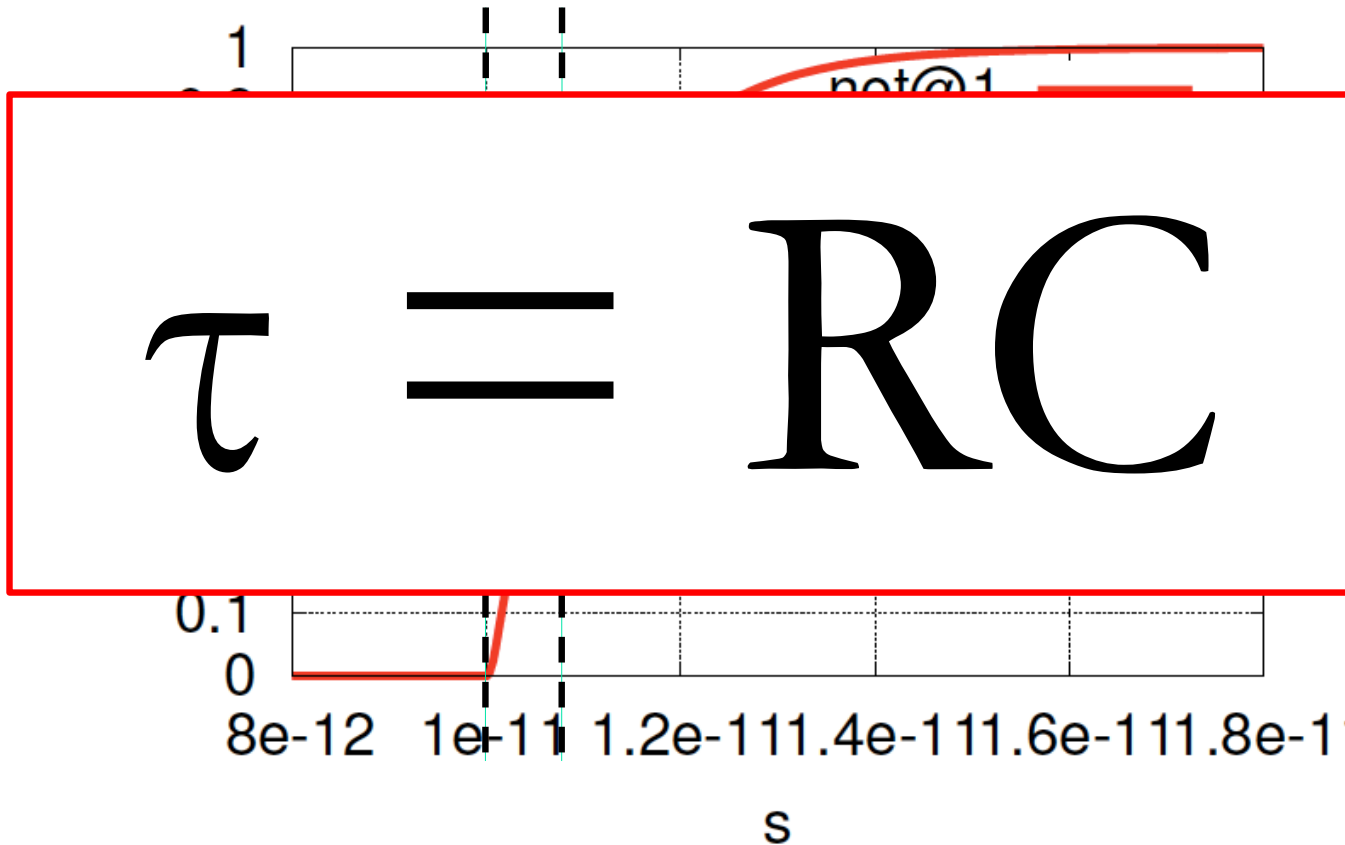


$$V_{10\%} = V_{OL} + 0.1 [V_{OH} - V_{OL}]$$

$$V_{90\%} = V_{OL} + 0.9 [V_{OH} - V_{OL}]$$

Delay Time: 50% (in)—50% (out)

*** spice deck for cell test_rc{sch} from library t

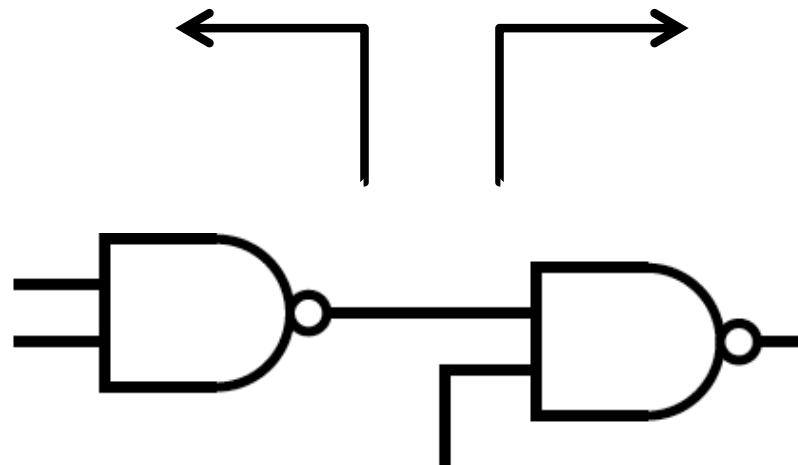


$$t_{\text{PLH}} \approx .69\text{ps} \approx .69\tau$$

Voltage Waveform at Output/Input Node

R_{drive} from
looking into
output stages

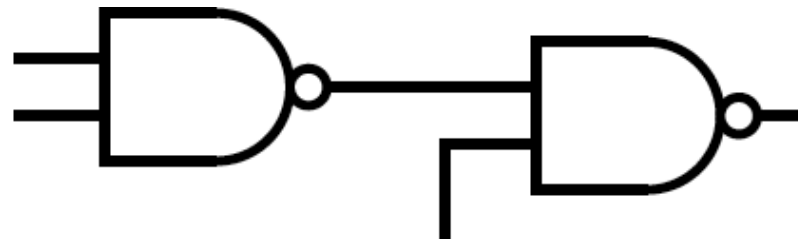
C_{load} from
looking into
input stages



Voltage Waveform at Output/Input Node

R_{drive} from
looking into
output stages
and wires

C_{load} from
looking into
input stages
and wires



What is C?



Capacitance

- Wire
- Fanout -- Total gate load
 - Logical Gate
 - MOSFET gate



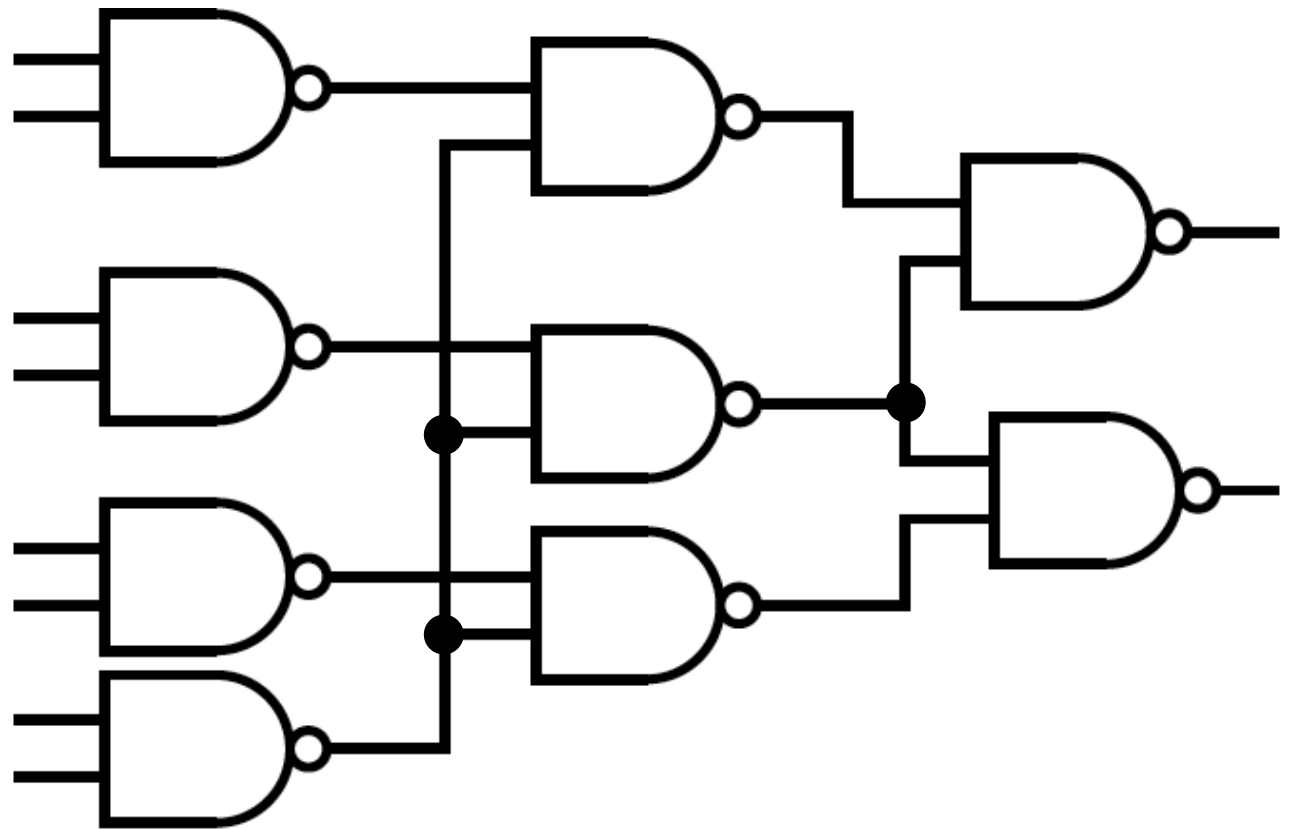
Fanout

- Number of things to which a gate output connects



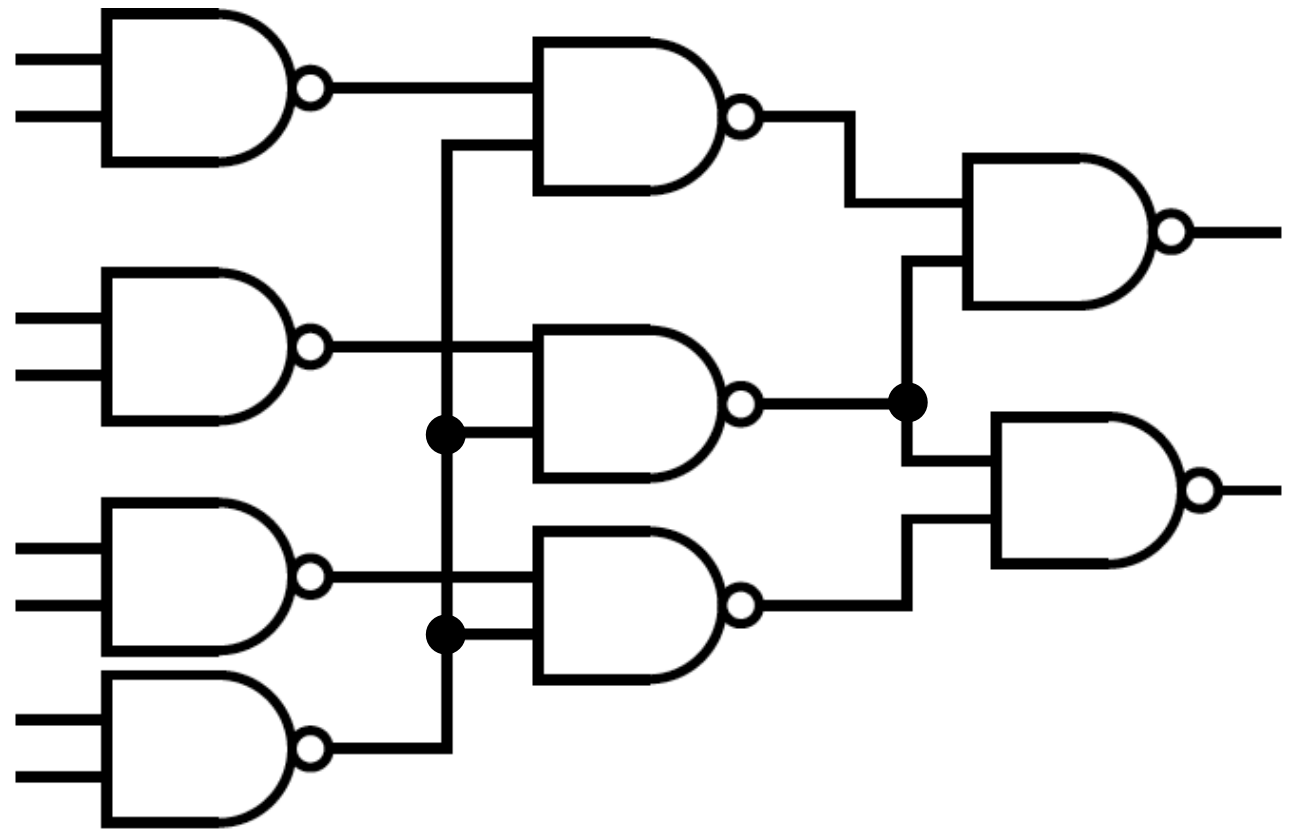
Fanout in Circuit

- ❑ Output routed to many gate inputs



Fanout in Circuit (preclass 3)

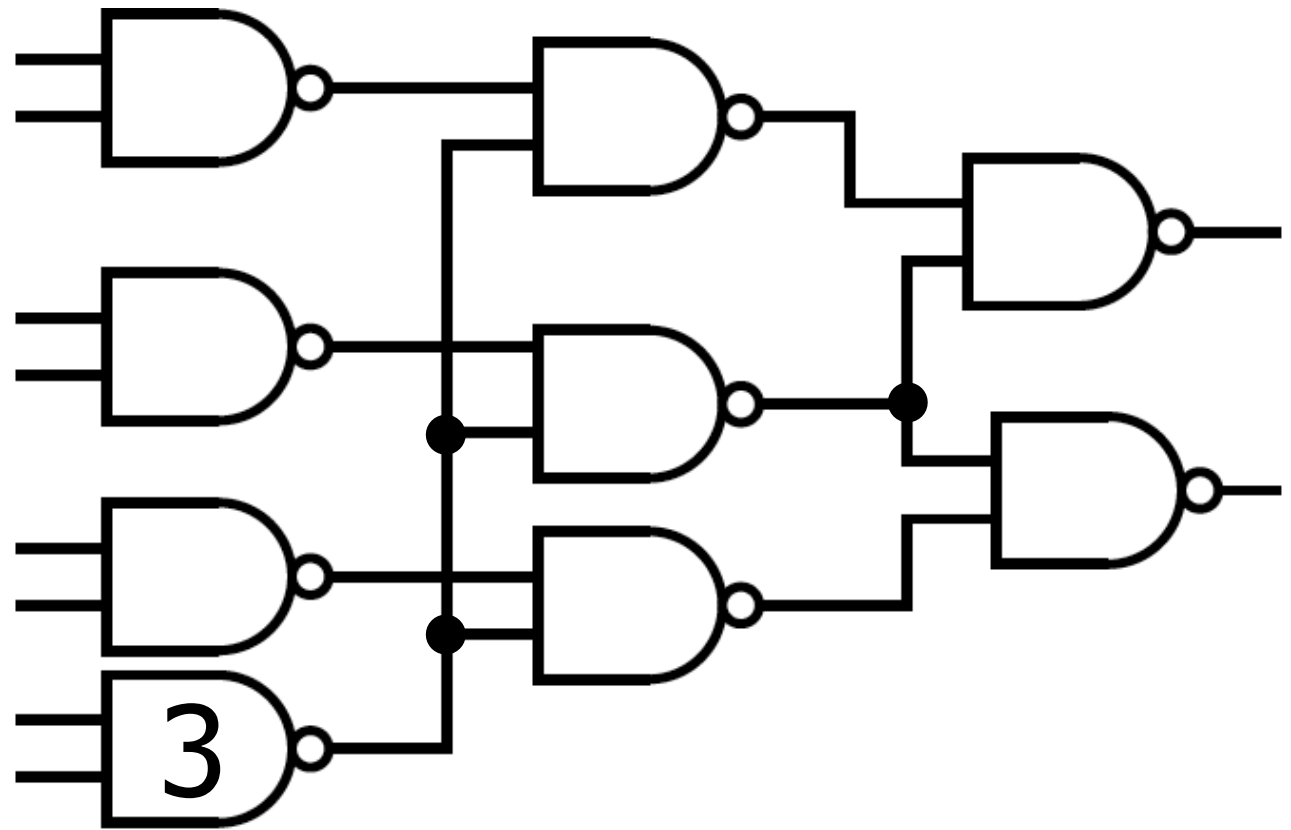
- ❑ Maximum fanout?
- ❑ Second?
- ❑ Min?





Fanout in Circuit

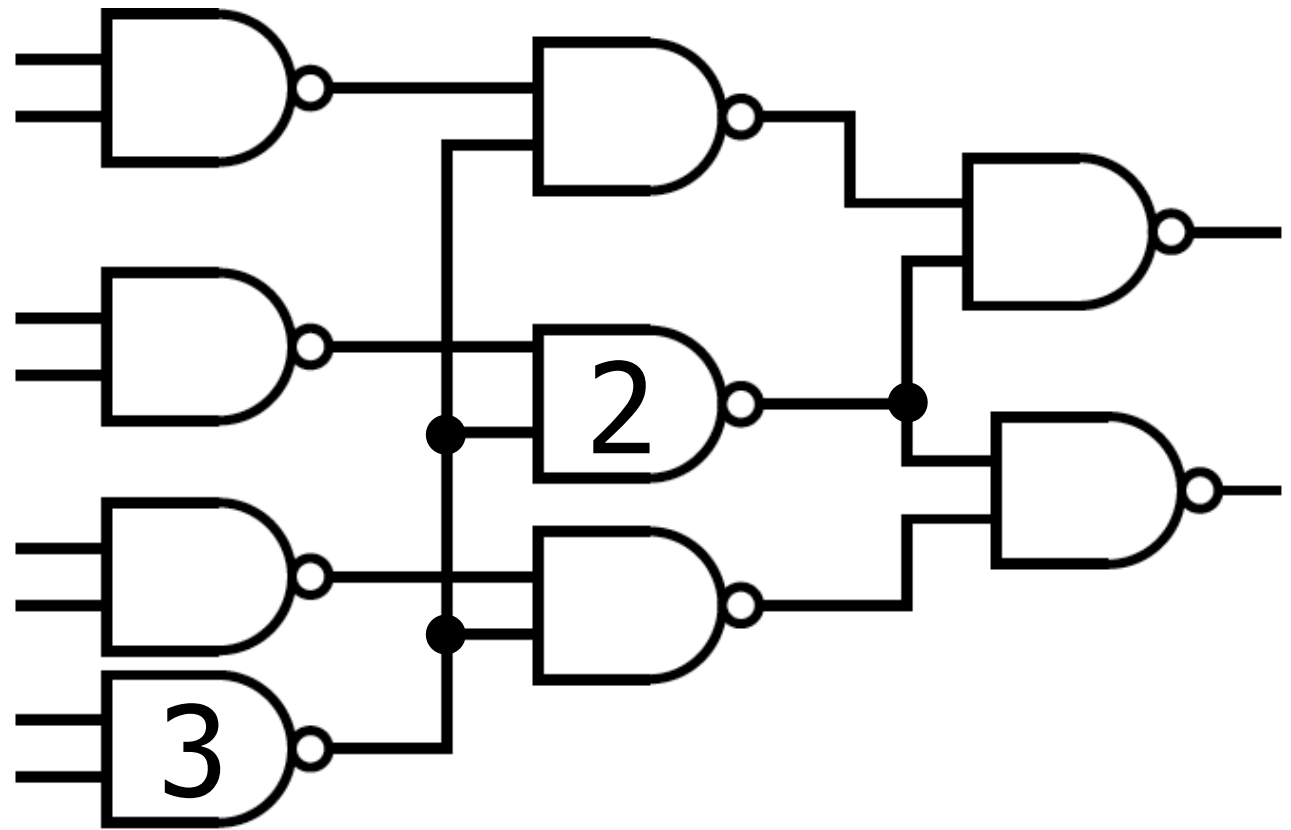
- ❑ Maximum fanout?
- ❑ Second?
- ❑ Min?





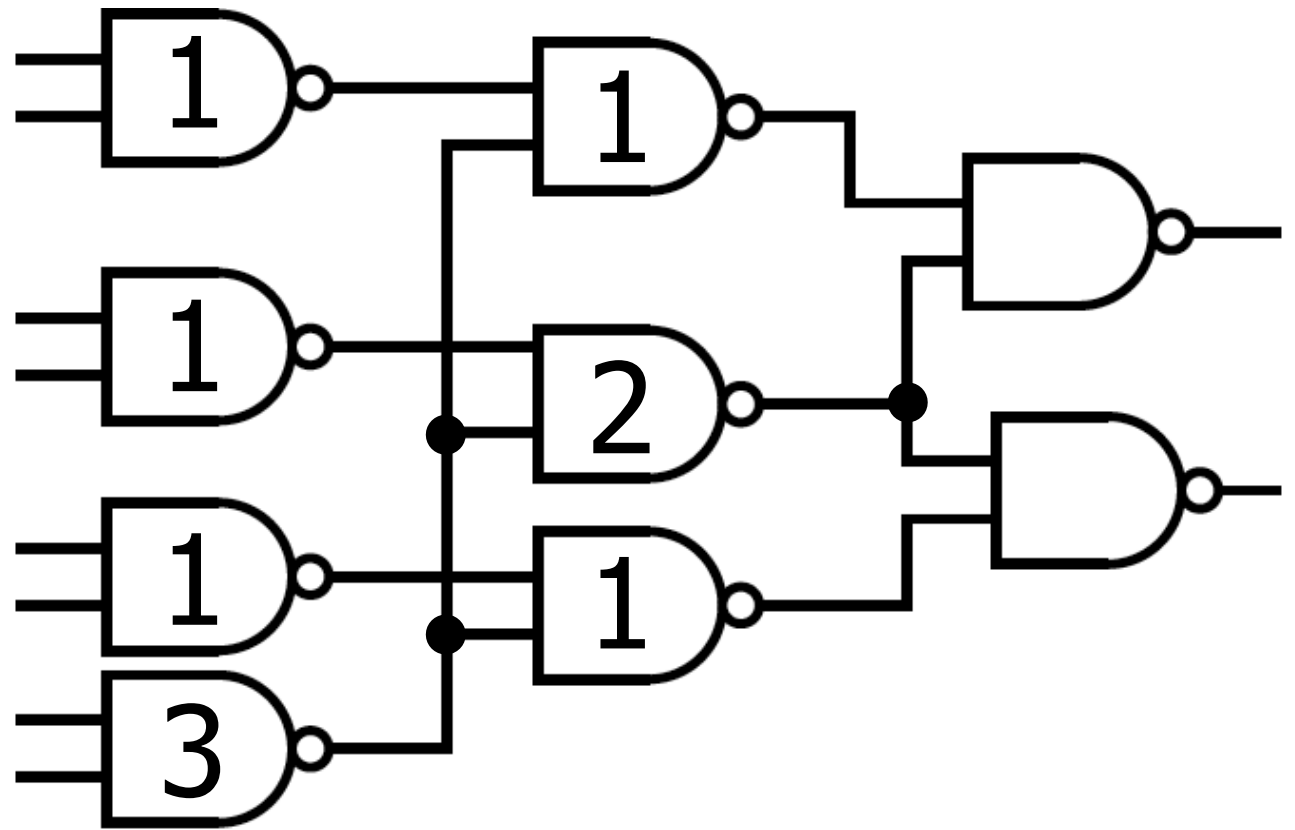
Fanout in Circuit

- ❑ Maximum fanout?
- ❑ Second?
- ❑ Min?



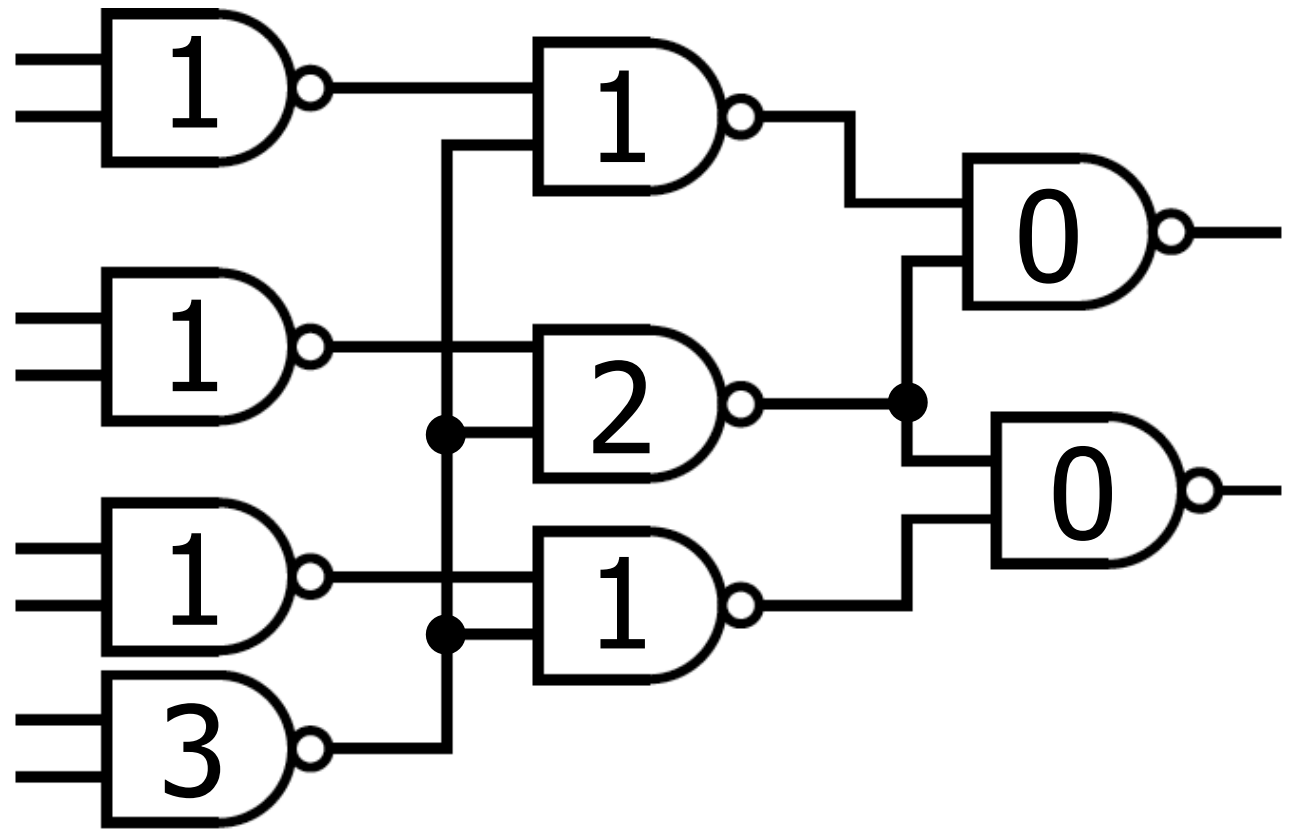
Fanout in Circuit

- ❑ Maximum fanout?
- ❑ Second?
- ❑ Min?



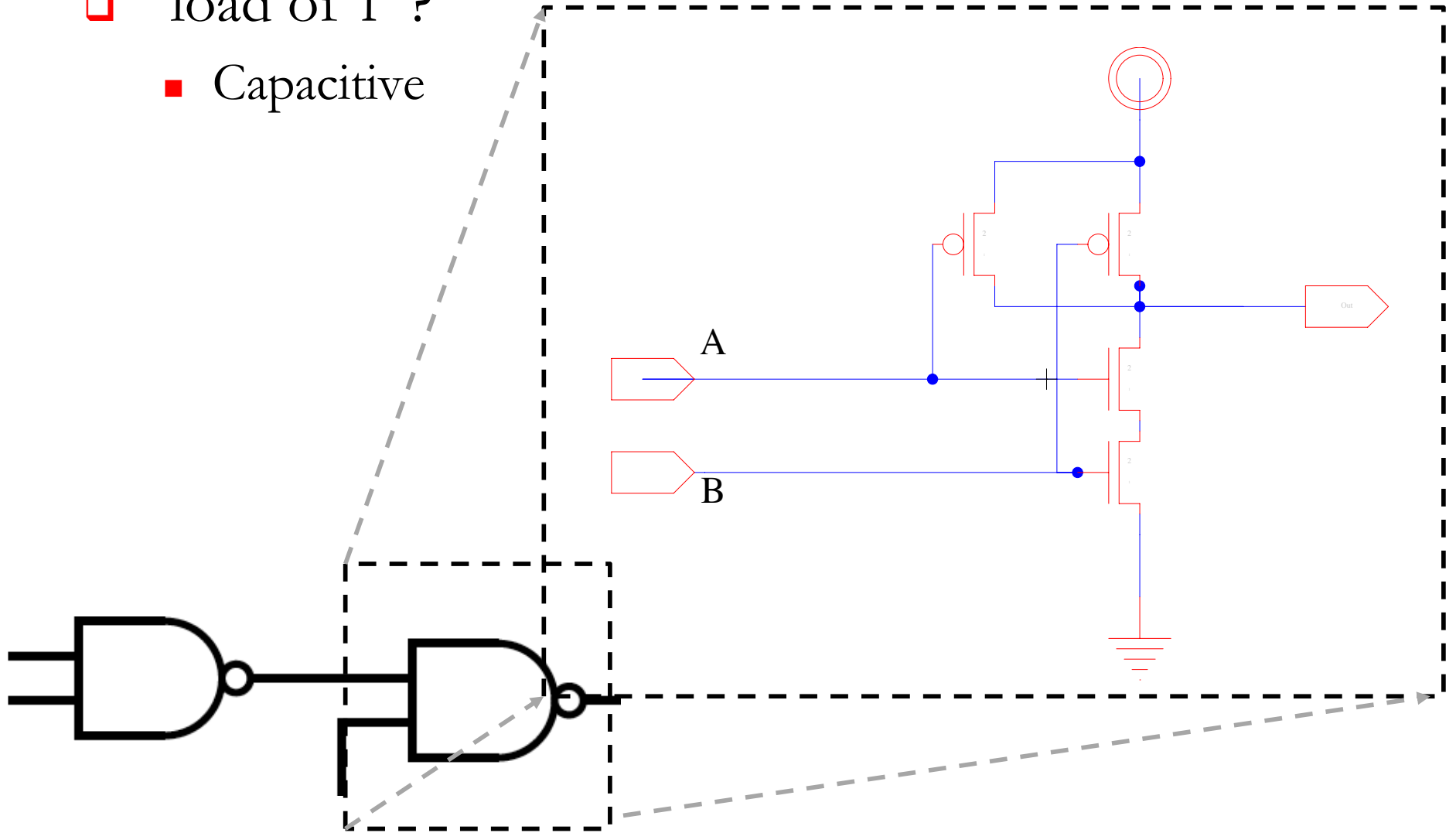
Fanout in Circuit

- ❑ Maximum fanout?
- ❑ Second?
- ❑ Min?



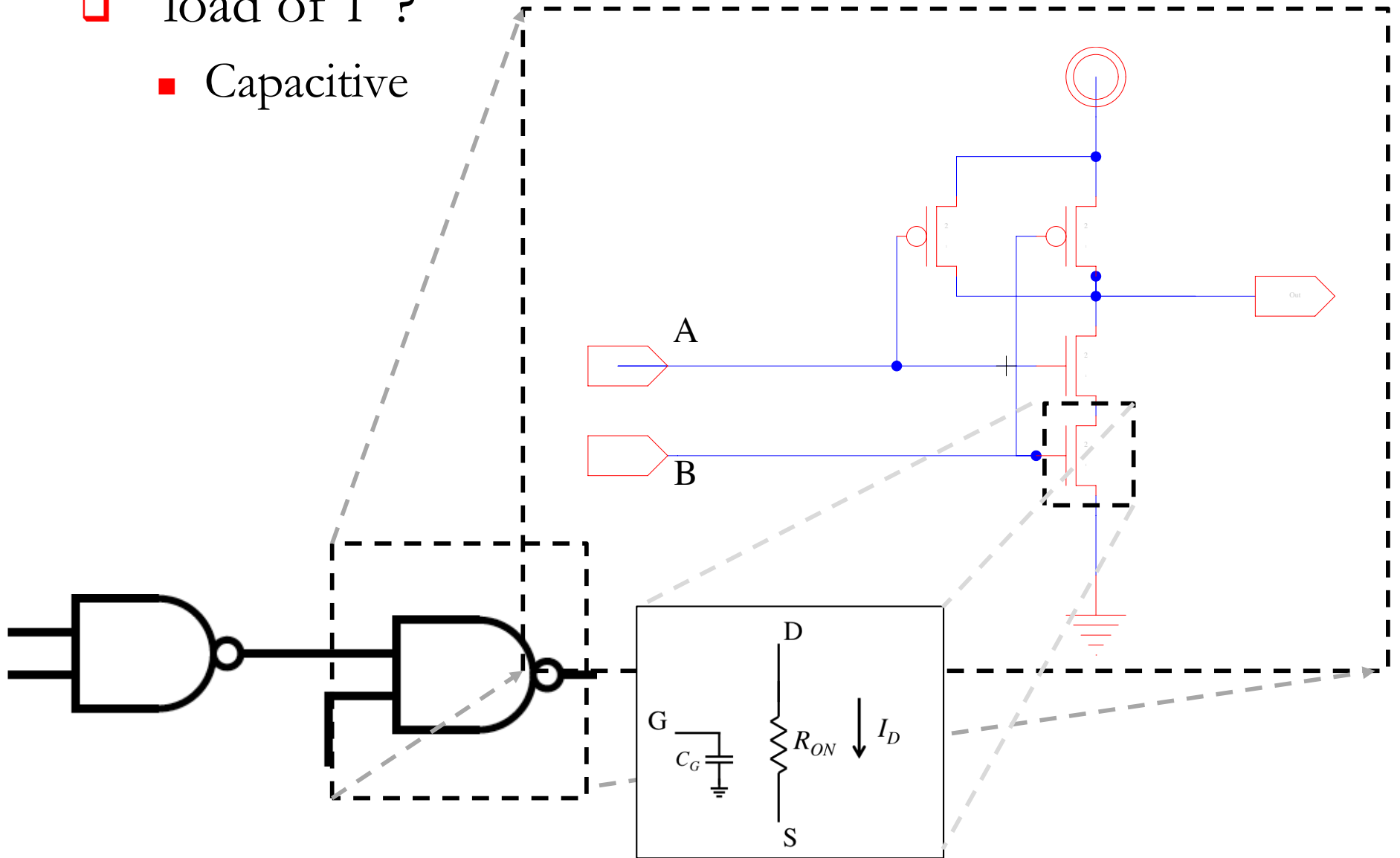
MOSFET Capacitance

- “load of 1”?
 - Capacitive



MOSFET Capacitance

- “load of 1”?
- Capacitive



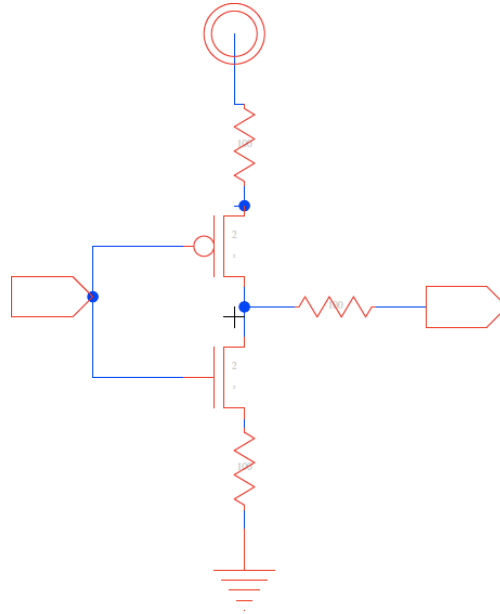


Lumped Capacitive Load

$$C_{load} = \sum_{i \in fanout} C_{G_i} + \sum_{i \in wires} C_{w_i}$$

What is R?

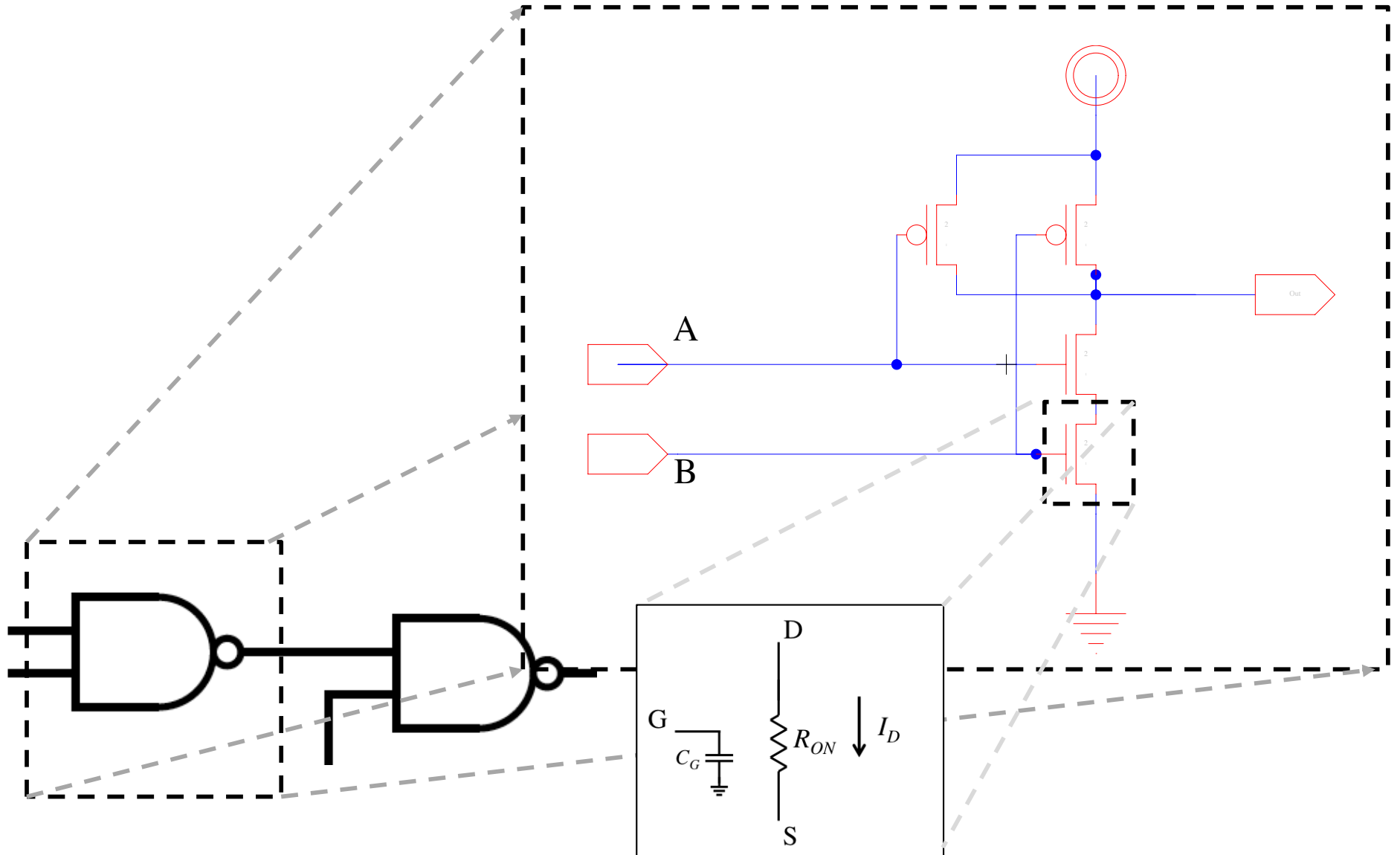
Resistance



- ❑ Wire resistance
 - From supply (V_{DD} or Gnd) to transistor source
 - From transistor output to gate it is driving
- ❑ Transistor equivalent resistance (R_{on})



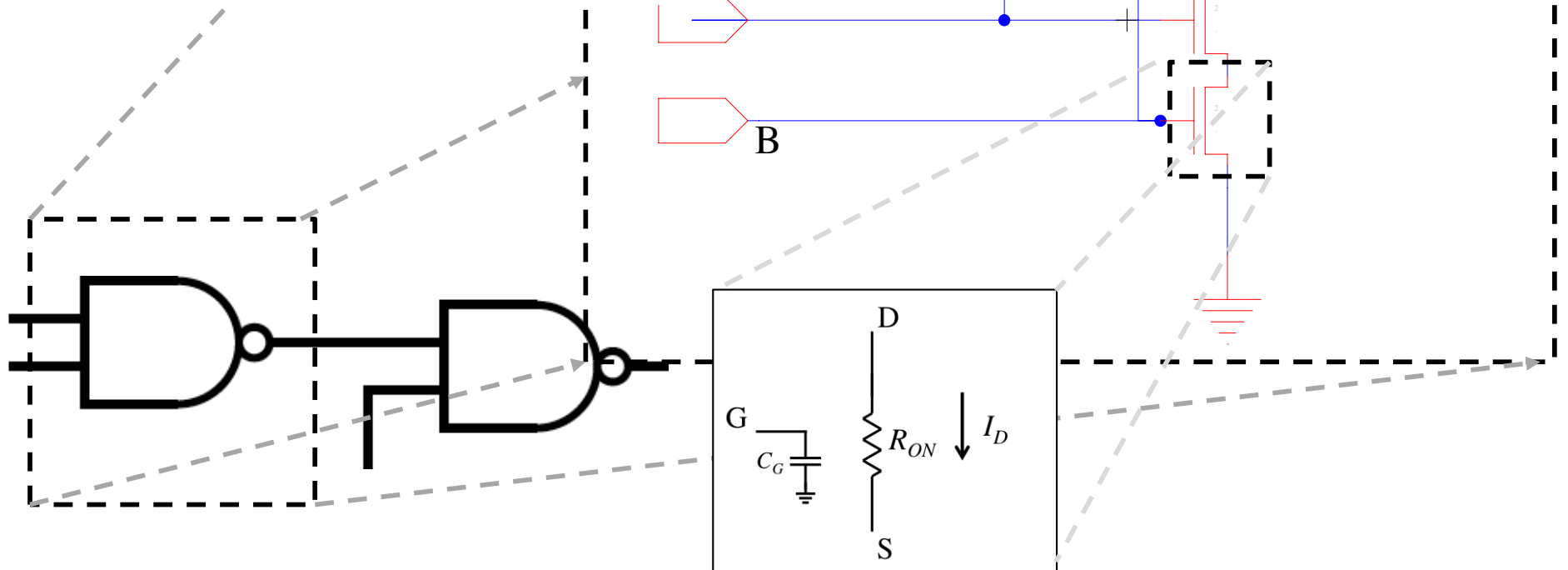
Equivalent Resistance



Equivalent Resistance (prelcass 4)

□ What resistances might transistors contribute?

- How many cases?
- Assume $R_{on} = R_{on,p} = R_{on,n}$

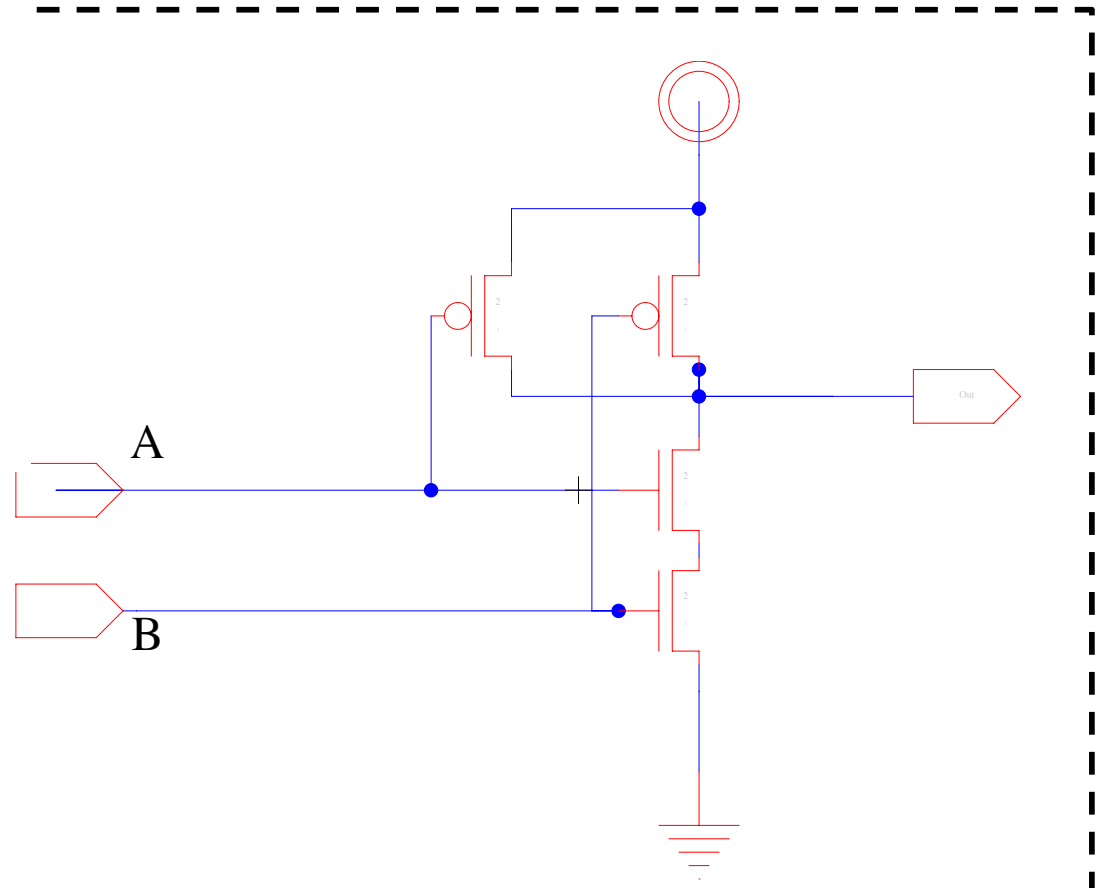


Equivalent Resistance (prelcass 4)

□ What resistances might transistors contribute?

- How many cases?
- Assume $R_{on} = R_{on,p} = R_{on,n}$

Input	Rout
00	
01	
10	
11	

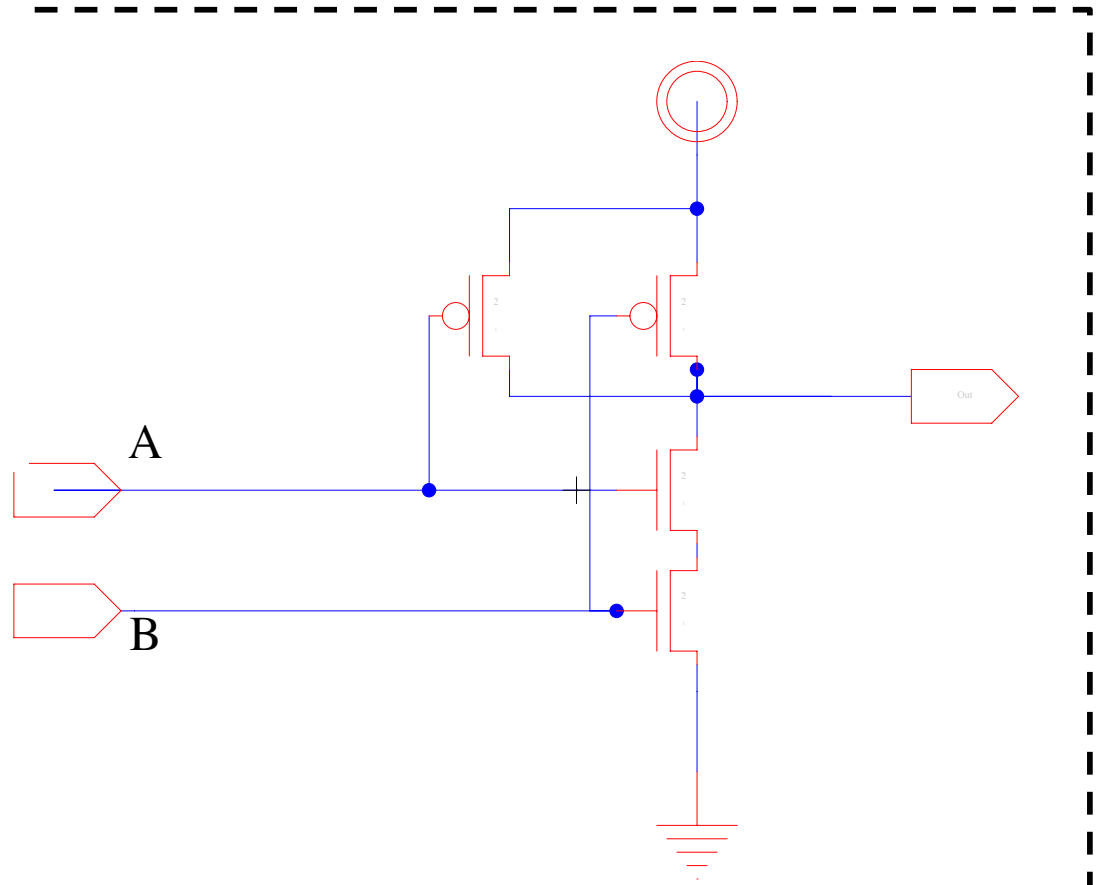


Rise/Fall Times

□ Rise and Fall time may differ

- Why?
- What is worst case?
- What is best case?

Input	Rout
00	$R_{on}/2$
01	R_{on}
10	R_{on}
11	$2R_{on}$





Lumped Resistive Source

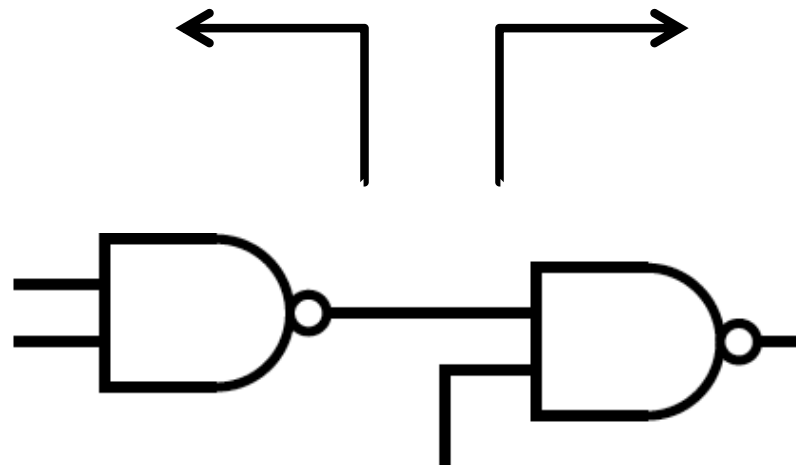
$$R_{drive} = R_{tr,net} + \sum_{i \in wires} R_{w_i}$$

$R_{tr,net}$ = transistor network resistance = parallel and series combination of R_{tr}

Voltage Waveform at Output/Input Node

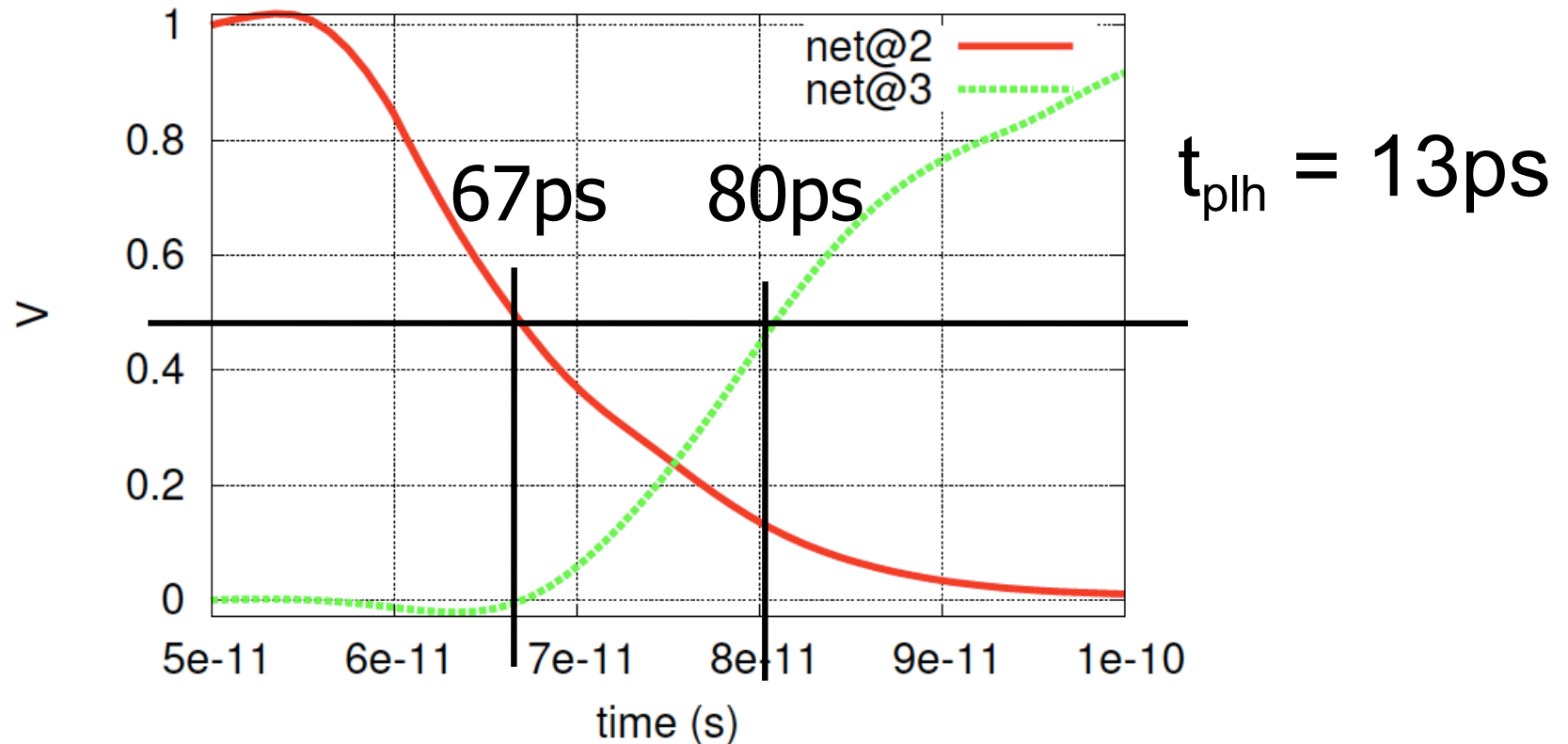
R_{drive} from
output stages
and wires

C_{Load} from
input stages
and wires



Measuring Delay

Measuring Gate Propagation Delay



- ❑ Next stage starts to switch before first finishes
- ❑ Measure from 50% of input swing to 50% of output swing



Characterizing Gate/Technology

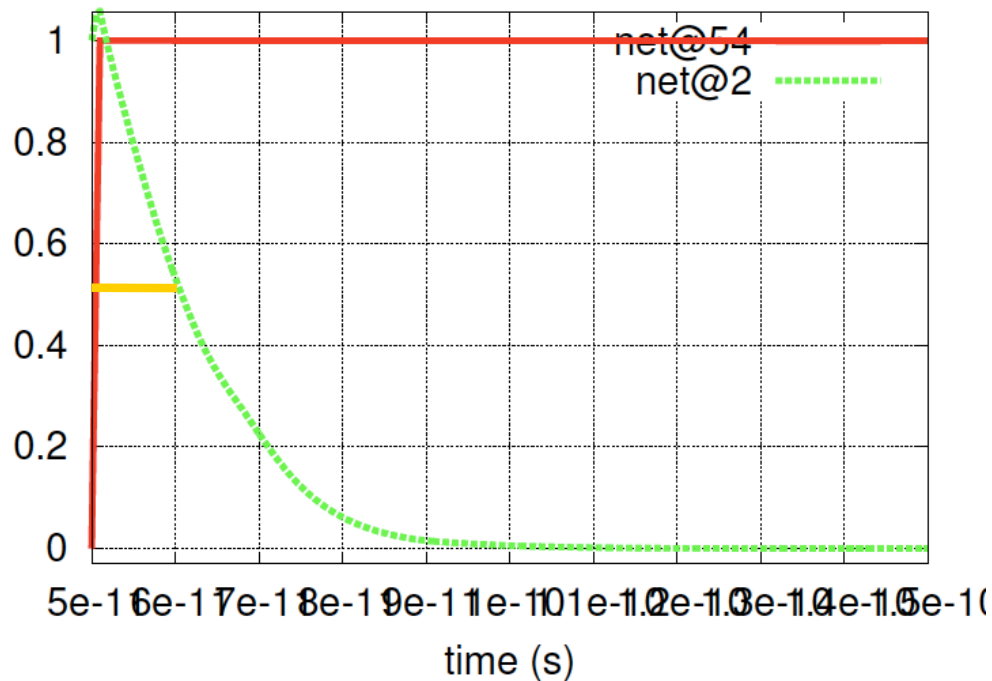
- Delay measure of a logic gate will be
 - Function of load on logic gate
 - Function of input signal rise time
 - Which, in turn, may be a function of input loading from the driving logic gate



Delay vs. Risetime

1ps input rise

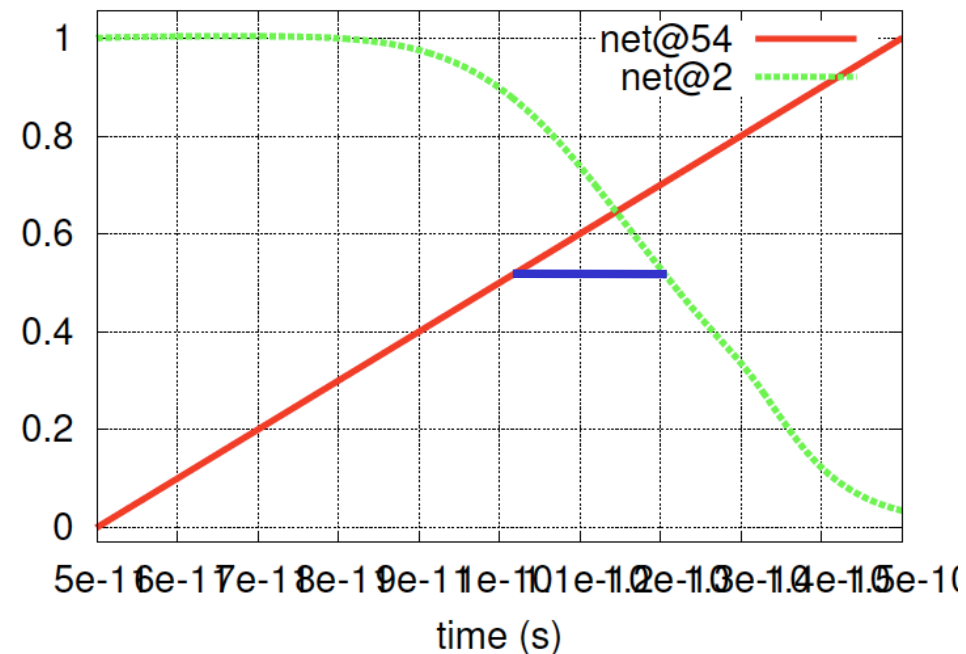
fast rise



10ps delay

100ps input rise

slow rise



20ps delay

- If we didn't know the input rise time, we wouldn't know what a 13ps delay meant

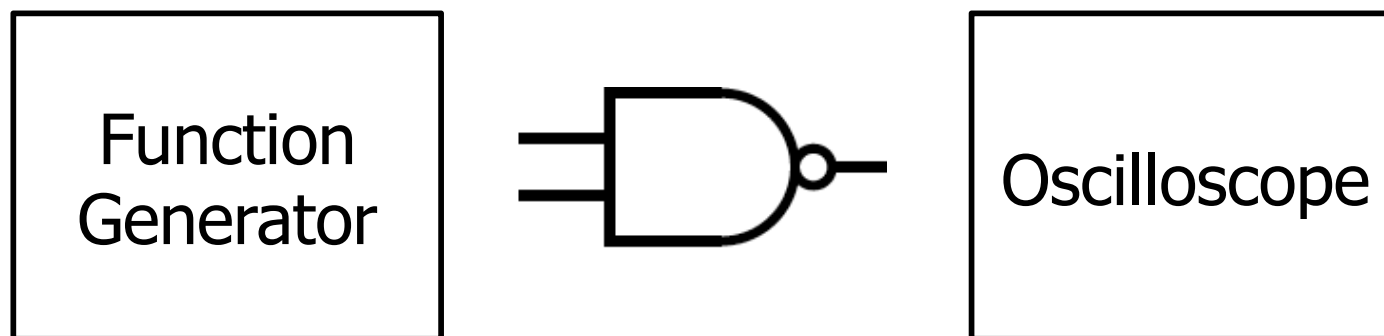


Characterizing Gate/Technology

- Delay measure will be
 - Function of load on gate
 - Function of input signal rise time
 - Which, in turn, may be a function of input loading
- Want to understand typical delay times
 - Allows us to compare designs with a (somewhat) normalized delay metric

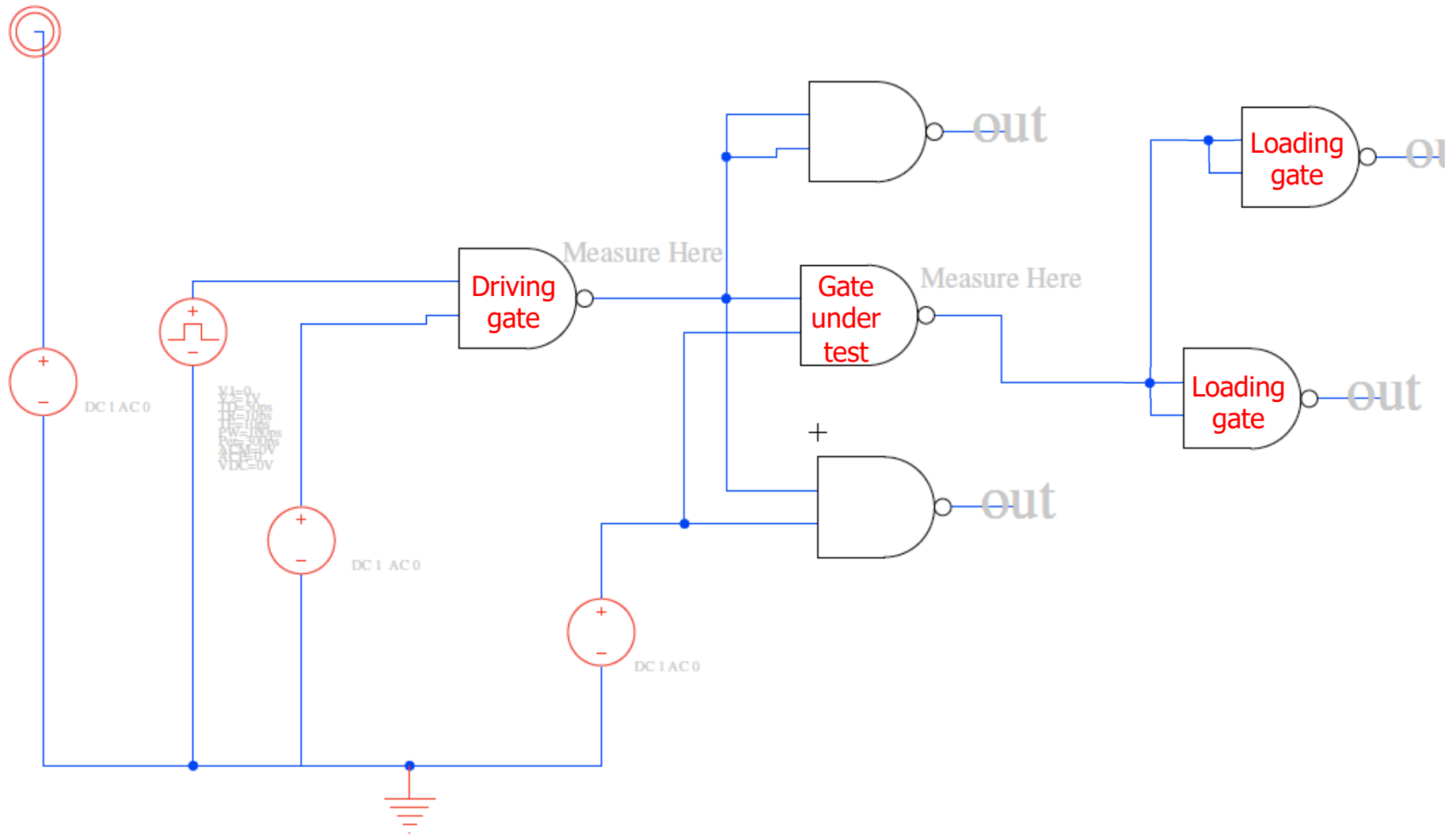
Standard Measurement for Characterization

- ❑ Drive with a gate
 - **Not** an ideal source
 - Input rise time typically would see in circuit
- ❑ Measure loaded gate
 - Typical loading – FO4



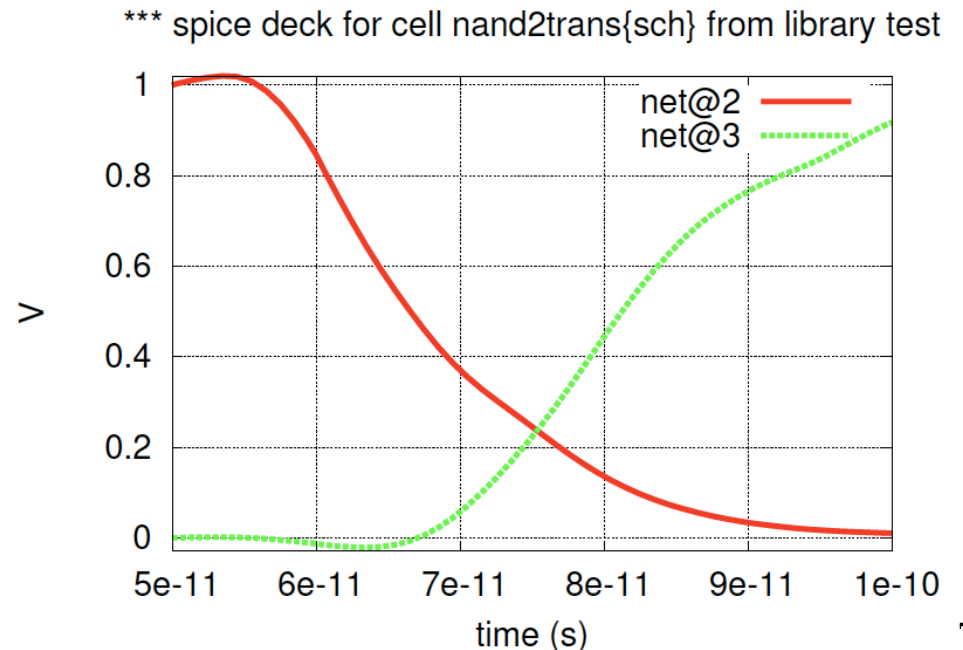
Not realistic measurement

HW2 Measurement Setup



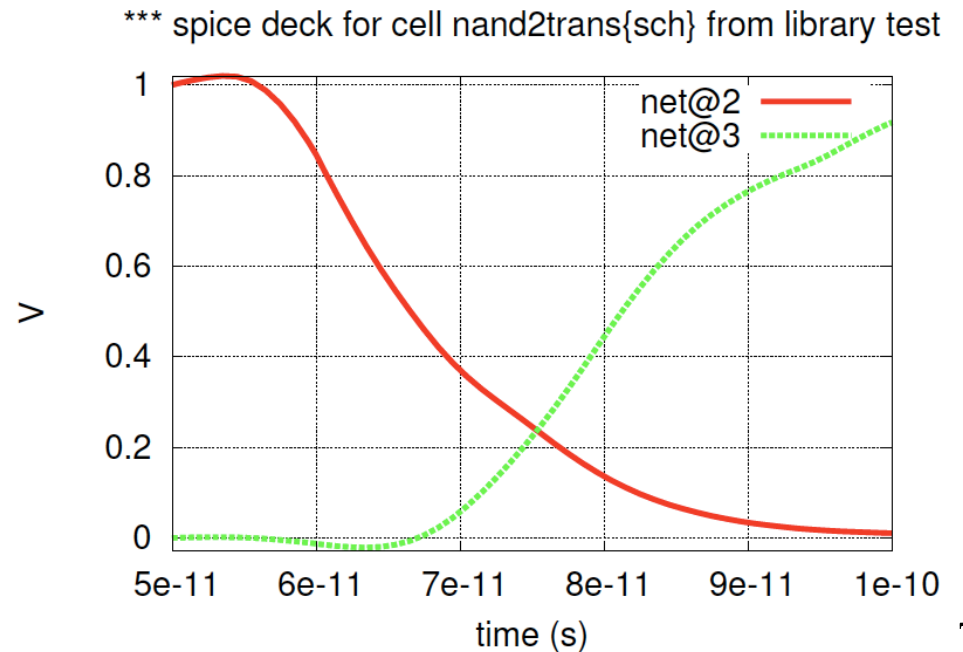
Measurement for Characterization

- Drive with a gate
 - **Not** an ideal source (how does delay change if drive is ideal?)
 - Input rise time typically would see in circuit
- Measure loaded gate
 - Typical loading – FO4



Measurement for Characterization

- Drive with a gate
 - **Not** an ideal source
 - Input rise time typically would see in circuit
- Measure loaded gate
 - Typical loading – FO4 (how does delay change if gate is unloaded?)





Big Ideas

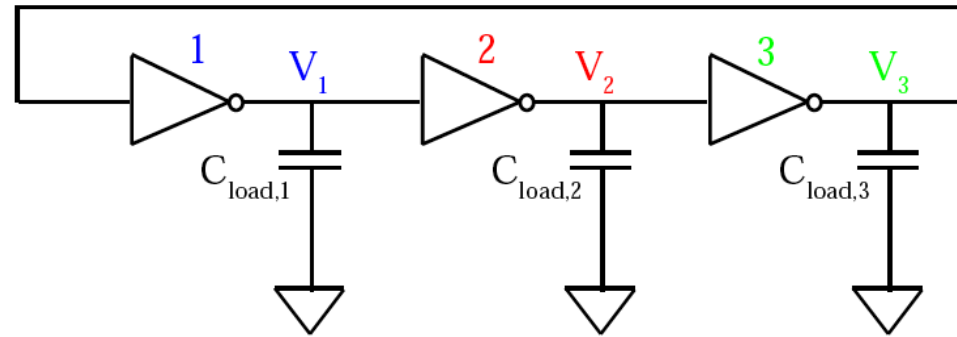
- ❑ MOSFET Transistor as switch
 - With limited drive
- ❑ Purpose-driven simplified modeling
 - Aid reasoning, sanity check, simplify design
- ❑ Analysis methodology
 - Zero order to understand switch state (logic)
 - First-order to get equivalent RC circuit (delay)



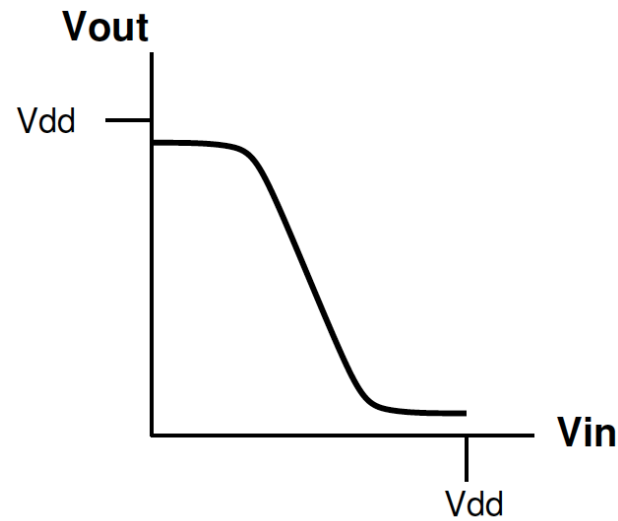
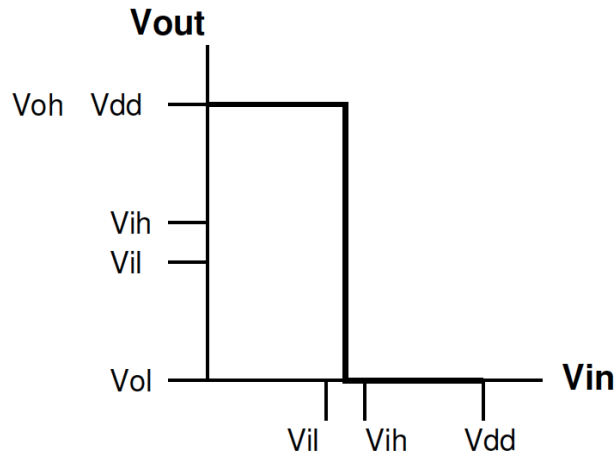
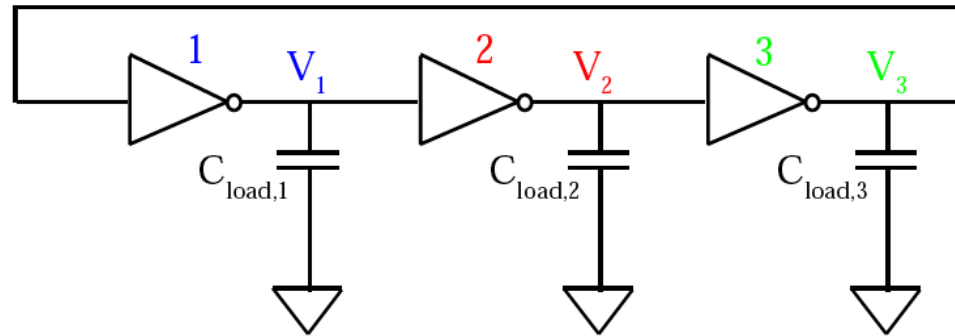
Admin

- ❑ HW 1 due 1/27 (Friday)
 - Leave enough time to submit on Canvas
 - If it records as after midnight will use up a late day
- ❑ HW2 out 1/27 (Friday) – due 2/3
- ❑ Setup Spice Work Flow
 - access to electric, setup for spice, run ngspice
 - See tool guides on website
 - <https://www.seas.upenn.edu/~ese3700/#tools>
 - read spice style guide on webpage:
 - https://www.seas.upenn.edu/~ese3700/spring2023/handouts/spice_style_guide.pdf

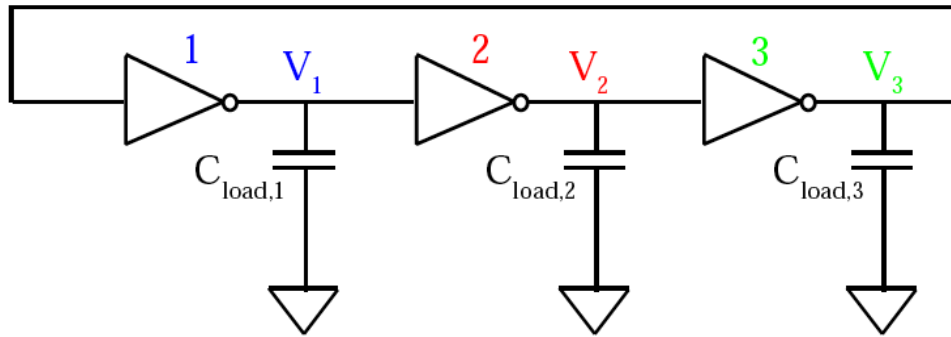
Ring Oscillator (Optional)



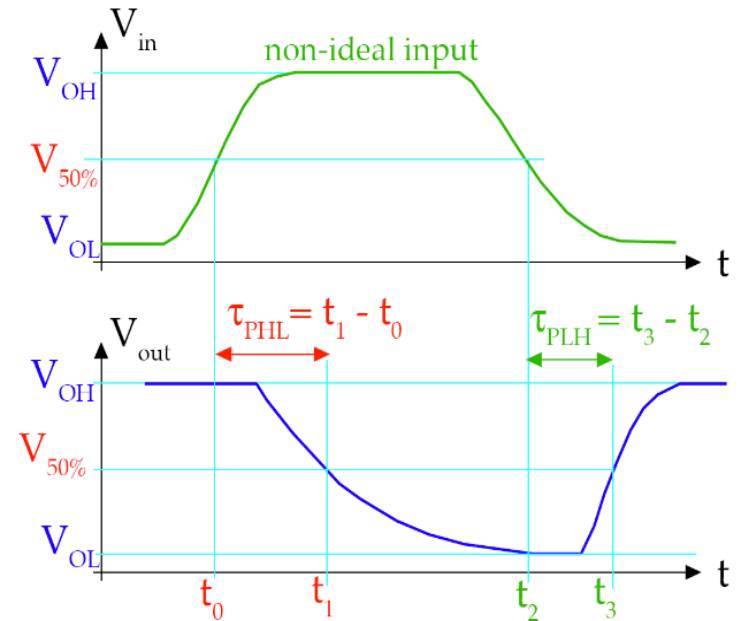
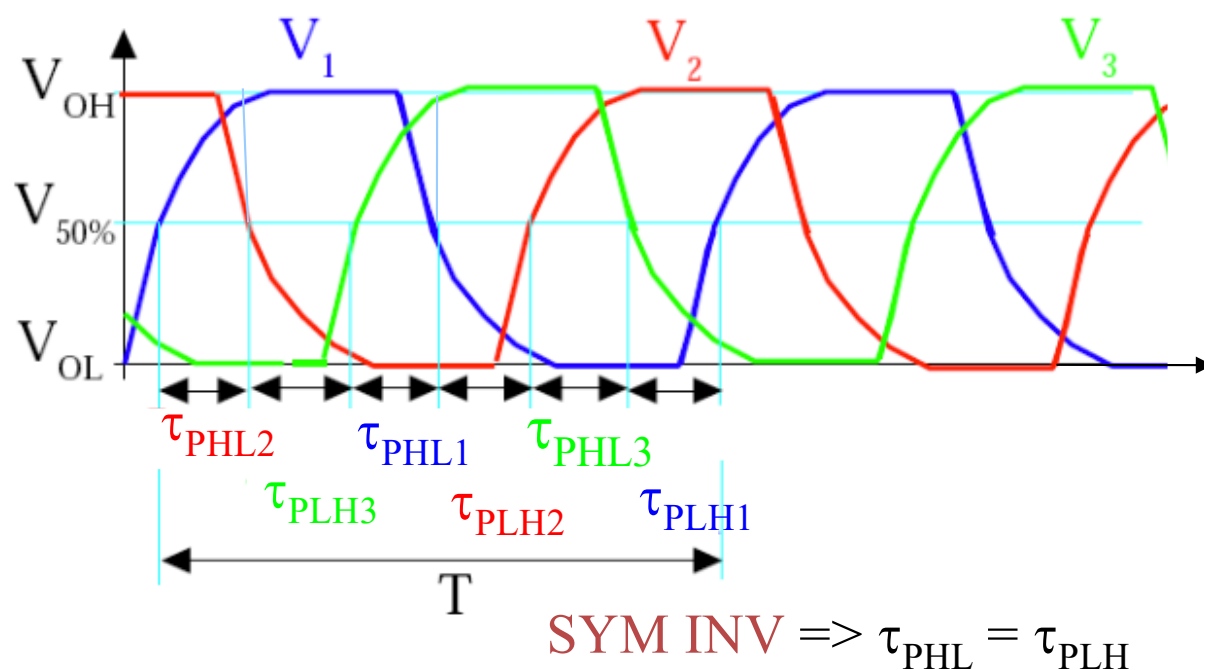
Ring Oscillator (Optional)



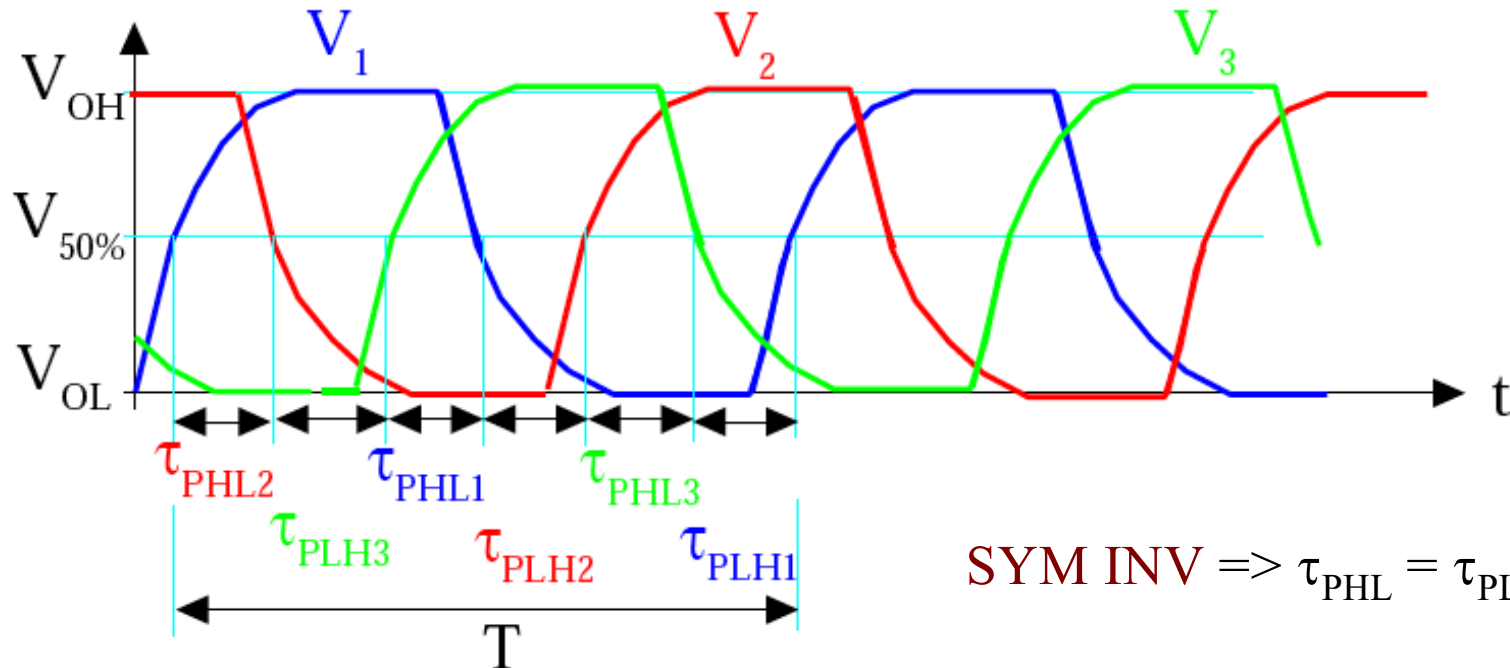
Ring Oscillator (Optional)



$C_{load,1} = C_{load,2} = C_{load,3}$ and **INV1** = **INV2** = **INV3** = **SYM INV**



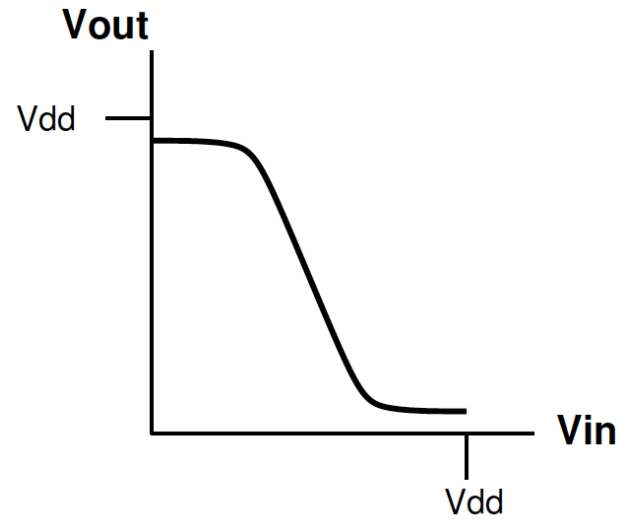
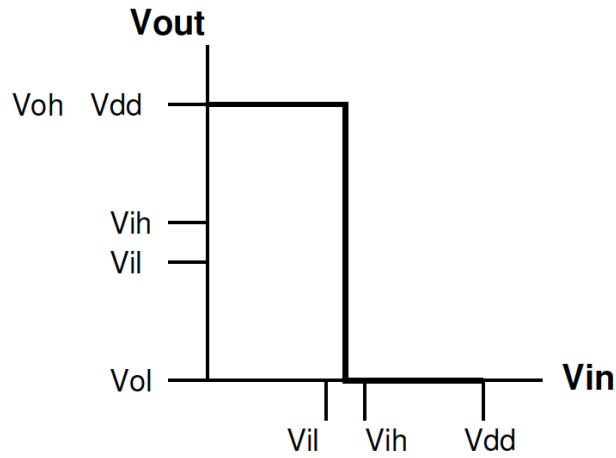
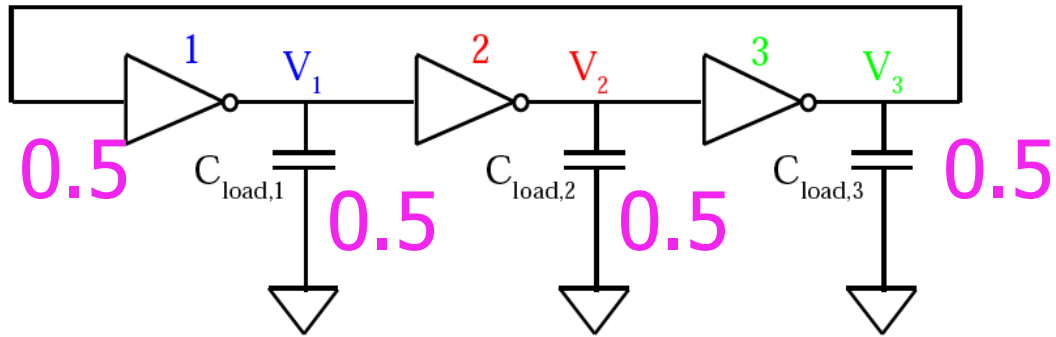
Ring Oscillator (Optional)



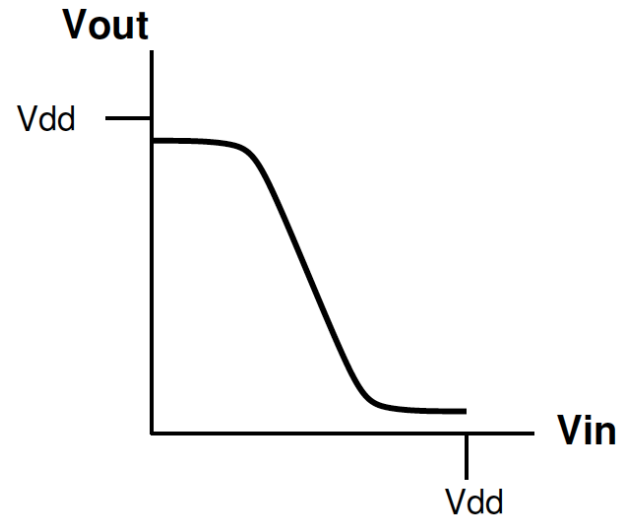
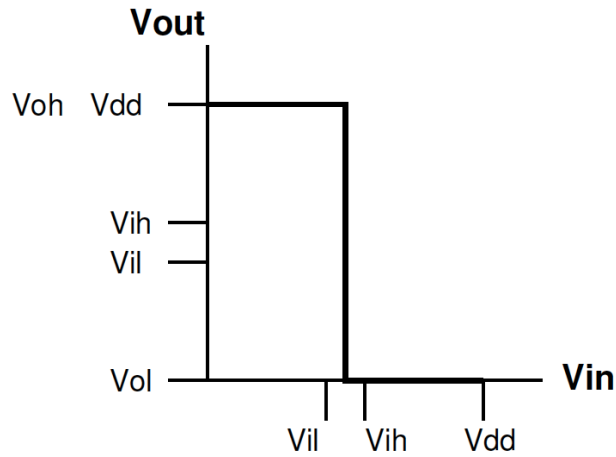
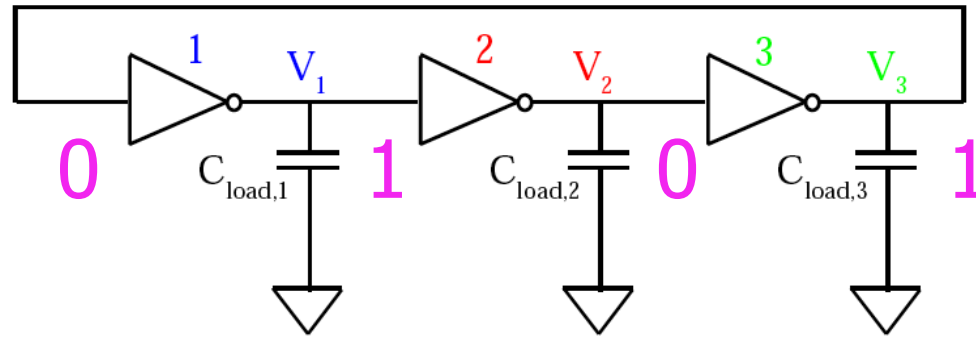
$$T = \tau_{PHL2} + \tau_{PLH3} + \tau_{PHL1} + \tau_{PLH2} + \tau_{PHL3} + \tau_{PLH1} = 6\tau_p$$

$$f = \frac{1}{T} = \frac{1}{6\tau_p} = \frac{1}{2n\tau_p} \rightarrow \tau_p = \frac{1}{2nf}$$

Ring Oscillator (Optional)



Ring Oscillator (Optional)





Acknowledgement

- ❑ Prof. André DeHon (University of Pennsylvania)
- ❑ Prof. Tania Khanna (University of Pennsylvania)