ESE370: Circuit-Level Modeling, Design, and Optimization for Digital Systems

Lec 3: January 25, 2023

Transistor First Order Model, Delay, and RC Response

Penn

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Today

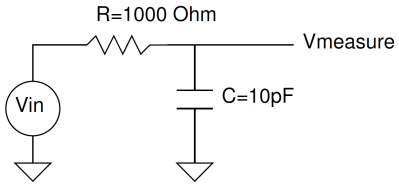
- Transistor First-Order Model
- RC Charging
  - RC Step Response Curve
- What is the C?
  - Capacitive load on logic gate output node
- What is the R?
  - Equivalent output resistance on the current path driving the output node
- Approximating and Measuring Delay
  - Tau estimate!

2

Final Voltage? (Preclass 1)

Assume V_{in} is 0 for $t < 0$ and steps to 1V at $t = 0$.

What value does $V_{measure}$ take on as $t \to \infty$?



3

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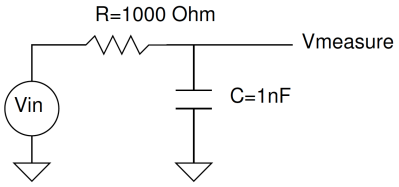
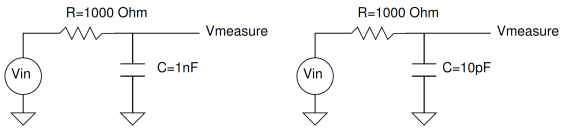


4

Final Voltage?

- Bonus question: Which one will settle faster?



A B

5

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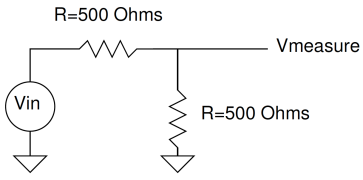

6

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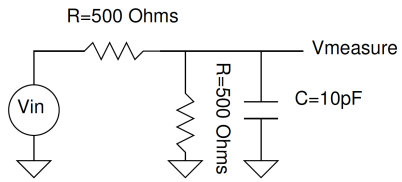

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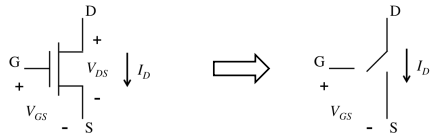
Conclude?

- DC/Steady-State
  - Ignore the capacitors
  - Look like "open circuit"

8

MOSFET – Zeroeth Order Model



- Ideal Switch
  - $V_{GS} > V_{th}$ → switch is closed, conducts
  - $V_{GS} < V_{th}$ → switch is open, does not conduct
- Gate draws no current from input
  - Loads input capacitively (gate capacitance)

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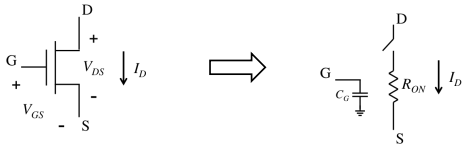
First Order Model



- Switch
  - Loads gate input capacitively
    - C_g
  - Has finite drive strength
    - R_{on}

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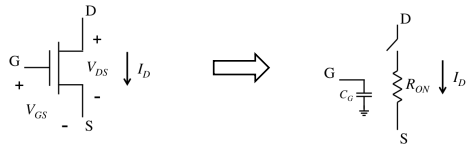
First Order Model



- Switch
  - Loads gate input capacitively
    - C_g
  - Has finite drive strength
    - R_{on}

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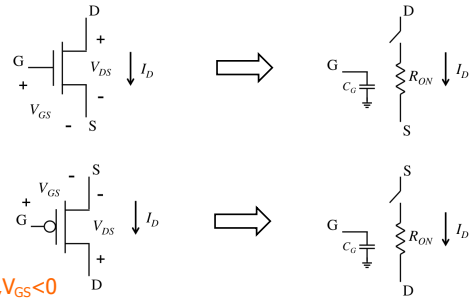
First Order Model - PMOS



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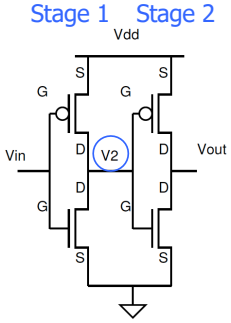
CMOS Buffer Gate



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Reminder: Zero-Order Model?

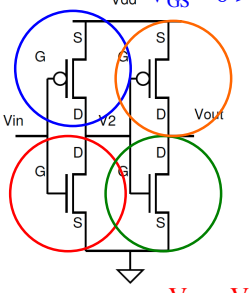
What happens when $V_{in} = V_{dd} > V_{thn}$?

$V_{th,p} = -V_{th,n}$

$V_{GS} = V_G - V_S$

Vdd $V_{GS} = 0 > V_{th,p}$

$V_{GS} = -V_{dd} < V_{th,p}$



V_2=Gnd=0

$V_{out} = V_{dd}$

$V_{GS} = 0 < V_{th,n}$

$V_{GS} = V_G - V_S = V_{dd} > V_{th,n}$

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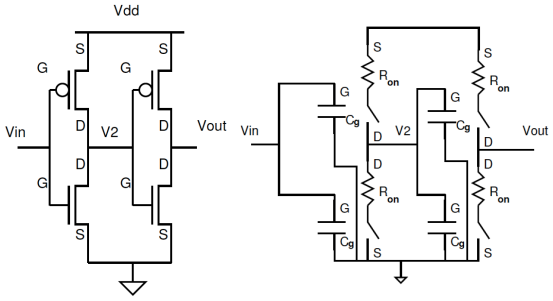
CMOS Buffer Gate - First Order



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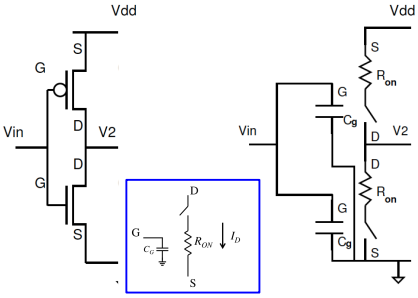
CMOS Buffer Gate - First Order



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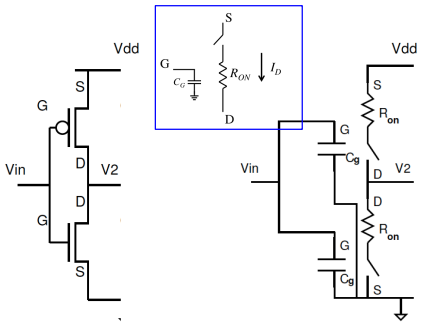
CMOS Buffer Gate - First Order



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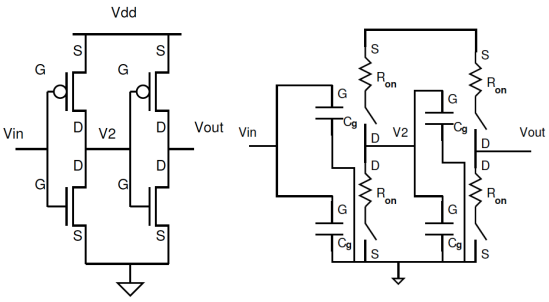
CMOS Buffer Gate - First Order



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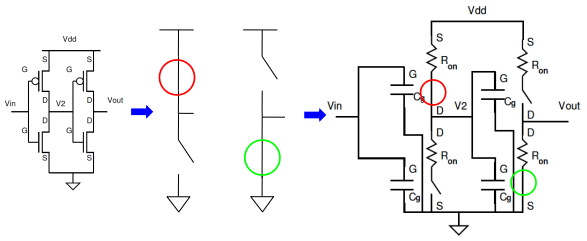
Zero-Order Model to Set Switches



- What is V_{IN} for this switch pattern?

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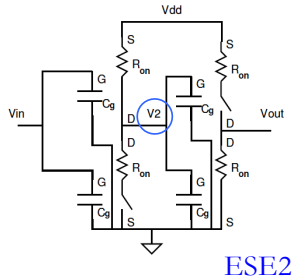
CMOS Buffer Gate - First Order



ESE215 problem

- Leaves an RC Circuit we can analyze

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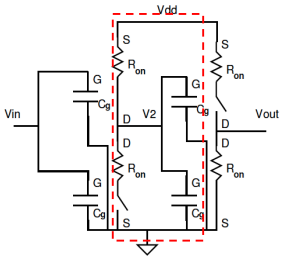
CMOS Buffer Gate - First Order



- Look at intermediary node V_2
  - Connected to output of stage 1 and input of stage 2

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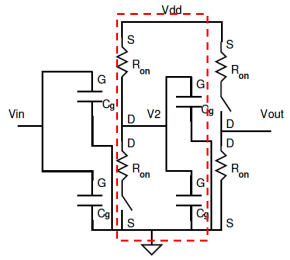
CMOS Buffer Gate - First Order



- What is equivalent circuit for the gate output of stage 1 driving V_2? What is load on the output of stage 1?

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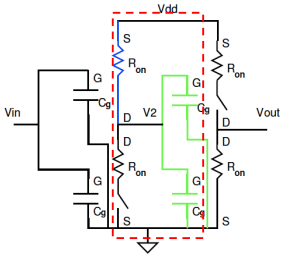
CMOS Buffer Gate - First Order



- Stage 1 equivalent circuit for the gate output
- Load on V_2
  - Capacitive, input of stage 2

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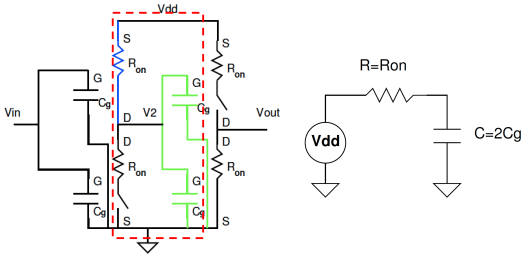
CMOS Buffer Gate - First Order



- Stage 1 equivalent circuit for the gate output
- Load on V_2
  - Capacitive, input of stage 2

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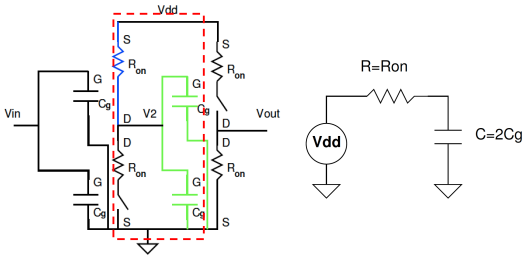
CMOS Buffer Gate - First Order



- What is time constant of V_2 when V_{in} switches from V_{DD} to 0?

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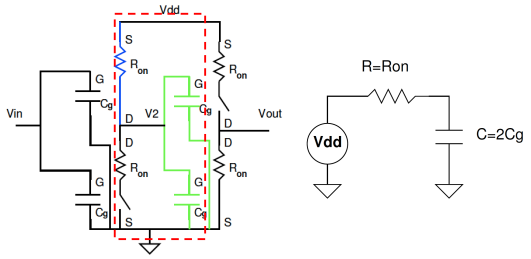
CMOS Buffer Gate - First Order



- What is time constant of V_2 when V_{in} switches from V_{DD} to 0?
  - $\tau = 2R_{on}C_g$

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First-Order Model

- Includes settling times/delay
- Voltage settling with capacitive loads
  - At least some basis for reasoning about delay

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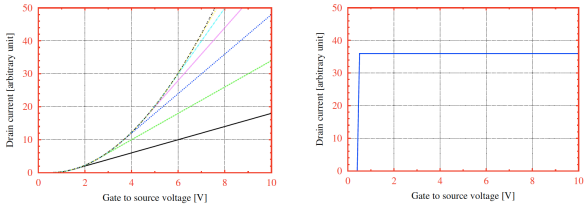
What is still missing?

IV curve

1st Order



28

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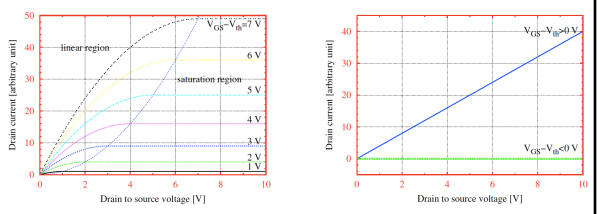
IV curve

1st Order



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What is still missing?

- What happens at intermediate voltages?
  - When the input is not rail-to-rail (not just gnd or V_{dd} inputs)
- Details of dynamics, including…
  - Input transition is not an ideal step
  - Intermediate drive strengths change with V_{GS}
    - Drain resistance changes
- Sub-threshold operation
  - When $V_{gs}<V_{th}$

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Design: Engineering Control

- V_{th}
  - Process engineer
- Drive strength (R_{on})
  - Circuit engineer
  - Control with sizing transistors
- Supply voltages (V_{dd})
  - Range set by process engineer
  - Detail use by circuit engineer

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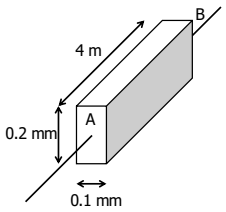
Wire Resistance



$$R = \frac{\rho L}{A}$$

- Sanity check
  - Wire twice as long = resistors in series
  - Wire twice as wide = resistors in parallel

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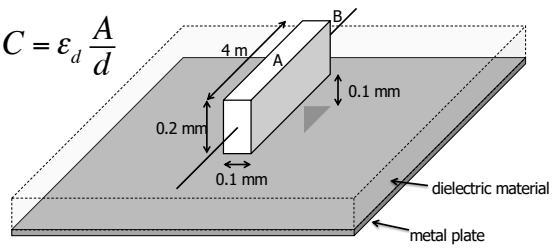
Wire Capacitance

$$C = \varepsilon_d \frac{A}{d}$$



- Sanity check
  - Wire twice as long = capacitors in parallel
  - Wire twice as wide = capacitors in parallel

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There are always Rs and Cs

- Every wire (connection) has resistance
- Every wire has capacitance
- (Every wire has inductance)
  - More later
- Dominant effects
  - $R_{big} + R_{small} \approx R_{big}$ ($R_{wire} << R_{on}$)?
  - $C_{big} \,||\, C_{small} \approx C_{big}$ ($C_{wire} << C_g$) ?
    - Today more likely ($C_{wire} >> C_g$)

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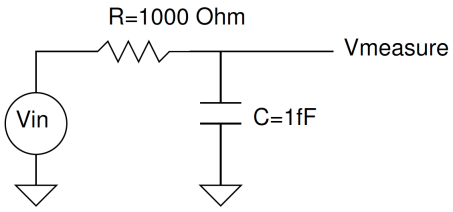
90% Rise Time? (preclass 2a)



What is final $V_{measure}$?
What is time constant, τ?

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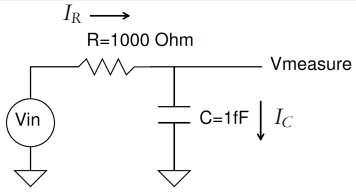
Governing Equations? (KCL)



- KCL @ $V_{measure}$
  - Kirchoff's Current Law
    - Sum of all currents into a node = 0
    - Current entering a node = current exiting a node
  - $I_R = I_C$

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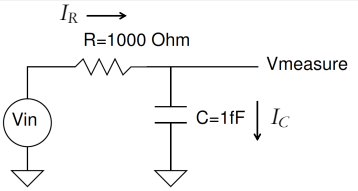
Governing Equations? (KCL)



$$I_R = I_C$$

$$\frac{V_R}{R} = C\frac{dV_C}{dt}$$

$$\frac{V_{in} - V_{measure}}{R} = C\frac{dV_{measure}}{dt}$$

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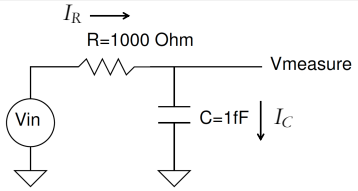
Governing Equations? (KCL)



$$I_R = I_C$$

$$\frac{V_R}{R} = C\frac{dV_C}{dt}$$

$$\frac{V_{in} - V_{measure}}{R} = C\frac{dV_{measure}}{dt}$$

$$0 = \frac{dV_{measure}}{dt} + \frac{1}{RC}V_{measure} - \frac{V_{in}}{RC}$$

$$V_{measure} = V_{in}\left(1 - \left(e^{-t/RC}\right)\right)$$

$$\tau = RC$$

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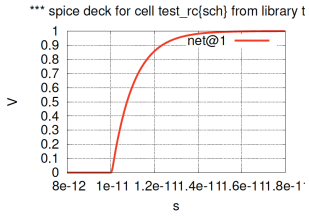
What does look like?



$$V_{measure} = V_{in}\left(1 - \left(e^{-t/RC}\right)\right)$$

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Shape of Curve (preclass 1b)

t (in ps)	$e^{-t/RC}$	$1-e^{-t/RC}$
0		
0.1		
1		
2		
2.3		

V_{in}=1

$$V_{measure} = V_{in}\left(1 - \left(e^{-t/RC}\right)\right)$$

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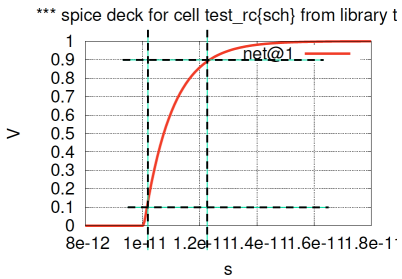
Rise Time: 10—90%



t_{rise} ~= 2.2ps ~= 2.2τ

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Shape of Curve (preclass 2c)

t (in ps)	$e^{-t/RC}$	$1-e^{-t/RC}$	
0	1	0	
0.1	0.9	0.1	10%
1	1/e = 0.37	0.66	
2	$1/e^2$ = 0.14	0.86	
2.3	0.1	0.9	90%

V_{in}=1

$$V_{measure} = V_{in}\left(1 - \left(e^{-t/RC}\right)\right)$$

At what time is $V_{measure}$ 50% of its value?

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Shape of Curve (preclass 2c)

t (in ps)	$e^{-t/RC}$	$1-e^{-t/RC}$	
0	1	0	
0.1	0.9	0.1	10%
0.69	0.5	0.5	50%
1	1/e = 0.37	0.66	
2	$1/e^2 = 0.14$	0.86	90%
2.3	0.1	0.9	

$V_{in}=1$

$$V_{measure} = V_{in}\left(1-\left(e^{-t/RC}\right)\right)$$

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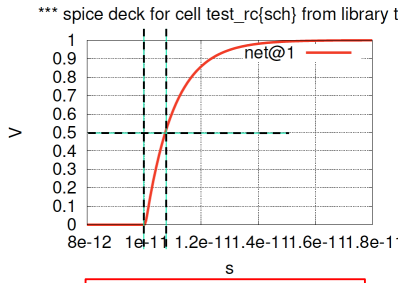
Delay Time: 50% (in)—50% (out)



t_{PLH} ~= .69ps ~= .69τ

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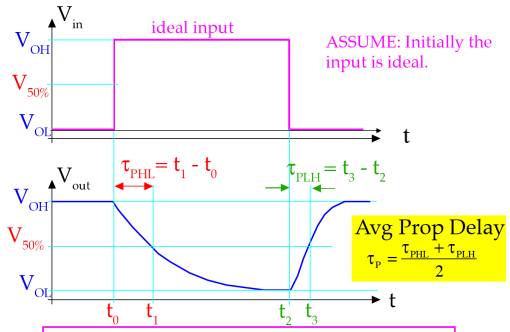
Propagation Delay Definitions



$V_{50\%} = V_{OL} + 0.5\,[V_{OH} - V_{OL}] = 0.5\,[V_{OL} + V_{OH}]$

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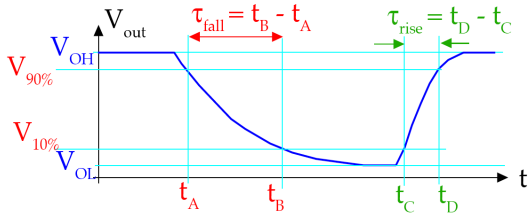
Rise/Fall Times



$V_{10\%} = V_{OL} + 0.1\,[V_{OH} - V_{OL}]$

$V_{90\%} = V_{OL} + 0.9\,[V_{OH} - V_{OL}]$

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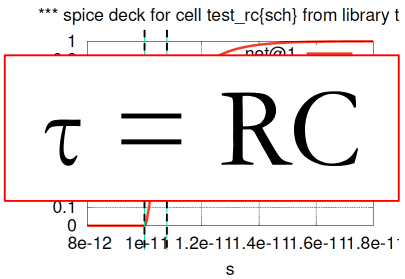
Delay Time: 50% (in)—50% (out)



$\tau = RC$

t_{PLH} ~= .69ps ~= .69τ

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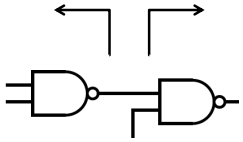
Voltage Waveform at Output/Input Node

R_{drive} from looking into output stages

C_{load} from looking into input stages



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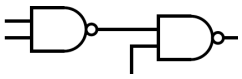
Voltage Waveform at Output/Input Node

R_{drive} from looking into output stages and wires

C_{load} from looking into input stages and wires



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What is C?

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Capacitance

- Wire
- Fanout -- Total gate load
  - Logical Gate
    - MOSFET gate

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Fanout

- Number of things to which a gate output connects

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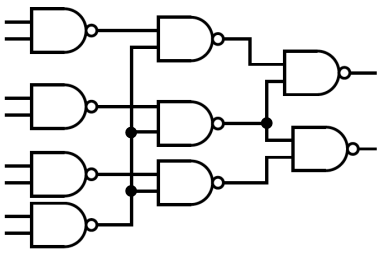
Fanout in Circuit

- Output routed to many gate inputs



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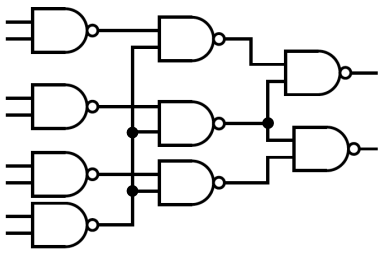
Fanout in Circuit (preclass 3)

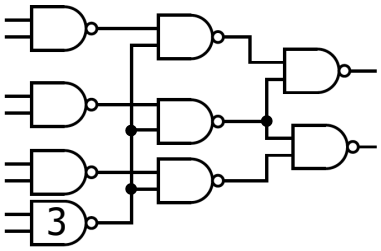
- Maximum fanout?
- Second?
- Min?



54

Fanout in Circuit

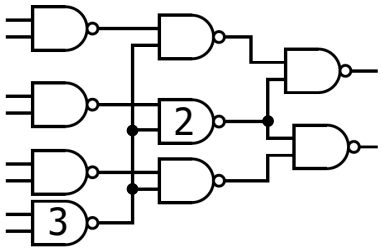
- Maximum fanout?
- Second?
- Min?



55

Fanout in Circuit

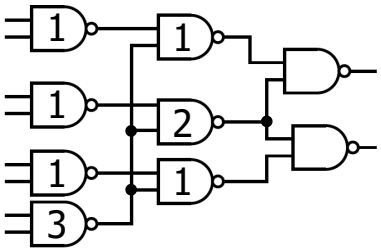
- Maximum fanout?
- Second?
- Min?



56

Fanout in Circuit

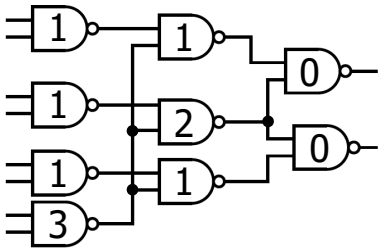
- Maximum fanout?
- Second?
- Min?



57

Fanout in Circuit

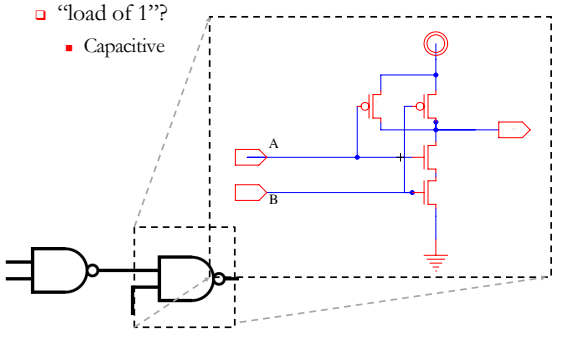
- Maximum fanout?
- Second?
- Min?



58

MOSFET Capacitance

- "load of 1"?
  - Capacitive



59

MOSFET Capacitance

- "load of 1"?
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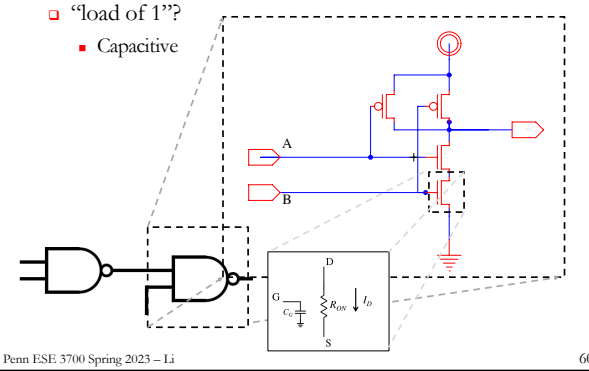

60

Lumped Capacitive Load

$$C_{load} = \sum_{i \in fanout} C_{G_i} + \sum_{i \in wires} C_{w_i}$$

61

What is R?

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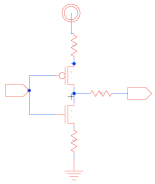
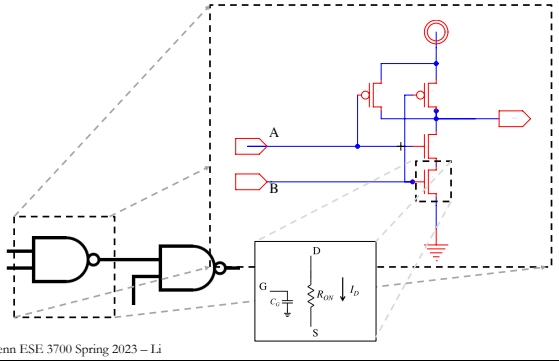
Resistance



- Wire resistance
  - From supply (Vdd or Gnd) to transistor source
  - From transistor output to gate it is driving
- Transistor equivalent resistance (R_{on})

63

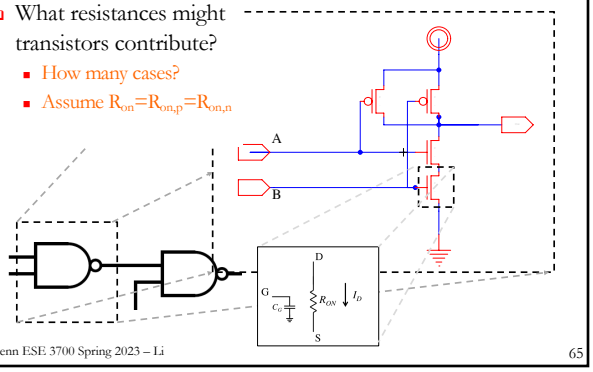
Equivalent Resistance



64

Equivalent Resistance (prelcass 4)

- What resistances might transistors contribute?
  - How many cases?
  - Assume $R_{on}=R_{on,p}=R_{on,n}$



65

Equivalent Resistance (prelcass 4)

- What resistances might transistors contribute?
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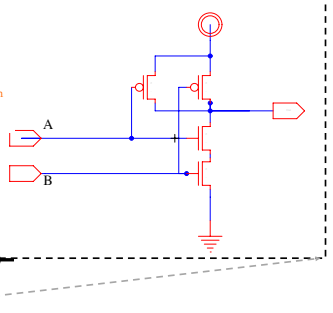
  - Assume $R_{on}=R_{on,p}=R_{on,n}$



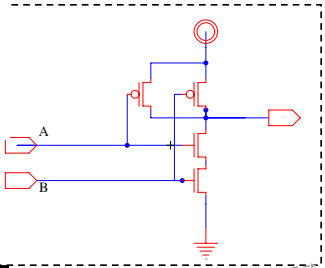
Input	Rout
00	
01	
10	
11	

66

Rise/Fall Times

- Rise and Fall time may differ
  - Why?
  - What is worst case?
  - What is best case?

Input	Rout
00	$R_{on}/2$
01	R_{on}
10	R_{on}
11	$2R_{on}$



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Lumped Resistive Source

$$R_{drive} = R_{tr,net} + \sum_{i \in wires} R_{w_i}$$

$R_{tr,net}$ = transistor network resistance = parallel and series combination of R_{tr}

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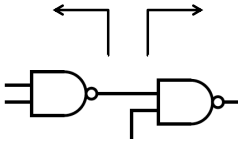
Voltage Waveform at Output/Input Node

R_{drive} from output stages and wires

C_{Load} from input stages and wires



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Measuring Delay

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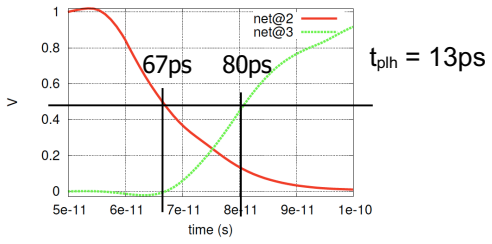
Measuring Gate Propagation Delay



- Next stage starts to switch before first finishes
- Measure from 50% of input swing to 50% of output swing

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Characterizing Gate/Technology

- Delay measure of a logic gate will be
  - Function of load on logic gate
  - Function of input signal rise time
    - Which, in turn, may be a function of input loading from the driving logic gate

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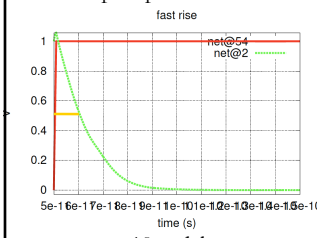
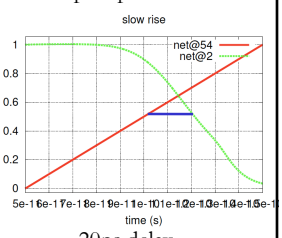
Delay vs. Risetime

1ps input rise



10ps delay

100ps input rise



20ps delay

- If we didn't know the input rise time, we wouldn't know what a 13ps delay meant

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Characterizing Gate/Technology

- Delay measure will be
  - Function of load on gate
  - Function of input signal rise time
    - Which, in turn, may be a function of input loading
- Want to understand typical delay times
  - Allows us to compare designs with a (somewhat) normalized delay metric

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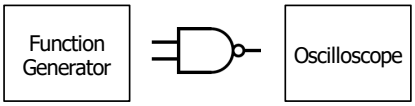
Standard Measurement for Characterization

- Drive with a gate
  - **Not** an ideal source
  - Input rise time typically would see in circuit
- Measure loaded gate
  - Typical loading – FO4



Not realistic measurement

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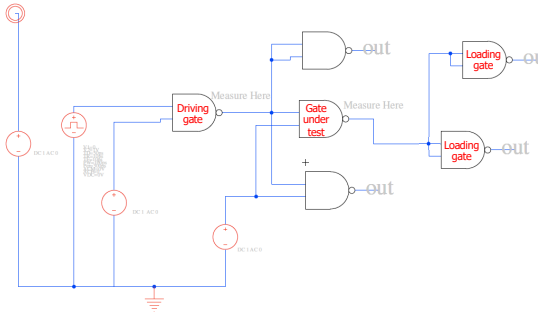
HW2 Measurement Setup



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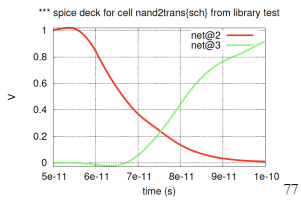
Measurement for Characterization

- Drive with a gate
  - **Not** an ideal source (how does delay change if drive is ideal?)
  - Input rise time typically would see in circuit
- Measure loaded gate
  - Typical loading – FO4



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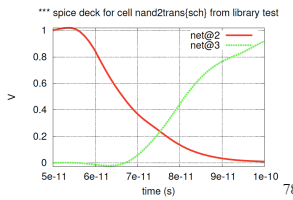
Measurement for Characterization

- Drive with a gate
  - **Not** an ideal source
  - Input rise time typically would see in circuit
- Measure loaded gate
  - Typical loading – FO4 (how does delay change if gate is unloaded?)



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Big Ideas

- MOSFET Transistor as switch
  - With limited drive
- Purpose-driven simplified modeling
  - Aid reasoning, sanity check, simplify design
- Analysis methodology
  - Zero order to understand switch state (logic)
  - First-order to get equivalent RC circuit (delay)

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Admin

- HW 1 due 1/27 (Friday)
  - Leave enough time to submit on Canvas
    - If it records as after midnight will use up a late day
- HW2 out 1/27 (Friday) – due 2/3
- Setup Spice Work Flow
  - access to electric, setup for spice, run ngspice
    - See tool guides on website
    - https://www.seas.upenn.edu/~ese3700/#tools
  - read spice style guide on webpage:
    - https://www.seas.upenn.edu/~ese3700/spring2023/handouts/spice_style_guide.pdf

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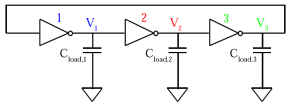
Ring Oscillator (Optional)



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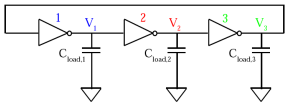
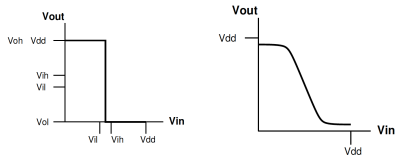
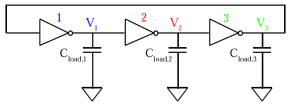
Ring Oscillator (Optional)



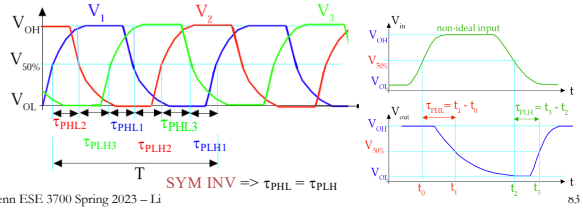


82

Ring Oscillator (Optional)

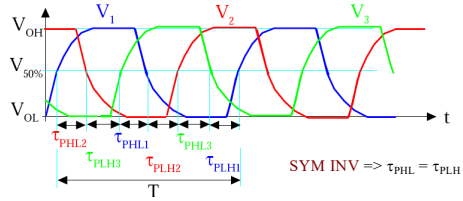


$C_{load,1} = C_{load,2} = C_{load,3}$ and INV1 = INV2 = INV3 = SYM INV



83

Ring Oscillator (Optional)



SYM INV => $\tau_{PHL} = \tau_{PLH} = \tau_P$

$T = \tau_{PHL2} + \tau_{PLH3} + \tau_{PHL1} + \tau_{PLH2} + \tau_{PHL3} + \tau_{PLH1} = 6\tau_P$

$$f = \frac{1}{T} = \frac{1}{6\tau_p} = \frac{1}{2n\tau_p} \rightarrow \tau_p = \frac{1}{2nf}$$

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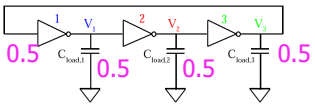
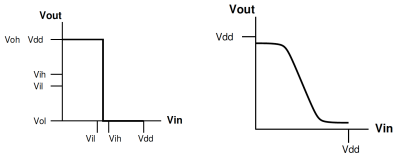
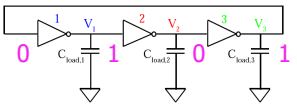
Ring Oscillator (Optional)

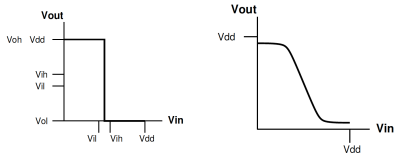




85

Ring Oscillator (Optional)





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Acknowledgement

- Prof. André DeHon (University of Pennsylvania)
- Prof. Tania Khanna (University of Pennsylvania)

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