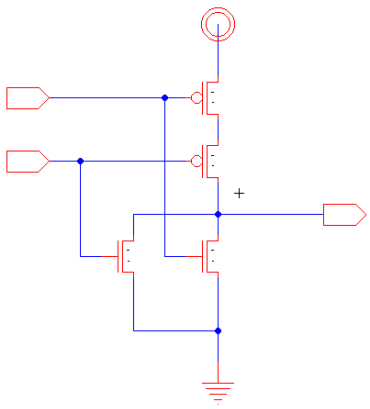
University of Pennsylvania
Department of Electrical and System Engineering
Circuit-Level Modeling, Design, and Optimization for Digital Systems

ESE3700, Spring 2024 HW1: Zeroth-order Model and Electric Monday, Jan. 22

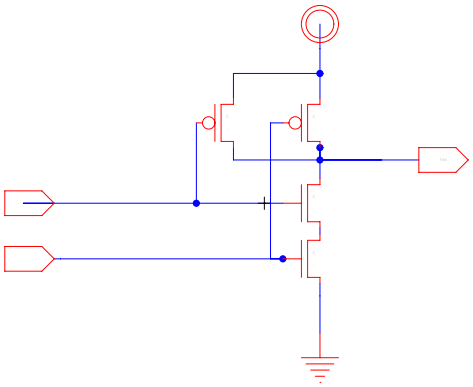
Due: Friday, February 2, 11:59PM

- **Problems:**

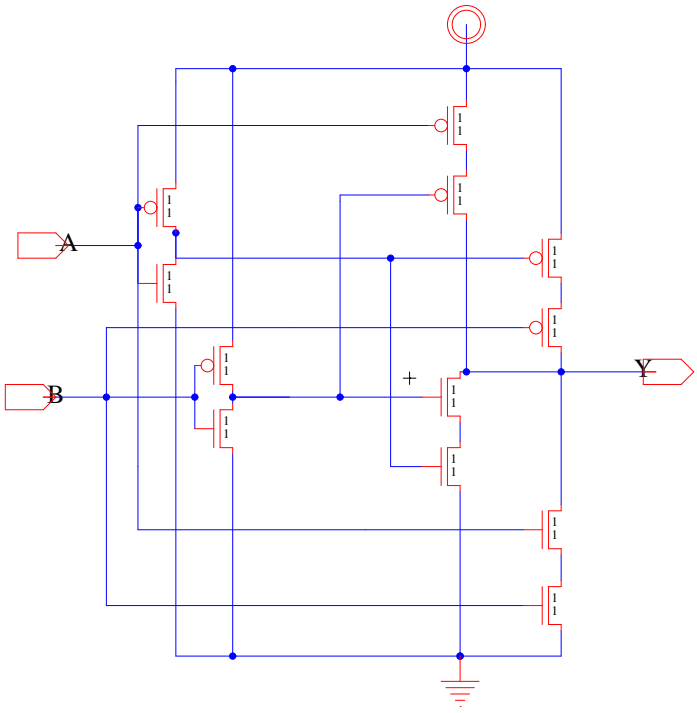
  1. Using zeroth-order transistor model reasoning, identify the function of the following transistor-level gates. Give their Boolean logic equation.
  (Show truth table of input cases for partial credit.)



(a)



(b)



(c)

2. Use electric to build the gate in 1(a) and create a schematic icon for the gate. There is information about the software at the end of this homework handout. Give all transistors a width of 2 and length of 1 (W=2 , L=1). Plan to take a couple of hours to read the tutorials and get familiar with electric. Submit an electric print out or screen shot of your gate and icon.

3. Simplify the following Boolean expressions or truth table into a minimum sum of products using Karnaugh maps.

   (a) $\overline{A} \cdot \overline{B} \cdot \overline{C} + A \cdot \overline{B} \cdot \overline{C} + \overline{A} \cdot B \cdot \overline{C} + A \cdot B \cdot \overline{C}$

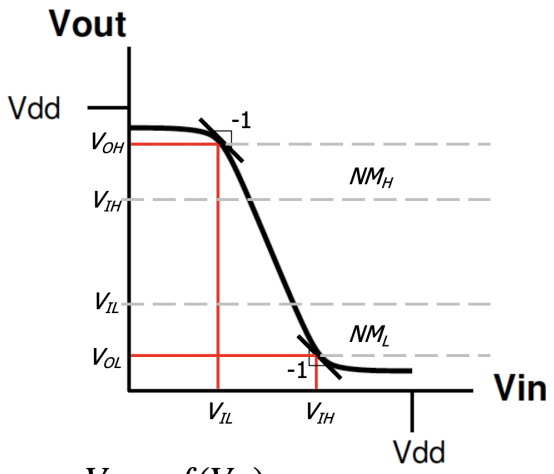
   (b) $\overline{A}{\cdot}\overline{B}{\cdot}\overline{C}{\cdot}\overline{D}{+}\overline{A}{\cdot}B{\cdot}\overline{C}{\cdot}D{+}\overline{A}{\cdot}B{\cdot}\overline{C}{\cdot}\overline{D}{+}A{\cdot}\overline{B}{\cdot}\overline{C}{\cdot}\overline{D}{+}\overline{A}{\cdot}\overline{B}{\cdot}C{\cdot}\overline{D}{+}A{\cdot}\overline{B}{\cdot}C{\cdot}\overline{D}{+}\overline{A}{\cdot}\overline{B}{\cdot}\overline{C}{\cdot}D$

   (c)

A	B	C	D	OUT
0	0	0	0	1
0	0	0	1	0
0	0	1	0	1
0	0	1	1	1
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	1
1	0	0	0	1
1	0	0	1	0
1	0	1	0	1
1	0	1	1	1
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	1

4. Design the following complementary gates from transistors using the zeroth-order switch model for the transistor. Try to minimize the number of transistors in each design. Draw in Electric.
   (a) NOR3
   (b) $\overline{A} \cdot \overline{B} + \overline{C}$
5. Lab 1 measurement (Part 1): from the data you collected in Lab 1, characterize the performance of your nand2 gate
   (a) Plot the Input and Output waveforms of the second nand2 gate when the input is driven with a square wave. Measure the propagation delay of the second nand2 gate at the 50% point (when the input crosses 50% to when the output crosses 50%). Also measure rise time at the output of the first nand2 (input to the second) from 10% to 90%.
   (b) Plot the voltage transfer characterstic (VTC), $V_{out} = f(V_{in})$, when the input is driven with a slow moving ramp waveform. Your axes should be V_{in} vs. V_{out} and should not include time.
   (c) Use the definition of noise margins below to identify workable noise margins for your measured gate from the gate-from- transistor lab. That is, identify V_{OL}, V_{IL}, V_{OH}, V_{IH}, $NM_L = V_{IL} - V_{OL}$, and $NM_H = V_{OH} - V_{IH}$.

   Definition of noise margins from VTC are captured in the image below. We will discuss this in greater detail in a future lecture.



$V_{OH} = f(V_{IL})$

$V_{OL} = f(V_{IH})$

Electric CAD Tool

We will be using the Electric VLSI Design System for schematic entry.

`http://www.staticfreesoft.com/`.

You can access this on the CETS computers by running:

electric

You can also download the java applet (.jar) and run it on your laptop (recommended):

`http://www.staticfreesoft.com/productsFree.html`

There is a complete online user's manual:

`http://www.staticfreesoft.com/documentsUser.html`

We will point you at specific parts of the manual to get started, but you may find it useful to read other parts as you get started or want to learn how to do more with the tool. There is also a tutorial on the course webpage, which is a good place to start:

`https://www.seas.upenn.edu/~ese3700/spring2024/handouts/elec_tutorial.pdf`

Initial instructions for running electric:

`http://www.staticfreesoft.com/jmanual/mchap01-03.html`

Create a Library

Start by creating a new library. Under the "File" menu, select "New Library". Perhas you want to name your library "ese370".

Drawing the Schematic for Your Gate

Read the tutorial on drawing a schematic gate:

`http://www.staticfreesoft.com/jmanual/mchap01-12-02.html`

Printing Your Schematic

This describes several methods.

`http://www.staticfreesoft.com/jmanual/mchap04-08.html`

We have had trouble with "Print" directly under the "File" menu, but "File→Export→PostScript" has worked fine.

Create an Icon for Your Gate

You need to do this now for your schematic gate. This will be useful for you for lab 2.

`http://www.staticfreesoft.com/jmanual/mchap01-11-07.html`

`http://www.staticfreesoft.com/jmanual/mchap01-12-04.html`

Save Library

Save your library before exiting. This is also under the "File" menu.