University of Pennsylvania
Department of Electrical and System Engineering
Circuit-Level Modeling, Design, and Optimization for Digital Systems

ESE3700, Spring 2024 HW3: Simple Circuit and MOS Models Fri. February 9

Due: Friday, February 16, 11:59PM

Unless otherwise noted, assume:

- 22nm PTM Spice models that you used on HW3: `/home1/e/ese3700/ptm/22nm_HP.pm`
- $V_{dd} = 0.8$V, $V_{thn} = 300$mV, $V_{thp} = -300$mV, $C_{OX} = 35\frac{fF}{\mu m^2}$, $L_{drawn} = 22nm$, $L_{eff} = 17nm$, $W = 44nm$, $n = 1.5$, $\nu_{SAT} = 10^5\frac{m}{s}$, λ =0, $\mu_n = 540\frac{cm^2}{V \cdot s}$, $\mu_p = 200\frac{cm^2}{V \cdot s}$, T=27C (300K)

Useful Ngspice commands (see spice style guide on course webpage for more) :

- dc (large-signal analysis), ac (transient/small-signal analysis), op (operating point analysis), plot, print, show (for non-linear devices)
- Tutorials: `http://ngspice.sourceforge.net/tutorials.html` ←The first link on this page is particularly helpful

For analytic device modeling, use the follow NMOS IV Model Equations

- Resistive:

$$I_D = \mu_n C_{OX} \left(\frac{W}{L}\right) \left(\left(V_{GS} - V_{th}\right) V_{DS} - \frac{\left(V_{DS}\right)^2}{2} \right) \tag{1}$$

- Saturated (Pinch Off):

$$I_D = \frac{1}{2} \mu_n C_{OX} \left(\frac{W}{L}\right) \left(V_{GS} - V_{th}\right)^2 \tag{2}$$

- Velocity Saturated:

$$I_D = \nu_{sat} C_{OX} W \left(V_{GS} - V_{th} - \frac{V_{DSAT}}{2} \right) \tag{3}$$

- Subthreshold:

$$I_D = I_S \left(\frac{W}{L}\right) e^{\frac{V_{GS} - V_{th}}{nkT/q}} \tag{4}$$

NOTE: The parameters are rough approximations and will not match SPICE perfectly.

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1. **TA Check-off**: To get ANY credit on this homework, you must demonstrate the following steps of your workflow to your TA:

   (a) Generate a SPICE deck from Electric
   (b) Run DC or transient simulation in ngspice
   (c) Plot simulation results (transfer function or waveforms) in ngspice

   You can go to TA office hours or submit a zoom video (must be less than 5 minutes, really should only be a couple of minutes) with your homework submission in Canvas. You have until the HW 3 due date to complete any demonstrations for credit. You will get a 1*HomeworkGrade if you complete the check off and if you don't you will get a 0 for the entire homework.

2. Include description of test and circuit schematics, ngspice simulation commands and results in homework turnin.

   (a) Using SPICE simulation results, what is the equivalent source-drain resistance R_{ds} for a $W = L = 1$ transistor with $V_{gs} = V_{ds} = V_{dd} = 0.8V$ (NMOS) or $V_{gs} = V_{ds} = -V_{dd} = -0.8V$ (PMOS)? Answer for both NMOS and PMOS transistors.

   (b) For the NMOS device, using equations calculate the equivalent source-drain resistance R_{ds} for a $W = L = 1$ transistor and compare to your SPICE results form part (a).

3. Part of the challenge of this question is designing and understanding your test circuit setup. Include your test and circuit schematics, ngspice simulation commands and results in homework turnin. All transistors should be minimum size ($W = L = 1$). From a SPICE simulation results, what is the RC time-constant for:

   (a) one transistor charging another transistor's gate input of the same size? **HINT:** One transistor charging another transistor doesn't mean your charging circuit only has 2 transistors.

   (b) one transistor *discharging* another transistor's gate input of the same size?

   (c) How do your answers to (a) and (b) relate?

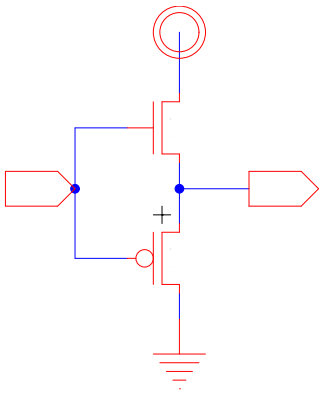
4. Using equations, estimate worst-case gate capacitance C_g for for an NMOS device with $W = L = 1$.

5. What is the RC time-constant for a transistor *discharging* another transistor's gate input?

   (a) Calculate the time constant based on R_{ds} from Problem 2(b) and C_g from Problem 4, and compare with your SPICE results from Problem 3.

   (b) What does this tell you about hand analysis vs SPICE simulations?

6. Consider the following circuit:

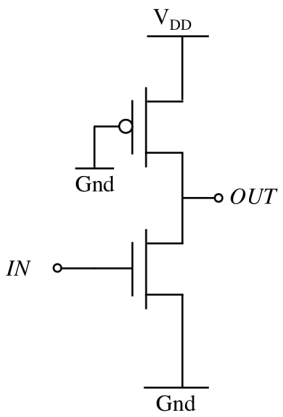


Assume: V_{dd}=0.8V, V_{thn}=250mV, V_{thp}=-250mV. Reason using your first-order transistor model.

(a) Is this a valid CMOS circuit? Explain why or why not?

(b) Run a transient spice simulation to verify your answer to part (a). Submit your test schematic and simulation results. Comment on the results.

7. Consider the circuit below, with an nMOS transistor loaded with a pMOS transistor with the gate tied to ground (Assume $V_{DD} = 0.8V$ and the transistors are biased such that $V_{SB} = 0$):



(a) For minimum sized devices, use spice to generate the VTC and identify V_{IL}, V_{IH}, V_{OL}, V_{OH}, NM_L, and NM_H.

(b) Resize the nMOS device with $W = 10$. Regenerate the VTC and identify V_{IL}, V_{IH}, V_{OL}, V_{OH}, NM_L, and NM_H.

(c) Compare the two VTCs from (a) and (b) and explain why the VTC shape changes between (a) and (b).