University of Pennsylvania
Department of Electrical and System Engineering
Circuit-Level Modeling, Design, and Optimization for Digital Systems

ESE3700, Spring 2024 HW5: Logic Delay and Energy Wednesday, February 28

Due: Wednesday, March 13, 11:59PM

Read the entire rest of the homework before you start. This problem requires a lot of SPICE work, and the more you plan your test schematics, the quicker you will be able to finish. Create a separate icon for each AND16 implementation (6 schematics 2 sizings for each design), and create a separate test schematic for each test you run. Then you can use the same test schematic to measure all implementations, by just instancing the different AND16 icons. "Save as..." is your friend.

1. Explore implementations of AND16 and compare delays. Assume the inputs are driven by minimum size inverters and output is loaded by $50C_0$.

   Consider 3 designs:

   - 16-input NAND gate followed by an inverter.
   - four 4-input NANDs feeding a 4-input NOR
   - four stages of alternating 2-input NANDs and 2-input NORs

   (a) Use the τ model to estimate the delay of each case assuming all transistors are W=L=1.

   (b) Use τ model to size the transistors in each circuit for minimum delay. Report your transistor sizings and the delay of each case. How much are you able to speedup each circuit by sizing?

   (c) Use SPICE to measure worst case delay for all 6 case circuits (minimum sized and your sized gates from 3b).

   - You can use the measure command to compute the propagation delay:

     ```
     meas tran delay trig v(vin) val=0.5 rise=1 targ v(vout) val=0.5 rise=1
     ```

     This will measure the amount of time between the voltage on net `vin` rising to 0.5V for the first time (`trig`) and the voltage on `vout` rising to 0.5V for the first time (`targ`). For more information on this command, see Sections 15.4.5 and 17.5.36 of the `ngspice` user's manual (`http://ngspice.sourceforge.net/docs/ngspice25-manual.pdf`).

2. Explore implementations of AND16 and compare energy consumption. Assume the inputs are driven by minimum size inverters and output is loaded by $50C_0$.

   Consider 3 designs:

   - 16-input NAND gate followed by an inverter.
   - four 4-input NANDs feeding a 4-input NOR
   - four stages of alternating 2-input NANDs and 2-input NORs

   (a) Assuming all transistors are W=L=1, estimate the switching energy for each case when the input switches from 16 0's to 16 1's and back to 16 0's. Express answer in terms of multiples of V_{dd} and C_0.

   (b) At the sizings determined for minimum delay, estimate the switching energy for each case when the input switches from 16 0's to 16 1's and back to 16 0's. How does this energy compare to minimum sized devices? What does this tell you about circuit optimization for delay and energy?

   (c) Assuming the output does change, identify a switching case that will consume the least energy.

   (d) Estimate the energy for the switching case identified above for all 6 sized circuit cases (3 circuits $\times$ 2 sizings). How does the picture differ looking at this case versus the worst-case switching in (b) and (d)?

   (e) Use SPICE to measure energy for all 6 case circuits (minimum sized and your sized gates from 3b). Note that text Section 5.5.4 discusses energy measurements with SPICE.

   - In `ngspice`, you can compute an integral using the measure (`meas`) command. For example, to compute the integral of the current through the source `vv_generi@0` from 100ps to 200ps, use the following:

     ```
     meas tran yint integ I(vv_generi@0) from=100ps to=200ps
     ```

3. Complete the following table with the SPICE results of Problem 1 and Problem 2:

Circuit	Sizing	Delay	E 0's→1's→0's	E case4c
NAND16-INV	min.			
	sized			
NAND4-NOR4	min.			
	sized			
(NAND2-NOR2)^2	min.			
	sized			

4. **Extra Credit:** Compare τ-model and SPICE results and discuss similarities and differences. We want to be able to use simple calculations like the τ model to size our circuits. Do they correlate well?

5. **Extra Credit:** For the fastest circuit and sizing, use SPICE to explore and fine tune transistor sizes. Can you reduce delay by fine tuning? How much? How does this difference compare to the delay difference between circuits and sizings in the τ model? Can you conclude if the τ model will mostly lead you in the right direction or if it will mislead you?