

University of Pennsylvania
Department of Electrical and System Engineering
Circuit-Level Modeling, Design, and Optimization for Digital Systems

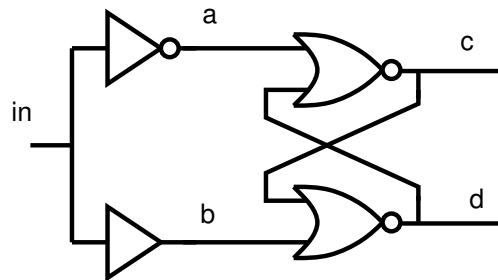
ESE3700, Spring 2024

HW6: Clocking and Registers

Wednesday, Apr 3

Due: Wednesday, April 10, 11:59PM

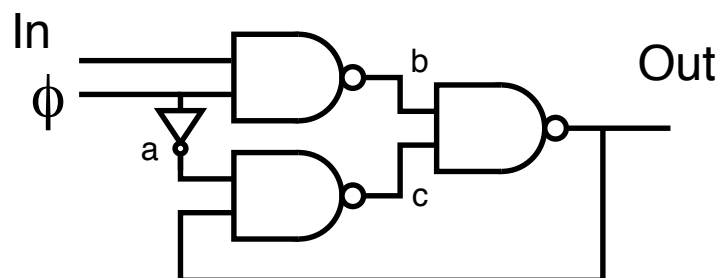
- Two phase clock generator: Build and simulate in SPICE the two-phase clock generator shown below. Drive it with a 100MHz square wave (VPULSE).



- include plot of SPICE simulation in writeup
- explain the operation of the circuit
- explain how you can modify the circuit to adjust the non-overlap period

(You will likely need this circuit for Project 2.)

- Gate-based latch: Build and simulate in SPICE the gate-based latch below:



- Explain how the latch operates.
- Characterize in SPICE; in writeup describe how the delays are related to the circuit.
 - the setup time - how long before ϕ transitions from 1 \rightarrow 0 must the input arrive in order for it to be held on the output once ϕ is 0?

- ii. hold time - how long after ϕ transitions from $1 \rightarrow 0$ must the input remain stable in order for it to be held on the output once ϕ is 0?
- iii. $\text{clk} \rightarrow \text{q}$ delay for the latch - how long after ϕ transitions from $0 \rightarrow 1$ before the input will be seen on the output (load with another latch for $\text{clk} \rightarrow \text{q}$ measurement)

Answers should be for worst-case data values (transitions).

3. Build and simulate in SPICE a register using the gate-based latch from the previous problem:

- (a) Explain how to build a register from the latch and how it operates.
- (b) Identify the benefits and limitations of this design
- (c) Characterize the register (setup time, hold time, $\text{clk} \rightarrow \text{q}$ delay (load with another one of these registers for comparison measurement))

4. Explore Register Operation

- (a) Using your register from the previous problem, cascade a 4 element long shift register and demonstrate proper operation on the input sequence: (first) 0 1 0 0 1 1 0 0 0 0 (last). (You may want to use a SPICE VPWL to supply the input.) [include schematic and waveform(s) demonstrating correct operation in turnin]
- (b) **Extra Credit:** Connect your register from (a) with a chain of three inverters in a feedback loop so that the output of the register toggles on every clock cycle.
 - i. How fast can you clock this design before it fails? (use SPICE to search for the frequency where the register just fails)
 - ii. At the highest frequency for correct operation, show how the clock cycle breaks down into into $\text{clk} \rightarrow \text{q}$ delay, logic propagation delay through the inverter chain, and setup time before the clock. Show waveforms from SPICE simulation, mark where transitions occur, and report the associated delays.

VPWL is one of the SPICE circuit elements you can insert in your Electric schematic. You control its behavior with the PWL string, which you can specify in Electric. The string is defined in Section 4.1.4 in the ngspice26 manual. It is a list of time voltage pairs. The signals is ramped linearly between the voltage at successive time points. The specification:

- 0ns 0 1ns 0 2ns 0.8 4ns 0.8 5ns 0 10ns 0 15ns 0 17ns 0.4 18ns 0.4 19ns 0.8 24ns 0.8 24.01ns 0 30ns 0

defines the following waveform:

