Course Webpage

Circuit-Level Modeling, Design, and Optimization for Digital Systems

Course: ESE3700

Units: 1.0 CU
Term: Spring 2024
When: MW 1:45pm-3:14pm EST (all times below are EST)
Where: Towne 307
Instructor: Tania Khanna (Levine 262, seas: taniak)
Instructor Office Hours: W 3:30-5pm and by appointment
TA: Richard Chang (seas: rchang24) (office hours: TBA)
TA: Peter Proenca (sease: peterpro) (office hours: TBA)

Prerequisites: ESE 1500, ESE 2150, CIS 2400 is also highly recommended. Roundup of topics you should be familiar with.
URL: `<http://www.seas.upenn.edu/~ese3700/>`

Quick Links: [Course Objectives] [Grading] [Policies] [Spring 2024 Calendar] [Reading] [Student Advice] [Ed Discussion] [Tool Guides]

Catalog Level Description: Circuit-level design and modeling of gates, storage, and interconnect. Emphasis on understanding physical aspects which drive energy, delay, area, and noise in digital circuits. Impact of physical effects on design and achievable performance.

Role and Objectives

The goal of this course is to teach students what they need to know about the physical aspects (area, delay, energy, noise) of electronic circuits to support high-speed, low-energy, area-efficient design of robust digital and computer systems. Students will learn:

https://www.seas.upenn.edu/~ese3700/

ESE3700: Circuit-Level Modeling, Design and Optimization for Digital Systems

Lec 1: January 22, 2024

Introduction and Overview

Course Structure: Staff

- Course Staff (complete info on course website)
- Instructor: Tania Khanna (she/her)
  - OH: W 3:30-5pm (Levine 262)
  - Or OH by appointment
  - Email: taniak@seas.upenn.edu
    - Best way to reach me

TA Introduction: Richard Chang

- Took ESE 3700 in Spring 2023
  - Also took ESE 5700 in Spring 2024
- Senior EE + accelerated MSE graduating in May 2024
- Interned at Lutron Electronics
- I enjoy watching sports and playing the piano
- I will watch all Formula 1 races, no matter what odd hours the races are at

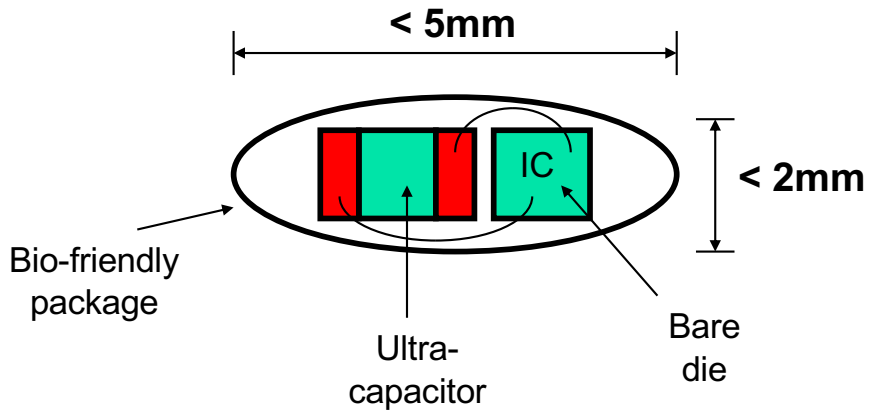
TA Introduction: Peter Proenca

- Took ESE 3700 in Spring 2023
- Junior studying CMPE
- Accelerated Masters – ESE
- I am interested in medicine and the combination of engineering and health.
- Outside of engineering I play a variety of instruments and I like to swim.

Where I come from

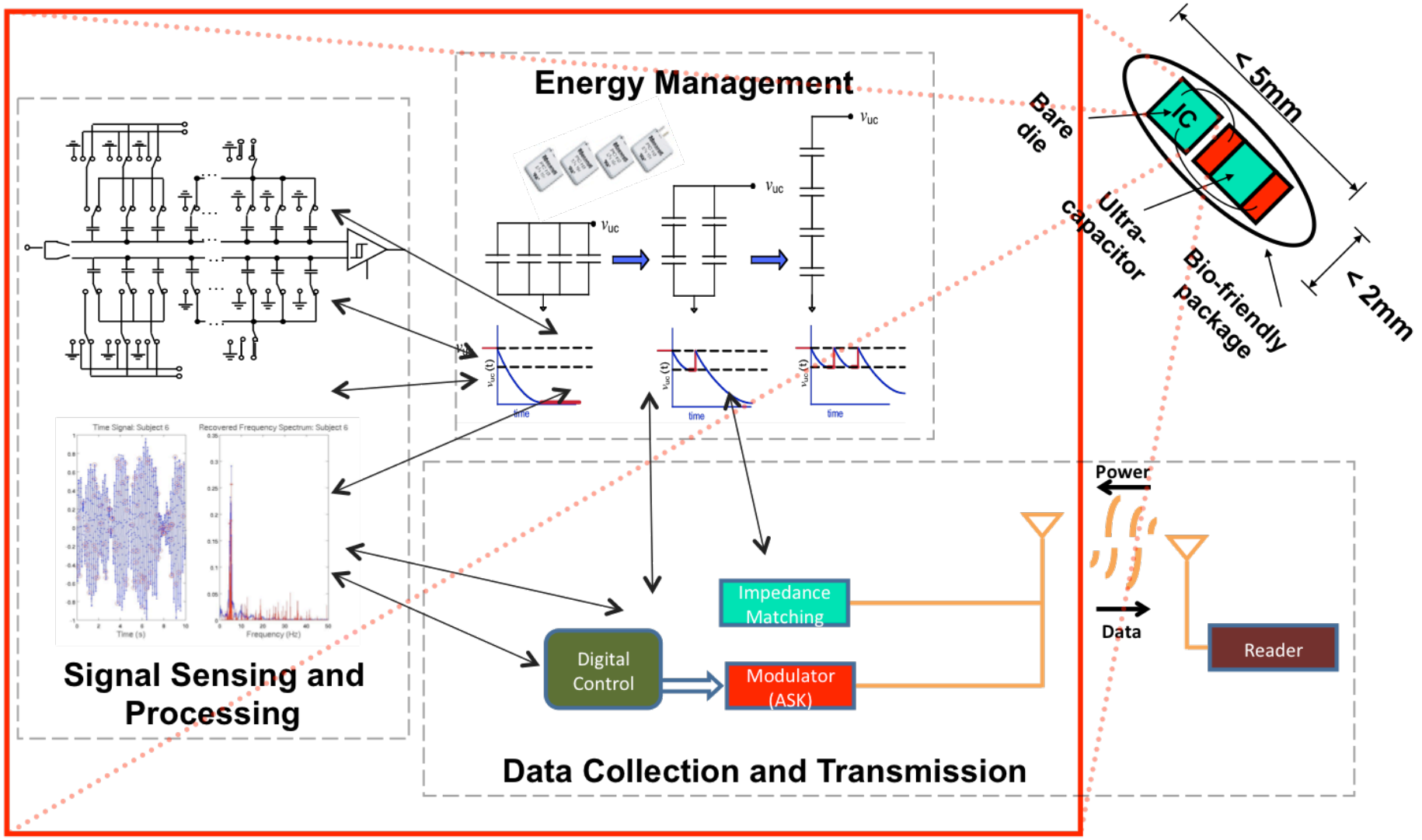
- VLSI Circuit Design
- Convex Optimization
  - System Hierarchical Optimization
- Biomedical Electronics
- Biometric Data Acquisition
  - Compressive Sampling
- ADC Design
  - SAR, Pipeline, Delta-Sigma
- Low Energy Circuits
  - Adiabatic Charging

Minimally Invasive Implant to Combat Healthcare Noncompliance



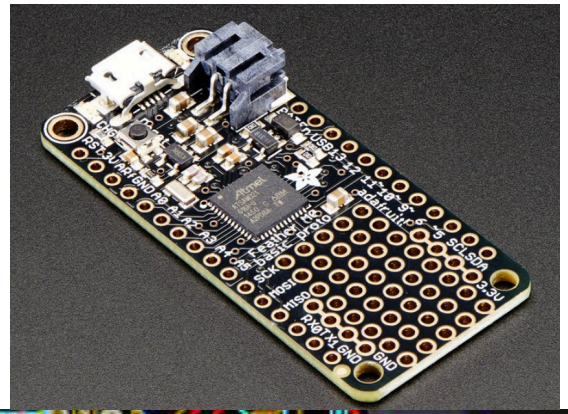
- Model for implants: reconfigurable RFID tags that continuously record specific biometric
  - During the read operation, energy storage element is recharged
- Size of package small enough to allow injection
- Actigraphy expected to be clinically useful
  - Platform allows for any sensor that gathers information on a slow time scale

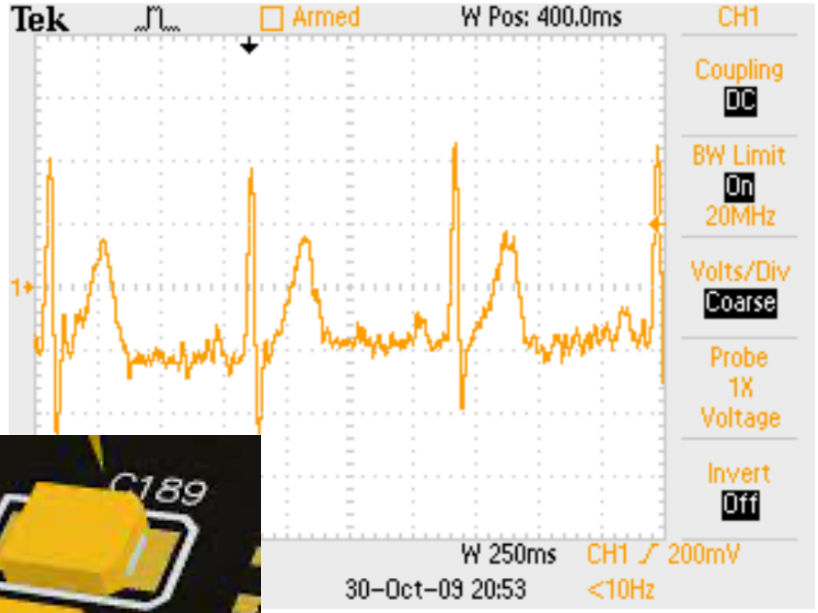
MicroImplant: An Electronic Platform for Minimally Invasive Sensory Monitors

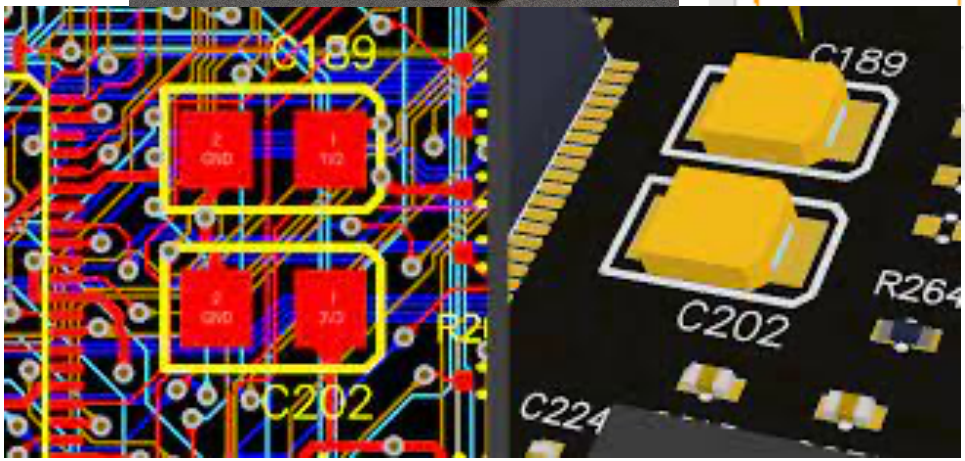


Shameless Plug - ESE 3400

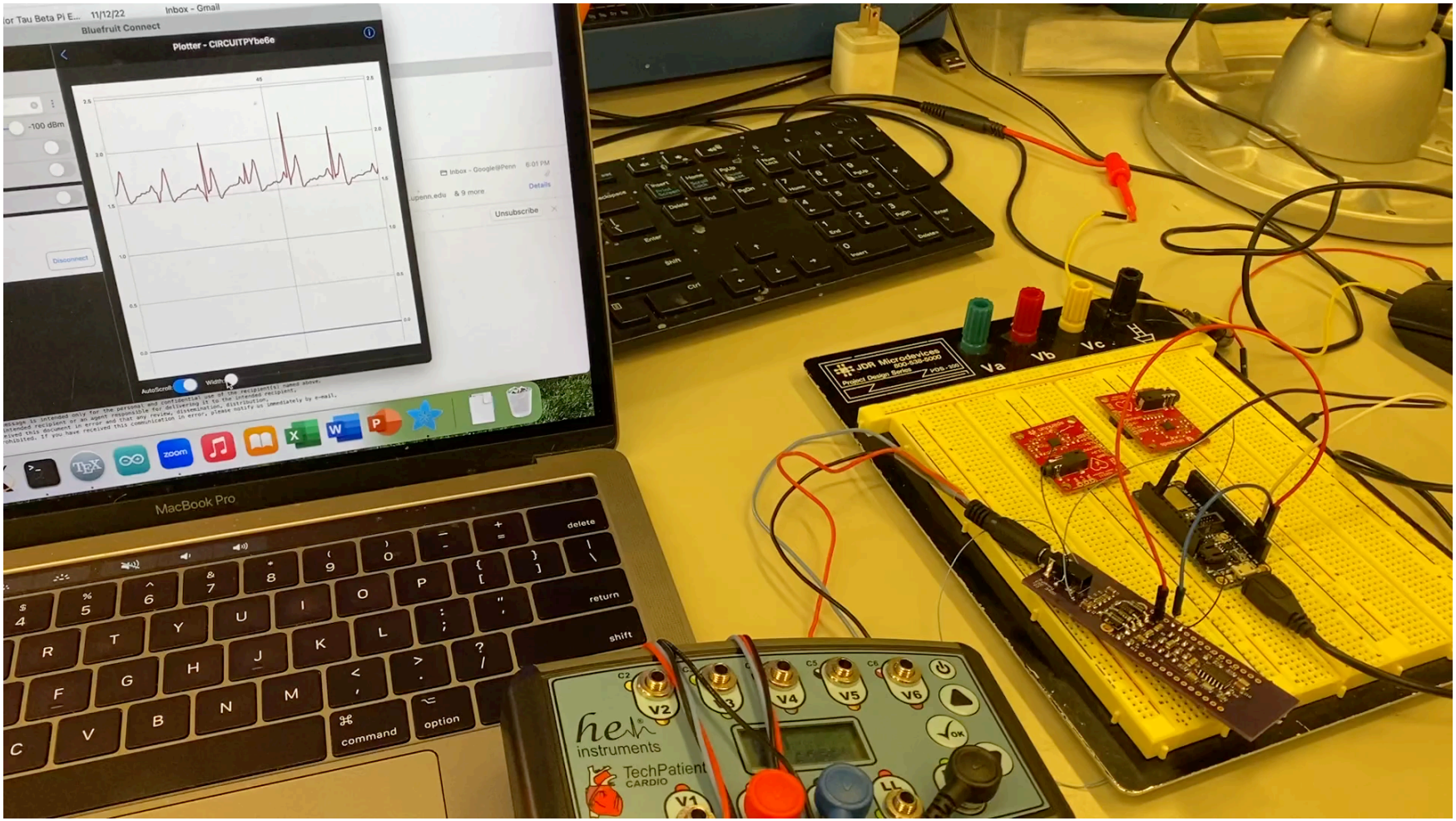
- Lab based inquiry into medical device design
  - Build ECG system with wireless communication



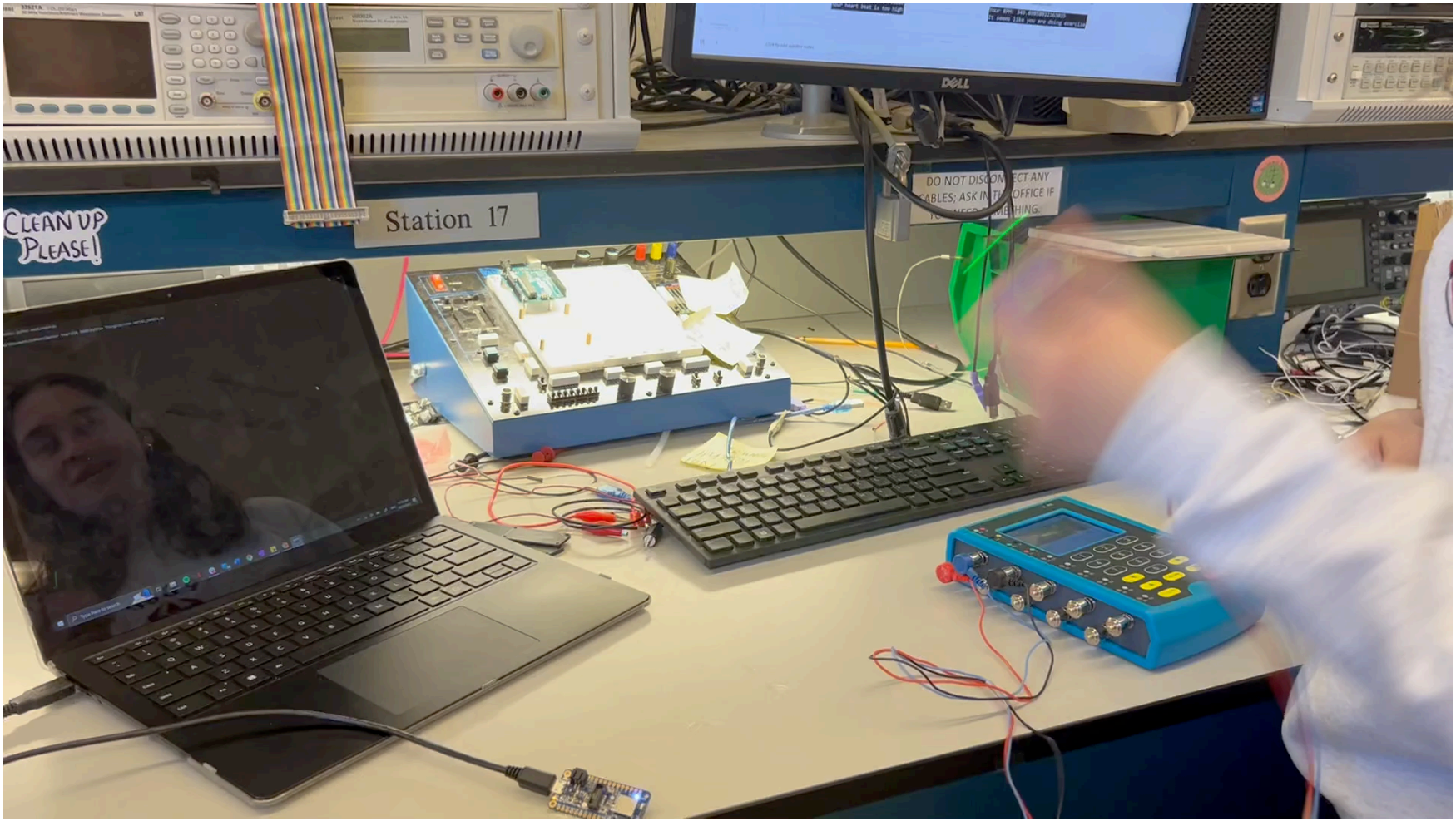


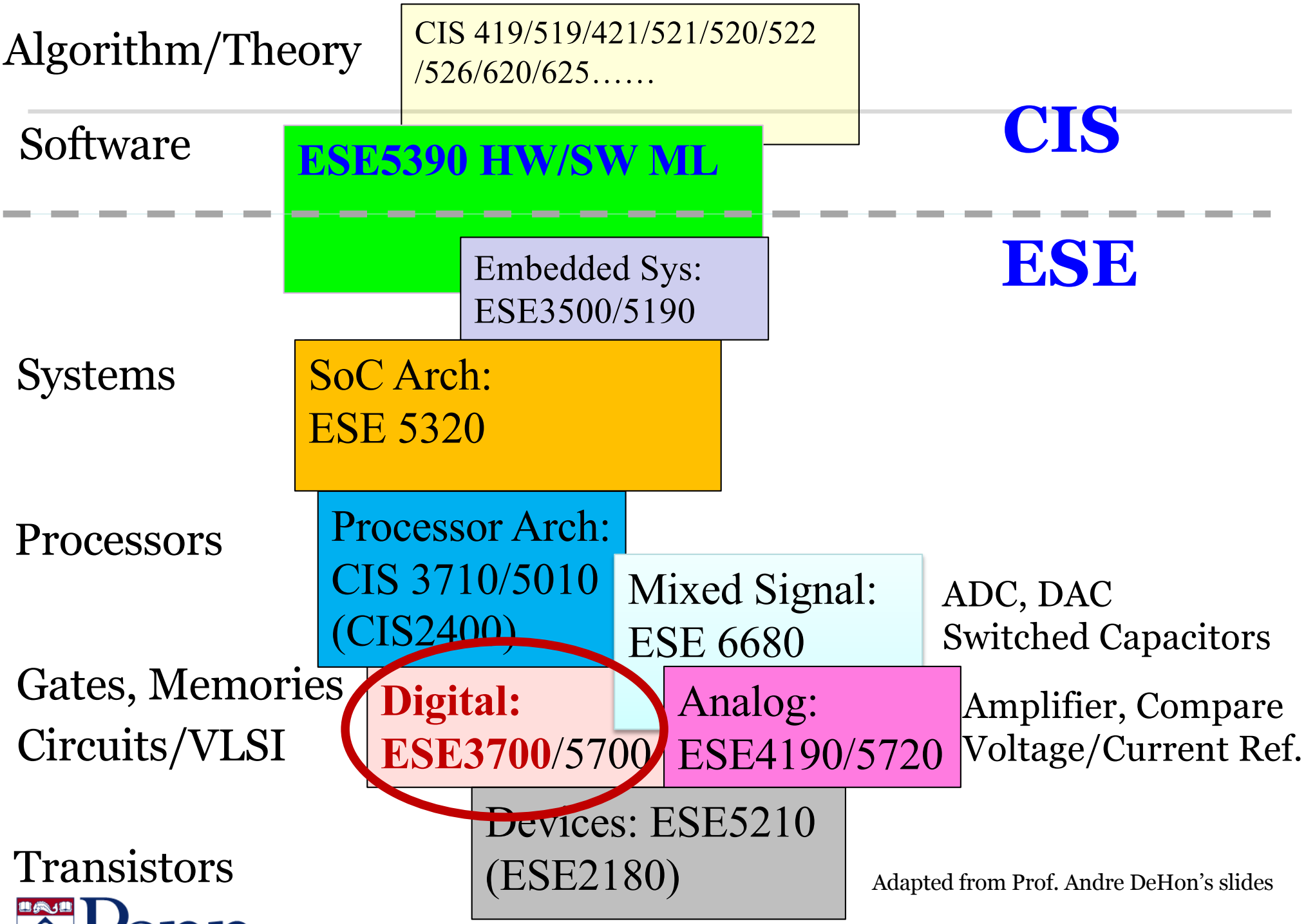


Shameless Plug - ESE 3400



Shameless Plug - ESE 3400



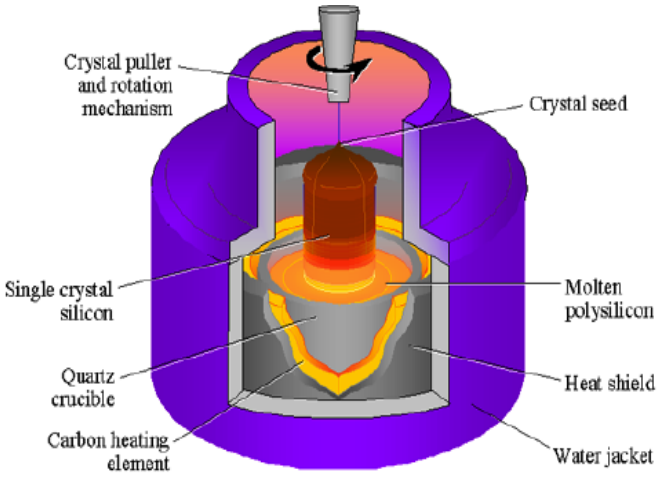


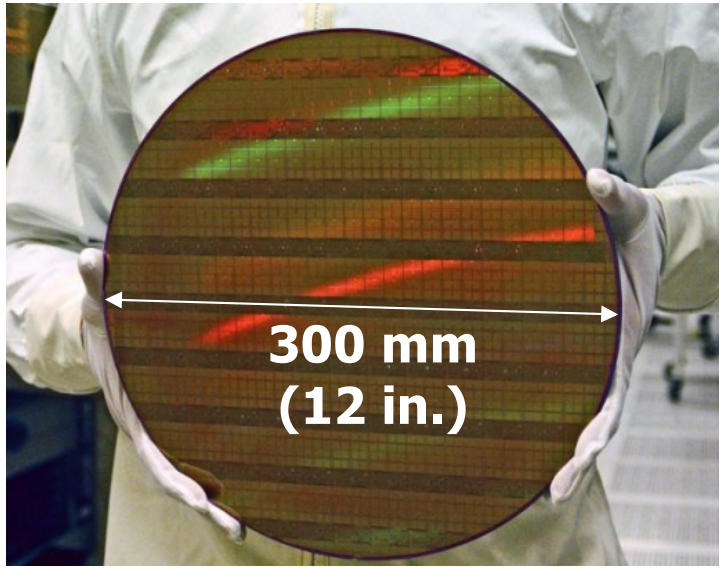
Adapted from Prof. Andre DeHon's slides

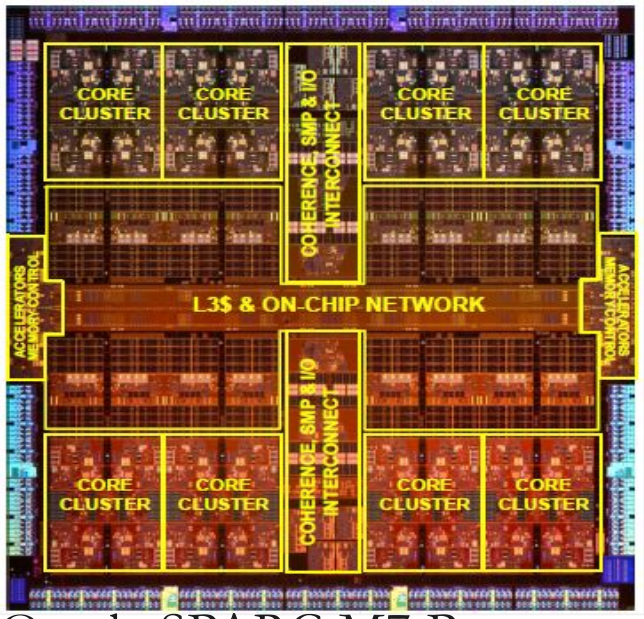
Lecture Outline

- Course Overview
  - Motivating questions
  - What this course is about
  - Learning objectives
  - What you need to know
- Course Details
  - Course structure
  - Course policies
  - Course content

VLSI Design



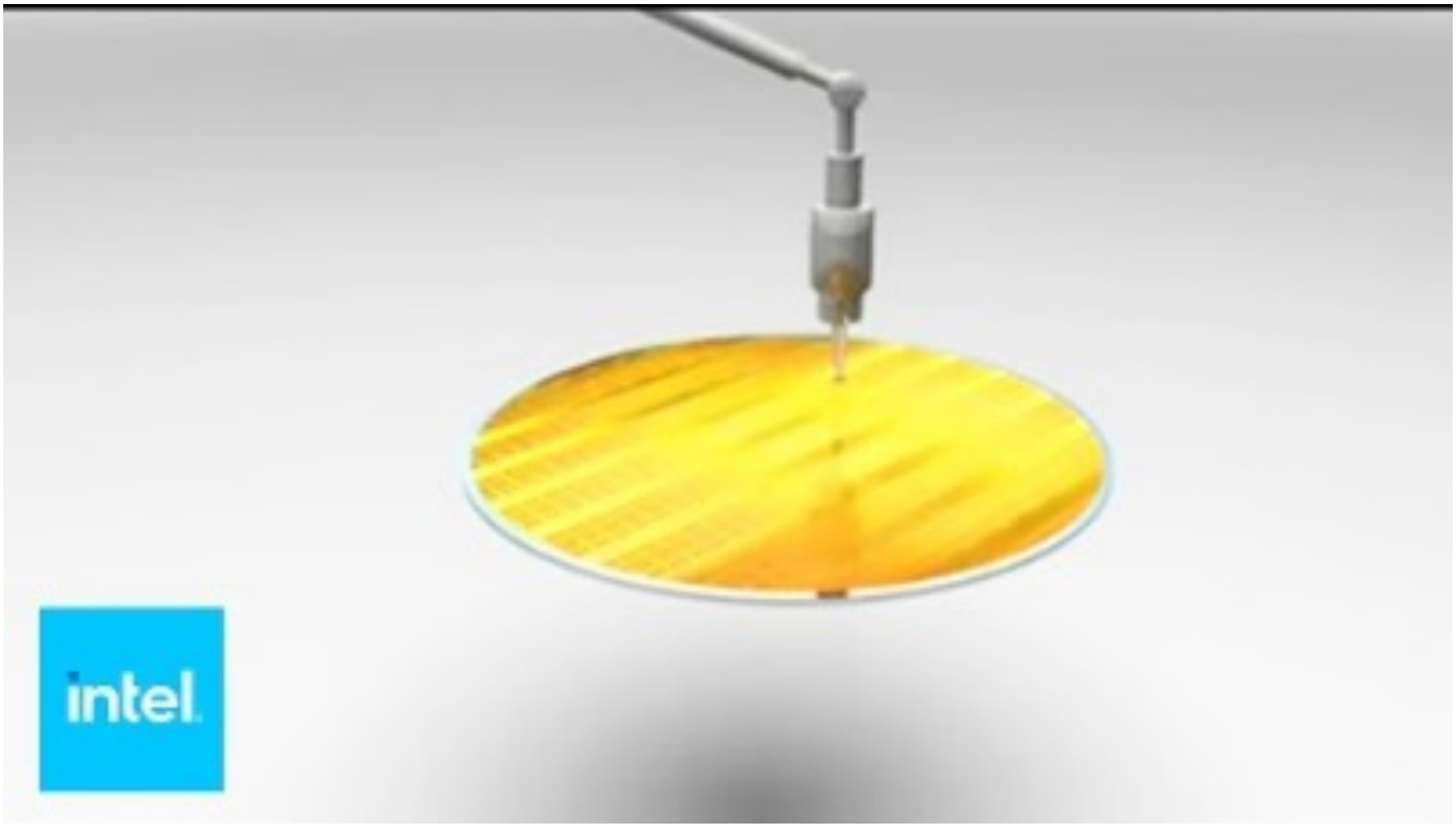




Oracle SPARC M7 Processor

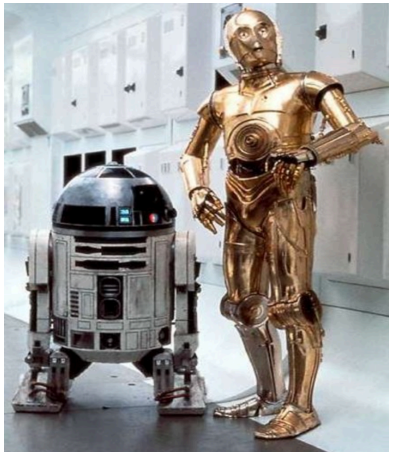
Intel: From Sand to Silicon

- https://www.youtube.com/watch?v=Q5paWn7bFg4



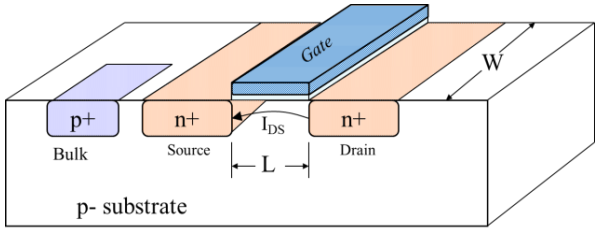
What This Course is About?

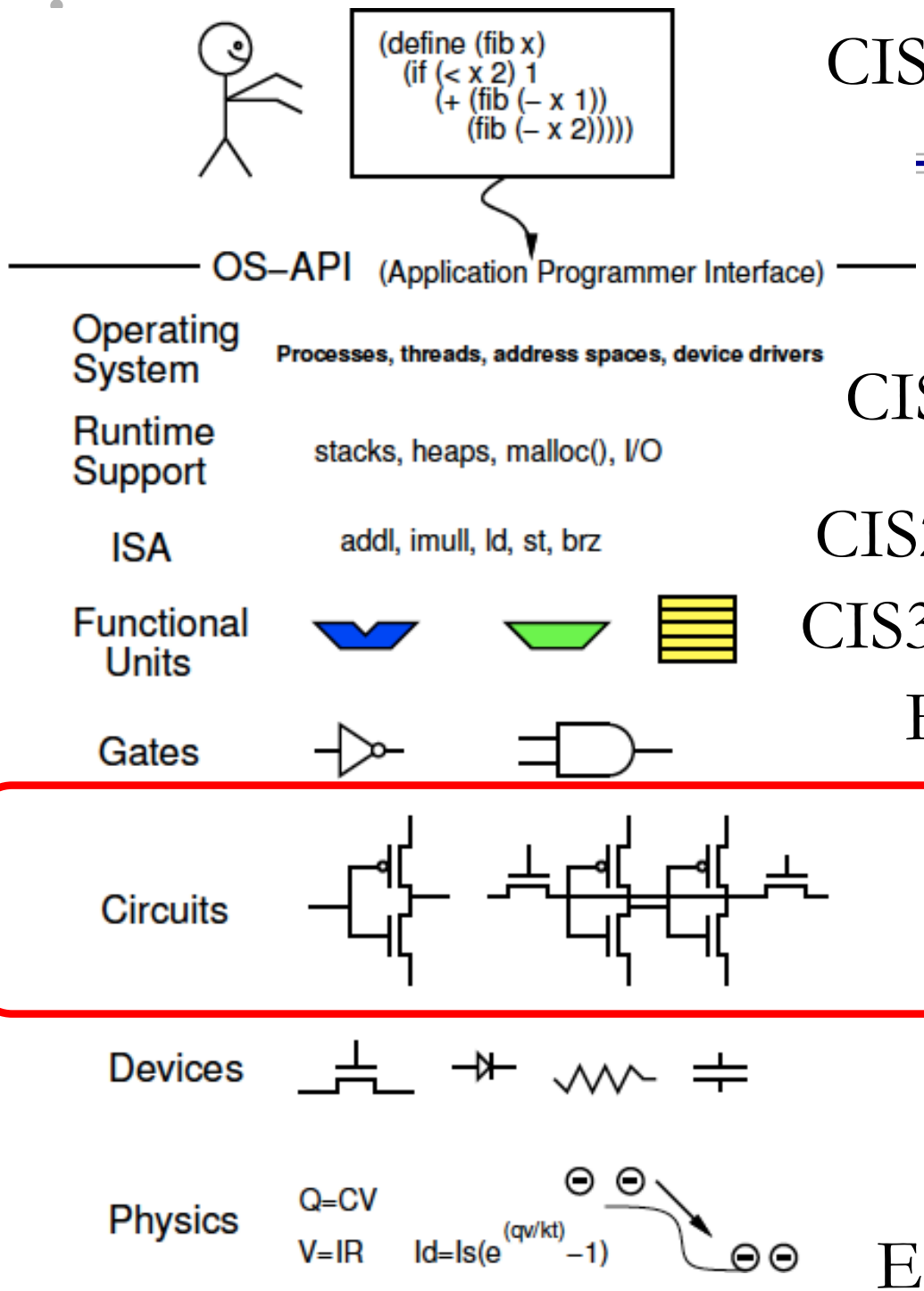
To build something you have to understand what building blocks you have available to you.



To build something really cool you need to have a fairly thorough understanding of how those building blocks work.

In VLSI our two primary building blocks are the NMOS and PMOS transistors. This is not a device physics course, but we will have to dive a bit into the workings of these transistors.





CIS120/121

CIS3800

CIS2400

CIS3710, ESE5320, ESE5390

ESE1500

We are here.

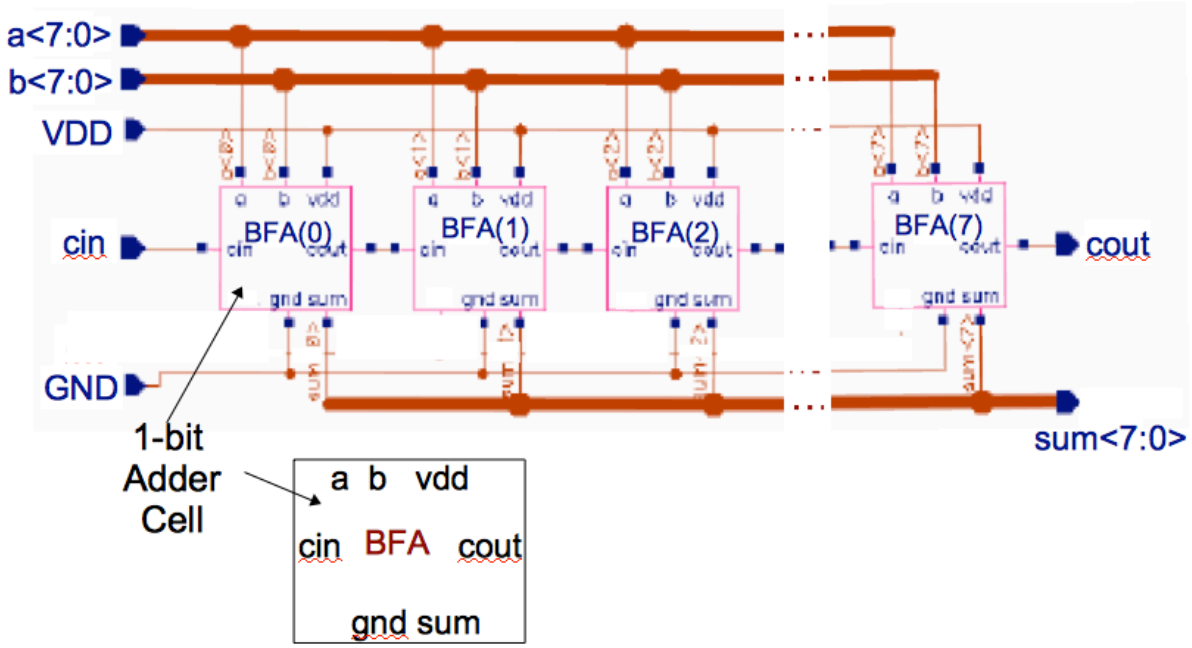
ESE2150, ESE3190

ESE2180

ESE1120/Phys1510

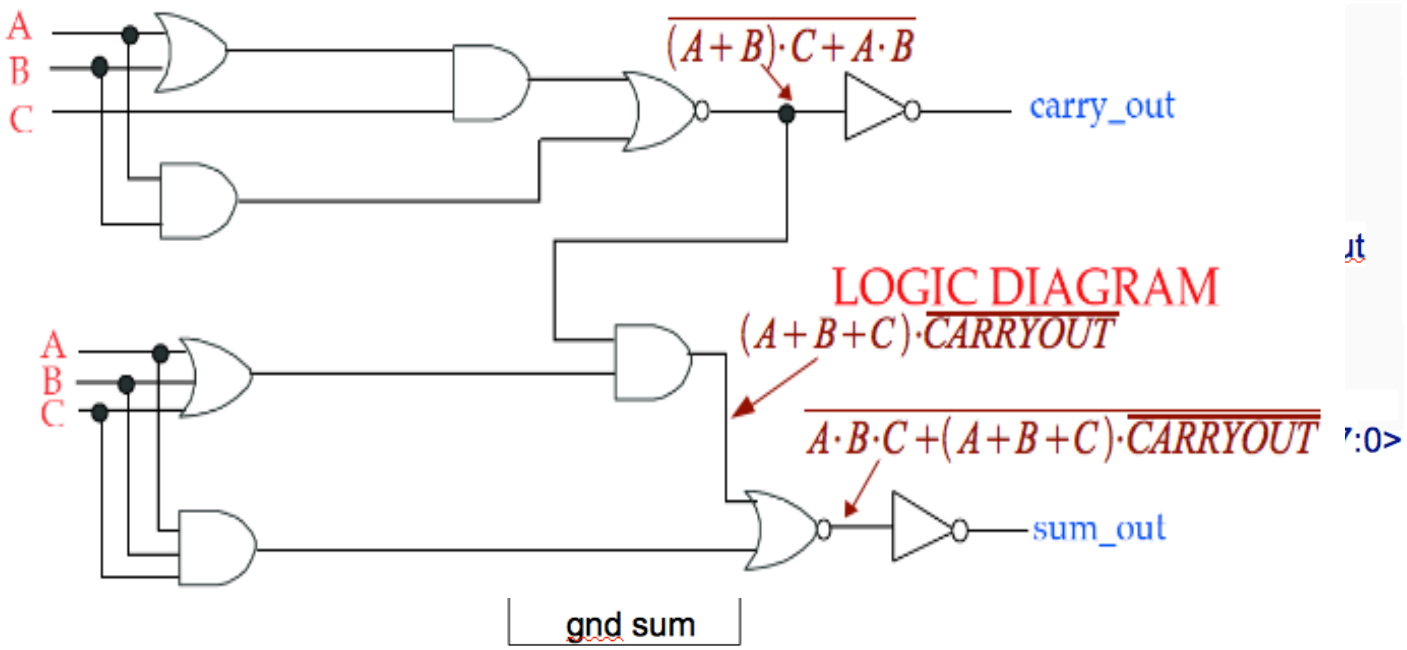
ESE 3700

- Circuit-Level Modeling, Design, and Optimization for Digital Systems
  - Design adder for functionality and performance



ESE 3700

- Circuit-Level Modeling, Design, and Optimization for Digital Systems
  - Design adder for functionality



ESE 3700

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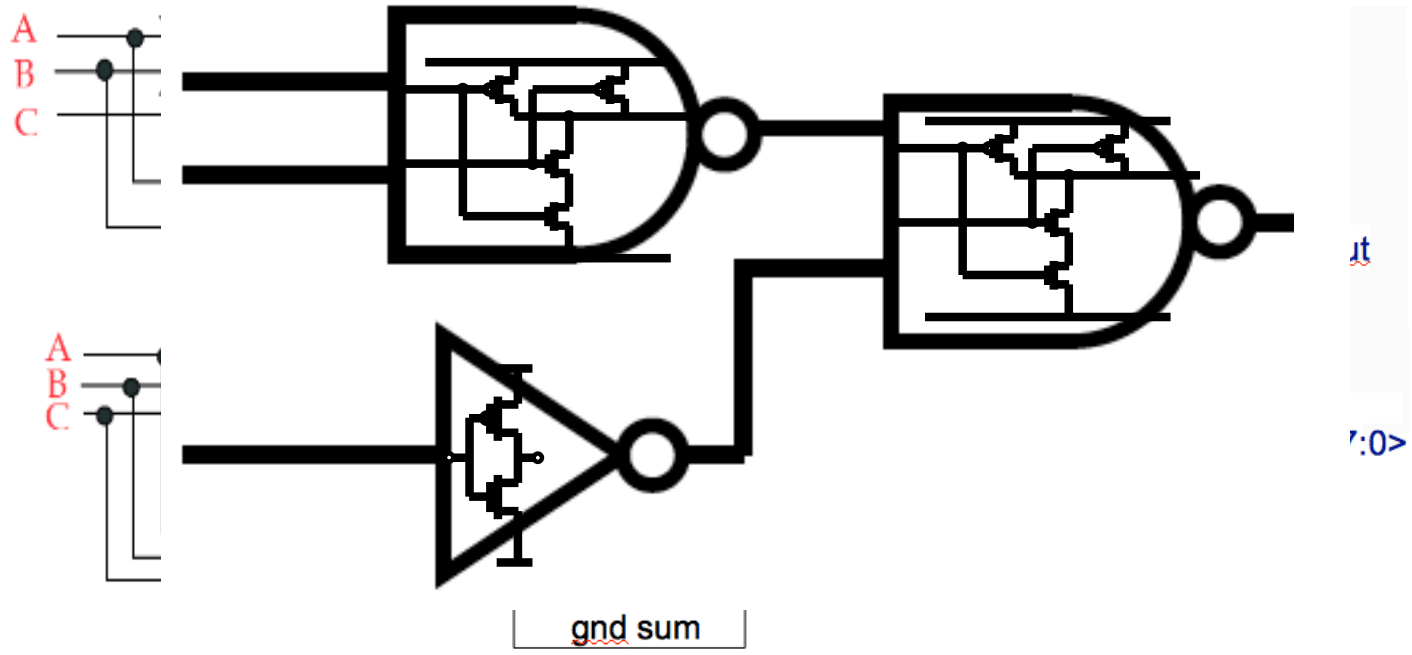
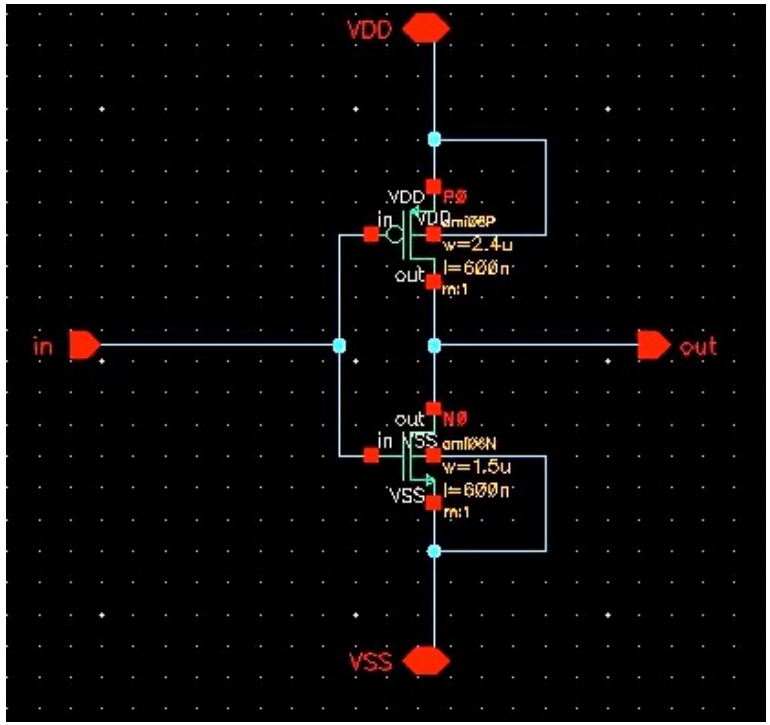
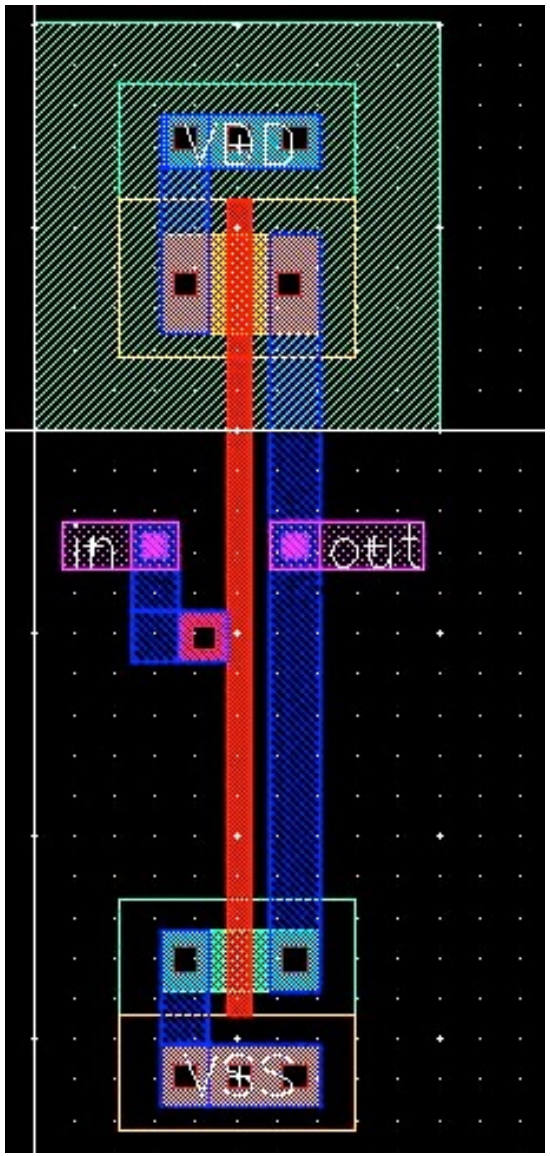


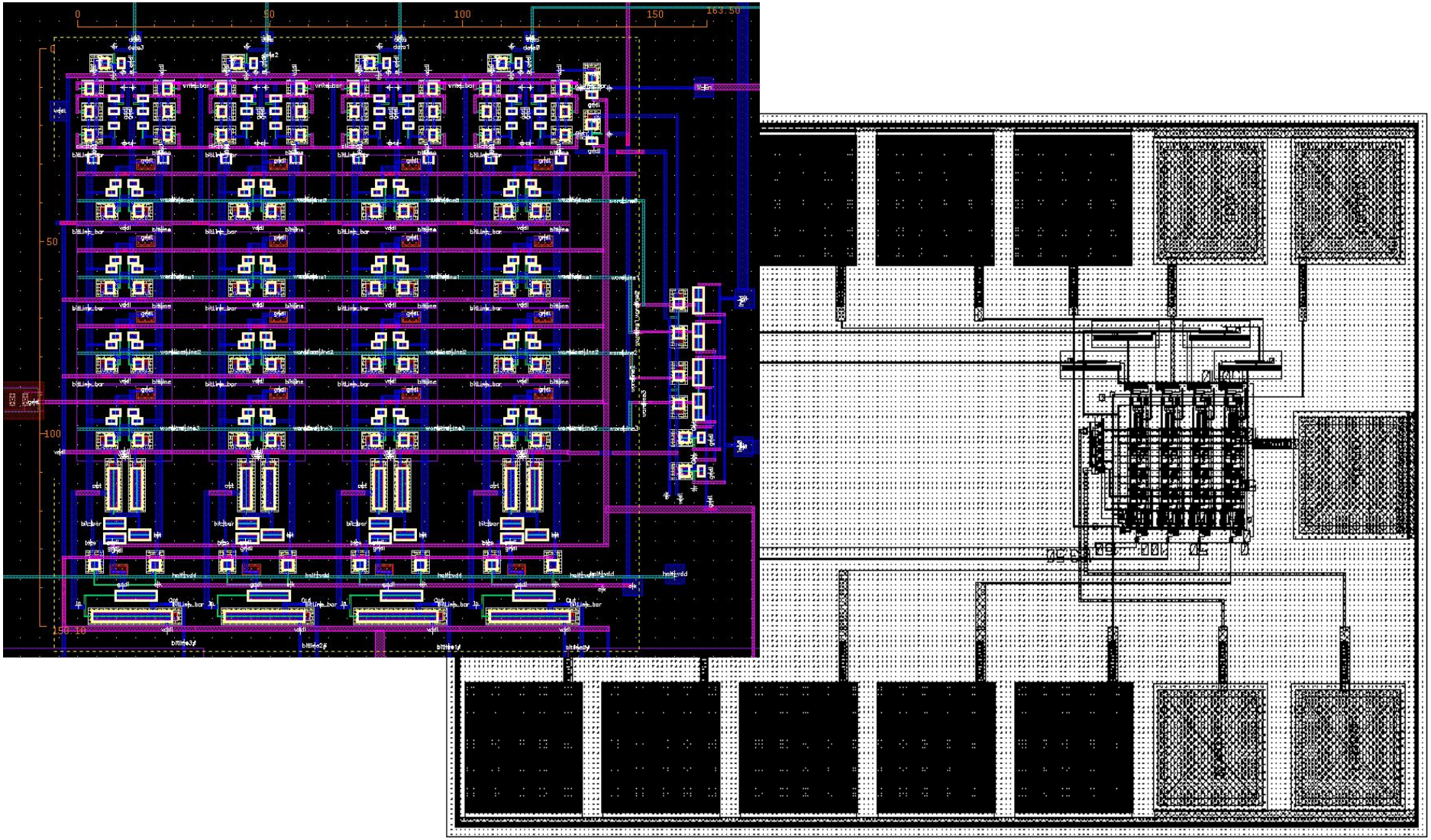
ESE 5700: Manufacturability



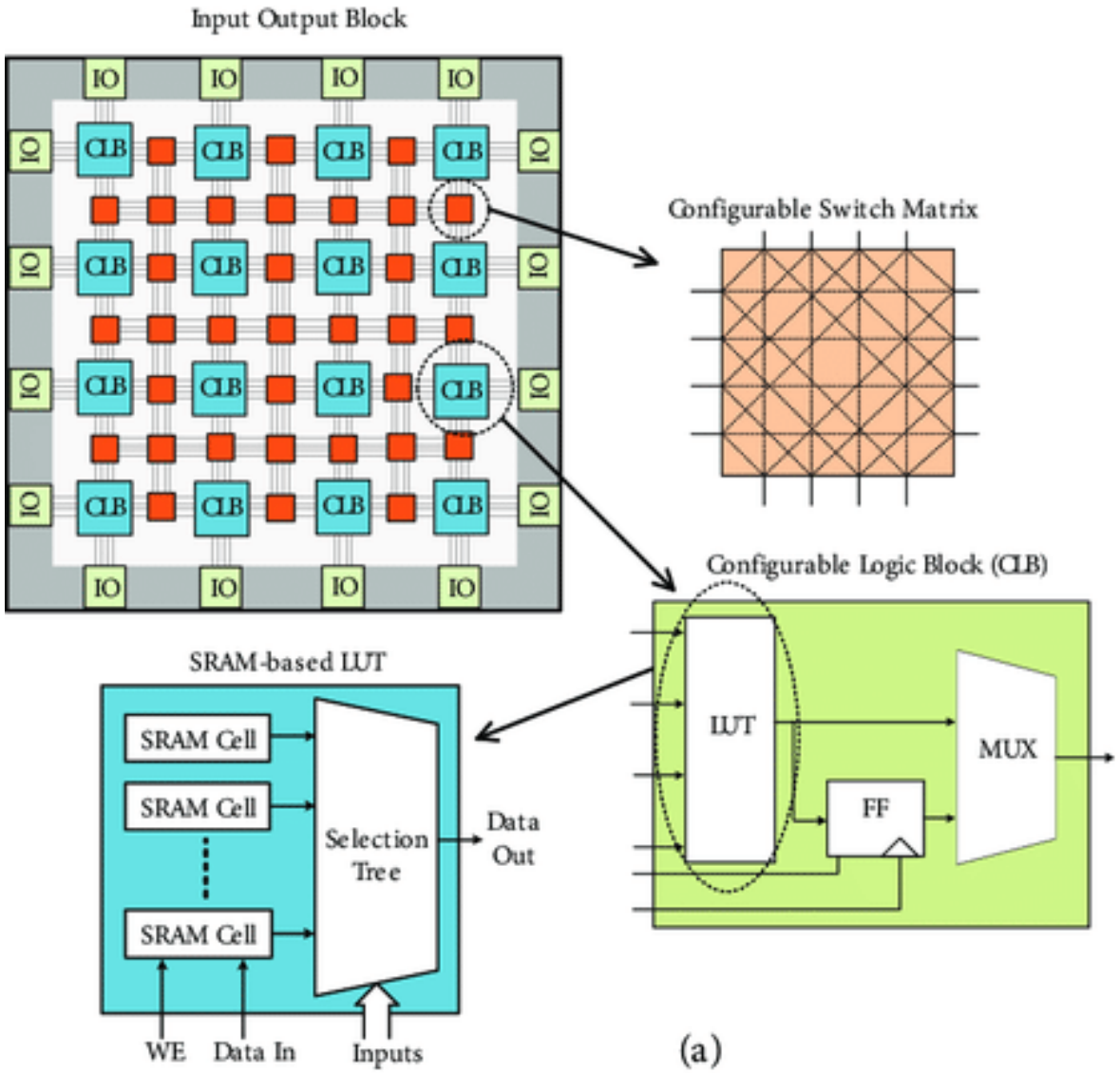
Schematic to layout



ESE 5700: 4x4 6T SRAM



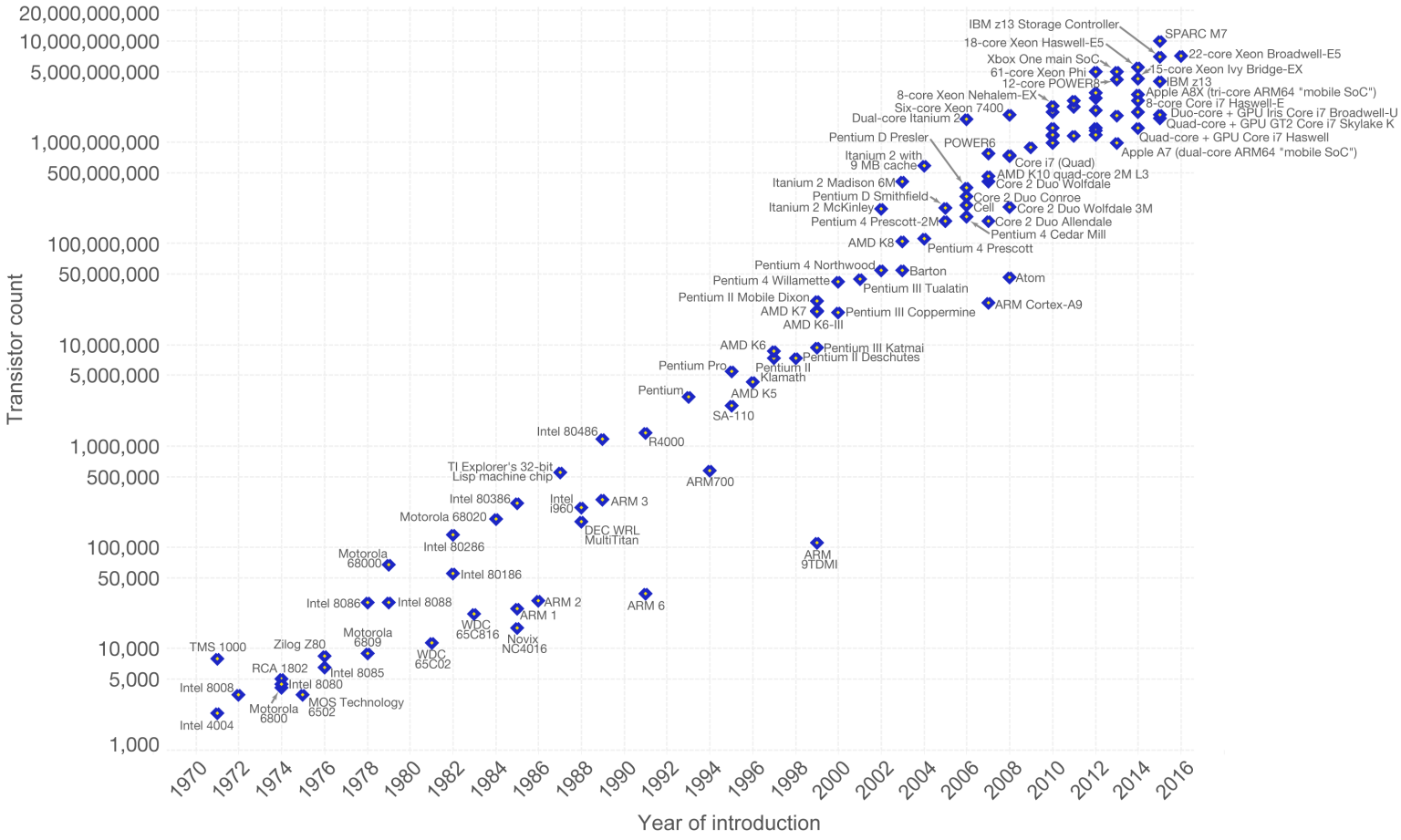
ESE 5700: Configurable Logic Block



Moore's Law

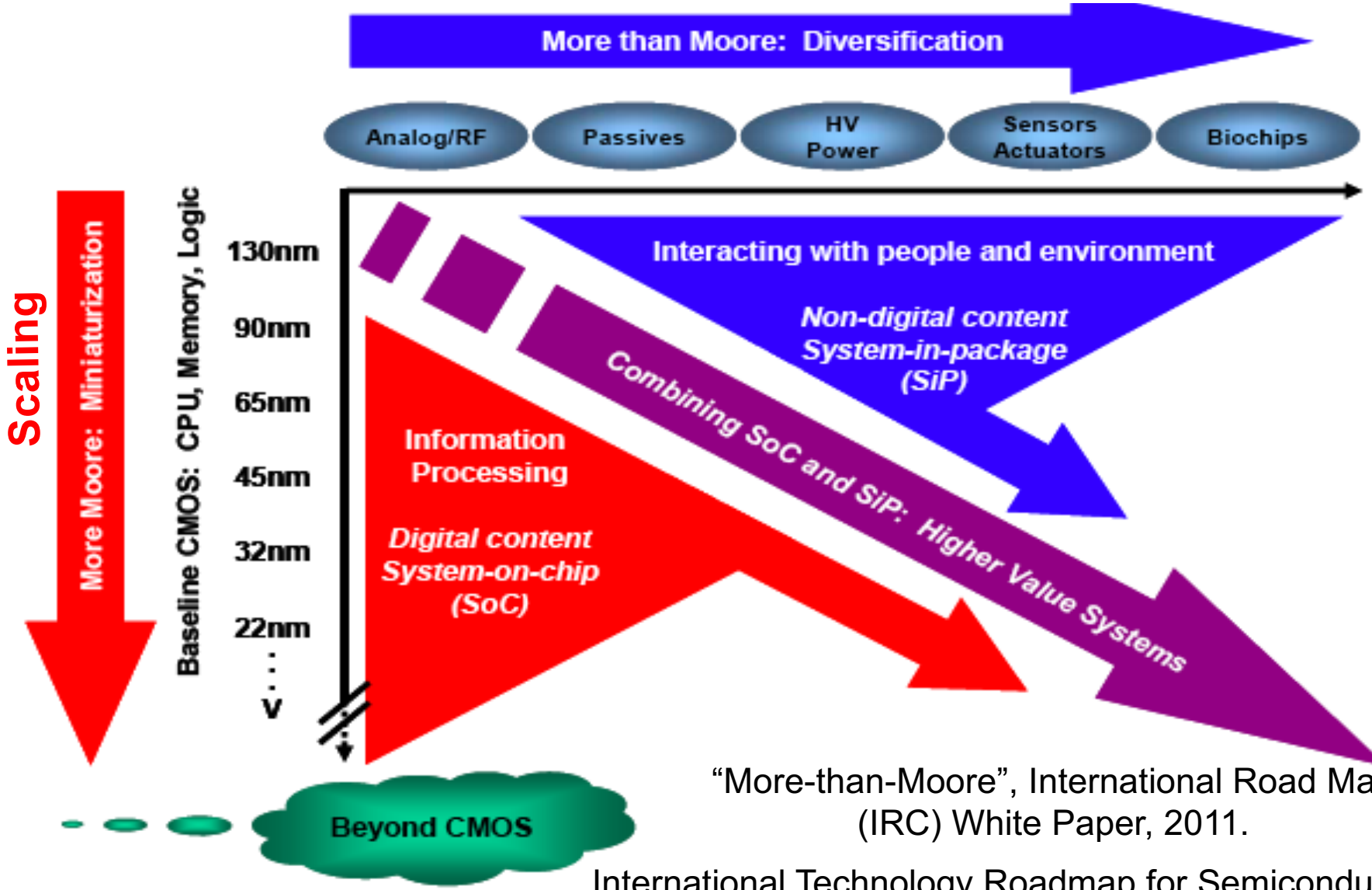
Moore's Law – The number of transistors on integrated circuit chips (1971-2016)

Moore's law describes the empirical regularity that the number of transistors on integrated circuits doubles approximately every two years. This advancement is important as other aspects of technological progress – such as processing speed or the price of electronic products – are strongly linked to Moore's law.



Data source: Wikipedia (https://en.wikipedia.org/wiki/Transistor_count)
The data visualization is available at OurWorldinData.org. There you find more visualizations and research on this topic.

More-than-Moore

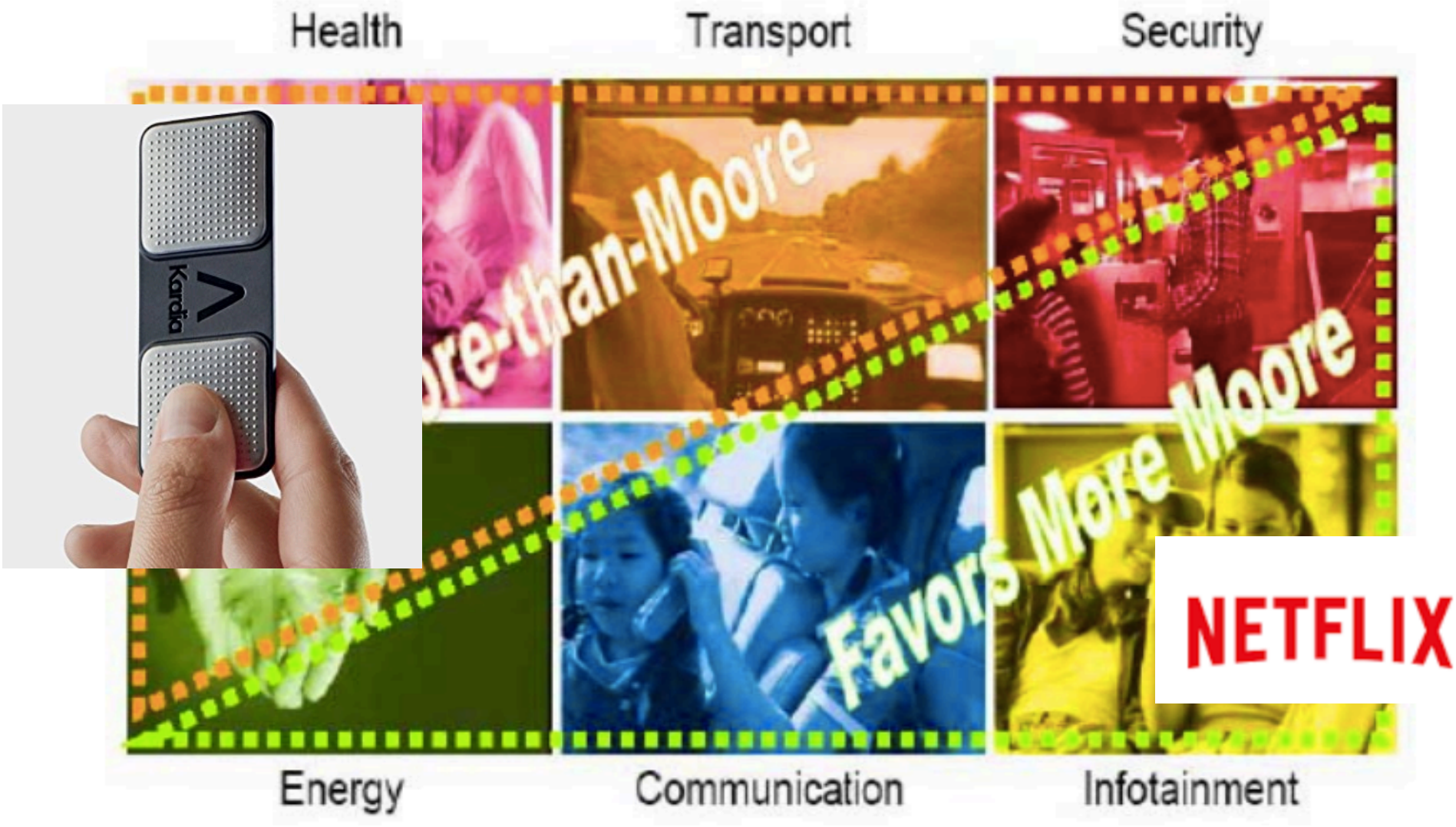


"More-than-Moore", International Road Map (IRC) White Paper, 2011.

International Technology Roadmap for Semiconductors

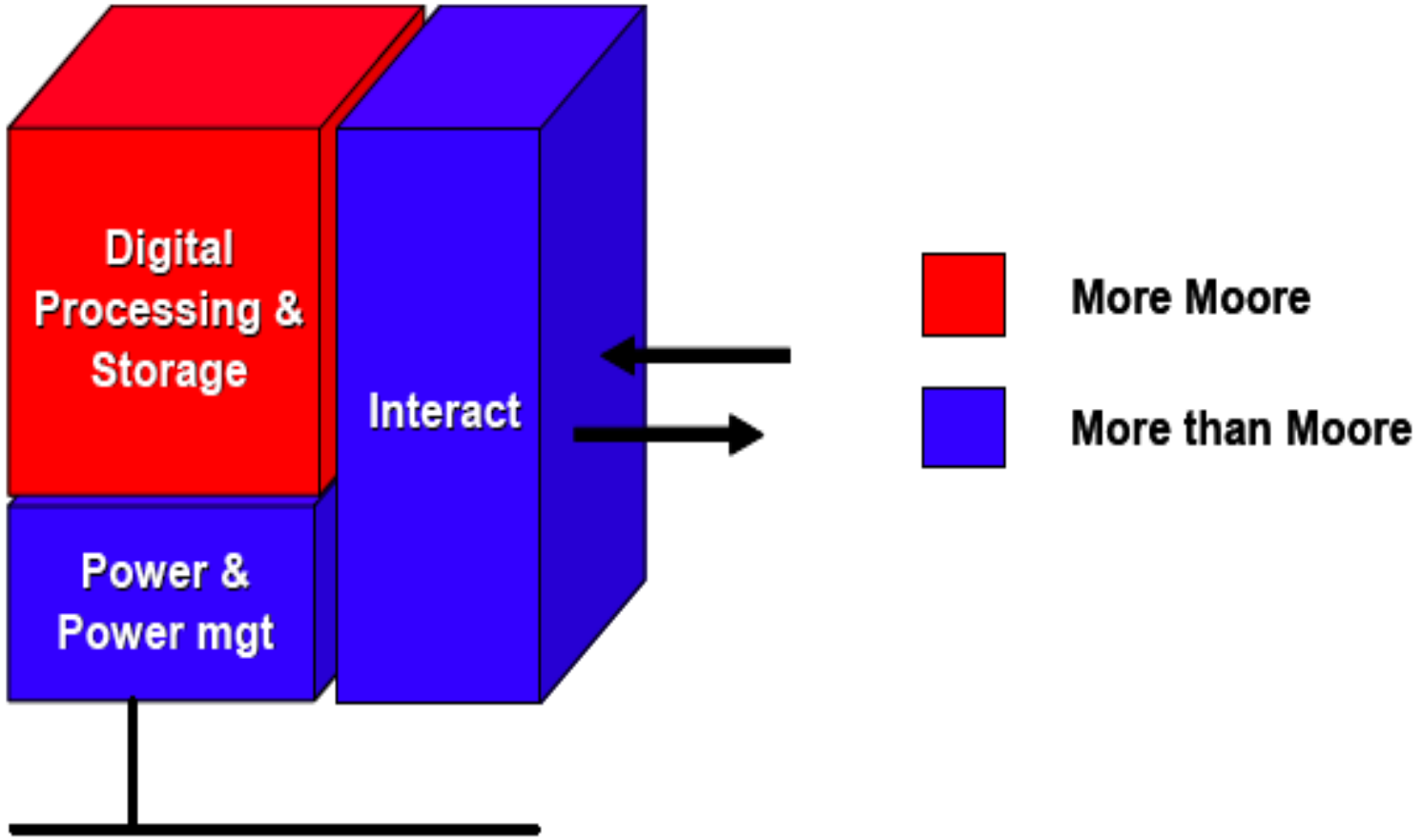
Societal Needs

Societal Needs

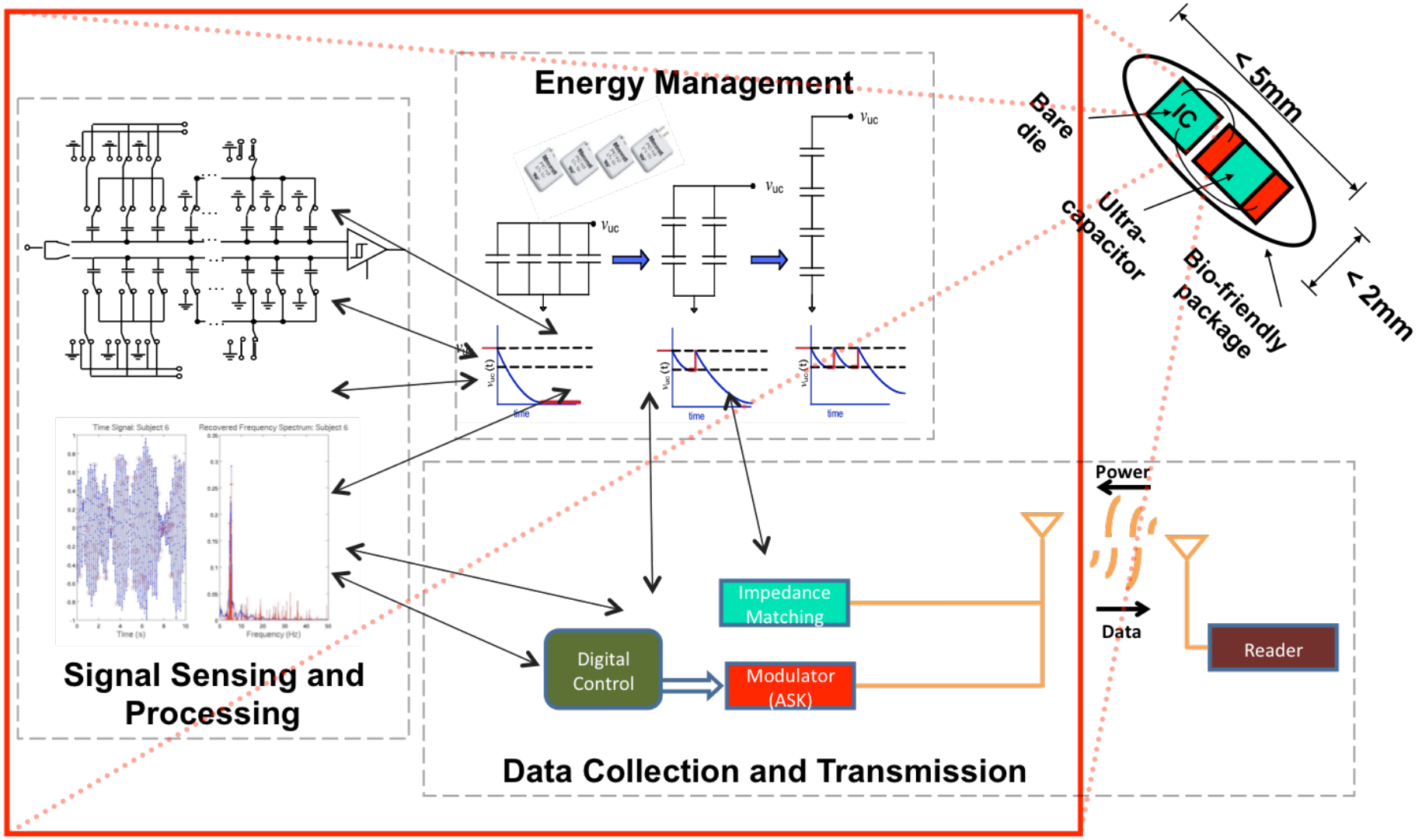


"More-than-Moore"

- Components Complement Digital Processing/Storage Elements in an Integrated System

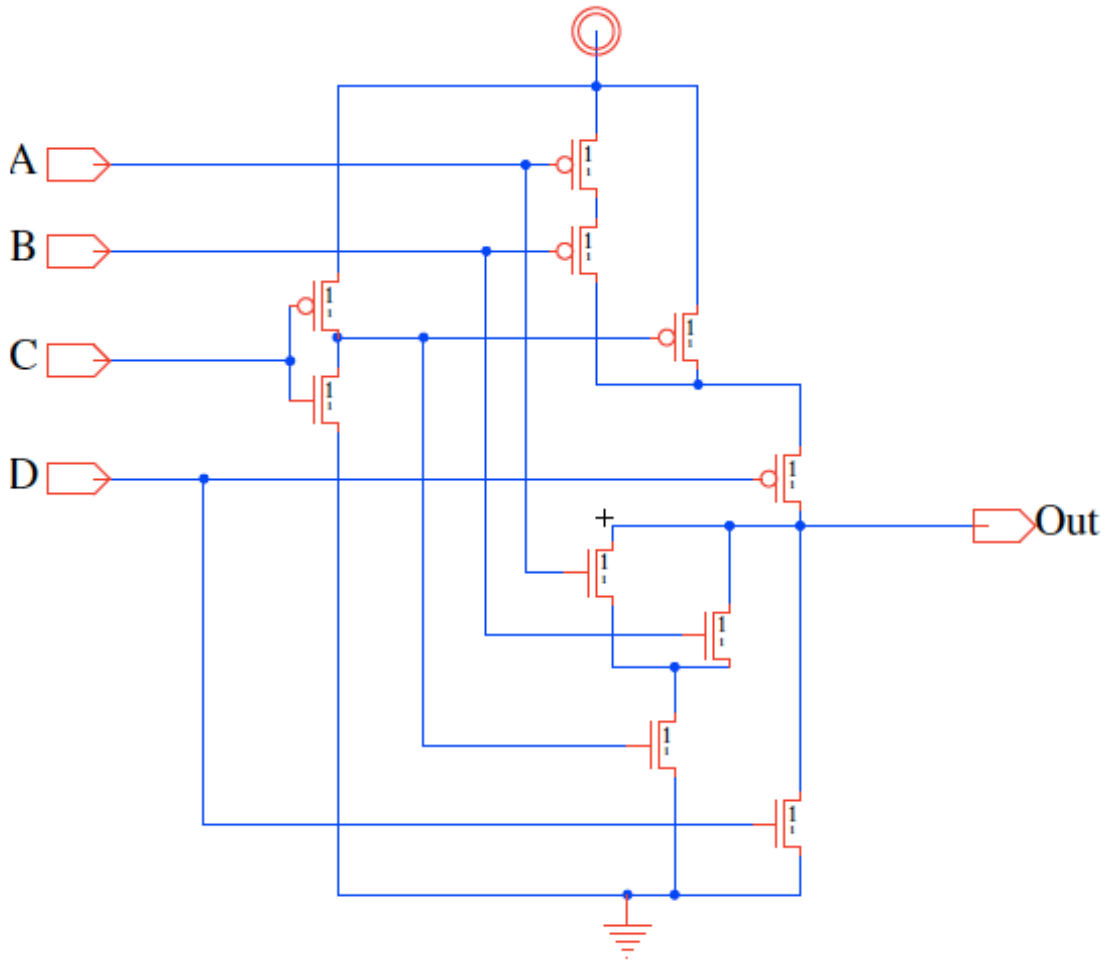


MicroImplant: An Electronic Platform for Minimally Invasive Sensory Monitors



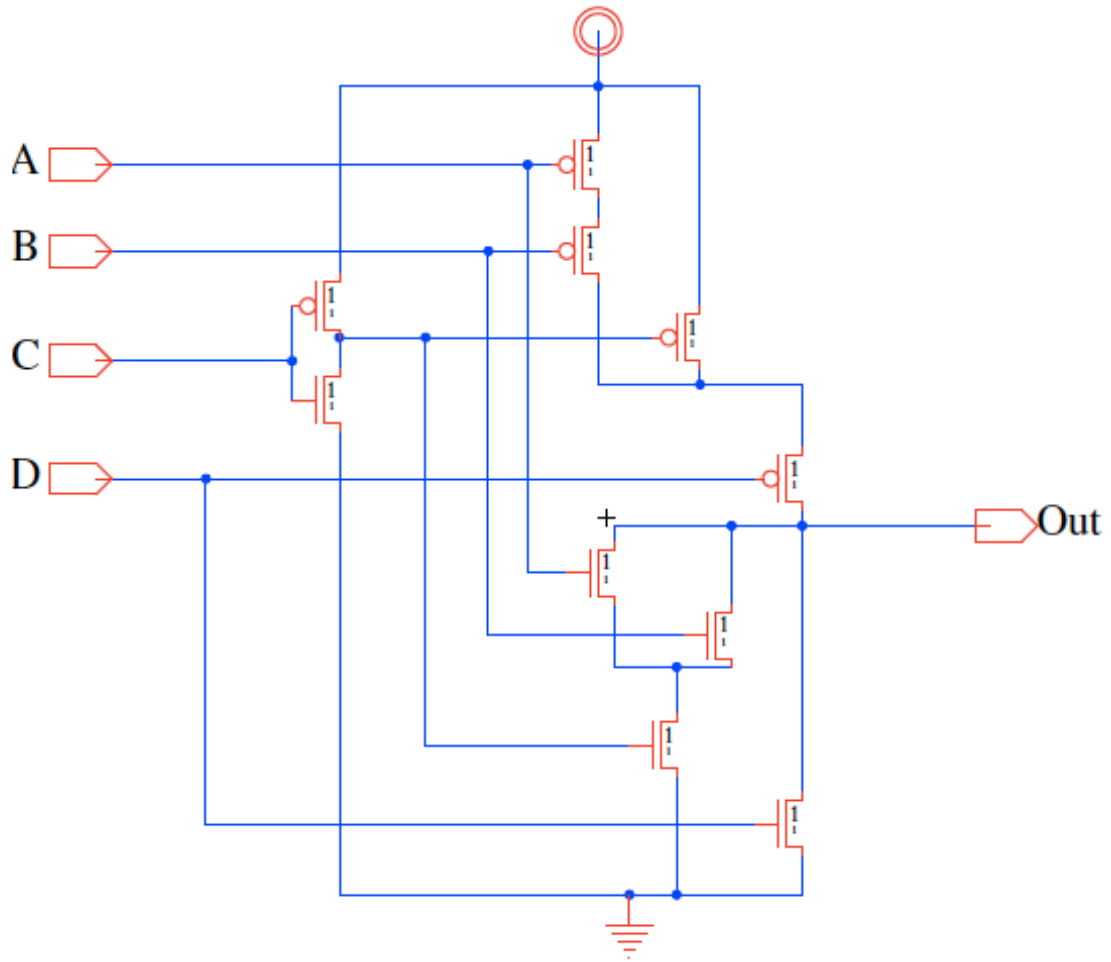
Sample Problems

- What does this circuit do?



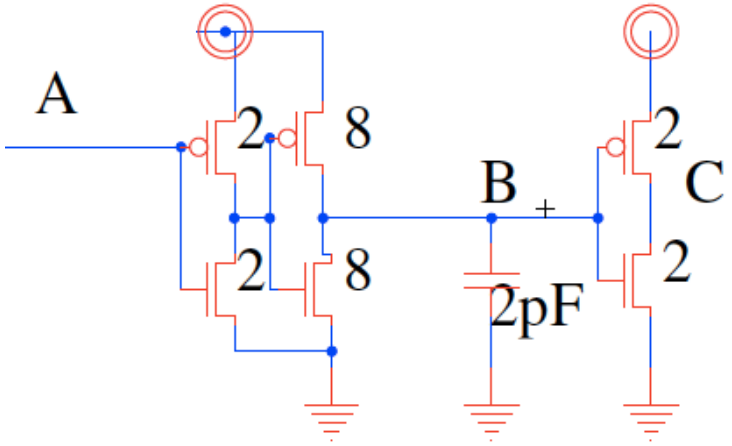
Sample Problems

- What does this circuit do? How fast does it operate?



Sample Problems (con't)

- What does this circuit do? How are A, B, C related?



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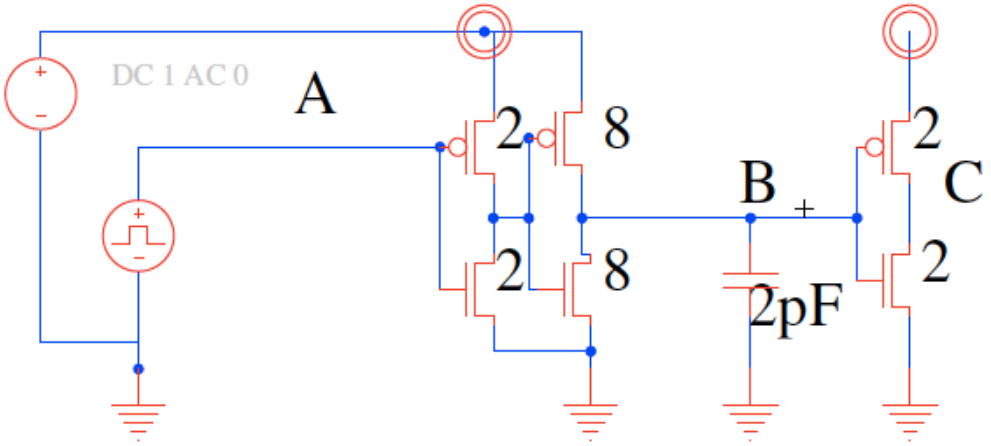
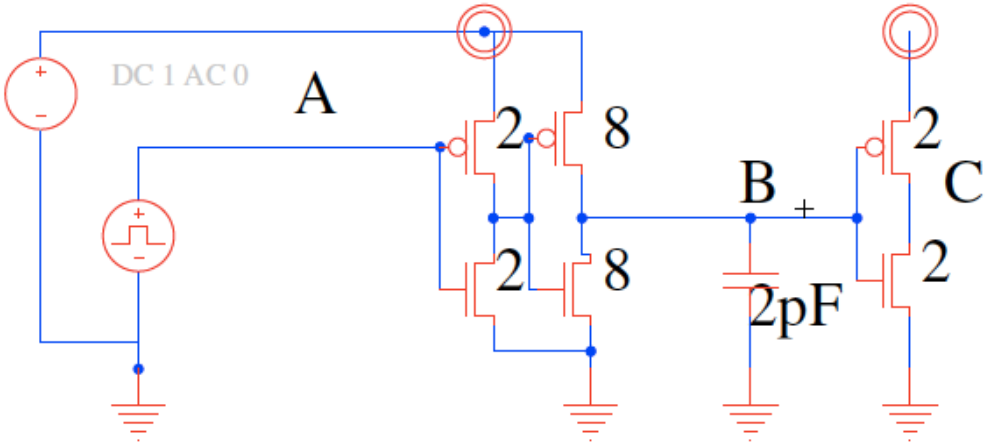
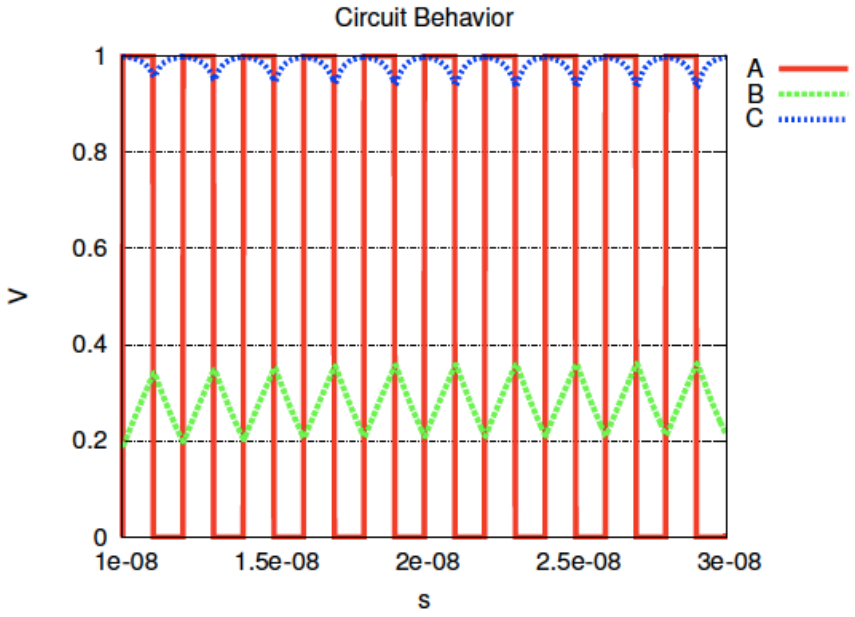


Sample Problems (con't)

- What's wrong here? How do we fix it?





Limits?

- Consider a 22nm technology
- Typical gate with W=3, 2-input NOR
- Use chip in cell phone
- What prevents us from running 1 billion transistor chip at 10GHz?

Impact of Voltage?

- If we have a chip running at 1GHz with a 1V power supply dissipating 1W.
- What happens to performance if we cut the power supply to 500mV?
  - Power?
  - Speed?

What this course is about

- Modeling and abstraction
  - Predict circuit behavior
  - …well enough to know your design will work
  - …with given performance spec(ification)s
    - Speed, energy, size, etc.
  - …well enough to reason about design and optimization
    - What knob can I turn to make faster?
    - How much faster can I expect to make it?

What this course is about (con't)

- Modeling and abstraction
  - Back-of-the-envelope calculations
    - Simple enough to reason about and estimate
      - …without a calculator
  - Sensitive to phenomena
    - Able to think through the details
  - With computer assistance
    - …understanding even that is a simplified approximation of phenomenology

Learning Objectives

- Disciplines for robust digital logic and signaling
  - (*e.g.*, regeneration, clocking)
- Where delay, energy, area, and noise arise in gates, memory, and interconnect
- Modeling these physical effects
  - back-of-the-envelope design
    - (*e.g.* RC and Elmore delay)
  - detailed simulation (*e.g.* SPICE)

Learning Objectives (con't)

- Tradeoffs in performance specs
  - Among delay, energy, area, noise
- How to design and optimize
  - logic, memory, and interconnect structures
  - at the gate, transistor, and wire level
- How technology scales
  - impact on digital circuits and computer systems

What you need to know

- See "knowledge roundup" topics page linked from course webpage
- ESE 1500 (CIS 2400)
  - Gates, Boolean logic, DeMorgan's, gate optimization, K-maps
  - Review: book chapter in Canvas
- ESE 2150
  - RLC circuit analysis
  - Review: 2150 lectures posted in Canvas
- Diagnostic Quiz on Canvas
  - Not graded, weighted as a homework assignment
  - Complete by Friday 1/26 midnight
  - 1500 and 2150 review materials in Canvas Files section

Course Structure: Websites

- Website (http://www.seas.upenn.edu/~ese3700/)
  - Course calendar is used for all handouts (preclass, lecture slides, assignments, and readings)
  - Canvas/Gradescope used for assignment submission, and grades
  - Ed Discussion used for announcements and discussions

Course Structure: Lectures

- MW 1:45pm-3:14pm Lecture in Towne 307
  - Preclass and lecture slides posted online before class
- Readings from textbook
- 2 lecture periods → Labs in Detkin

ESE3700 Spring 2024 Working Schedule

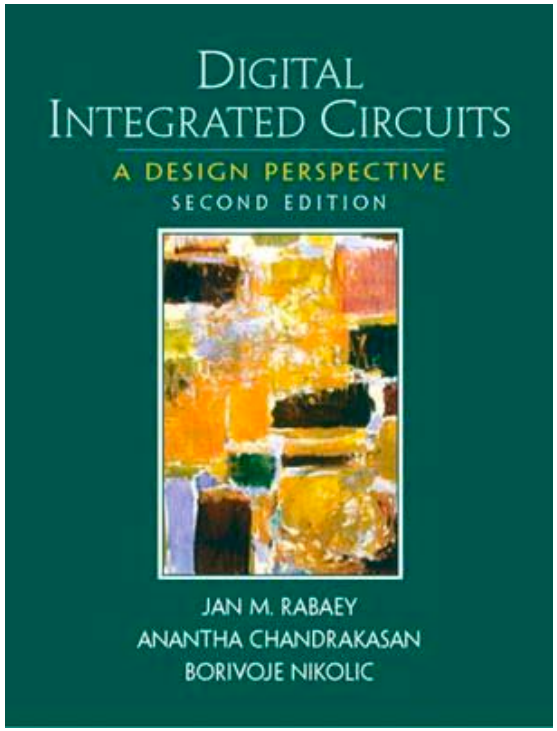
Wk	Lect.	Date		Lecture	Slides	Due	Reading
2		1/22	M	Intro/Overview	[lec1]		1 through 1.2; review course web page completely
	2	1/24	W	Transistor Introduction (basics) and Gates from Transistors			review ESE215; 6.2 through static properties in 6.2.1
		1/26	F			Diagnostics Quiz (canvas)	
3		1/29	M	Lab 1 (Detkin): Gate from Discrete Transistors			
	3	1/31	W	Transistor Introduction (first order), Delay and RC Response		ADD DATE	3.1, 1.3.3
		2/2	F			HW 1	
4	4	2/5	M	Regenerative Property			1.3.2
	5	2/7	W	MOS Intro, Transistor Operating Regions: Part 1			2.1-2.3, 3.3.1-3.3.2 (page 92)
		2/9	F			HW 2	
5	6	2/12	M	MOS Transistor Operating Regions: Part 2, Parasitics			3.3.2 (remainder)
	7	2/14	W	Layout and Area, MOS Scaling			2.3, 3.5
		2/16	F			HW 3	
6	8	2/19	M	MOS Variation			3.3.3, 3.4
		2/21	W	Midterm 1 (during class)			

Course Structure: Lectures

- No recordings. I expect you to be in lecture.
- Statistically and empirically speaking, you will do better if you come to lecture
- Better if interactive, **everyone** engaged
  - Asking and answering questions
  - Actively thinking about material every day
- Two things
  - Preclass worksheet exercises
    - Primes you for topic of the day
    - Will be addressed during lecture
  - Ask questions of individuals

Course Structure: Textbook

- Textbook
  - *Digital Integrated Circuits, A Design Perspective*, Jan M. Rabaey, Anantha Chandrakasan, and Borivoje Nikolic, 2nd edition
    - Great reference text with great detail
    - REALLY!! useful for projects



Course Structure: SPICE

- Simulation Program with Integrated Circuit Emphasis
  - Industry standard analog circuit simulator
  - Non-linear, differential equation solver specialized for circuits
- Integrated circuits – simply impractical to build to debug
  - Must simulate to optimize/validate design

Course Structure: Assignments/Exams

- Homework – week long (6 total) [25%]
  - Due (mostly) F at midnight
  - Submit in Canvas/Gradescope
- Projects – 2-3 weeks long (2 total) [30%]
  - Design/Simulation oriented
  - On two main topics
    - 1: Computation - Solo
    - 2: Memory – Team of 2
      - Milestone Turn-in for feedback
- Midterms [25%] (2 total)
  - In class
- Final exam [20%]

Course Structure: Admin

- Use course calendar
  - Lectures and preclass online before class
    - Will post night before class
    - Reserve the right to change them (usually minor)
  - Homework/projects linked
    - Homework 1 out now
  - Reading for whole term specified
- Take notes!
  - Especially on the examples we do in class
  - Slides have a lot of questions – not a lot of answers

Course Policies

See course web page for full details

- Turn assignments in on Canvas/Gradescope
  - Anything handwritten/drawn must be clearly legible
    - No handwritten work allowed on projects
  - Submit CAD generated figures, graphs, results when specified
  - Late Policy – allowed **5 late days** for whole semester
    - Can only use a max of three days on each project
    - Allowed late days (D) for group projects
      - If max (Student 1, Student 2) ≤ 3, D= max (Student 1, Student 2)
      - If max (Student 1, Student 2) > 3, D=3
- Individual work (HW & Project*)
  - CAD drawings, simulations, analysis, writeups
  - May discuss strategies, but acknowledge help

Course Content

- Logic (Computation) [11 weeks]
  - Combinational logic
  - Sequential logic
- Memory/Storage [2 weeks]
- Communication/Interconnect [2 weeks]

Course Content (con't)

- Logic
  - Transistors → Gates
  - **Lab:** build gate, measure delay
  - Regeneration (noise margins)
  - Delay
  - Area (no layout → ESE370)
  - Energy
  - Synchronous (flip-flops, clocking, dynamic)
  - **Project 1:** fast ripple-carry adder

Course Content (con't)

- Memory/Storage
  - No Lab component
  - RAM Organization
    - Memory cells and periphery circuits
  - Driving Large Capacitances
  - Signal amplification/regeneration
  - **Project 2:** design a SRAM

Course Content (con't)

- Communication/Interconnect
  - Noise
    - Crosstalk
    - Inductive
    - Ionizing particles, shot
  - Transmission Lines
  - **Lab:** Cable noise and PCB trace T-line behaviour
    - Measure inductive ground bounce, crosstalk
    - Experiment with PCB transmissions lines, termination

Ed Discussion Posting Policy

- All posts must be in accordance with the collaboration policy
- Search if your questions has been asked already
- Posts about labs and projects must include a *good faith* attempt at the answer
  - What have you tried so far?
- Exact values of your results should not be posted (use orders of magnitude)
- Posts against these rules may not be answered and may be removed
- If in doubt, post privately to instructors

Advice

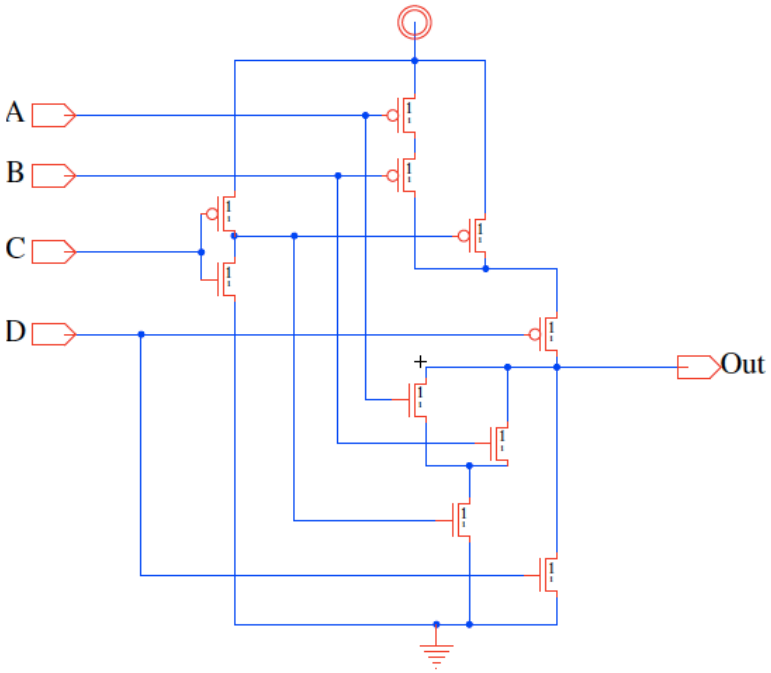
- Course is hard (but valuable)
- Should be thinking about this material every day
- Go to office hours
- MUST READ TEXT!
- Learning is spread over all components
  - Lecture, reading, **homework, projects**, exams
- Cannot pass the class if you don't turn in projects
  - Give yourself enough time. They will take you longer than you think

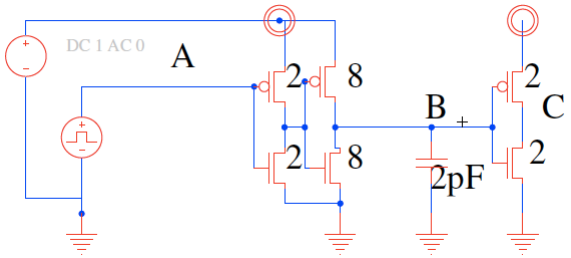
Advice from your fellow students:

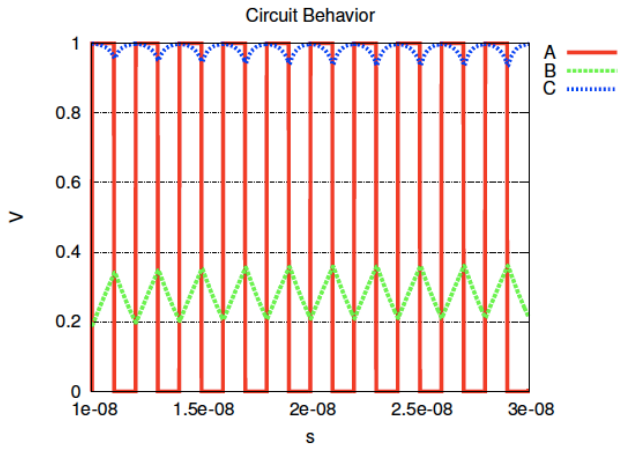
- Q: As a current or former student that did very well in ESE 3700, what advice do you have for future students to be successful in ESE 3700?
  - "The most important thing for me was to **attend lecture**"
  - "make sure you **start early** on the projects"
  - "ESE 3700 is a class that **moves quickly**… best ways to stay abreast of the material was to engage with it … **ask questions and engage** in conversation in class (or in office hours) regularly"
  - "ESE 3700 is a very **rewarding class, but not an easy class**. The biggest advice I can offer is to **stay on top of the work**."
  - "will be both very **challenging and rewarding**, and quite **unique compared to other classes at Penn**"
- See course webpage for full answers

Big Ideas

- Model (a.k.a. analysis and simulation) to enable real-life robust IC design and optimization







Grace Hopper Lecture

- Thursday 3-4pm in Glandt Forum (Singh Center)

ESE Grace Hopper Lecture – "Disrupting NextG"

January 25 at 3:00 PM - 4:00 PM

As 5G takes to the airwaves, we now turn our imagination to the next generation of wireless technology. The promise of this technology has created an international race to innovate, with significant investment by government as well as industry. And much innovation is needed as 6G aspires to not only support significantly higher data rates than 5G, but also improved reliability along with excellent coverage indoors and out, including for underserved areas. New architectures including edge computing must be designed to drastically enhance efficient resource allocation while also reducing latency for real-time control. Breakthrough energy-efficiency architectures, algorithms and hardware will be needed so that wireless devices can be powered by tiny batteries, energy-harvesting, or over-the-air power transfer. And machine learning may will play a big role in the underlying technologies for NextG as well as the "killer apps" that will drive its deployment and success. This talk will describe what the wireless future might look like along with some of the innovations and breakthroughs required to realize this vision.

Andrea Goldsmith
Dean of the School of Engineering and Applied Science & The Arthur LeGrand Doty Professor of Electrical and Computer Engineering, Princeton University

Andrea Goldsmith is the Dean of Engineering and Applied Science and the Arthur LeGrand Doty Professor of Electrical and Computer Engineering at Princeton University. She was previously the Stephen Harris Professor of Engineering and Professor of Electrical Engineering at Stanford University, where she is now Harris Professor Emerita. Her research interests are in information theory, communication theory, and signal processing, and their application to wireless communications, interconnected systems, and biomedical devices. She founded and served as Chief Technical Officer of Plume WiFi (formerly Accelera, Inc.) and of Quantenna (QTNA), Inc, and she serves on the Board of Directors for Intel (INTC), Medtronic (MDT), Crown Castle Inc (CCI), and the Marconi Society. She also serves on the Presidential Council of Advisors on Science and Technology (PCAST). Dr. Goldsmith is a

https://events.seas.upenn.edu/event/ese-grace-hopper-lecture-title-tbd/

Admin

- Find web, get text, assigned reading…
  - http://www.seas.upenn.edu/~ese3700
  - https://canvas.upenn.edu/courses/
  - https://edstem.org/us/courses/53825/discussion/
- To do:
  - Check your access to Canvas and Ed Discussion
  - Diagnostic Quiz (in Canvas) – due by F 1/26
    - Review as needed
  - HW 1 out now – due F 2/2
    - Need lab and future lectures to finish

Acknowledgement

- Prof. André DeHon (University of Pennsylvania)
- Prof. Jing Li (University of Pennsylvania)