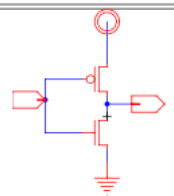
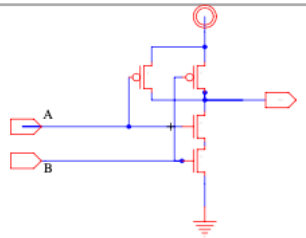
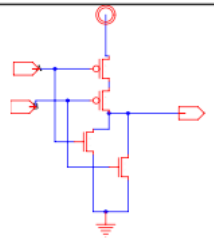
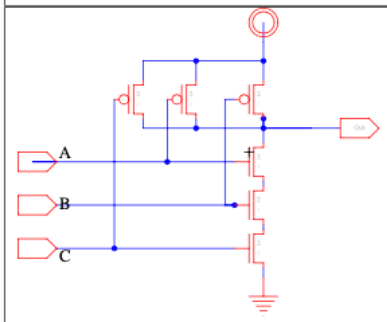
ESE3700: Circuit-Level Modeling, Design and Optimization for Digital Systems

Lec 10: February 28, 2024

Energy and Power Basics

Reminder: Sized with drive $\frac{R_0}{2}$

	$R_{p0} = R_{n0}$			$R_{p0} = 2R_{n0}$		
	W_p	W_n	C_a	W_p	W_n	C_a
	2	2	$4C_0$	4	2	$6C_0$
	2	4	$6C_0$	4	4	$8C_0$
	4	2	$6C_0$	8	2	$10C_0$
	2	6	$8C_0$	4	6	$10C_0$

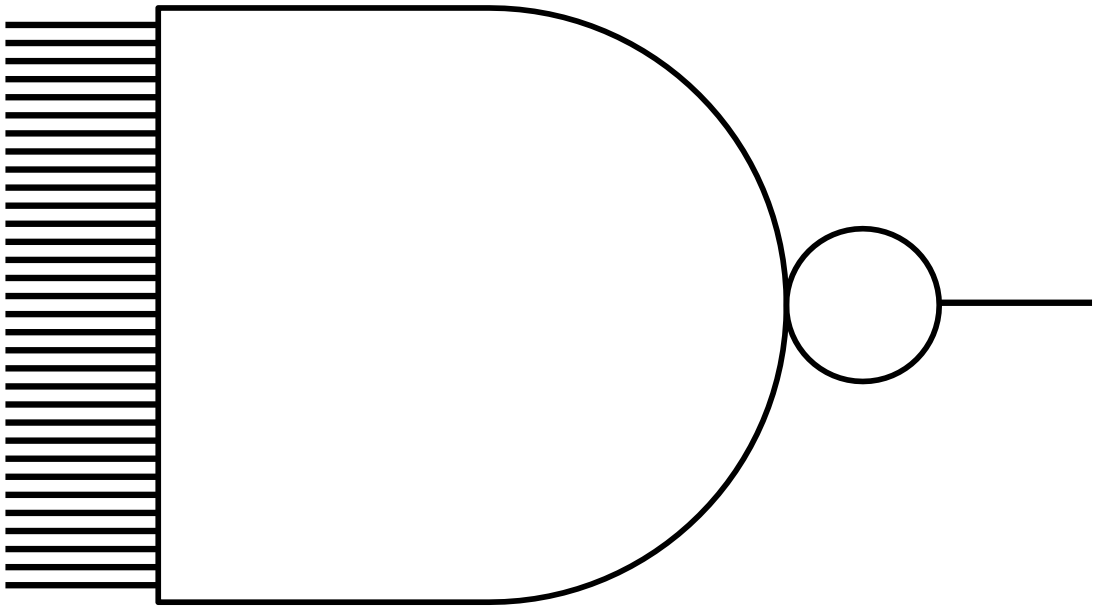
For k-input nand gate with drive $\frac{R_0}{2}$

	$R_{p0} = R_{n0}$	$R_{p0} = 2R_{n0}$
What is C_{in} as a function of k?	$(2+2k)C_0$	$(4+2k)C_0$

nand32 (preclass 1, row 1)

- single-stage nand32
  - Delay with $R_0/2$ input drive and $4C_0$ load?

$R_{n0}=R_{p0}$ case only



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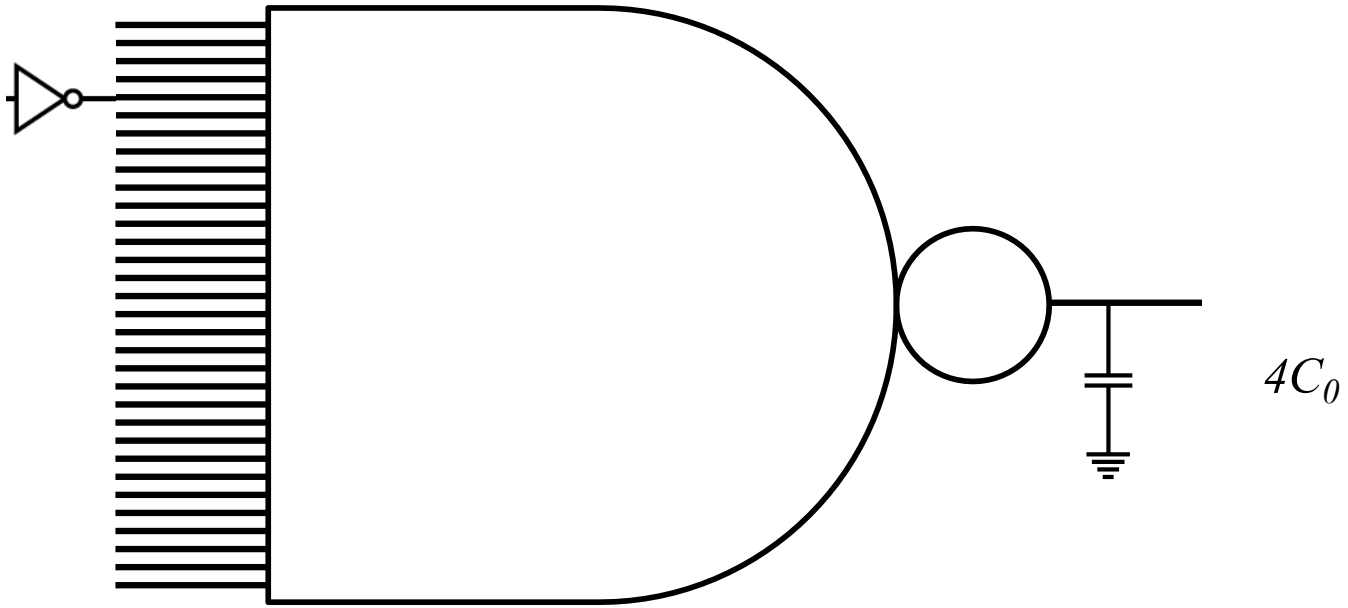

Which is Faster? (preclass 1, rows 2&3)

- nand32

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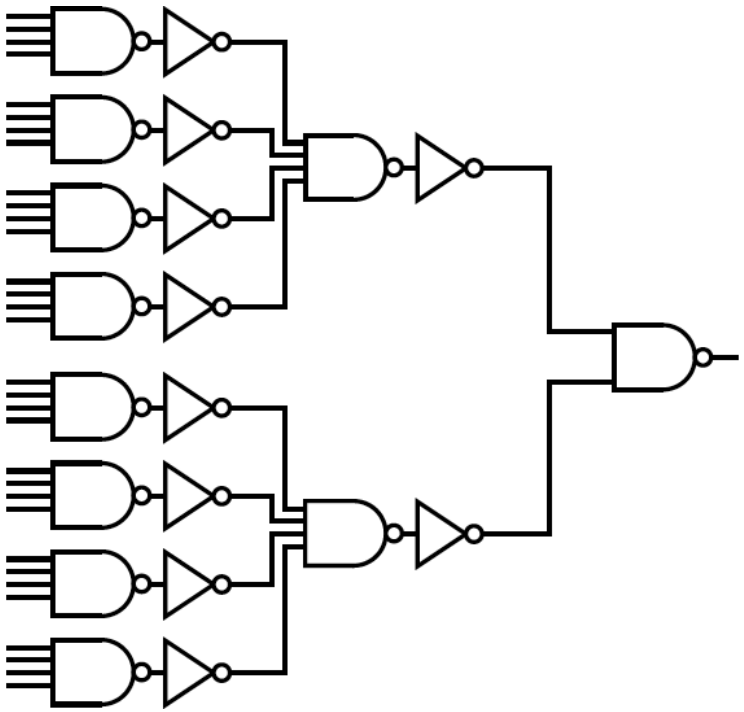
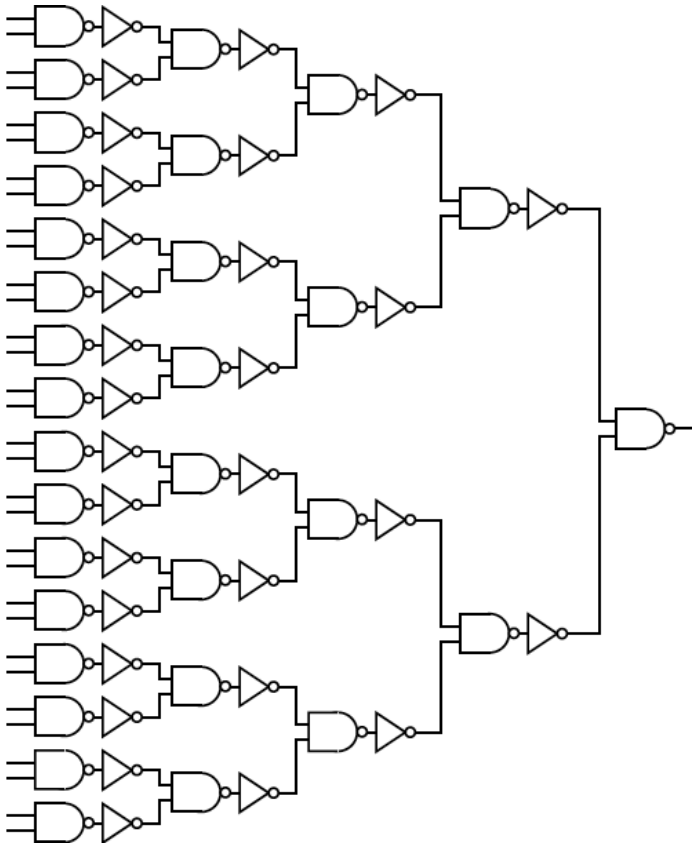


nand4-inv-nand4-inv-nand2

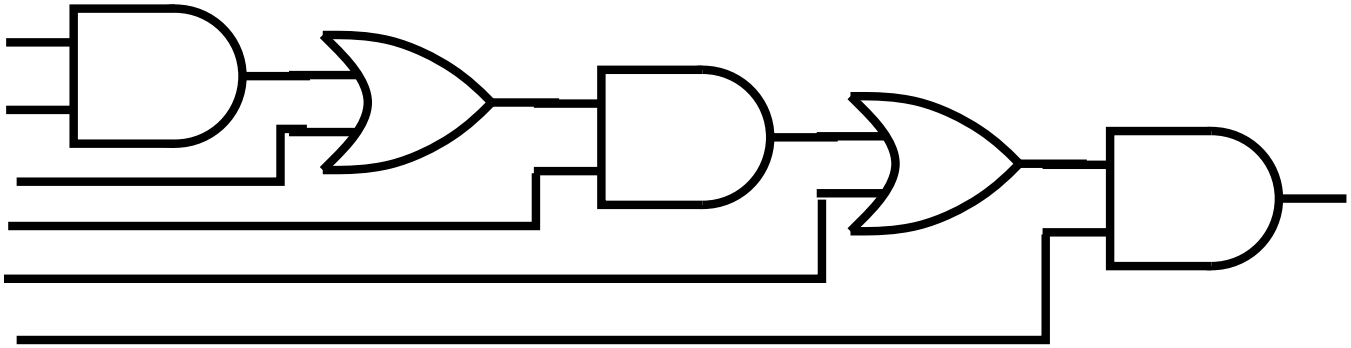


$(\text{nand2-inv})^4\text{-nand2}$

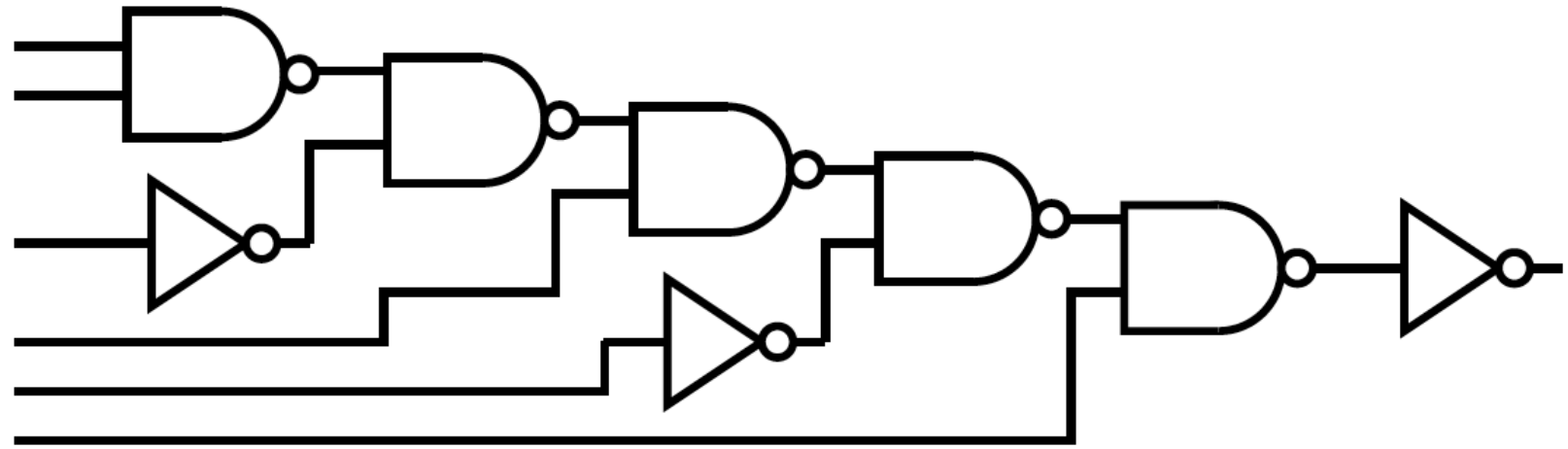
Lesson

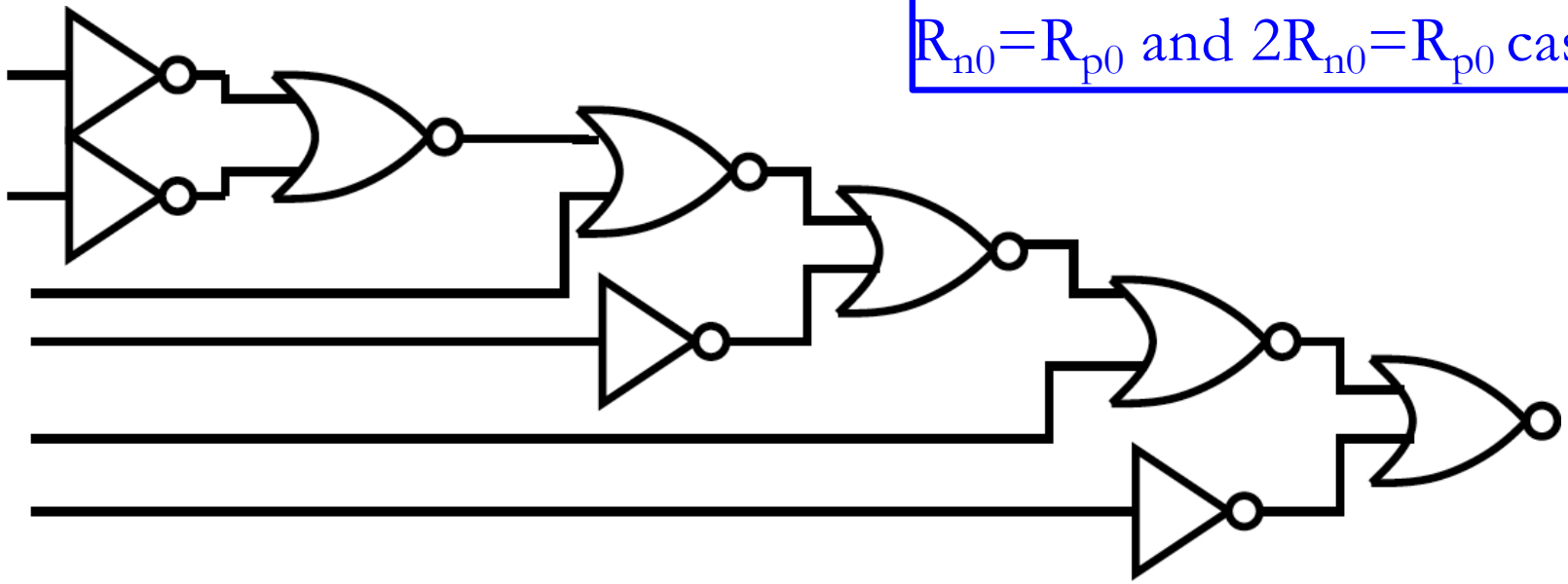
- Large gates are slow / inefficient
  - High capacitive load / drive current
- Small gates can be inefficient
  - Need many stages
- Staging over moderate size gates minimizes delay
- Exact size will be technology dependent

And-Or Chain



Delay of each implementation? (preclass 2)

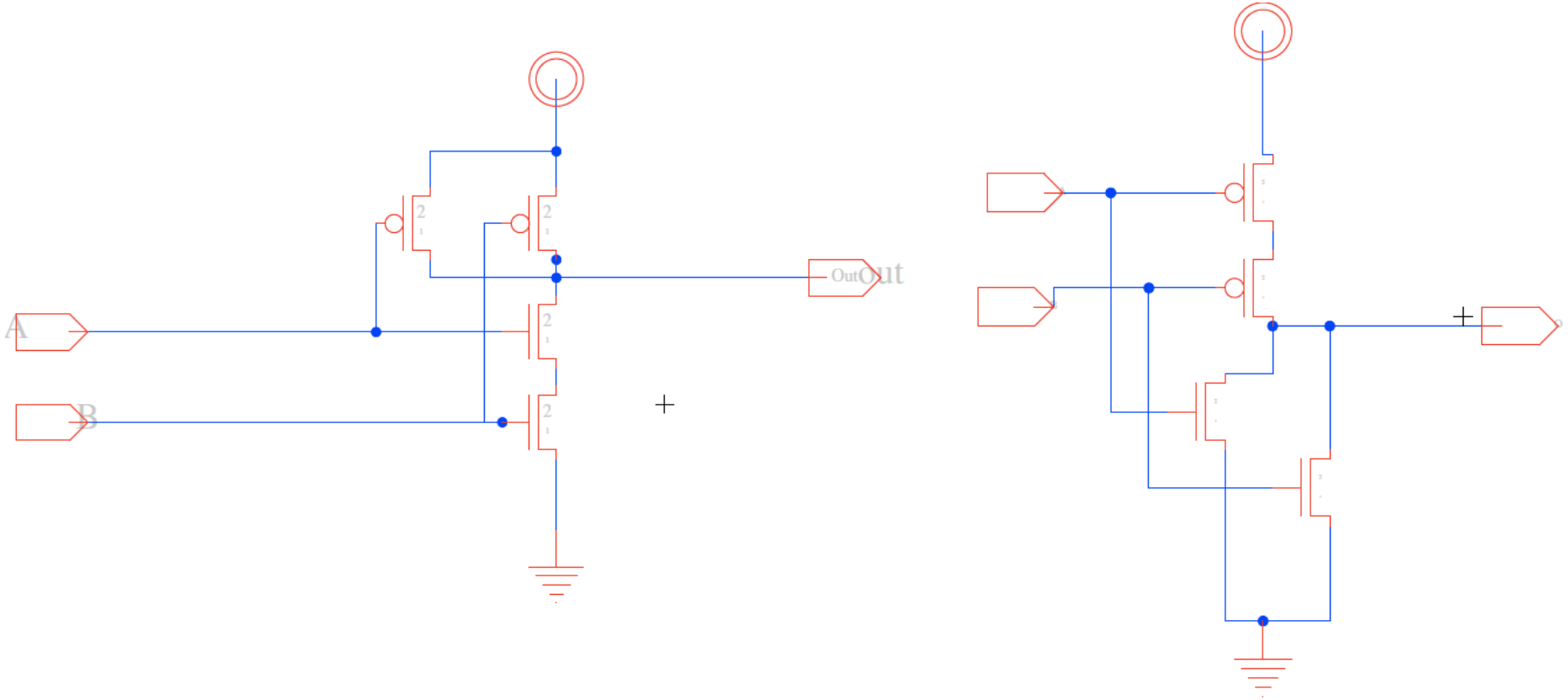




$R_{n0}=R_{p0}$ and $2R_{n0}=R_{p0}$ cases

Take Away?

- nor vs. nand



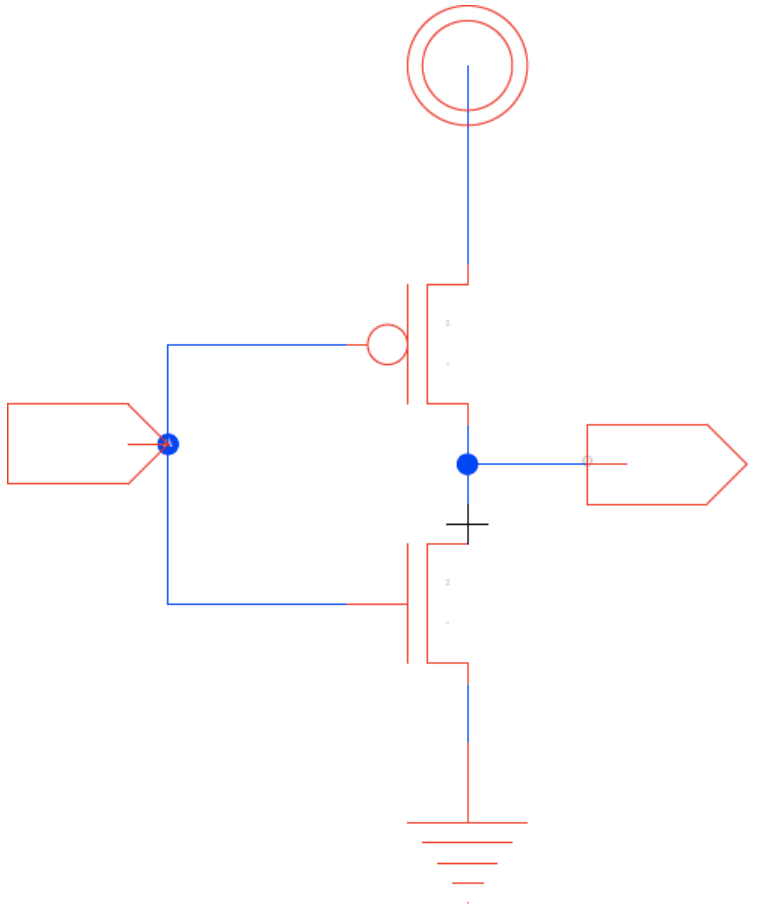
Today

- Power Sources
  - Static power
  - Switching power
    - Dynamic switching power
    - Short circuit power (if time)

Power

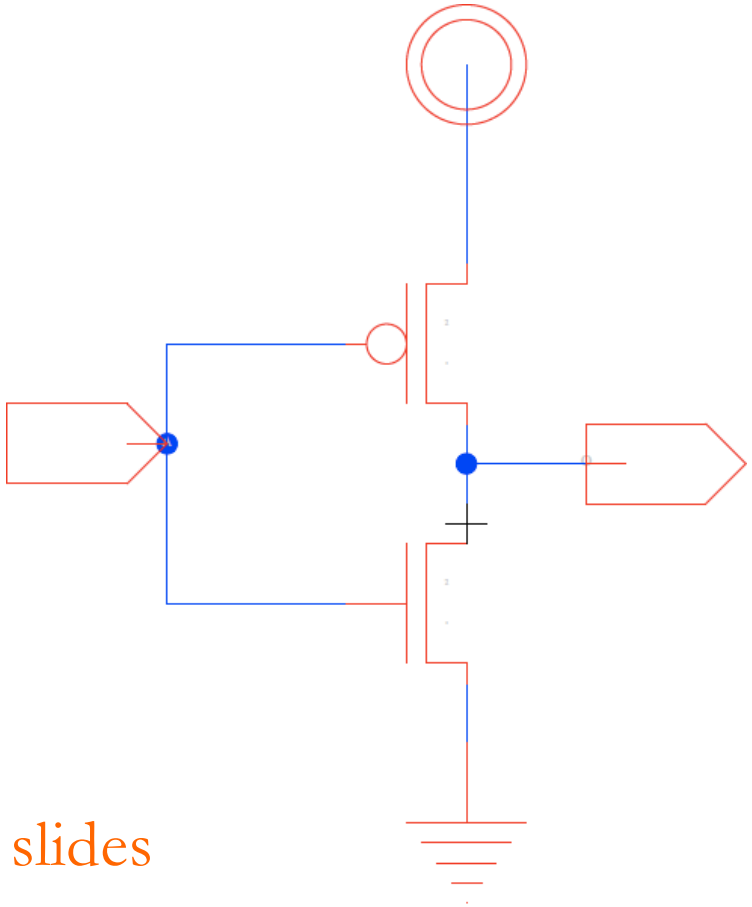
- $P = I \times V$

- Tricky part:
  - Understanding I
  - (pairing with correct V)



Inverter Current Simplification (preclass 3)

- What is $I_{pwr,gnd}$?
  - 0V
  - 140mV
  - 400mV
  - 500mV
  - 600mV
  - 860mV
  - 1V

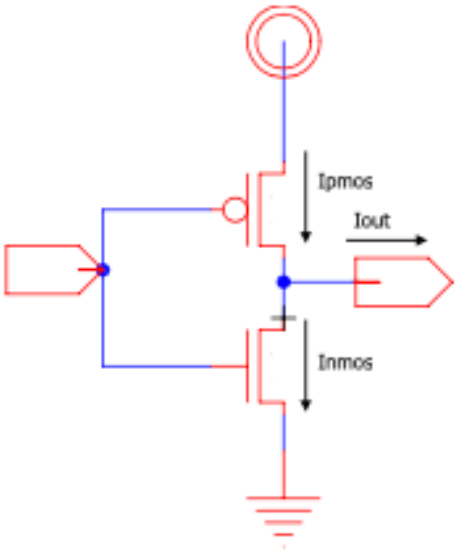


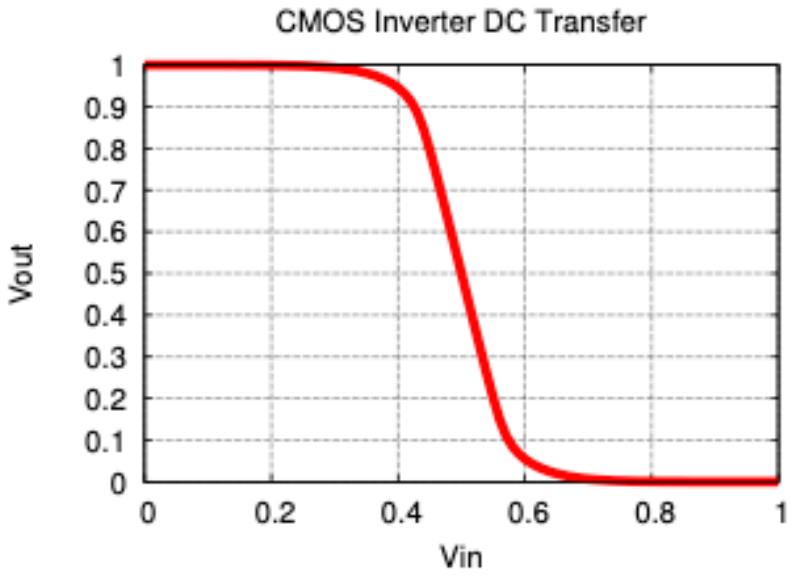
  - From preclass – see next two slides

Preclass 3

Device	V_{gs}	I_d
NMOS	$V_{gs} < V_{thn}$	$(3 \times 10^{-7})\, e^{\frac{V_{gs}-V_{thn}}{40mV}}$
	$V_{gs} > V_{thn}$	$1.8 \times 10^{-4}\,(V_{gs} - V_{thn})$
PMOS	$V_{gs} > V_{thp}$	$(3 \times 10^{-7})\, e^{-\left(\frac{V_{gs}-V_{thp}}{40mV}\right)}$
	$V_{gs} < V_{thp}$	$-1.8 \times 10^{-4}\,(V_{gs} - V_{thp})$

Consider an inverter:





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1. V_{dd}=1V, V_{thn}=300mV, V_{thp}=-300mV, assume steady-state operation at V_{in} given.

V_{in}	I_{pmos}	I_{nmos}	$\approx I_{pwr,gnd}$	
0V				A
140mV				B
400mV				C
500mV				D
600mV				E
860mV				F
1V				G

Approximate $I_{pwr,gnd} \approx \min(I_{nmos}, I_{pmos})$.

Useful: $e^{-1} \approx 0.37$, $e^{-4} \approx 0.02$, $e^{-7.5} \approx 6 \times 10^{-4}$,

Preclass 3

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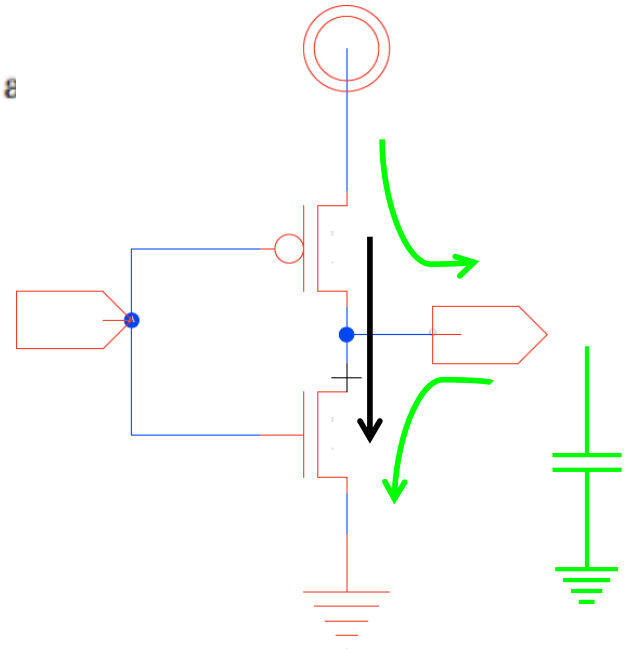

Preclass 4

Device	V_{gs}	V_{ds}	I_d
NMOS	$V_{gs} < V_{thn}$	any	$(3 \times 10^{-7})\, e^{\frac{V_{gs}-V_{thn}}{40mV}}$
	$V_{gs} > V_{thn}$	$V_{ds} < V_{gs} - V_{thn}$	$3.6 \times 10^{-4}\,(V_{gs} - V_{thn}) \times V_{ds}$
		$V_{ds} > V_{gs} - V_{thn}$	$1.8 \times 10^{-4}\,(V_{gs} - V_{thn})$
PMOS	$V_{gs} > V_{thp}$	any	$(3 \times 10^{-7})\, e^{-\left(\frac{V_{gs}-V_{thp}}{40mV}\right)}$
	$V_{gs} < V_{thp}$	$V_{ds} > V_{gs} - V_{thp}$	$-3.6 \times 10^{-4}\,(V_{gs} - V_{thp}) \times V_{ds}$
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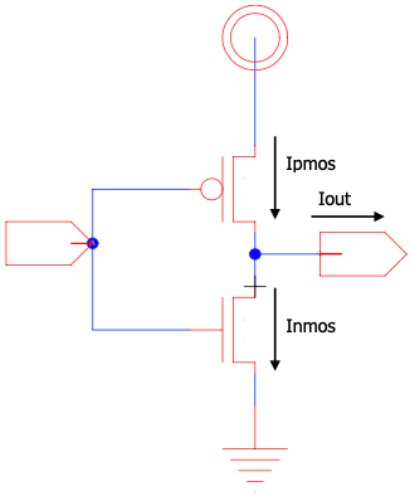
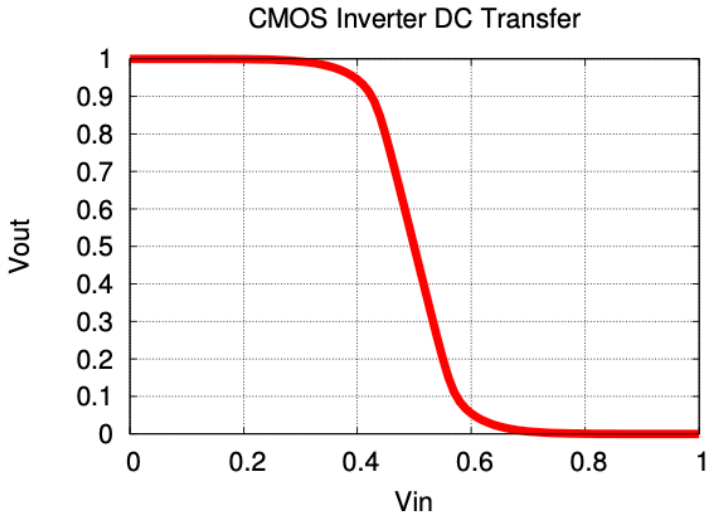
Consider an inverter:





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V_{in}	$I_{pmos} = I_{nmos} = I_{pwr,gnd}$	Vout	
0V			A
140mV			B
400mV			C
500mV			D
600mV			E
860mV			F
1V			G

Approximate $I_{pwr,gnd} \approx \min(I_{nmos}, I_{pmos})$.

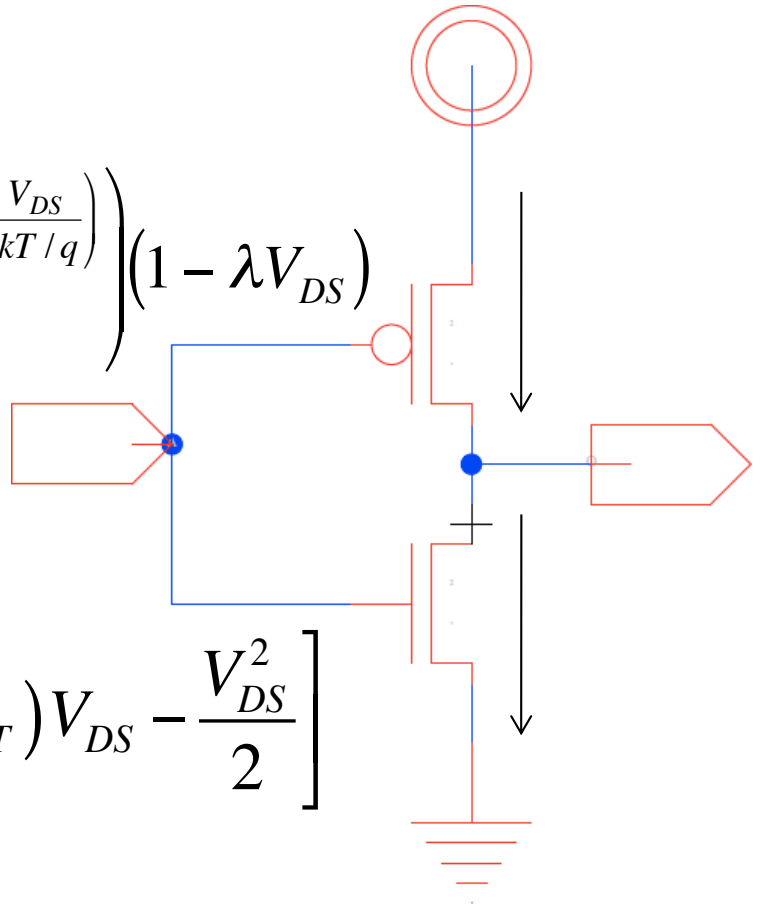
Understanding Currents

Static Power

Operating Modes

- Steady-State: $V_{in}=V_{dd}$
  - PMOS: subthreshold
  - NMOS: resistive

$$I_{DSp} = -I_S'\left(\frac{W}{L}\right)e^{-\left(\frac{V_{GS}-V_T}{nkT/q}\right)}\left(1-e^{\left(\frac{V_{DS}}{kT/q}\right)}\right)\left(1-\lambda V_{DS}\right)$$



$$I_{DSn} = \mu_n C_{OX}\left(\frac{W}{L}\right)\left[\left(V_{GS}-V_T\right)V_{DS}-\frac{V_{DS}^2}{2}\right]$$

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  - PMOS: subthreshold
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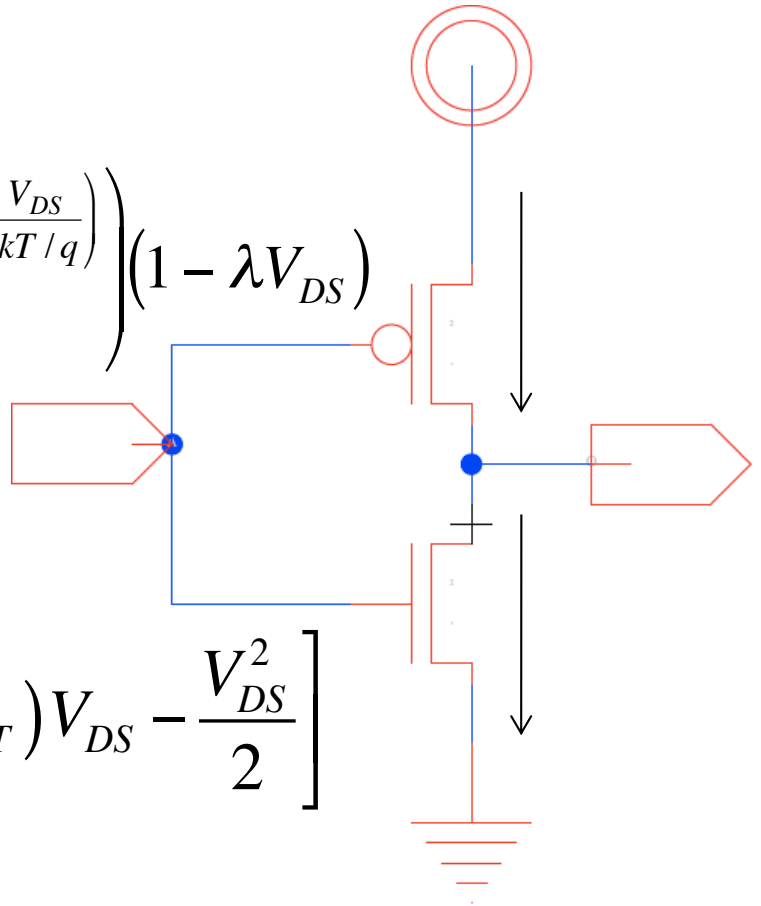
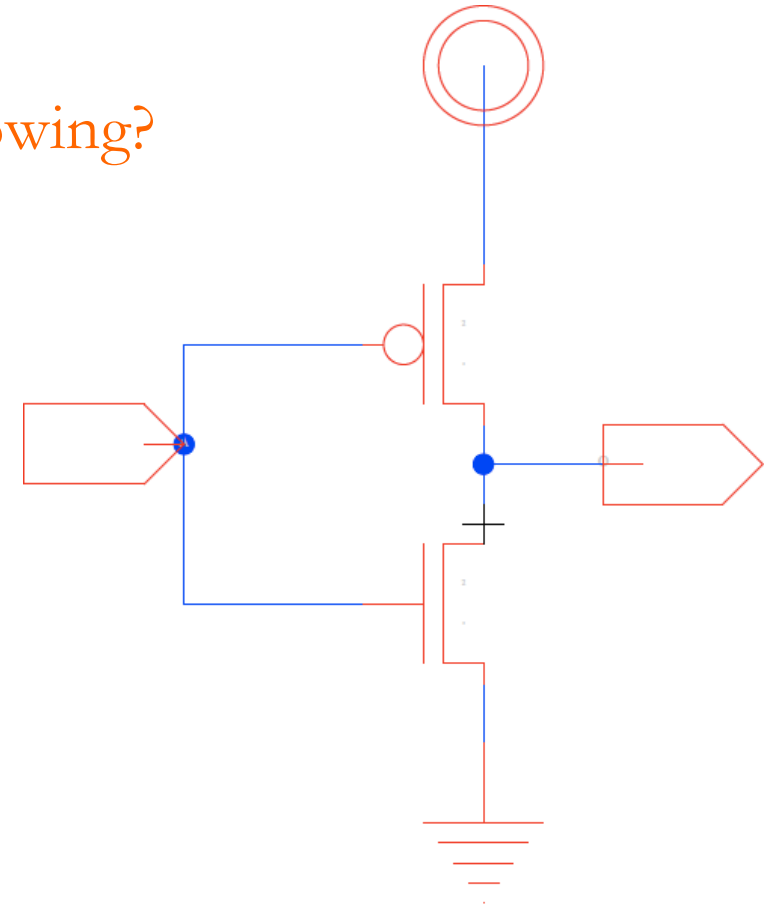


Which current determines I_{static} ?

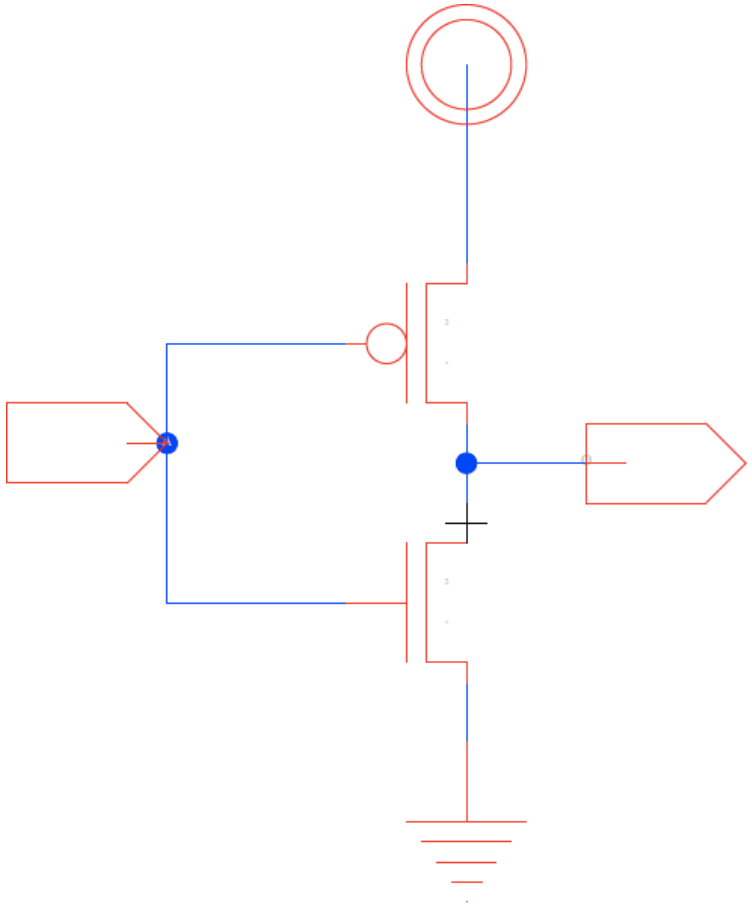
Static Power

- $P = I \times V$
- What V should we use?
  - Where is the static current flowing?



Data Dependent?

- How does the binary value of the input impact I_{static}?



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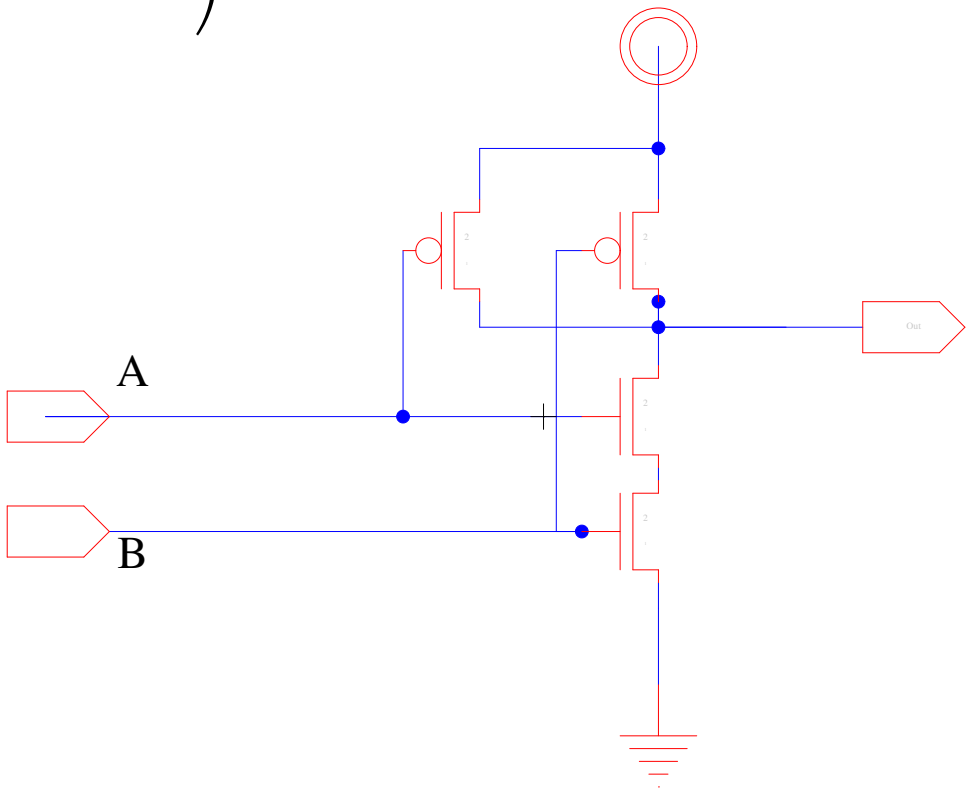

Data Dependent Leakage Current

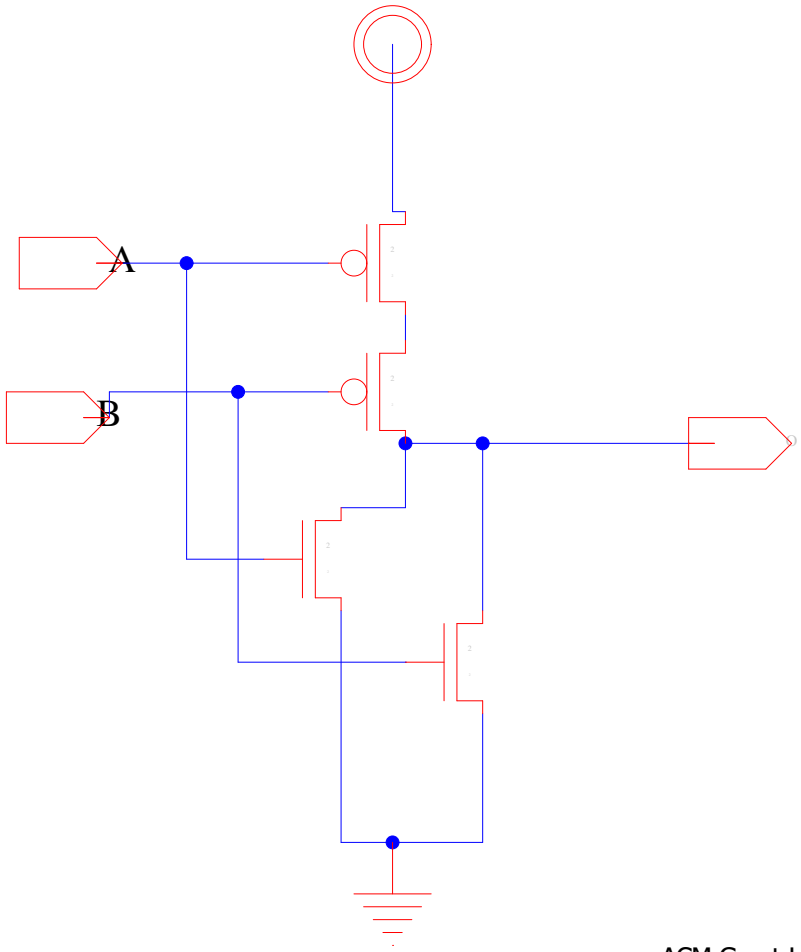

Table 1. Standard CMOS Gates Leakage Currents

	Temp °C	*0*	*25*	*50*	*75*	*100*
	Logic Lv.	Leakage Current (T°) [pA] @ 1,2 Vdd				
NOT	*0*	65,9	163,9	353,9	682,9	1203,9
	1	4, 4	10,4	23,5	49,0	93,3
NOR	*0 0*	131,9	327,7	707,9	1365,8	2405,7
	0 1	4, 4	10,4	23,5	48,1	90,1
	1 0	6,2	11,8	24,1	49,0	93,3
	1 1	2,3	4,4	9,3	19,3	37,4
NAND	*0 0*	9,4	24,5	57,5	120,9	231,2
	0 1	65,9	163,9	353,9	682,9	1202,8
	1 0	52,0	128,4	279,7	545,8	972,8
	1 1	8,8	20,7	47,1	98,0	186,6
XOR	*0 0*	258,7	640,8	1388,7	2692,5	4768,1
	0 1	154,5	383,4	836,0	1633,8	2916,9
	1 0	140, 6	347,9	761,8	1496,7	2686,9
	1 1	135,6	333,8	727,8	1424,7	2549,0

ACM Great Lakes Symposium on VLSI Stresa, I. (n.d.). Analysis of data dependence of leakage current in CMOS cryptographic hardware. In GLSVLSI '07 proceedings of the 2007 ACM Great Lakes Symposium on VLSI : Stresa - Lago Maggiore, Italy, March 11-13, 2007 /. New York, N.Y. :: Association for Computing Machinery. https://doi.org/10.1145/1228784.1228808

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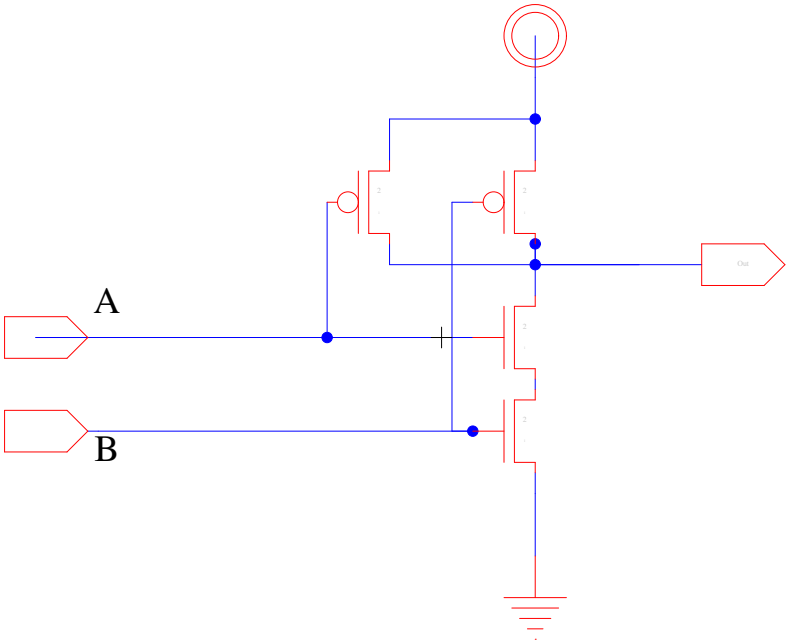

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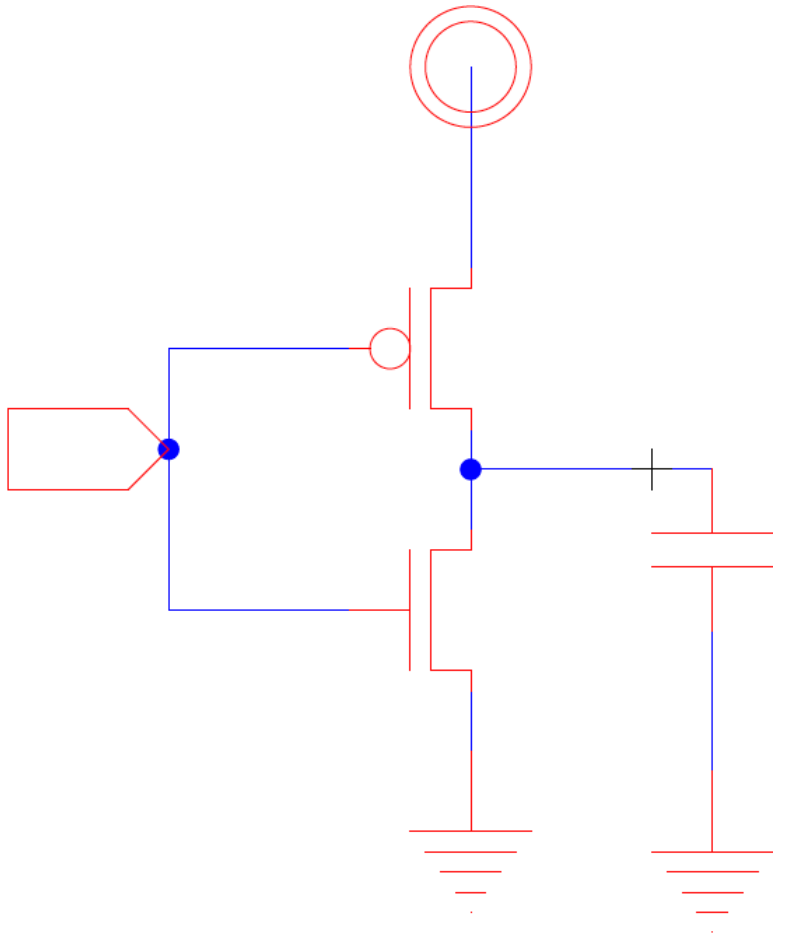
Understanding Currents

Dynamic Switching Currents

Power: During Switching

- $P = IV$
- Input switch: 1→0
- Where does I go?
  - V_{in}=Gnd



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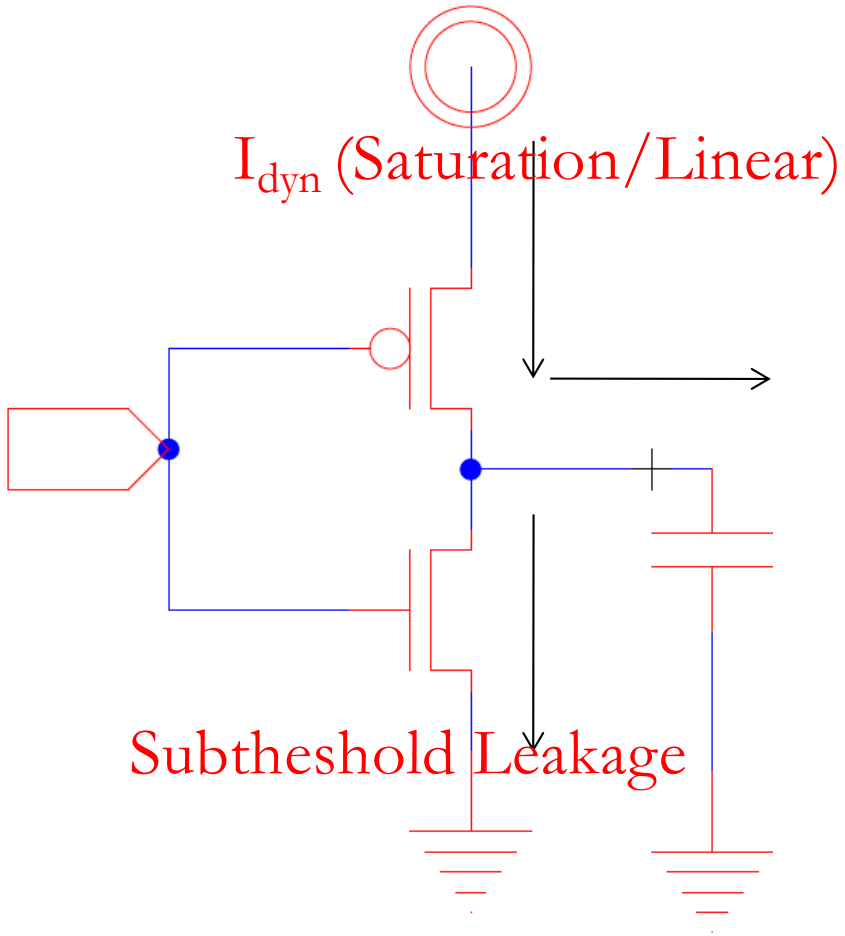
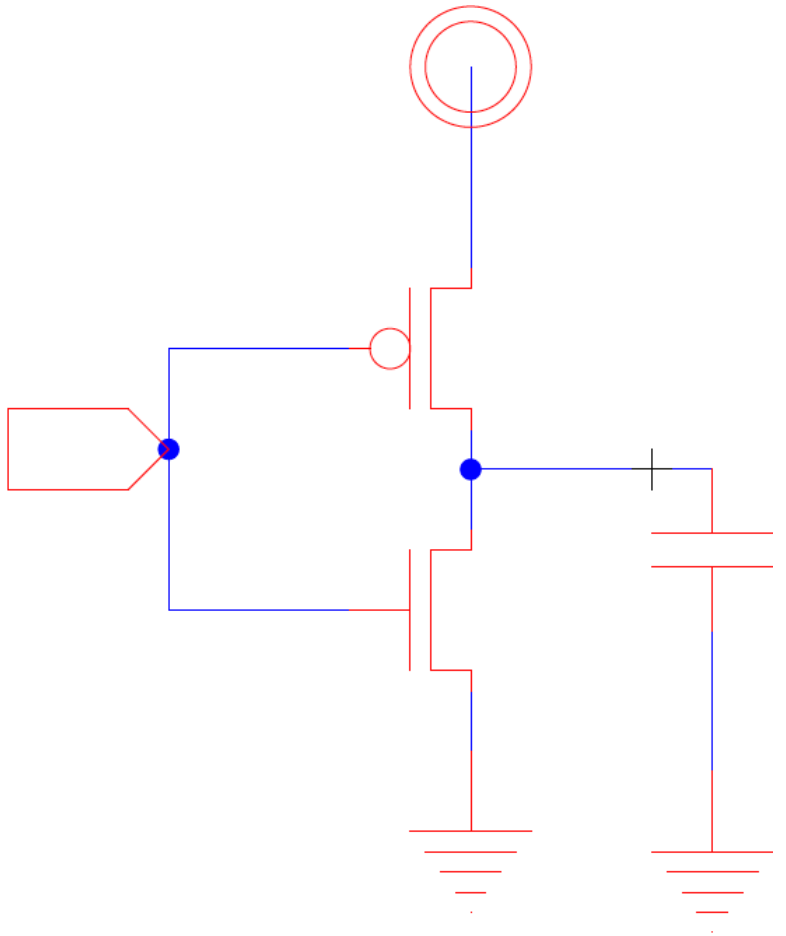


Power: During Switching

- $P = IV$
- Input switch 0→1
- Where does I go?
  - $V_{in}=V_{dd}$



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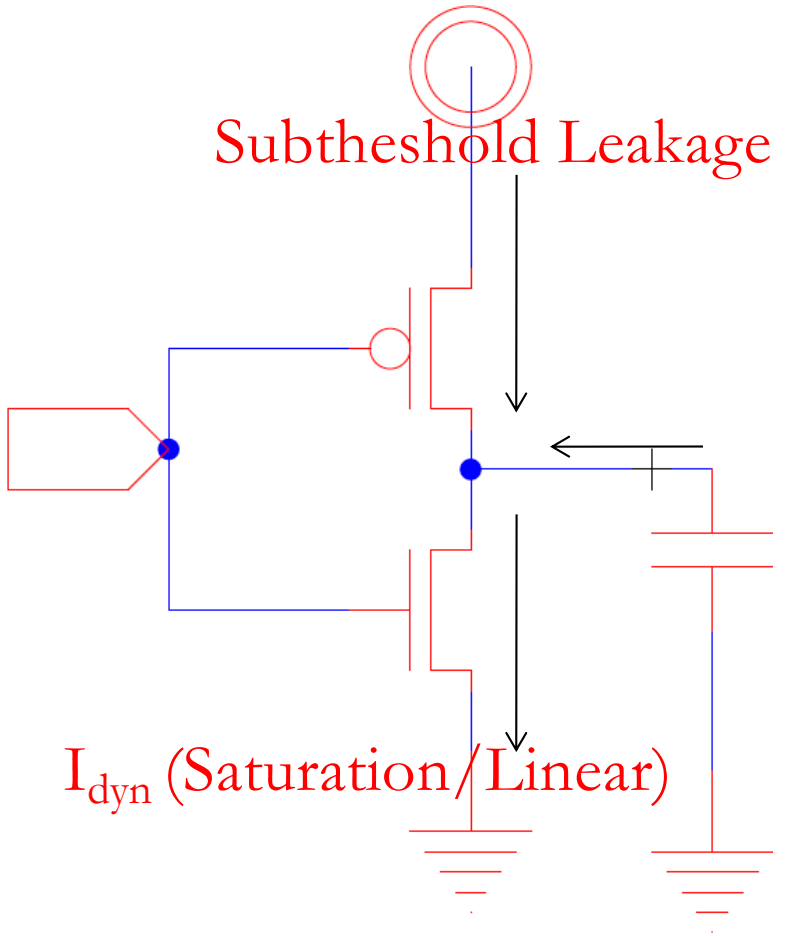
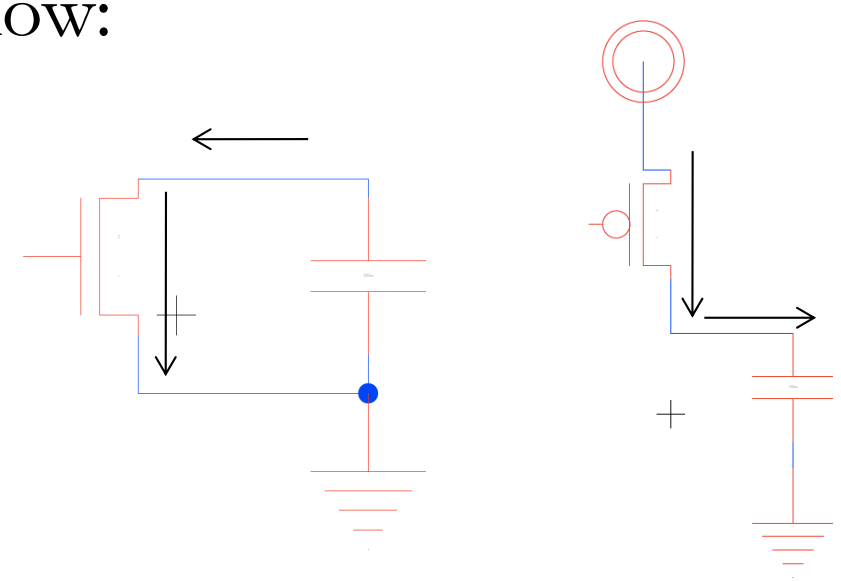


Switching Currents

- Dynamic current flow:

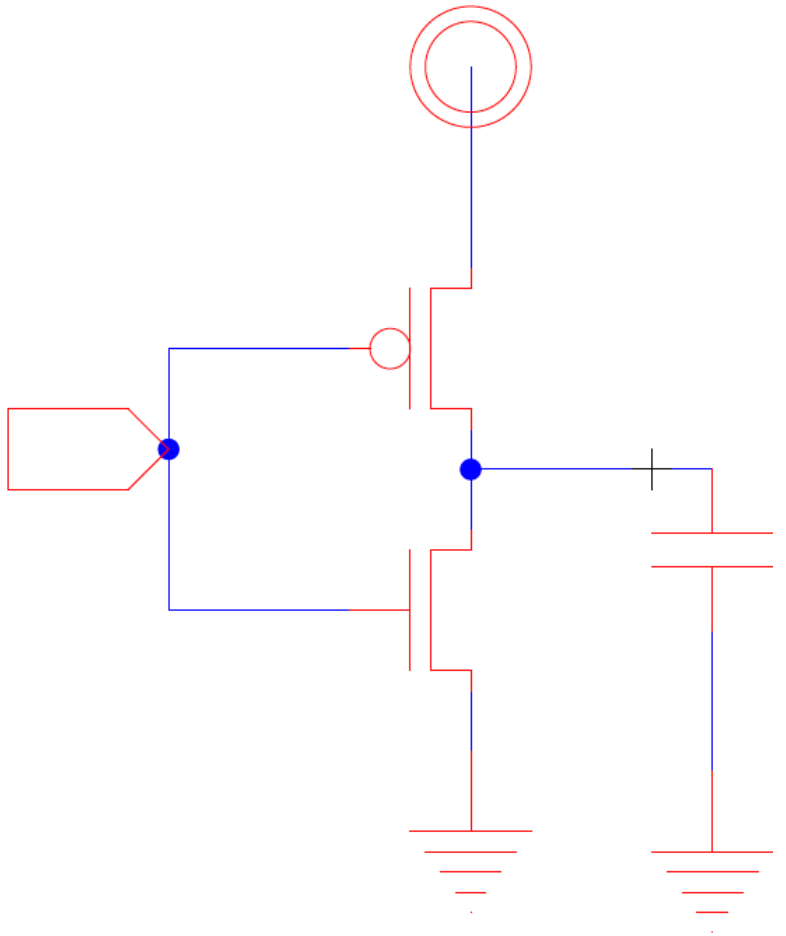


Understanding Currents

Short Circuit Currents

Power: During Switching

- $P = IV$
- Where does I go?
  - $V_{in}=V_{dd}/2$
    - And $V_{dd}>V_{thn}+|V_{thp}|$



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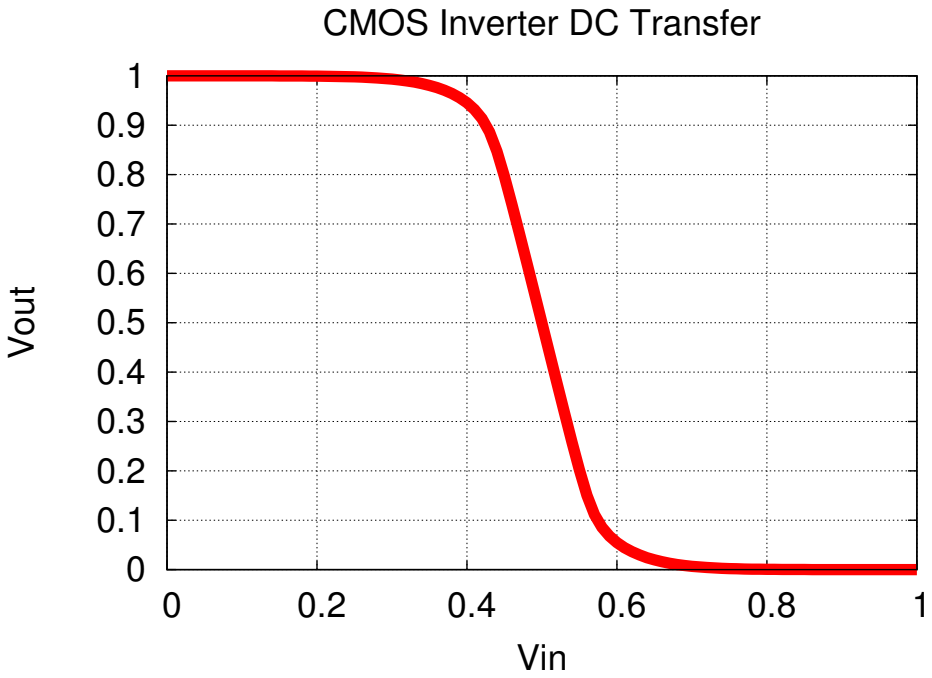
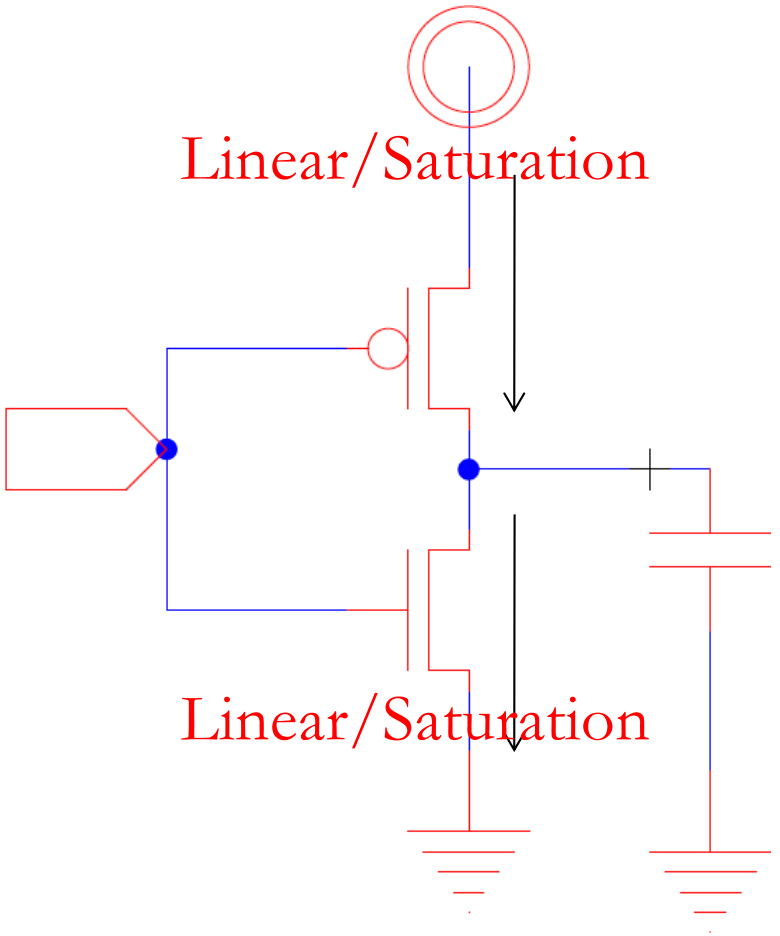
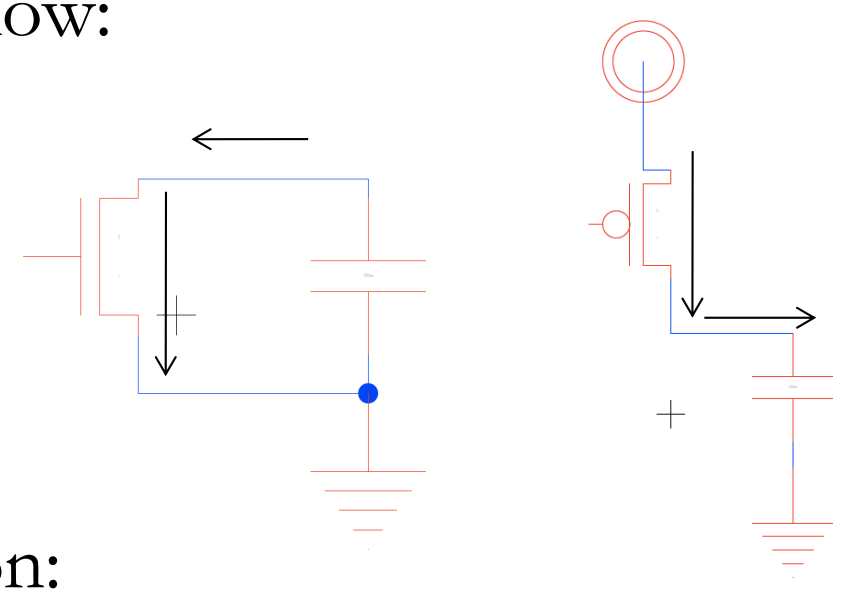


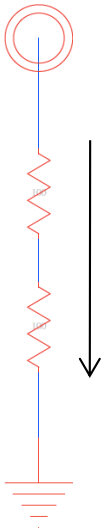


Switching Currents

- Dynamic current flow:

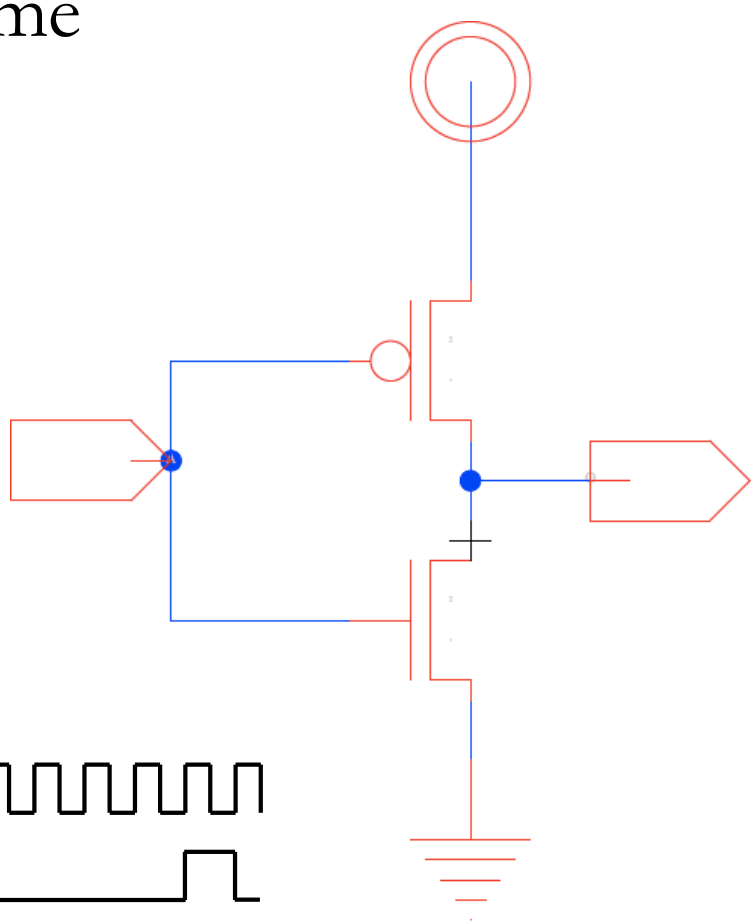


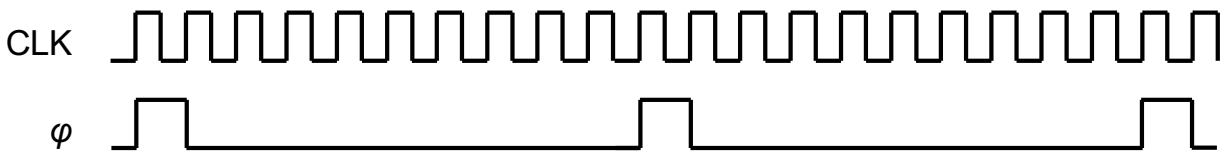
- If both transistor on:
  - Current path from V_{dd} to Gnd
  - Short circuit current



Currents Summary

- Current (I) changes over time
- At least two components
  - I_{static} – no switching
  - I_{switch} – when switching
    - I_{dyn} and I_{sc}



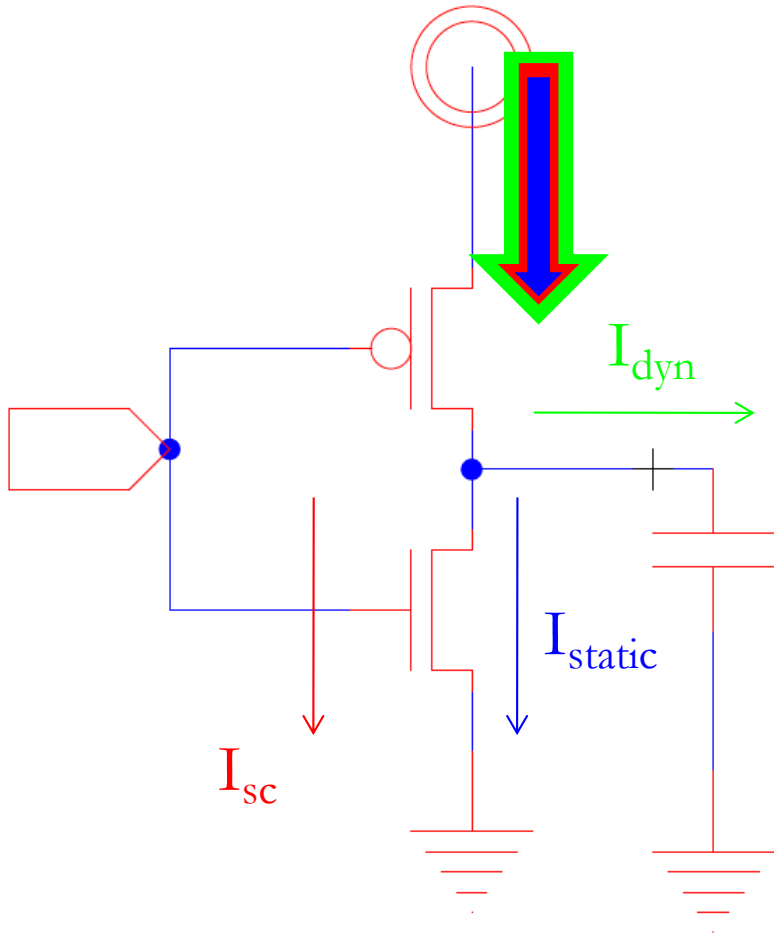


Switching

Dynamic Power

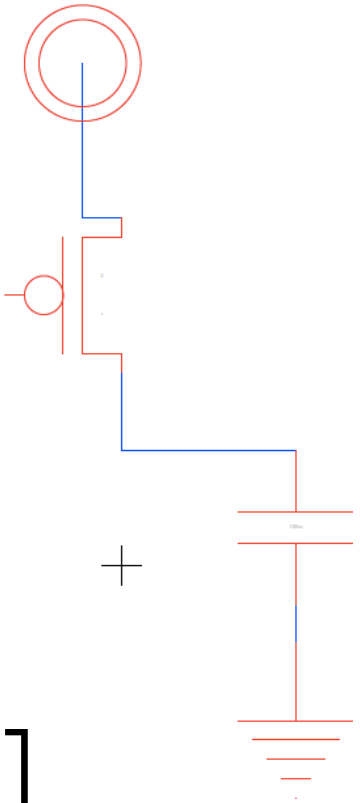
Switching Currents

- $I_{total}(t) = I_{static}(t) + I_{switch}(t)$
- $I_{switch}(t) = I_{sc}(t) + I_{dyn}(t)$



Charging

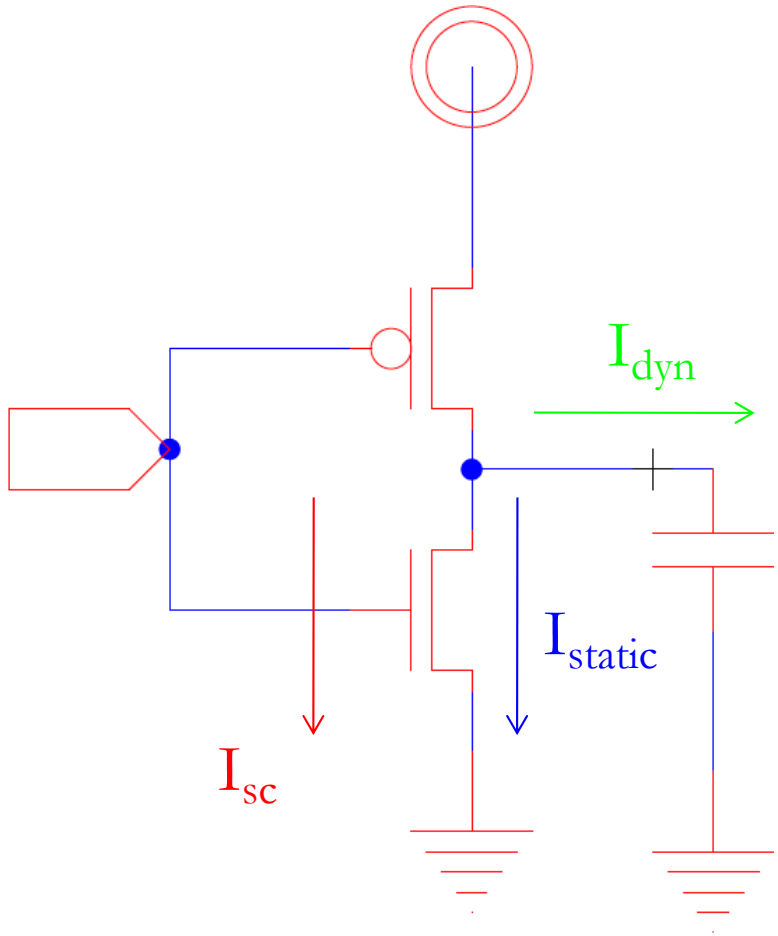
- $I_{dyn}(t)$ – why is it changing?
  - $I_{ds} = f(V_{ds}, V_{gs})$
  - and V_{gs}, V_{ds} changing



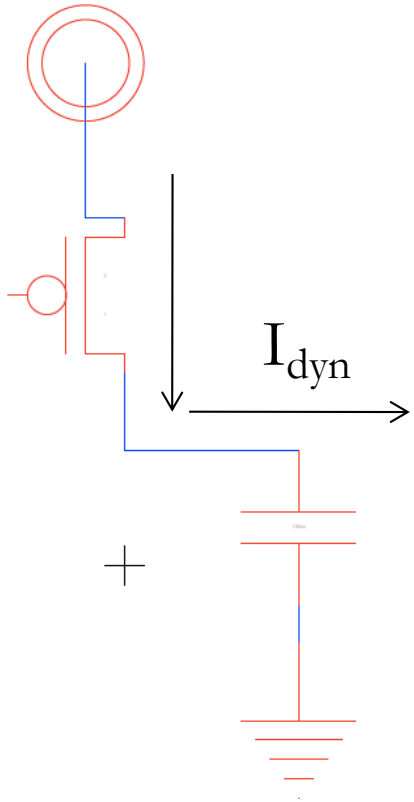
$$I_{DS} \approx \nu_{sat} C_{OX} W \left(V_{GS} - V_T - \frac{V_{DSAT}}{2} \right)$$

$$I_{DS} = \mu_n C_{OX} \left(\frac{W}{L} \right) \left[\left(V_{GS} - V_T \right) V_{DS} - \frac{V_{DS}^2}{2} \right]$$

Switching Energy – focus on $I_{dyn}(t)$



Switching Energy – focus on $I_{dyn}(t)$

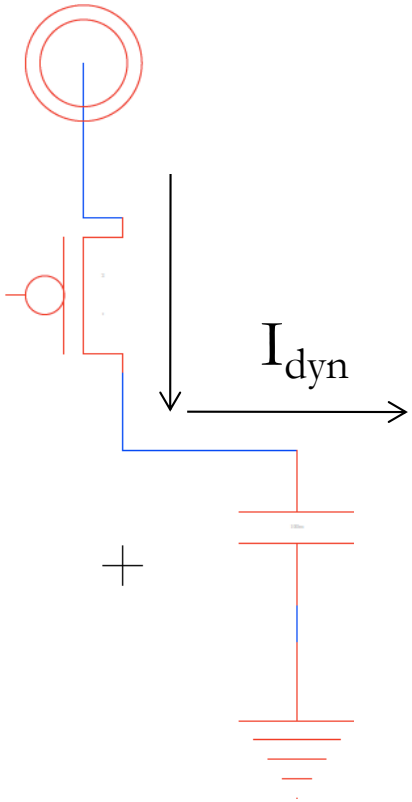


$$E = \int P(t)\,dt$$
$$= \int I(t)V_{dd}\,dt$$
$$= V_{dd}\int I(t)\,dt$$

Switching Energy

- Do we know what this is?

$$\int I_{dyn}(t)\,dt$$



$$E = \int P(t)\,dt$$

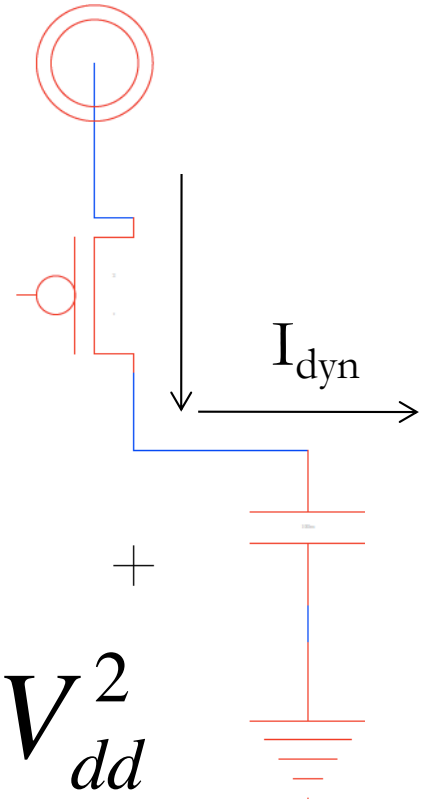
$$= \int I(t)V_{dd}\,dt$$

$$= V_{dd}\int I(t)\,dt$$

Switching Energy

- Do we know what this is?

$$Q = \int I_{dyn}(t)\,dt$$
$$= CV$$



$$E = \int P(t)\,dt$$
$$= \int I(t)V_{dd}\,dt$$
$$= V_{dd}\int I(t)\,dt$$

$$\Rightarrow \quad E = CV_{dd}^2$$

Capacitor charging energy

Switching Power

- Every time output switches 0→1 pay:
  - $E = CV^2$
- P_{dyn} = (# 0→1 trans) × CV^2 / time
- # 0→1 trans = ½ # of transitions
- P_{dyn} = (# trans) × ½CV^2 / time

Charging Power

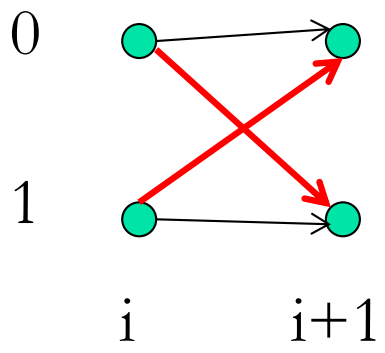
- P_{dyn} = (#0→1 trans) × CV^2 / time
- Often like to think about switching frequency
- Useful to consider per clock cycle
  - Frequency f = 1/clock-period = clock-cycles/time
- P_{dyn} = (#0→1 trans/clock-cycle) CV^2 f

Data Dependent Activity

- Consider an 8b counter
  - How often do each of the following switch?
    - Low bit?
    - High bit?
- Assuming random inputs
  - Activity at output of nand2?
  - Activity at output of xor2?

Gate Output Switching (random inputs)

Output states



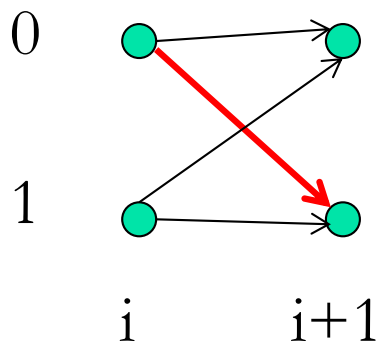
$$P(out_i != out_{i+1}) = P(out_i=0)*P(out_{i+1}=1) + P(out_i=1)*P(out_{i+1}=0)$$

Probablity of output switch of nand2?

Probablity of output switch of xor2?

Gate Output Switching (random inputs)

Output states



$$P(out_i \rightarrow out_{i+1}=0 \rightarrow 1)=P(out_i=0)*P(out_{i+1}=1)$$

Dynamic Power

- P_{dyn} = (#0→1 trans/clock-cycle) CV^2 f
- Let a = activity factor

  a = average $\#tran_{0\rightarrow1}$/clock

  a = probability of $\#tran_{0\rightarrow1}$

- $P_{dyn} = aCV^2$ f

Activity Factor

- Let a = activity factor
  - a = average #tran$_{0\rightarrow1}$/clock
  - a = probability of #tran$_{0\rightarrow1}$

$$a = p(out_i = 0)p(out_{i+1} = 1)$$

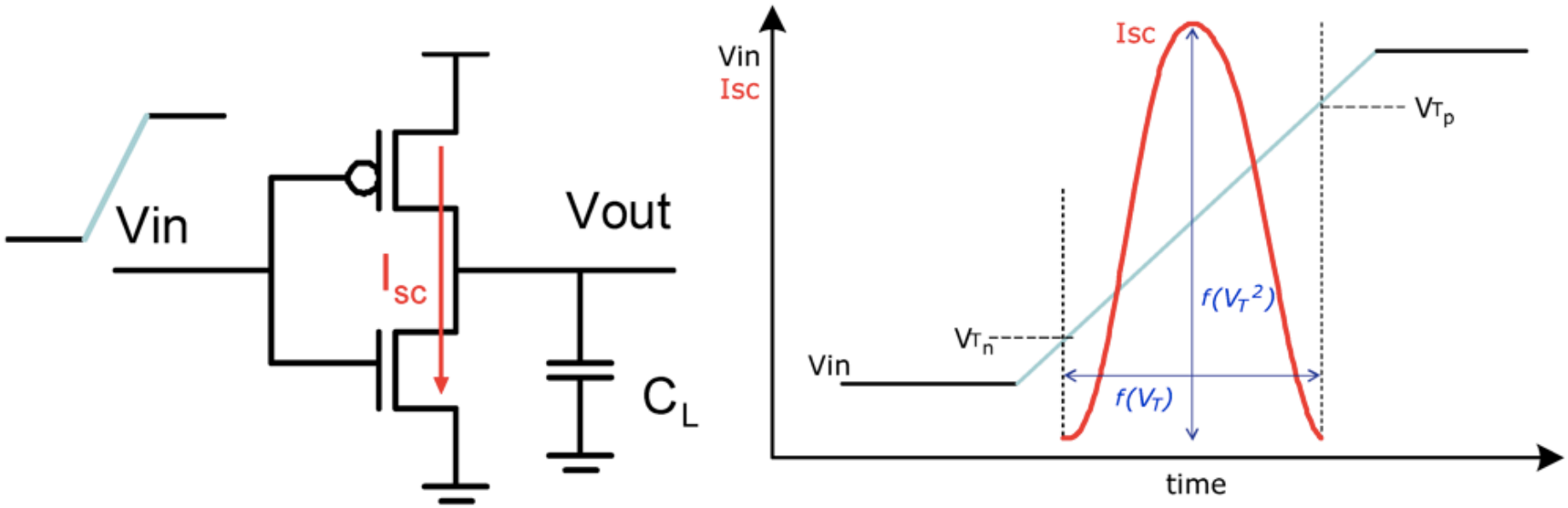
$$a = \frac{N_0}{2^N}\frac{N_1}{2^N} = \frac{N_0(2^N - N_0)}{2^{2N}}$$

Switching

Short Circuit Power

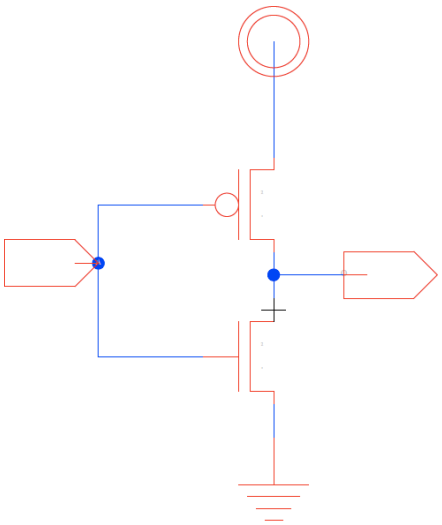
Short Circuit Power

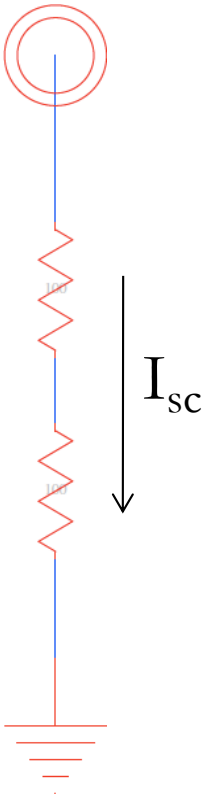
- Between V_{TN} and V_{dd} - V_{TP}
  - Both N and P devices conducting

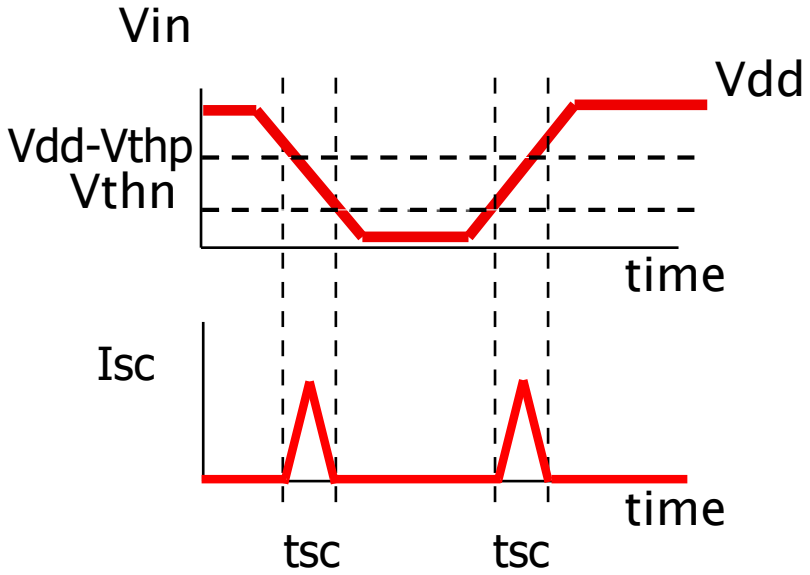


Short Circuit Power

- Between V_{TN} and V_{dd} - V_{TP}
  - Both N and P devices conducting
- Roughly:



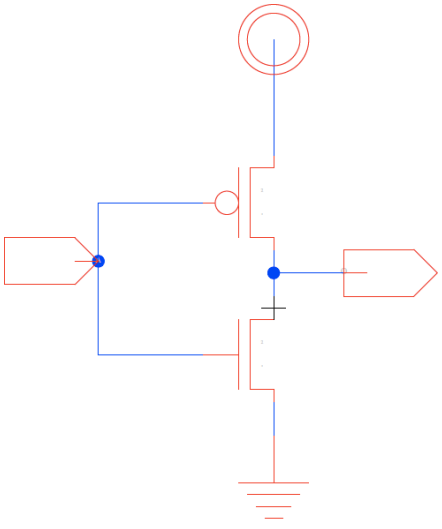


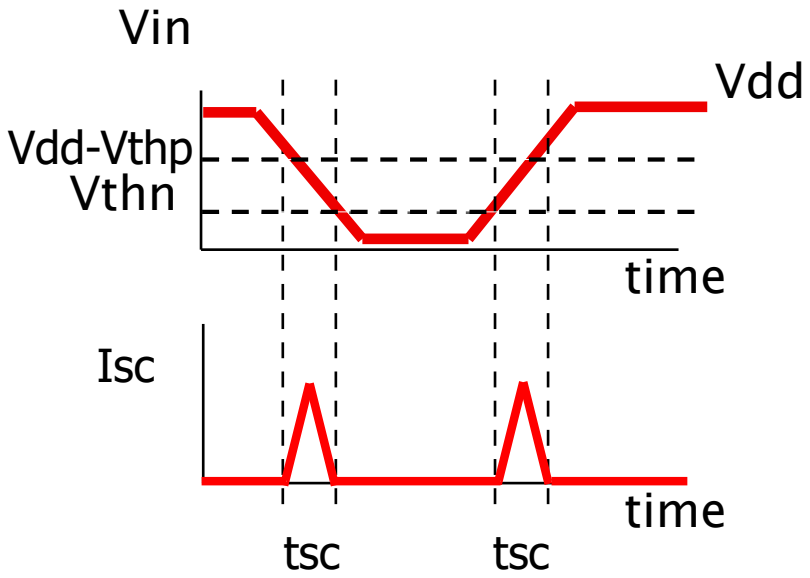


Peak Current

- I_{peak} around $V_{dd}/2$
  - If $|V_{TN}| = |V_{TP}|$ and sized equal rise/fall

$$I_{DS} \approx \nu_{sat} C_{OX} W \left(V_{GS} - V_T - \frac{V_{DSAT}}{2} \right)$$





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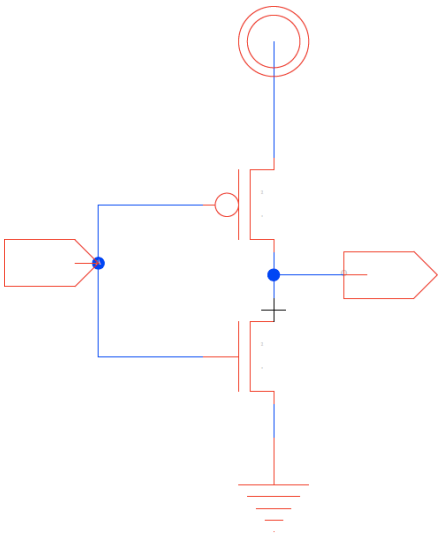
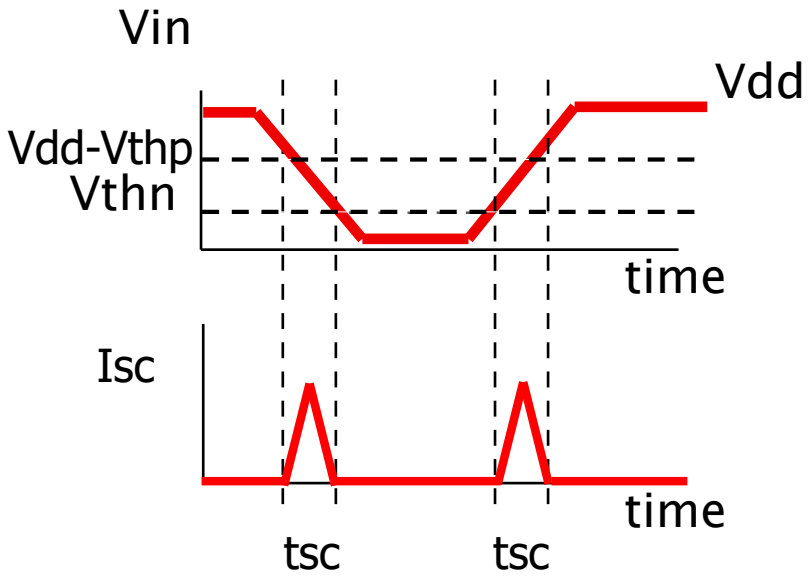
$$\int I(t)dt \approx I_{peak} \times t_{sc} \times \left(\frac{1}{2} \right)$$





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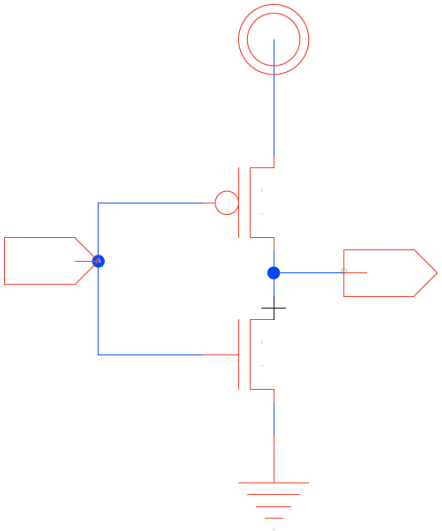
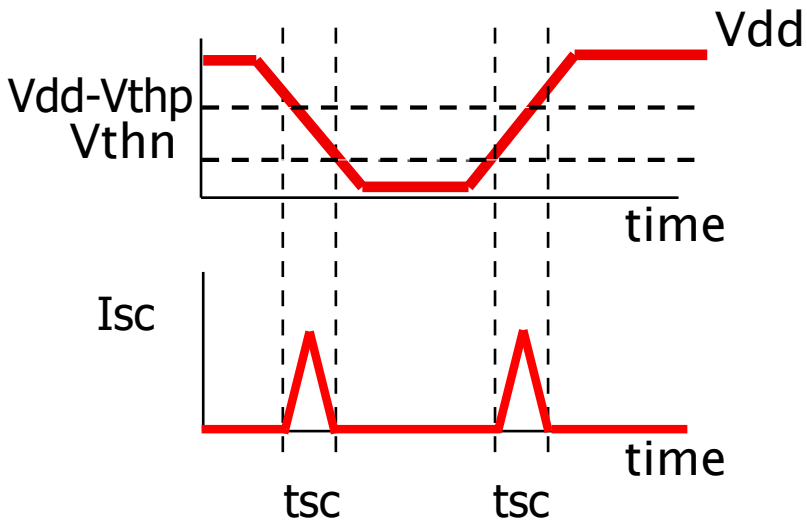
$$E = V_{dd} \times I_{peak} \times t_{sc} \times \left(\frac{1}{2} \right)$$

Vin





Short Circuit Energy

- Make it look like switching an equivalent capacitance, C_{SC}
  - $Q = I \times t$
  - $Q = CV$

$$E = V_{dd} \times \left(I_{peak} \times t_{sc} \times \left(\frac{1}{2} \right) \right)$$

$$E = V_{dd} \times (C_{SC} V_{dd}) = C_{SC} V_{dd}^2$$

Short Circuit Energy

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  - $Q = CV$

$$E = V_{dd} \times \left(I_{peak} \times t_{sc} \times \left(\frac{1}{2} \right) \right)$$

$$E = V_{dd} \times (C_{SC} V_{dd}) = C_{SC} V_{dd}^2$$

$$C_{SC} = \frac{I_{peak} t_{sc}}{2 V_{dd}}$$

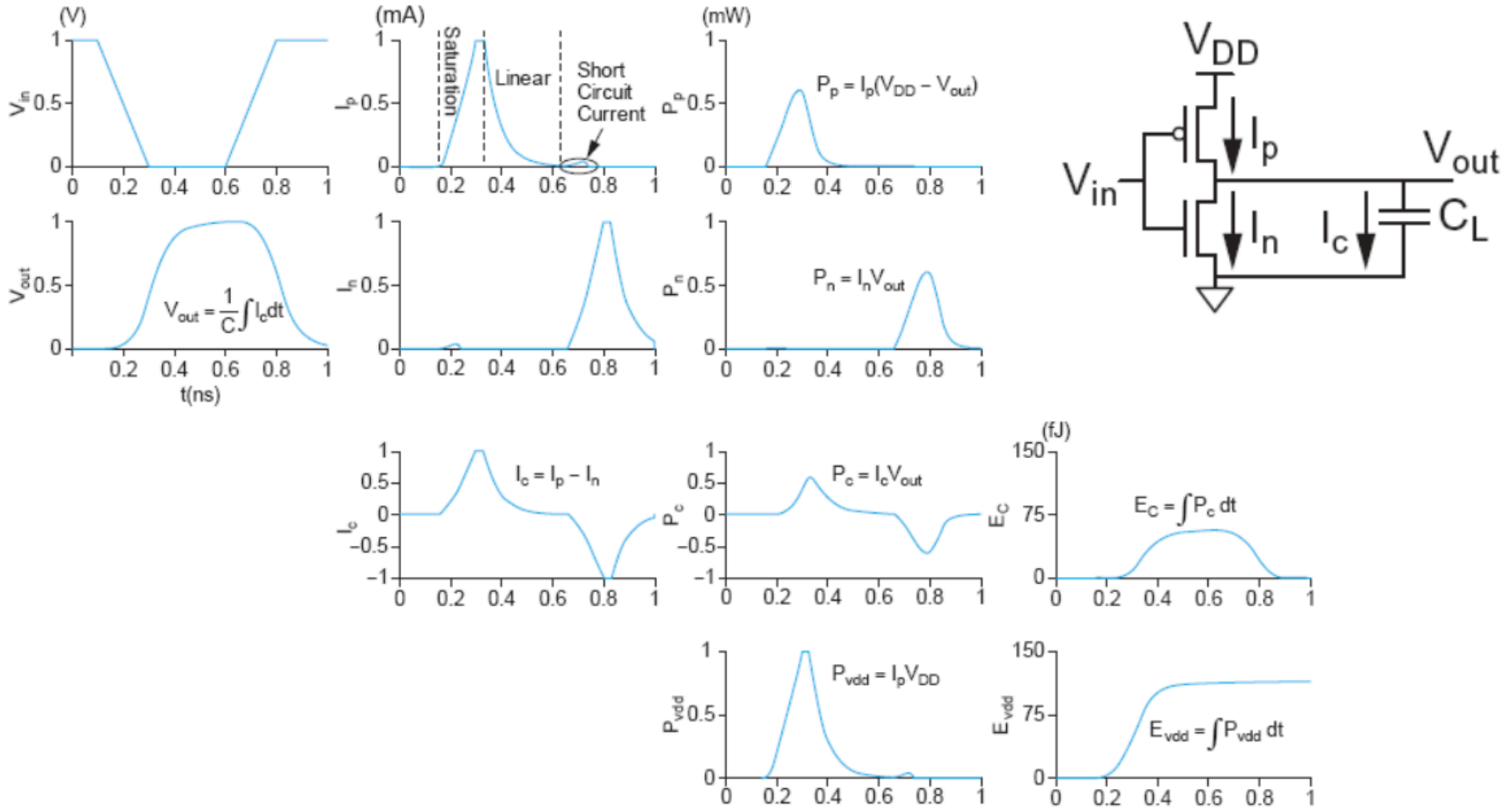
Short Circuit Energy

- Every time switch (0→1 and 1→0)
  - Also dissipate short-circuit energy: $E = C_{sc}V^2$
  - C_{cs} "fake" capacitance (for accounting)

Total Power

- $P_{tot} = P_{static} + P_{sc} + P_{dyn}$
- $P_{dyn} + P_{sc} = aC_{load}V^2f + 2aC_{sc}V^2f$
- $P_{tot} \approx a(C_{load} + 2C_{sc})V^2f + VI'_s(W/L)e^{-Vt/(nkT/q)}$

Switching Waveforms



Ideas

- Three components of power
  - Static
  - Dynamic
  - Short-circuit
- $P_{tot} = P_{static} + P_{dyn} + P_{sc}$

Admin

- HW 5 out now
  - A lot of SPICE
  - Start early
  - Create your schematics, icons and test schematics with care to minimize the time spent
  - Due Wednesday 3/13 (after spring break)
- Sparse TA OH during spring break
  - Keep and eye on Ed for updates
- I will still hold my office hours during break

Acknowledgement

- Prof. André DeHon (University of Pennsylvania)
- Prof. Jing Li (University of Pennsylvania)