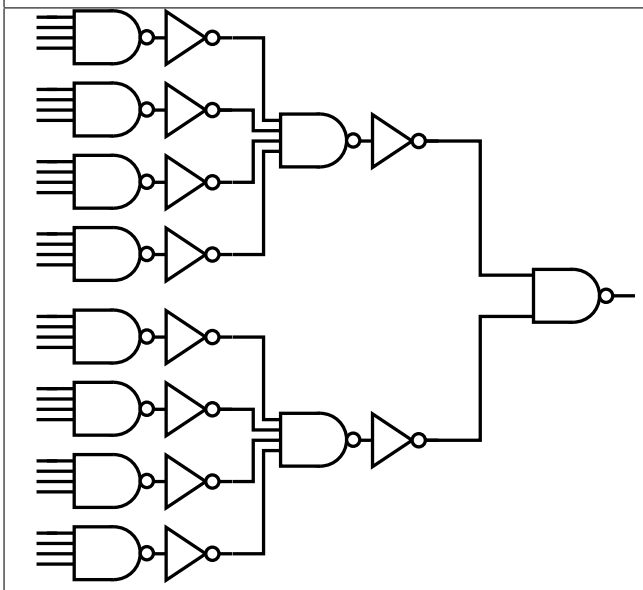
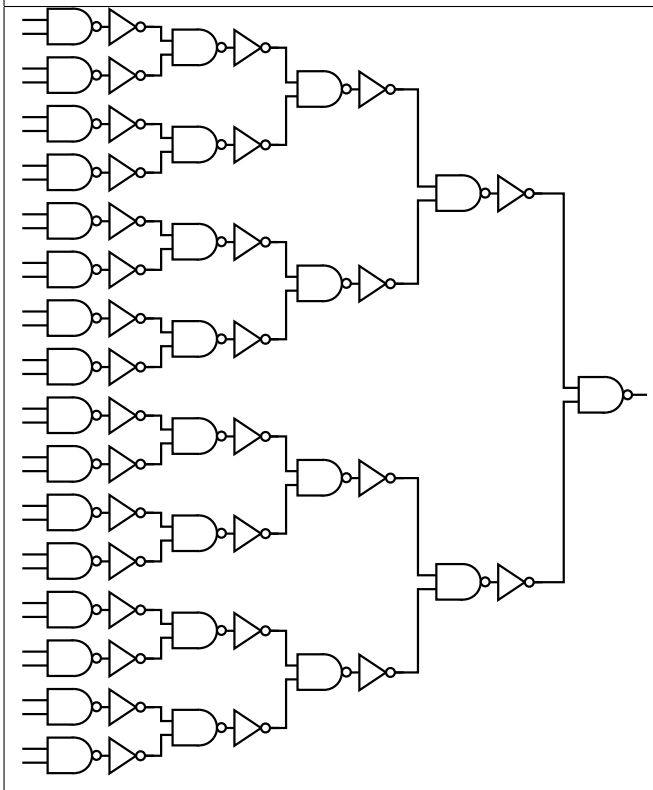
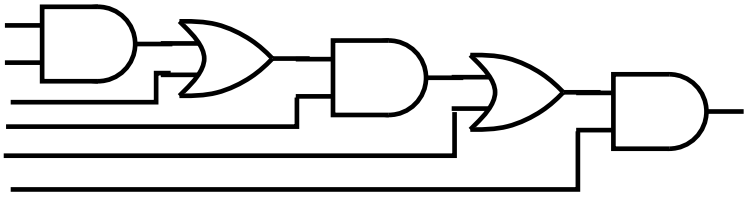
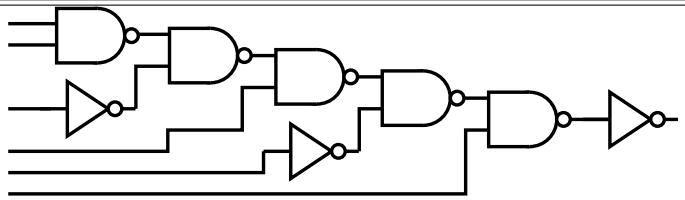
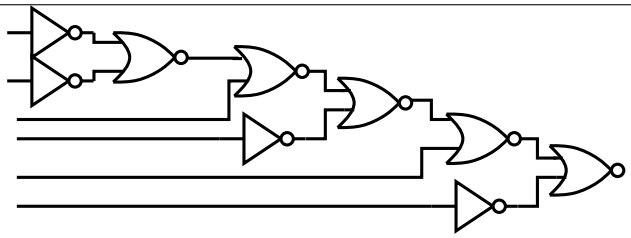
1. Assuming sized for $\frac{R_0}{2}$ drive as above, and input also driven by $R_{drive} = \frac{R_0}{2}$, compare the delay of the following three nand32 implementations for the $R_{p0} = R_{n0}$ case. Include the delay of driving the input and assume each implementation has an output load of $4C_0$.

Organization	**Delay**
single-stage nand32	
	
	

2. What is the delay for each of the two implementations below for this logical computaiton:

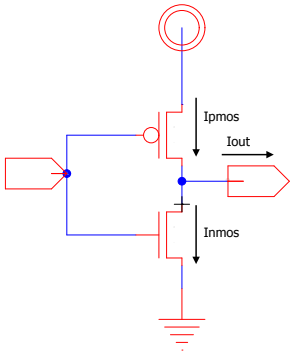


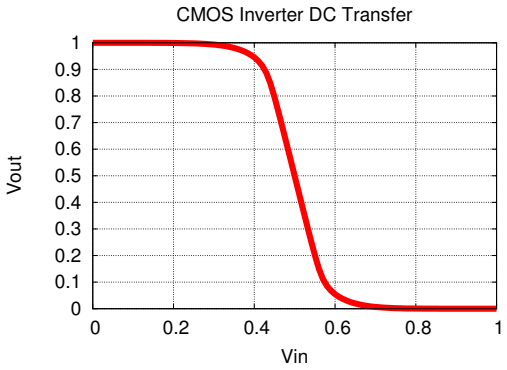
Assume $R_{drive} = \frac{R_0}{2}$ sizing of gates from previous page, and input also driven by $R_{drive} = \frac{R_0}{2}$. Assume each implementation has an output load of $2C_0$.

	Delay	
	$R_{p0} = R_{n0}$	$R_{p0} = 2R_{n0}$
		
		

Device	V_{gs}	I_d
NMOS	$V_{gs} < V_{thn}$	$(3 \times 10^{-7})\, e^{\frac{V_{gs}-V_{thn}}{40mV}}$
	$V_{gs} > V_{thn}$	$1.8 \times 10^{-4}\,(V_{gs} - V_{thn})$
PMOS	$V_{gs} > V_{thp}$	$(3 \times 10^{-7})\, e^{-\left(\frac{V_{gs}-V_{thp}}{40mV}\right)}$
	$V_{gs} < V_{thp}$	$-1.8 \times 10^{-4}\,(V_{gs} - V_{thp})$

Consider an inverter:





Useful: $e^{-1} \approx 0.37$, $e^{-4} \approx 0.02$, $e^{-7.5} \approx 6 \times 10^{-4}$

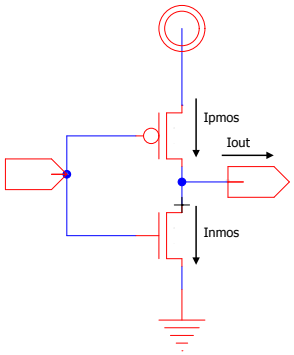
3. V_{dd}=1V, V_{thn}=300mV, V_{thp}=-300mV.

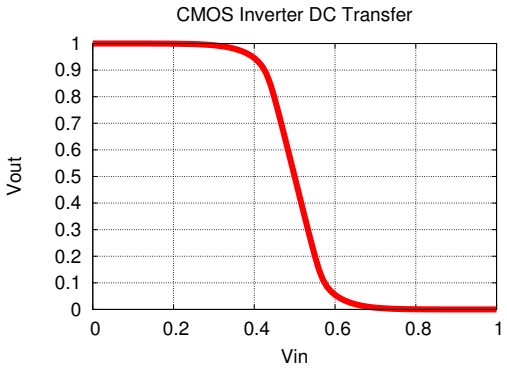
V_{in}	I_{pmos}	I_{nmos}	$\approx I_{pwr,gnd}$	
0V				A
140mV				B
400mV				C
500mV				D
600mV				E
860mV				F
1V				G

Approximate $I_{pwr,gnd} \approx \min(I_{nmos}, I_{pmos})$.

Device	V_{gs}	V_{ds}	I_d
NMOS	$V_{gs} < V_{thn}$	any	$(3 \times 10^{-7})\, e^{\frac{V_{gs}-V_{thn}}{40mV}}$
	$V_{gs} > V_{thn}$	$V_{ds} < V_{gs} - V_{thn}$	$3.6 \times 10^{-4}\,(V_{gs} - V_{thn}) \times V_{ds}$
		$V_{ds} > V_{gs} - V_{thn}$	$1.8 \times 10^{-4}\,(V_{gs} - V_{thn})$
PMOS	$V_{gs} > V_{thp}$	any	$(3 \times 10^{-7})\, e^{-\left(\frac{V_{gs}-V_{thp}}{40mV}\right)}$
	$V_{gs} < V_{thp}$	$V_{ds} > V_{gs} - V_{thp}$	$-3.6 \times 10^{-4}\,(V_{gs} - V_{thp}) \times V_{ds}$
		$V_{ds} < V_{gs} - V_{thp}$	$-1.8 \times 10^{-4}\,(V_{gs} - V_{thp})$

Consider an inverter:





Useful: $e^{-1} \approx 0.37$, $e^{-4} \approx 0.02$, $e^{-7.5} \approx 6 \times 10^{-4}$

4. V_{dd}=1V, V_{thn}=300mV, V_{thp}=-300mV, assume steady-state operation at V_{in} given.

V_{in}	$I_{pmos} = I_{nmos} = I_{pwr,gnd}$	Vout	
0V			A
140mV			B
400mV			C
500mV			D
600mV			E
860mV			F
1V			G

Approximate $I_{pwr,gnd} \approx \min(I_{nmos}, I_{pmos})$.