ESE3700: Circuit-Level Modeling Design, and Optimization for Digital Systems

Lec 11: March 11, 2024

Energy and Power Tradeoffs

Previously

- Three components of power
  - Static
  - Dynamic
  - Short circuit
- $P_{tot} = P_{static} + P_{dyn} + P_{sc}$

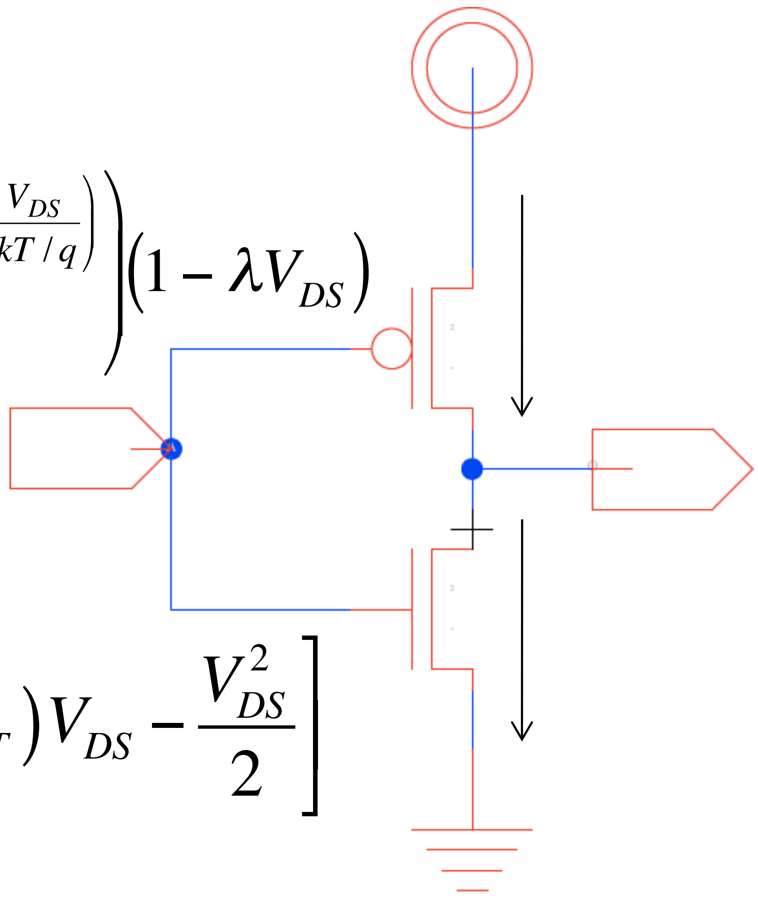
Leakage

Static Power

Operating Modes

- Steady-State: $V_{in}=V_{dd}$
  - PMOS: subthreshold
  - NMOS: resistive

$$I_{DSp} = -I_S'\left(\frac{W}{L}\right)e^{-\left(\frac{V_{GS}-V_T}{nkT/q}\right)}\left(1-e^{\left(\frac{V_{DS}}{kT/q}\right)}\right)\left(1-\lambda V_{DS}\right)$$

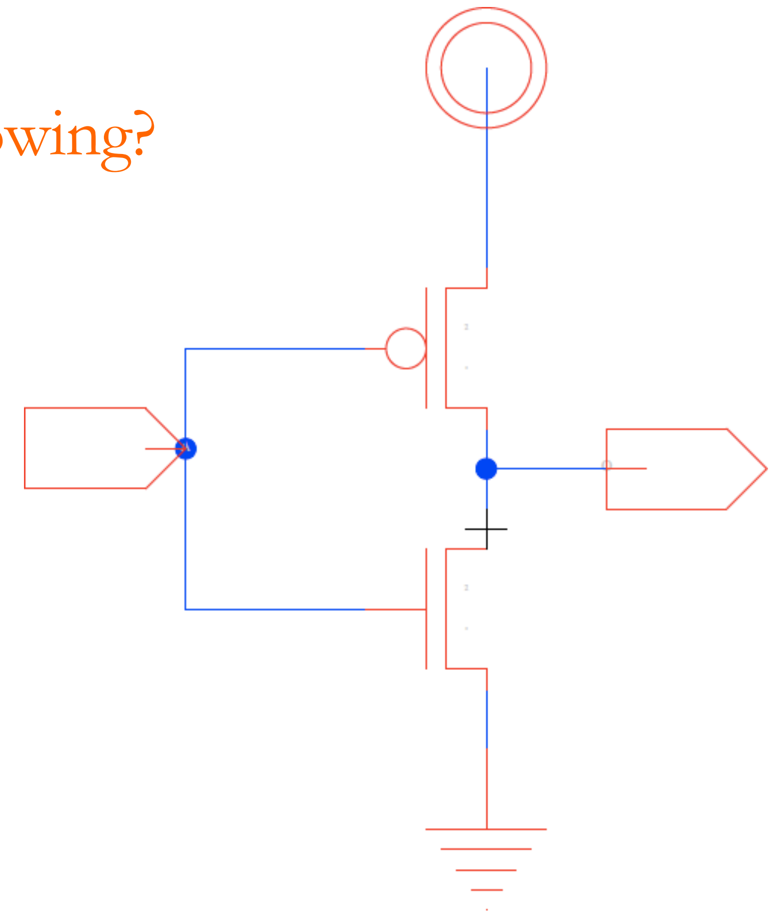


$$I_{DSn} = \mu_n C_{OX}\left(\frac{W}{L}\right)\left[\left(V_{GS}-V_T\right)V_{DS}-\frac{V_{DS}^2}{2}\right]$$

Which current determines I_{static} ?

Static Power

- $P = I \times V$
- What V should we use?
  - Where is the static current flowing?



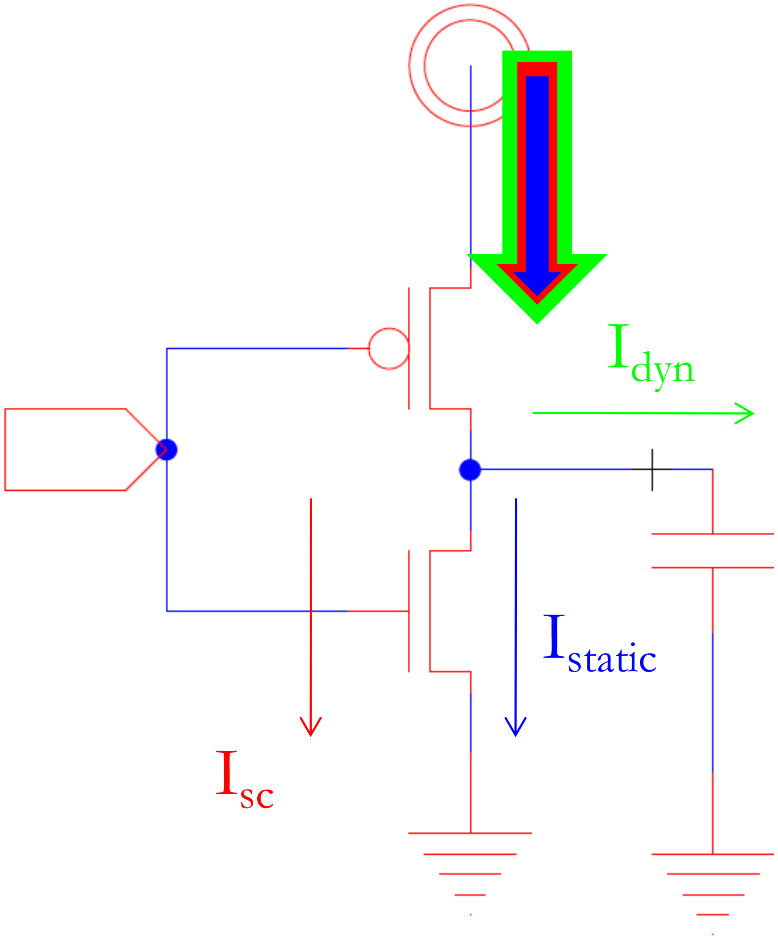
Switching

Dynamic Power

Switching Currents

- $I_{total}(t) = I_{static}(t) + I_{switch}(t)$

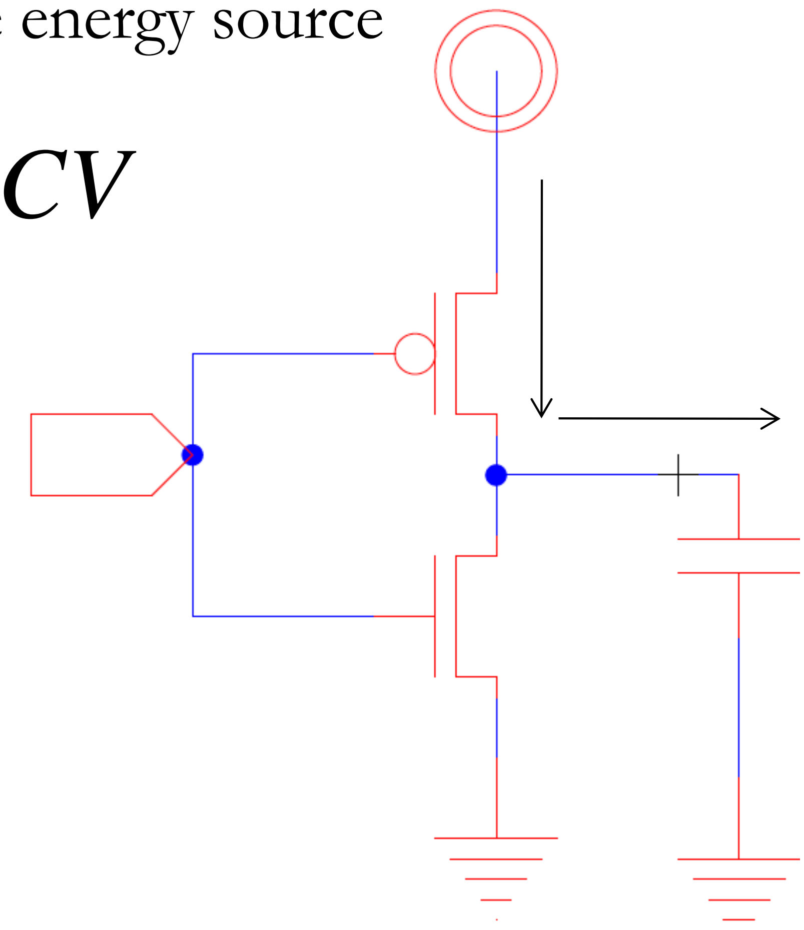
- $I_{switch}(t) = I_{sc}(t) + I_{dyn}(t)$



Switching (Dynamic)

- CMOS circuit switching output from 0→1
  - Spends energy CV_{dd}^2 charging load
  - CV_{dd}^2 energy is pulled from the energy source

$$Q = \int I(t)\,dt = CV$$



$$E = \int P(t)\,dt$$

$$E = V_{dd} \int I(t)\,dt$$

$$E = CV_{dd}^2$$

Switching Power

- Every time output switches 0→1 pay:
  - $E = CV^2$

- $P_{dyn} = (\# \; 0 \rightarrow 1 \text{ trans}) \times CV^2 / \text{time}$

Charging Power

- P_{dyn} = (#0→1 trans) × CV^2 / time

- Often like to think about switching frequency
- Useful to consider per clock cycle
  - Frequency f = 1/clock-period = clock-cycles/time

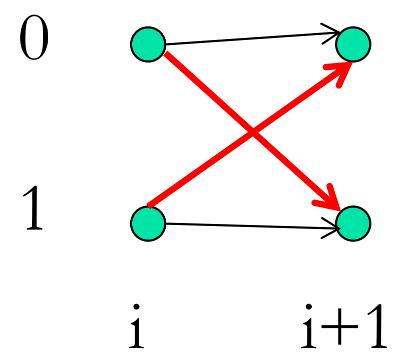
- P_{dyn} = (#0→1 trans/clock-cycle) CV^2 f

Data Dependent Activity

- Consider an 8b counter
  - How often do each of the following switch?
    - Low bit?
    - High bit?
- Assuming random inputs
  - Activity at output of nand2?
  - Activity at output of xor2?

Gate Output Switching (random inputs)

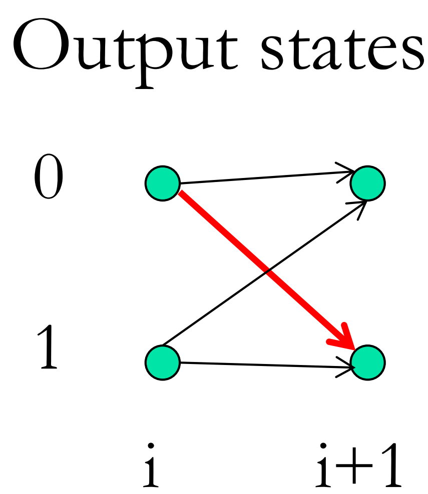
Output states



$$P(out_i != out_{i+1}) = P(out_i=0)*P(out_{i+1}=1) + P(out_i=1)*P(out_{i+1}=0)$$

Probablity of output switch of nand2?
Probablity of output switch of xor2?

Gate Output Switching (random inputs)



$$P(out_i \rightarrow out_{i+1} = 0 \rightarrow 1) = P(out_i=0)*P(out_{i+1}=1)$$

Dynamic Power

- P_{dyn} = (#0→1 trans/clock-cycle) $CV^2 f$
- Let a = activity factor

  a = average $\#tran_{0\rightarrow1}$/clock

  a = probability of $\#tran_{0\rightarrow1}$

- $P_{dyn} = aCV^2 f$

Activity Factor

- Let a = activity factor
  - a = average #tran$_{0\rightarrow 1}$/clock
  - a = probability of #tran$_{0\rightarrow 1}$

$$a = p(out_i = 0)p(out_{i+1} = 1)$$

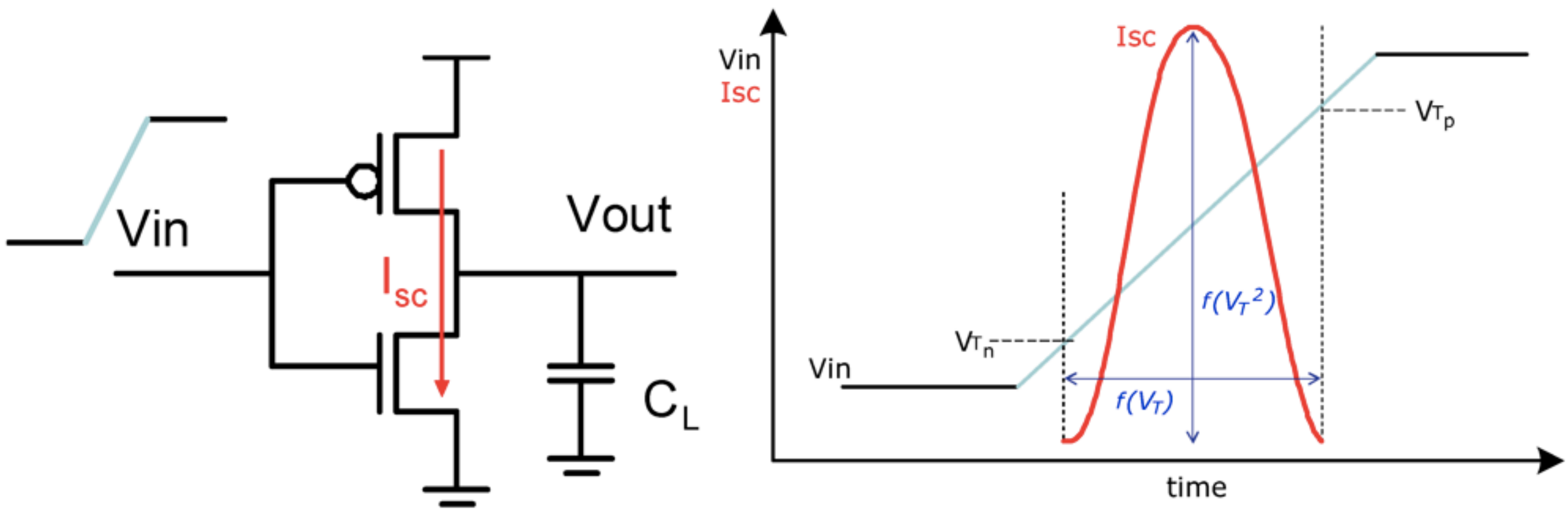
$$a = \frac{N_0}{2^N}\frac{N_1}{2^N} = \frac{N_0(2^N - N_0)}{2^{2N}}$$

Switching

Short Circuit Power

Short Circuit Power

- Between V_{TN} and V_{dd} - V_{TP}
  - Both N and P devices conducting



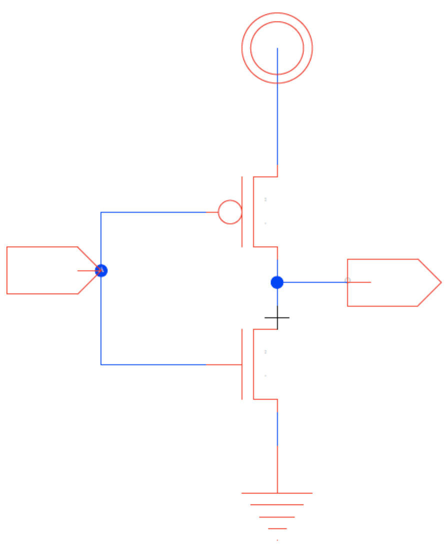
Peak Current

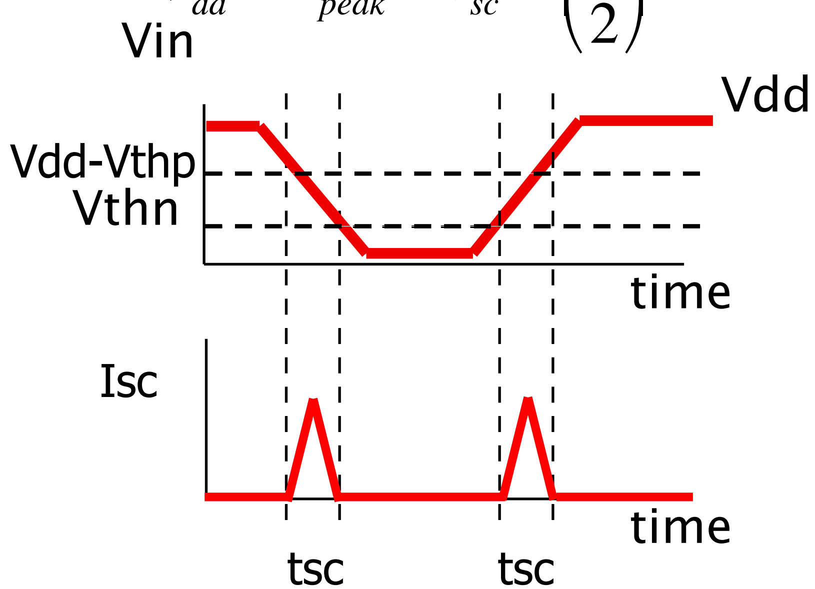
- I_{peak} around $V_{dd}/2$
  - If $|V_{TN}| = |V_{TP}|$ and sized equal rise/fall

$$I_{DS} \approx v_{sat} C_{OX} W \left(V_{GS} - V_T - \frac{V_{DSAT}}{2} \right)$$

$$\int I(t)dt \approx I_{peak} \times t_{sc} \times \left(\frac{1}{2}\right)$$

$$E = V_{dd} \times I_{peak} \times t_{sc} \times \left(\frac{1}{2}\right)$$





Short Circuit Energy

- Make it look like switching an equivalent capacitance, C_{SC}

$$E = V_{dd} \times \left(I_{peak} \times t_{sc} \times \frac{1}{2} \right)$$

$$E = C_{SC} V_{dd}^2$$

$$C_{SC} = \frac{I_{peak} t_{sc}}{2V_{dd}}$$

Short Circuit Energy

- Every time switch (0→1 and 1→0)
  - Also dissipate short-circuit energy: $E = C_{sc}V^2$
  - C_{cs} “fake” capacitance (for accounting)

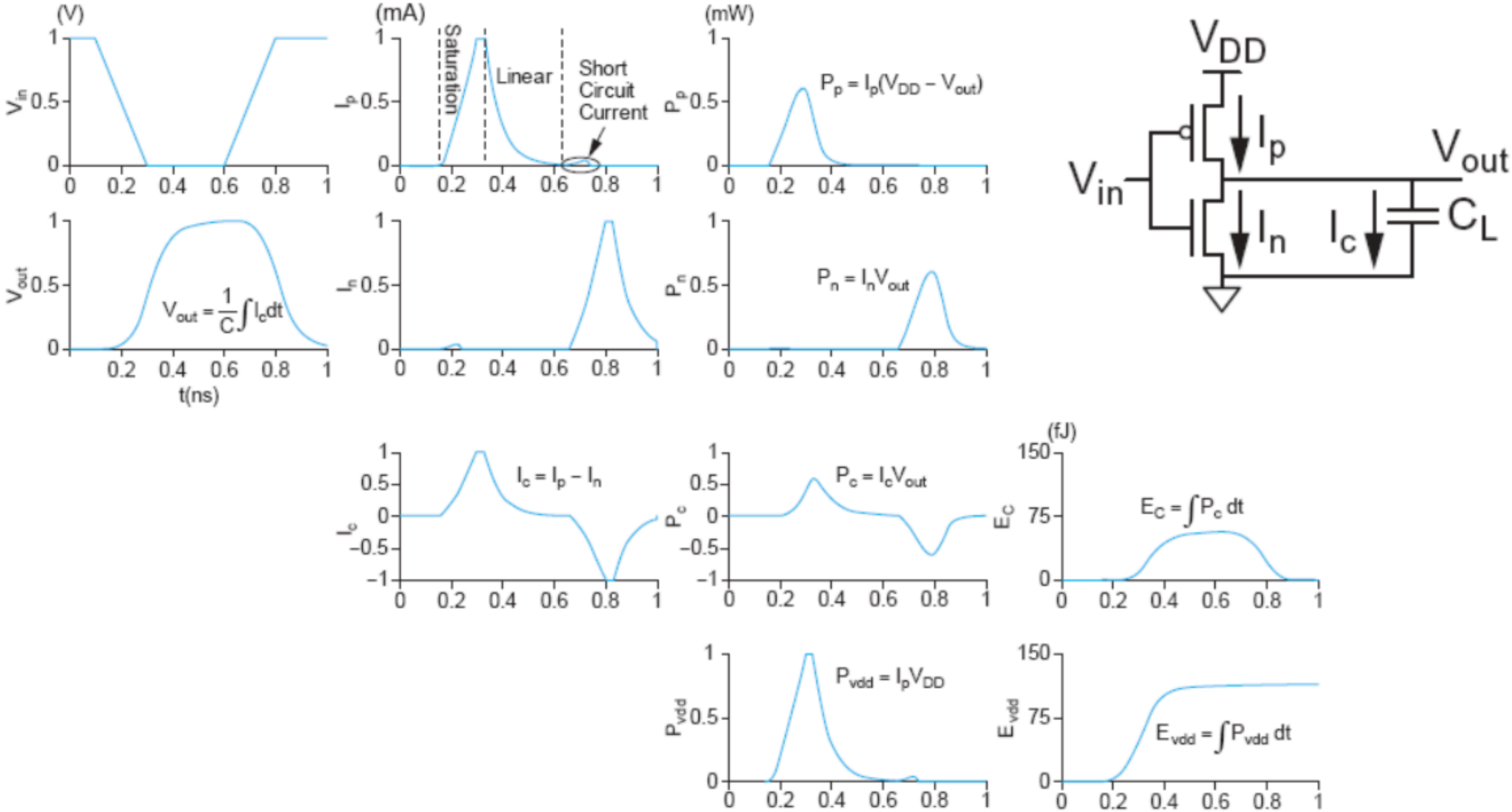
Total Power

- $P_{tot} = P_{static} + P_{sc} + P_{dyn}$

- $P_{dyn} + P_{sc} = aC_{load}V^2f + 2aC_{sc}V^2f$

- $P_{tot} \approx a(C_{load} + 2C_{sc})V^2f + VI'_s(W/L)e^{-Vt/(nkT/q)}$

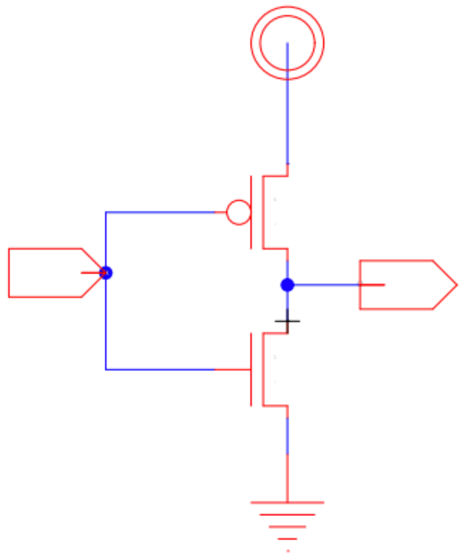
Switching Waveforms

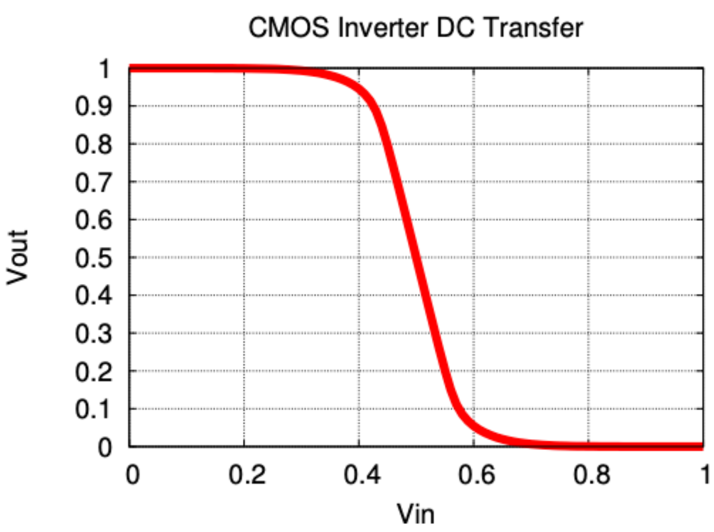


Preclass 1

Device	V_{gs}	I_d
NMOS	$V_{gs} < V_{thn}$	$(3 \times 10^{-7})\, e^{\frac{V_{gs}-V_{thn}}{40mV}}$
	$V_{gs} > V_{thn}$	$1.8 \times 10^{-4}\,(V_{gs} - V_{thn})$
PMOS	$V_{gs} > V_{thp}$	$(3 \times 10^{-7})\, e^{-\left(\frac{V_{gs}-V_{thp}}{40mV}\right)}$
	$V_{gs} < V_{thp}$	$-1.8 \times 10^{-4}\,(V_{gs} - V_{thp})$

Consider an inverter using the pmos and nmos devices described above:





Preclass 1

V_{in}	I_{static}	$I_{dynamic}$	I_{sc}
0V			
140mV			
400mV			
500mV			
600mV			
860mV			
1V			

Reminder:

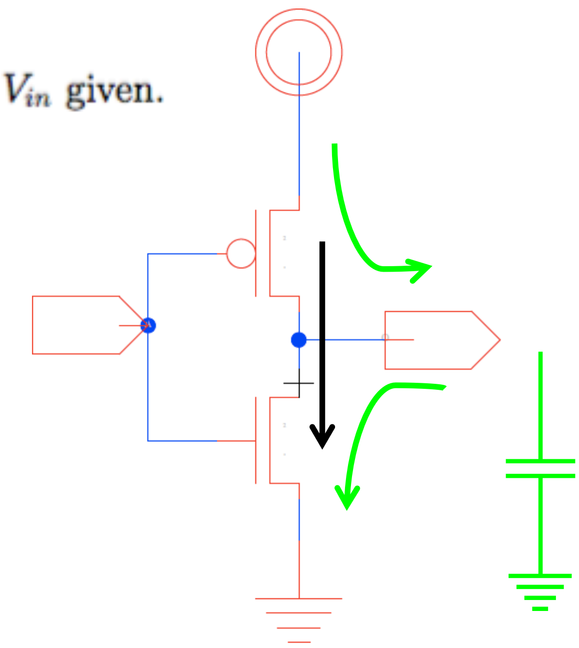
Device	V_{gs}	I_d
NMOS	$V_{gs} < V_{thn}$	$(3 \times 10^{-7})\, e^{\frac{V_{gs}-V_{thn}}{40mV}}$
	$V_{gs} > V_{thn}$	$1.8 \times 10^{-4}\,(V_{gs} - V_{thn})$
PMOS	$V_{gs} > V_{thp}$	$(3 \times 10^{-7})\, e^{-\left(\frac{V_{gs}-V_{thp}}{40mV}\right)}$
	$V_{gs} < V_{thp}$	$-1.8 \times 10^{-4}\,(V_{gs} - V_{thp})$

1. V_{dd}=1V, V_{thn}=300mV, V_{thp}=-300mV, assume steady-state operation at V_{in} given.

V_{in}	I_{pmos}	I_{nmos}	$\approx I_{pwr,gnd}$	
0V	126uA	180pA	180pA	A
140mV	100uA	6nA	6nA	B
400mV	54uA	18uA	18uA	C
500mV	36uA	36uA	36uA	D
600mV	18uA	54uA	18uA	E
860mV	6nA	100uA	6nA	F
1V	180pA	126uA	180pA	G

Approximate $I_{pwr,gnd} \approx \min(I_{nmos}, I_{pmos})$.

Useful: $e^{-1} \approx 0.37$, $e^{-4} \approx 0.02$, $e^{-7.5} \approx 6 \times 10^{-4}$,



Design Tradeoffs

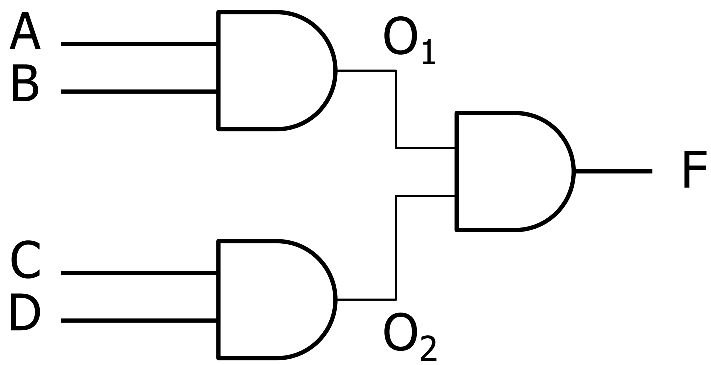
Reduce Dynamic Power?

- $P_{dyn} = aCV^2 f$

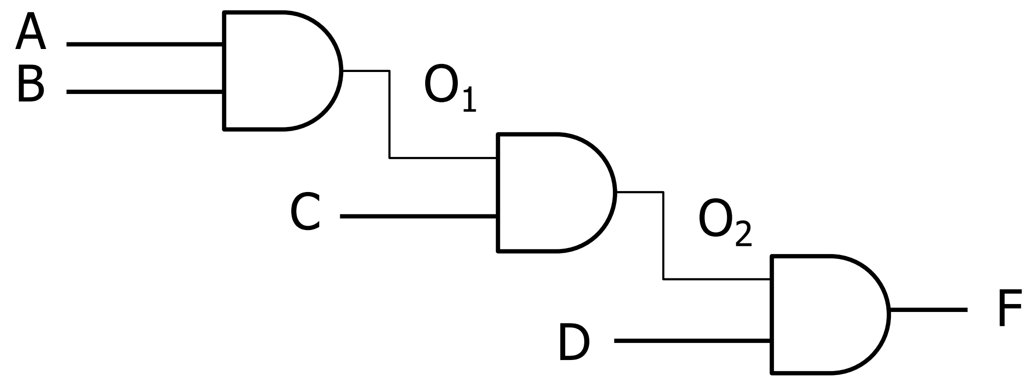
- How do we reduce dynamic power?

Reduce Activity Factor

Tree



Chain

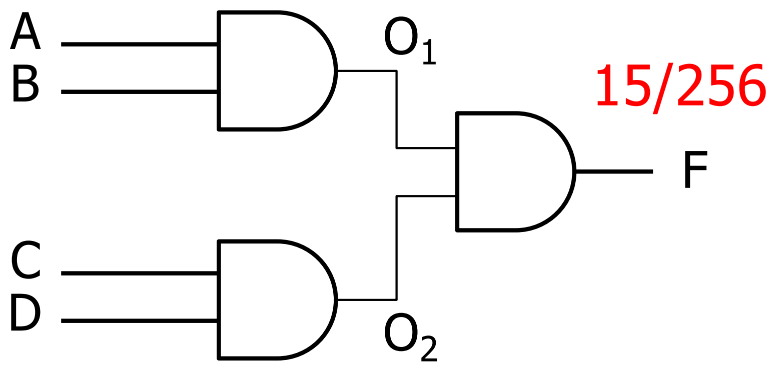


$$a = p(out_i = 0)\,p(out_{i+1} = 1)$$

$$a = \frac{N_0}{2^N}\frac{N_1}{2^N} = \frac{N_0(2^N - N_0)}{2^{2N}}$$

Reduce Activity Factor

Tree



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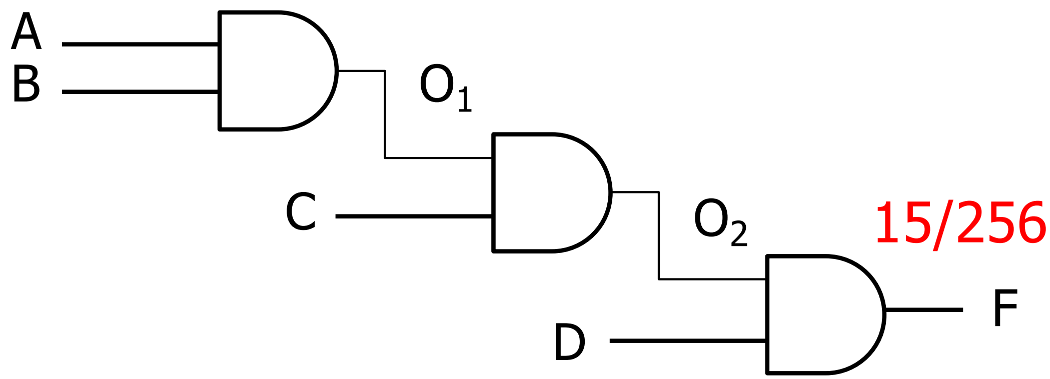

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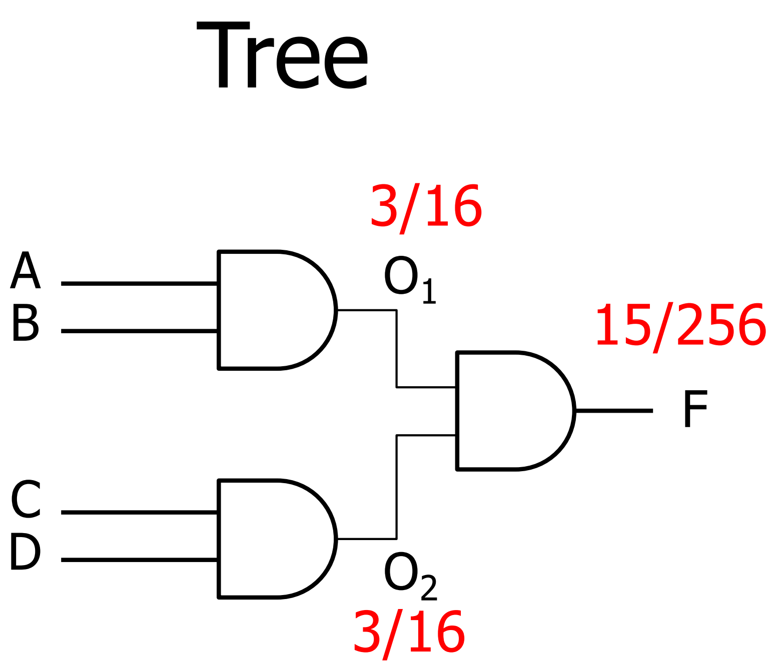
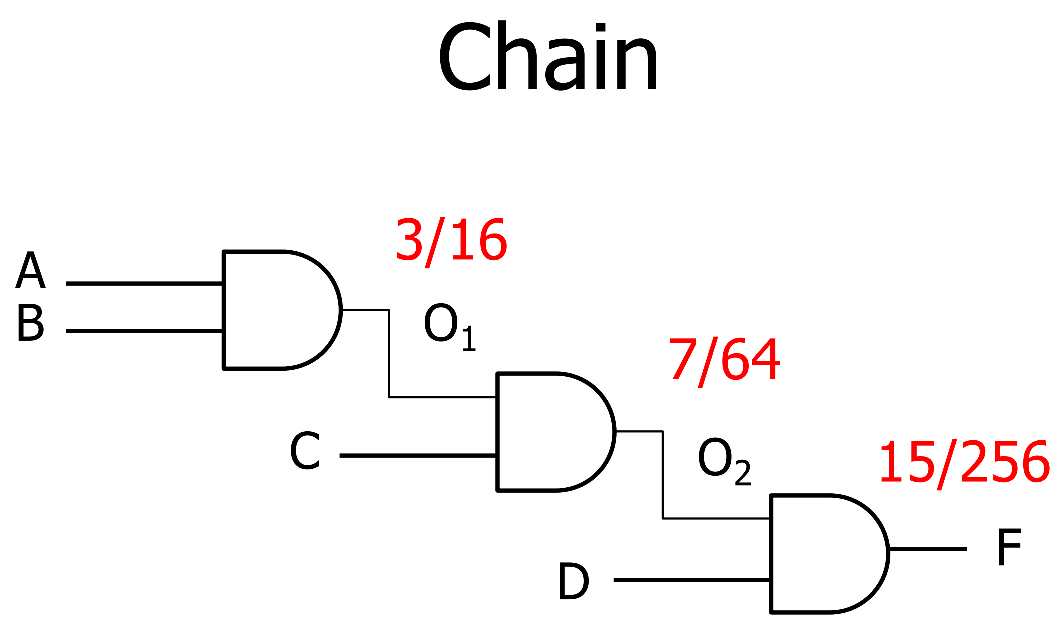
Reduce Activity Factor





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$$a = \frac{N_0}{2^N}\frac{N_1}{2^N} = \frac{N_0(2^N - N_0)}{2^{2N}}$$

Reduce V_{dd} (Preclass 2)

- V_{dd}=520mV, V_{thn}=|V_{thp}|=300mV

V_{in}	I_{static}	$I_{dynamic}$	I_{sc}
0V			
140mV			
260mV			
380mV			
520mV			

Reduce V_{dd} (Preclass 2)

- V_{dd}=520mV, V_{thn}=|V_{thp}|=300mV

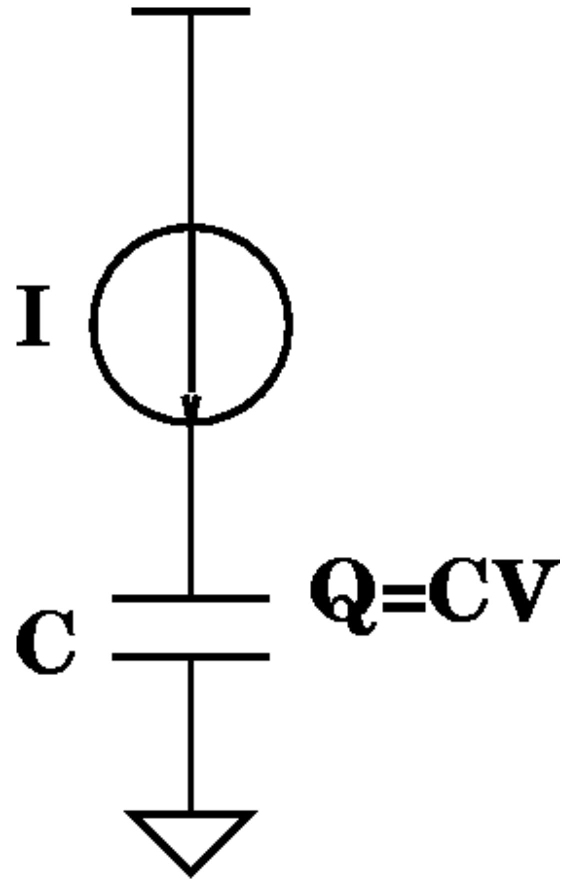
V_{in}	I_{static}	$I_{dynamic}$	I_{sc}
0V	180pA	39.6uA	
140mV	6nA	14.4uA	
260mV	111nA		
380mV	6nA	14.4uA	
520mV	180pA	39.6uA	

Reduce V_{dd}

- What happens as reduce V?
  - Energy?
    - Static
    - Switching
  - Delay?

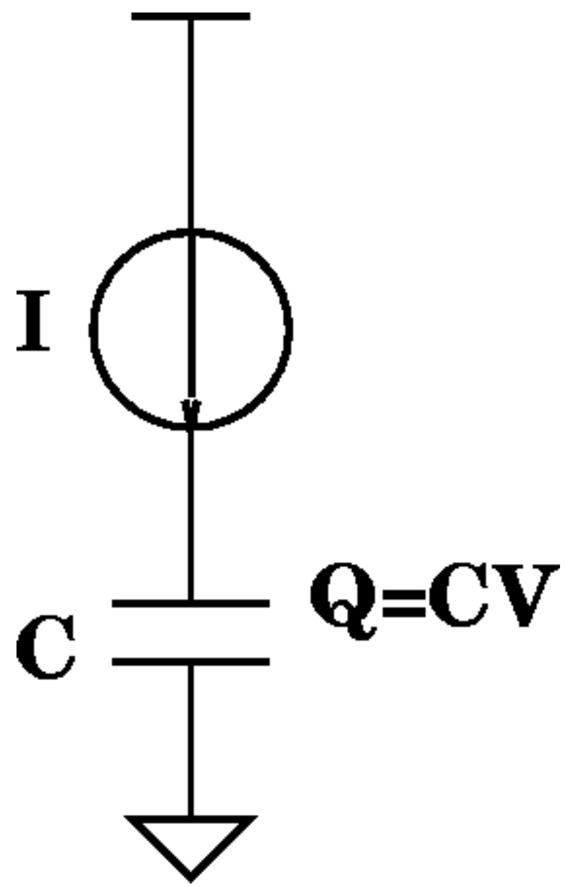
Reduce V_{dd}:

- $\tau_{gd}=Q/I=(CV)/I$
- $I_d=(\mu C_{OX}/2)(W/L)(V_{gs}-V_{TH})^2$
- τ_{gd} impact?



Reduce V_{dd}:

- $\tau_{gd}=Q/I=(CV)/I$
- $I_d=(\mu C_{OX}/2)(W/L)(V_{gs}-V_{TH})^2$
- τ_{gd} impact?
- $\tau_{gd} \propto \frac{1}{V}$



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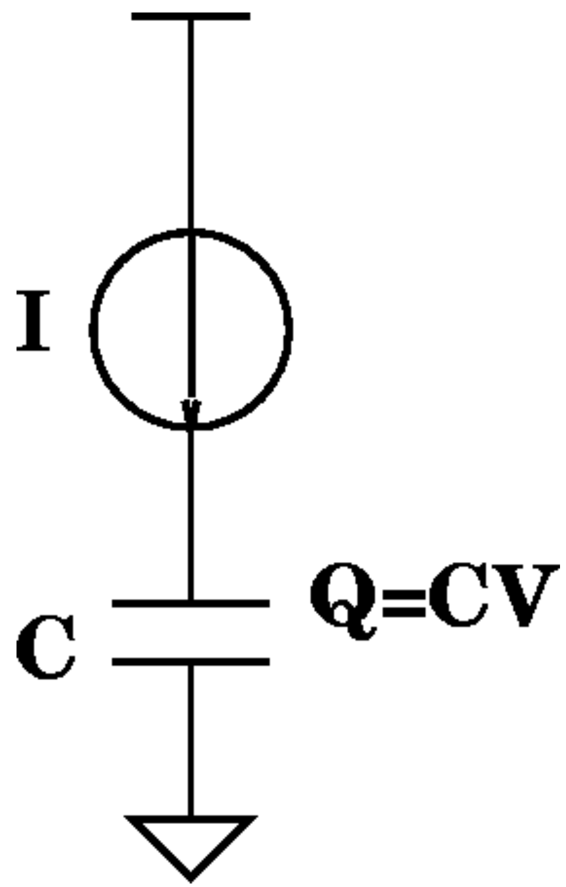
- $I_d=(\mu C_{OX}/2)(W/L)(V_{gs}-V_{TH})^2$
- τ_{gd} impact?
- $\tau_{gd} \propto \frac{1}{V}$
- Ignoring leakage:

$$E \propto V^2$$



Reduce V_{dd}:

- $\tau_{gd}=Q/I=(CV)/I$
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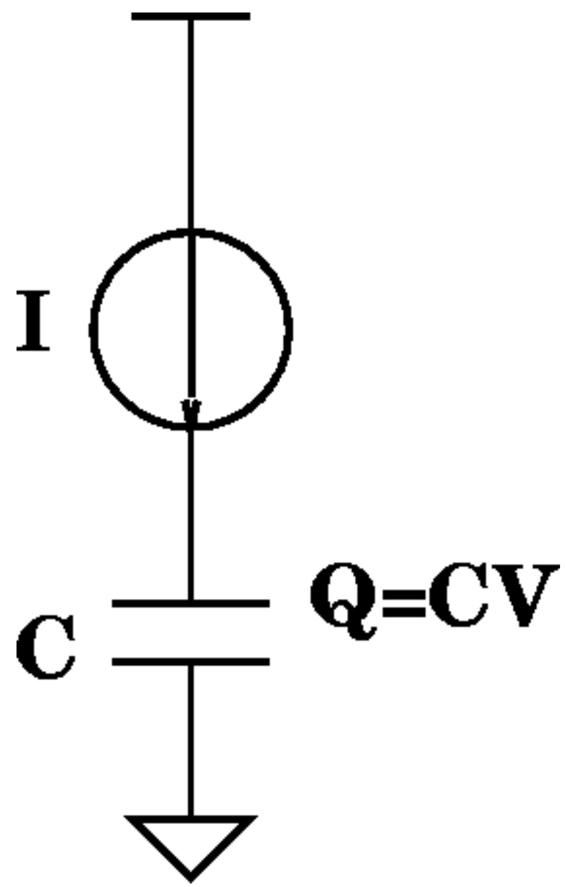
- τ_{gd} impact?
- $\tau_{gd} \propto \frac{1}{V}$
- Ignoring leakage:

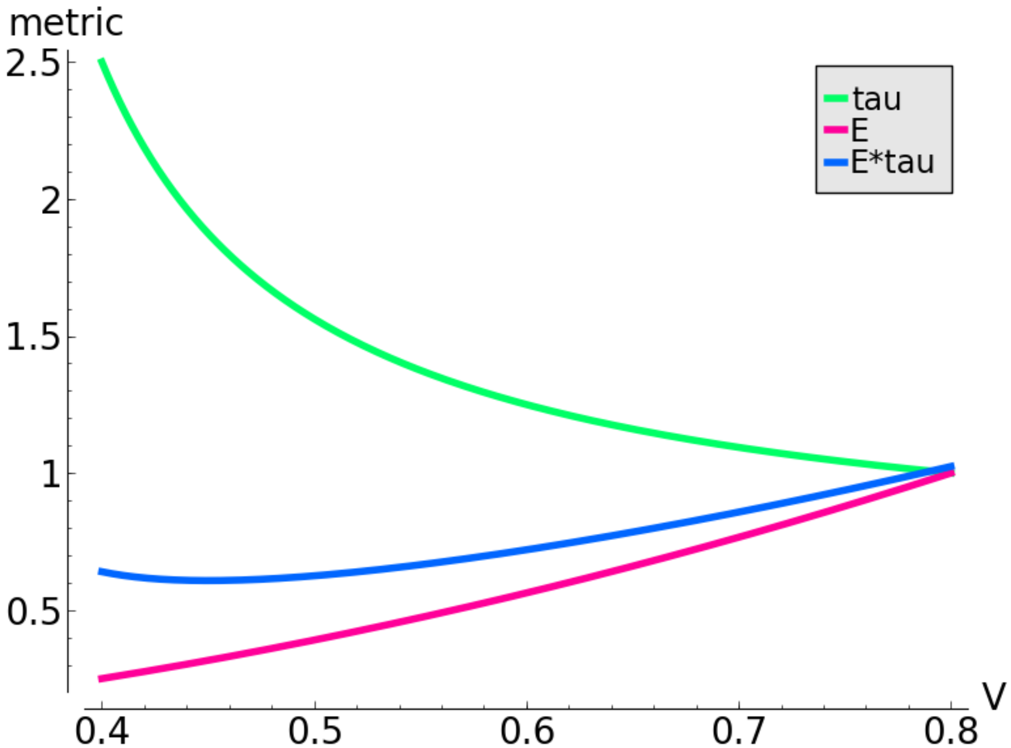
$$E \propto V^2$$

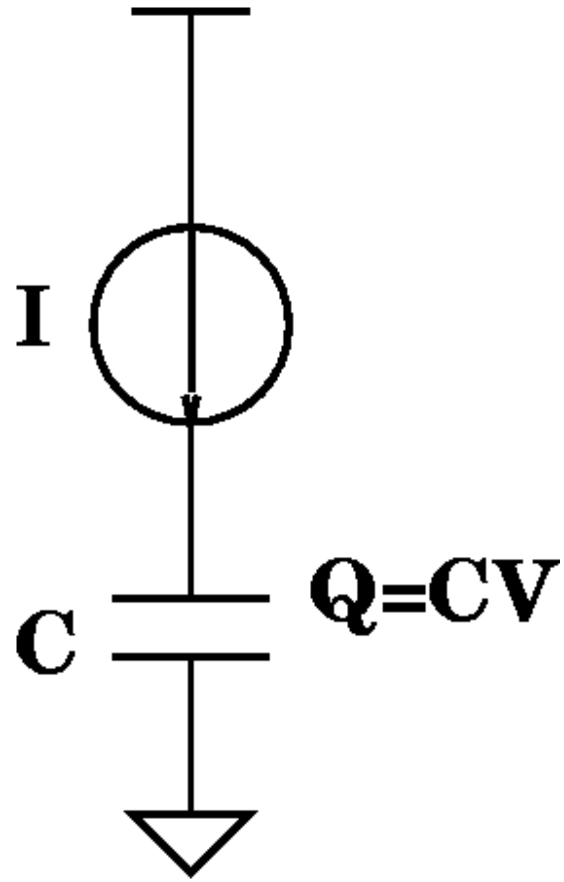
$$E\tau^2 \approx Const$$



Reduce V_{dd}: Velocity Saturation

- $\tau_{gd}=Q/I=(CV)/I$
- $I_d=(\nu_{sat}C_{OX})(W)(V_{gs}-V_{TH}-V_{DSAT}/2)$
- τ_{gd} impact?





Reduce V_{dd} (Preclass 3)

- $V_{thn}=|V_{thp}|=300mV$, $V_{in}=V_{dd}$, estimate $E\tau$

V_{dd}	I_{dyn}	$\tau/(\tau@V_{dd}=1)$	$E_{switch}/(E_{switch}@V_{dd}=1)$	$E\tau$
1V		1	1	1
700mV				
500mV				
350mV				
260mV				

Reduce V_{dd} (Preclass 3)

- $V_{thn}=|V_{thp}|=300mV$, $V_{in}=V_{dd}$, estimate Eτ

V_{dd}	I_{dyn}	$\tau/(\tau@V_{dd}=1)$	$E_{switch}/(E_{switch}@V_{dd}=1)$	Eτ
1V	126uA	1	1	1
700mV	72uA	1.225	0.49	.6
500mV	36uA	1.75	0.25	.437
350mV	9uA	4.9	0.12	.588
260mV	111nA	295	0.07	20.6

Increase V_{th} (Preclass 4)

- What is impact of increasing threshold on
  - Delay?
  - Leakage?
- V_{dd}=1V, V_{in}=V_{dd}

V_{thn}= -V_{thp}	I_{dyn}	$\tau/(\tau@V_{th}$=300mV)	I_{static}	$I_{stat}/(I_{stat}@V_{th}$=300 mV)
300mV				
460mV				
600mV				

Increase V_{th} (Preclass 4)

- What is impact of increasing threshold on
  - Delay?
  - Leakage?
- V_{dd}=1V, V_{in}=V_{dd}

V_{thn}= -V_{thp}	I_{dyn}	τ/(τ@V_{th}=300mV)	I_{static}	I_{stat}/(I_{stat}@V_{th}=300 mV)
300mV	126uA	1	180pA	1
460mV	97uA	1.3	3.6pA	0.02
600mV	72uA	1.75	108fA	0.0006

Big Ideas

- Three components of power
  - Static
  - Dynamic
  - Short-circuit
- $P_{tot} = P_{static} + P_{dyn} + P_{sc}$
- Tradeoff (knobs: V_{dd}, V_{th}, a, etc.)
  - Speed
  - Switching energy
  - Leakage energy
  - Want to look at the energy-delay product for optimality
- Energy-Delay tradeoff: $E\tau^2$, $E\tau$

Admin

- HW 5 due Wednesday 3/13
- Proj 1 release Wednesday 3/13
  - Design and optimize 8-bit adder
    - Have baseline built and characterized 1 week from release
  - Due ~2 weeks on Friday 3/29

Acknowledgement

- Prof. André DeHon (University of Pennsylvania)
- Prof. Jing Li (University of Pennsylvania)