

ESE3700: Circuit-Level Modeling Design, and Optimization for Digital Systems

Lec 12: March 13, 2024

Ratioed Logic and Design-Space Exploration





Today

- Ratioed Logic
 - Break all the rules... (lose our nice properties)
 - Not rail-to-rail signals, steady-state-current...
 - Correctness

Ratioed Logic





Previously

- ❑ Restoration and Noise Margins
 - Allows for gate abstraction
- ❑ CMOS Gates
 - Drive outputs rail-to-rail
 - Only one PDN/PUN turned on in steady state
 - Only subthreshold leakage current in steady state



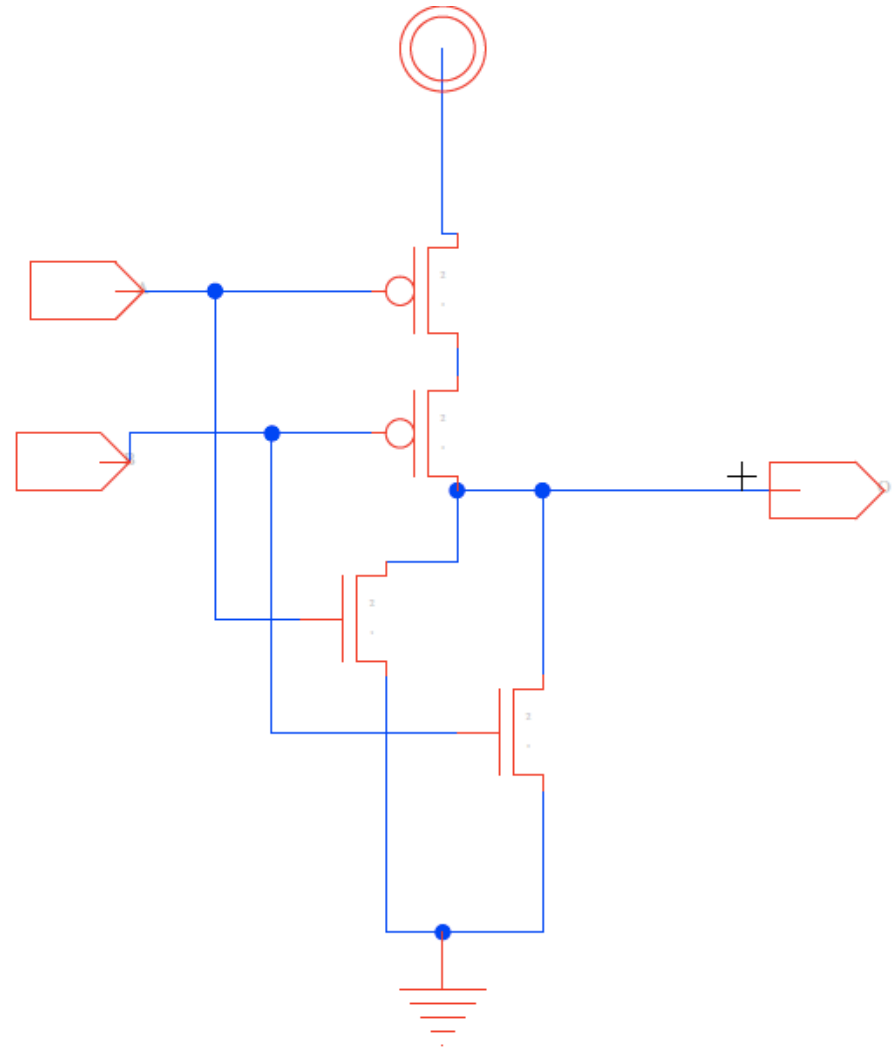
Today

□ Ratioed Gates

- Break all the rules... (nice properties)
 - No rail-to-rail outputs, steady-state-current is not subthreshold...
- Logic correctness
- Performance
- Power implications

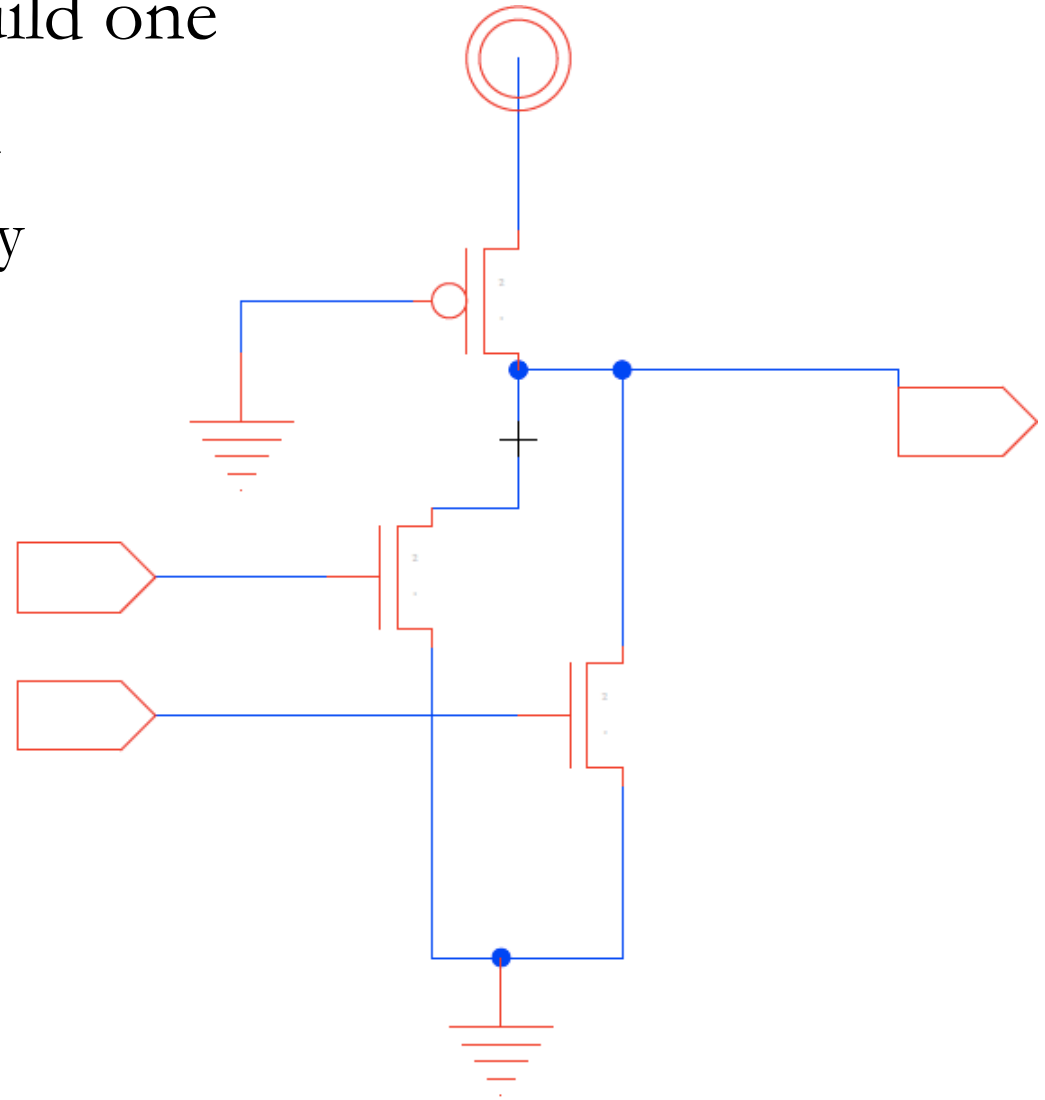
Idea

- ❑ Building both pull-up and pull-down can be expensive – many gates
- ❑ Seems wasteful to build logic function twice
 - Once in pullup, once in pulldown
 - Large gate capacitance



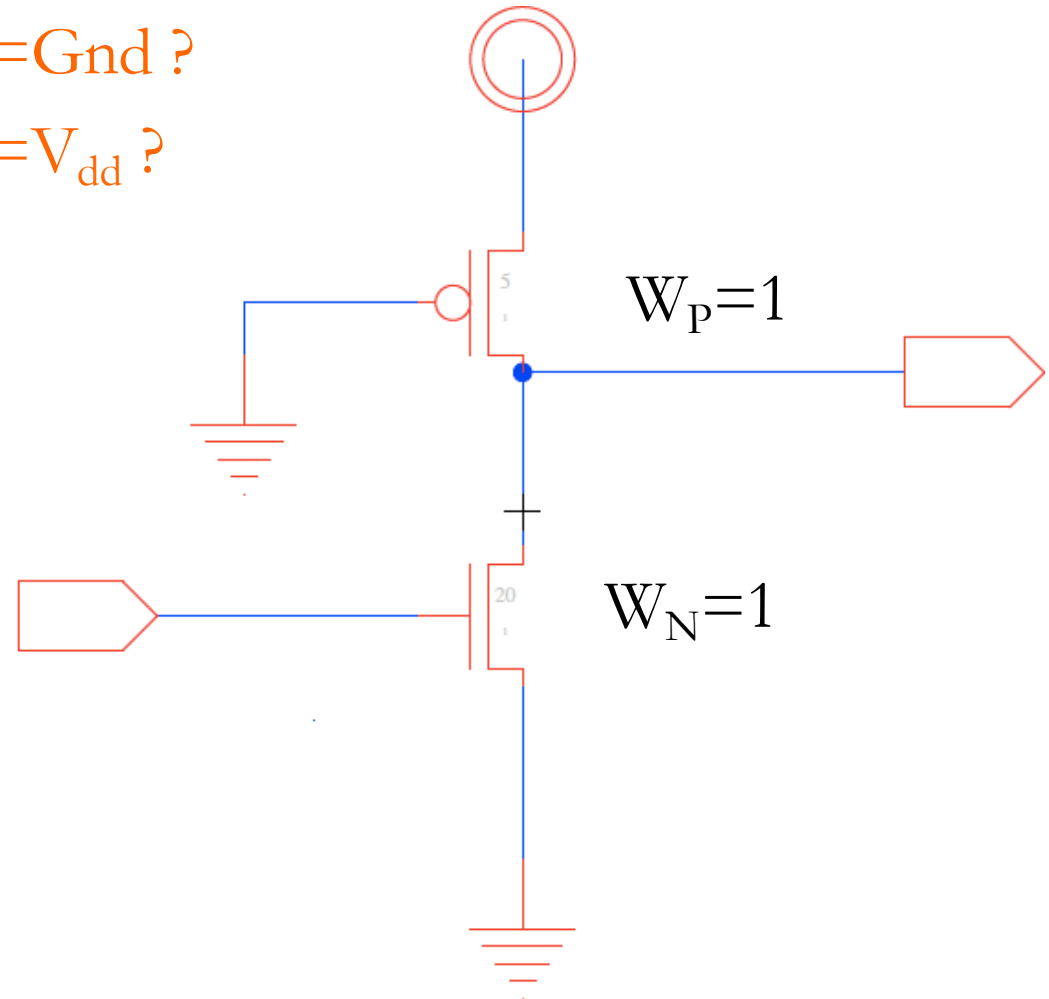
Idea

- ❑ Maybe only need to build one
- ❑ Build NFET pulldown
 - Exploit high N mobility
 - traditional



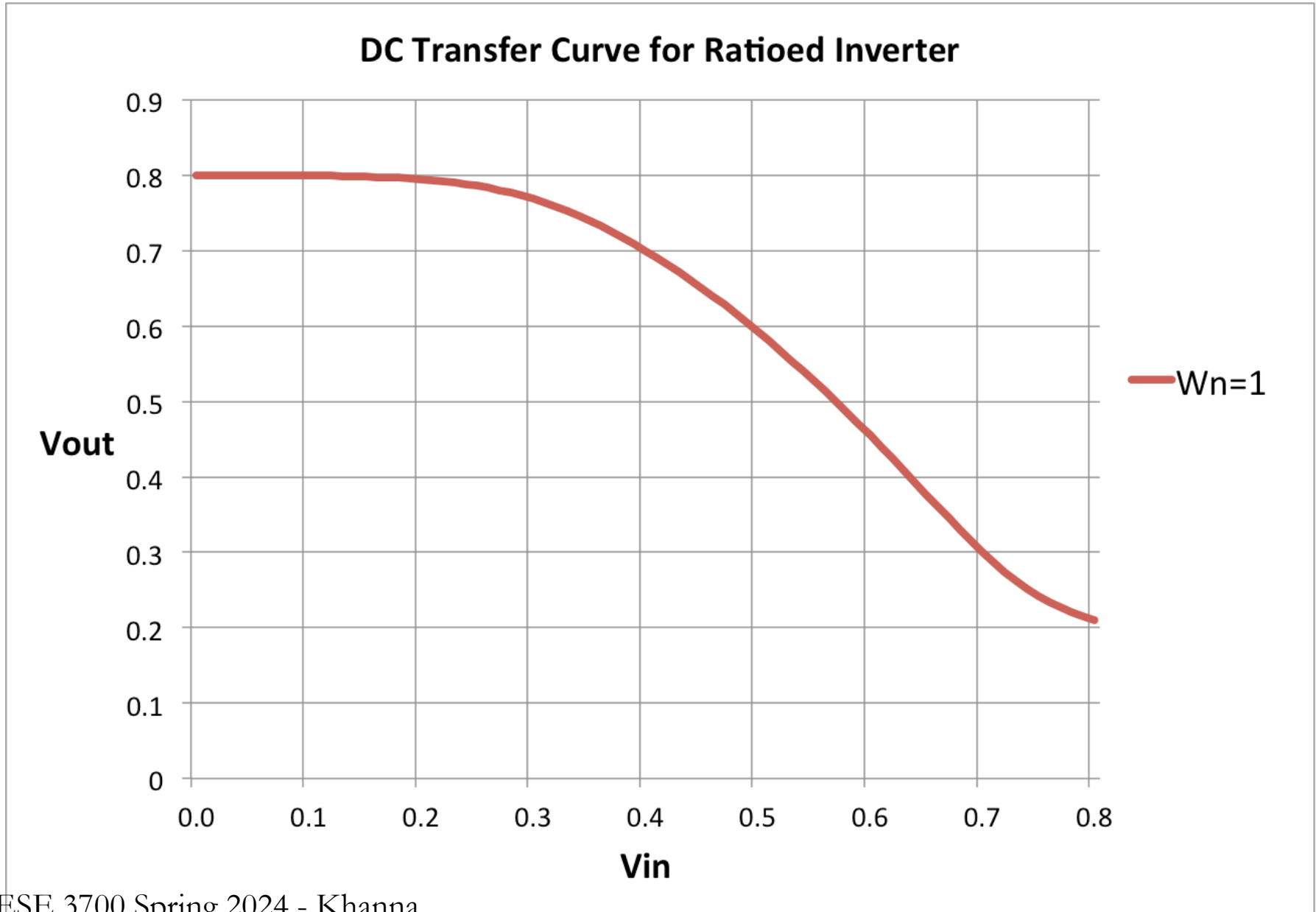
Ratioed Inverter

- Does this work?
 - What is V_{out} for $V_{in} = Gnd$?
 - What is V_{out} for $V_{in} = V_{dd}$?



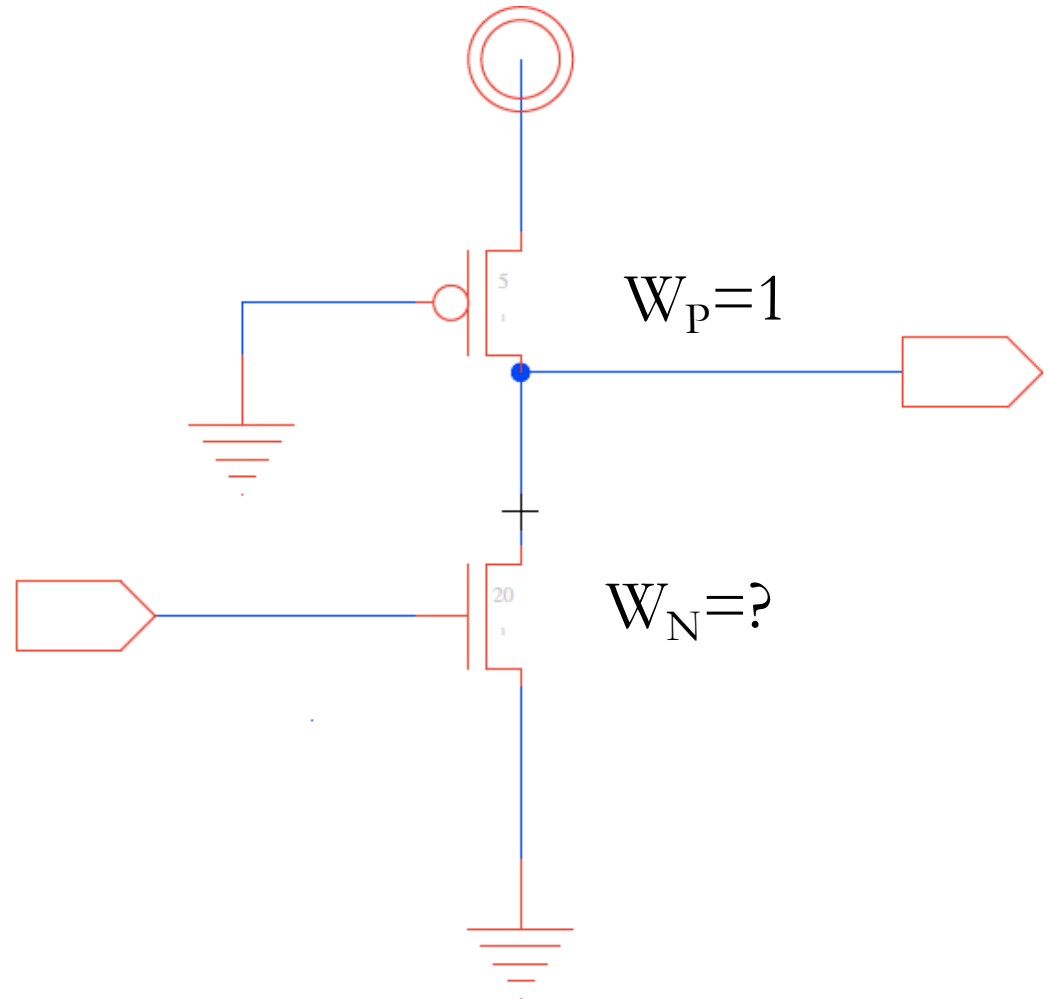


Ratioed Inverter in 22nm

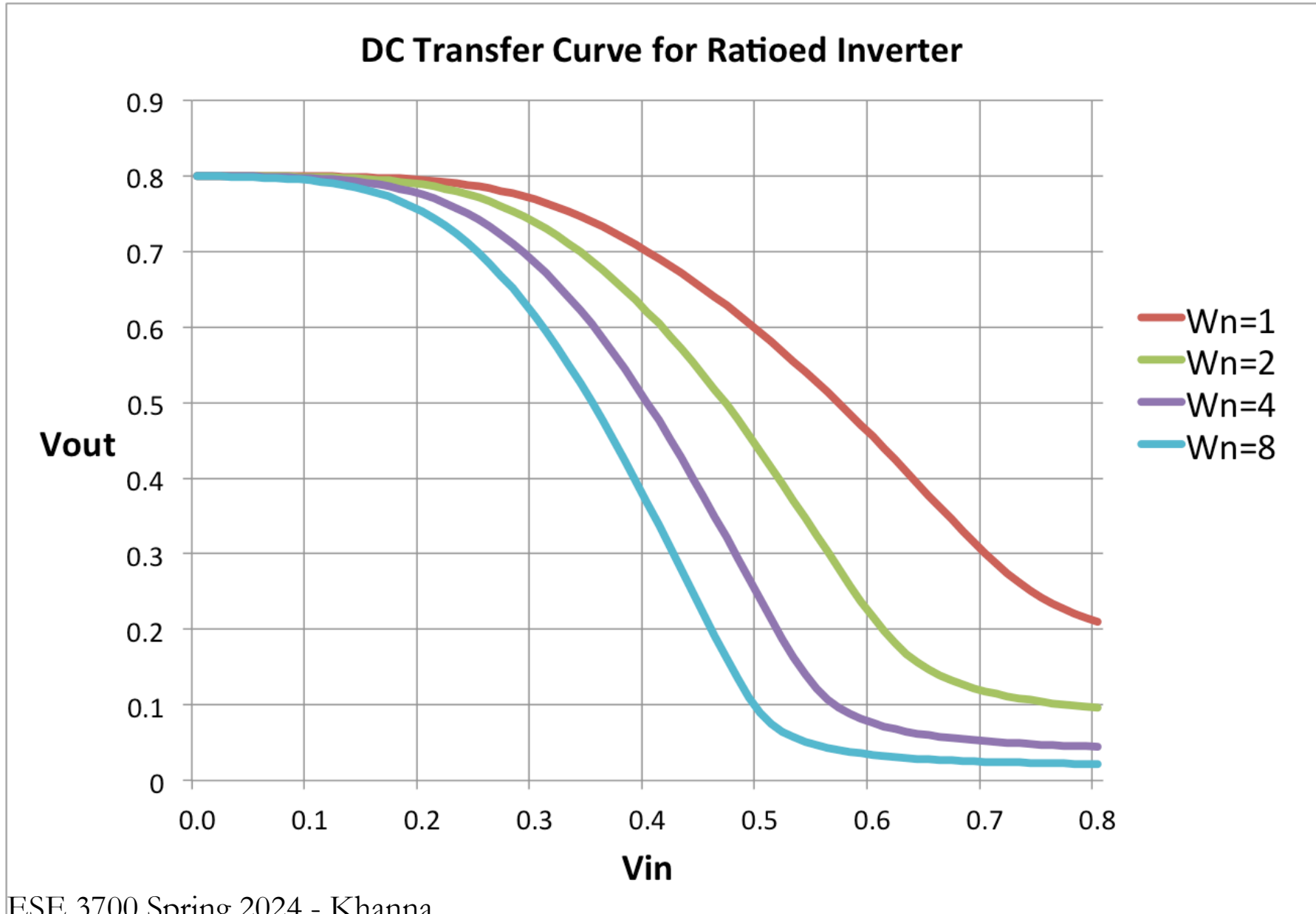


Ratioed Inverter (Preclass 1)

- How do we need to size N to make it “work”?
 - $V_{DD}=0.8$

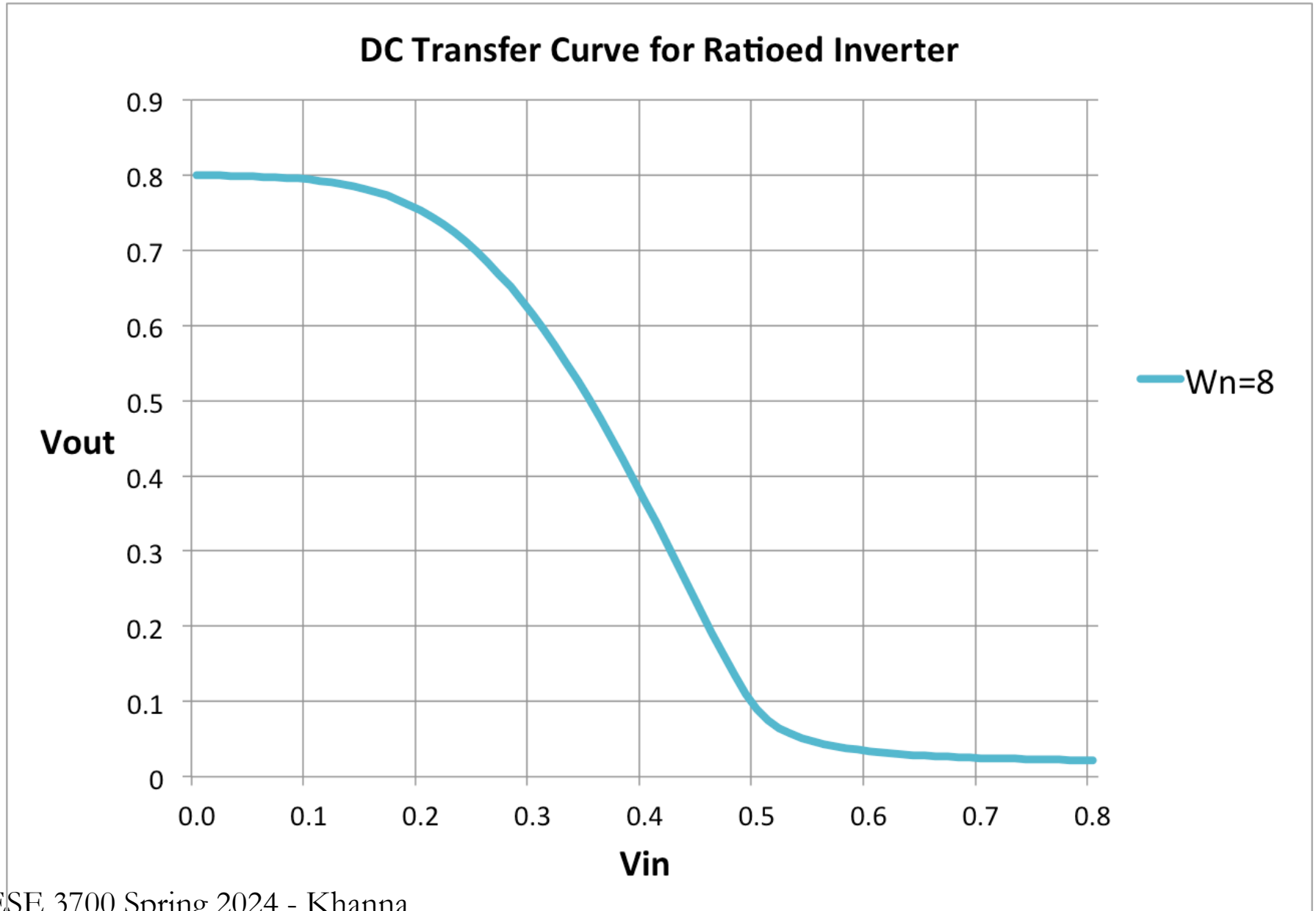


Ratioed Inverter in 22nm



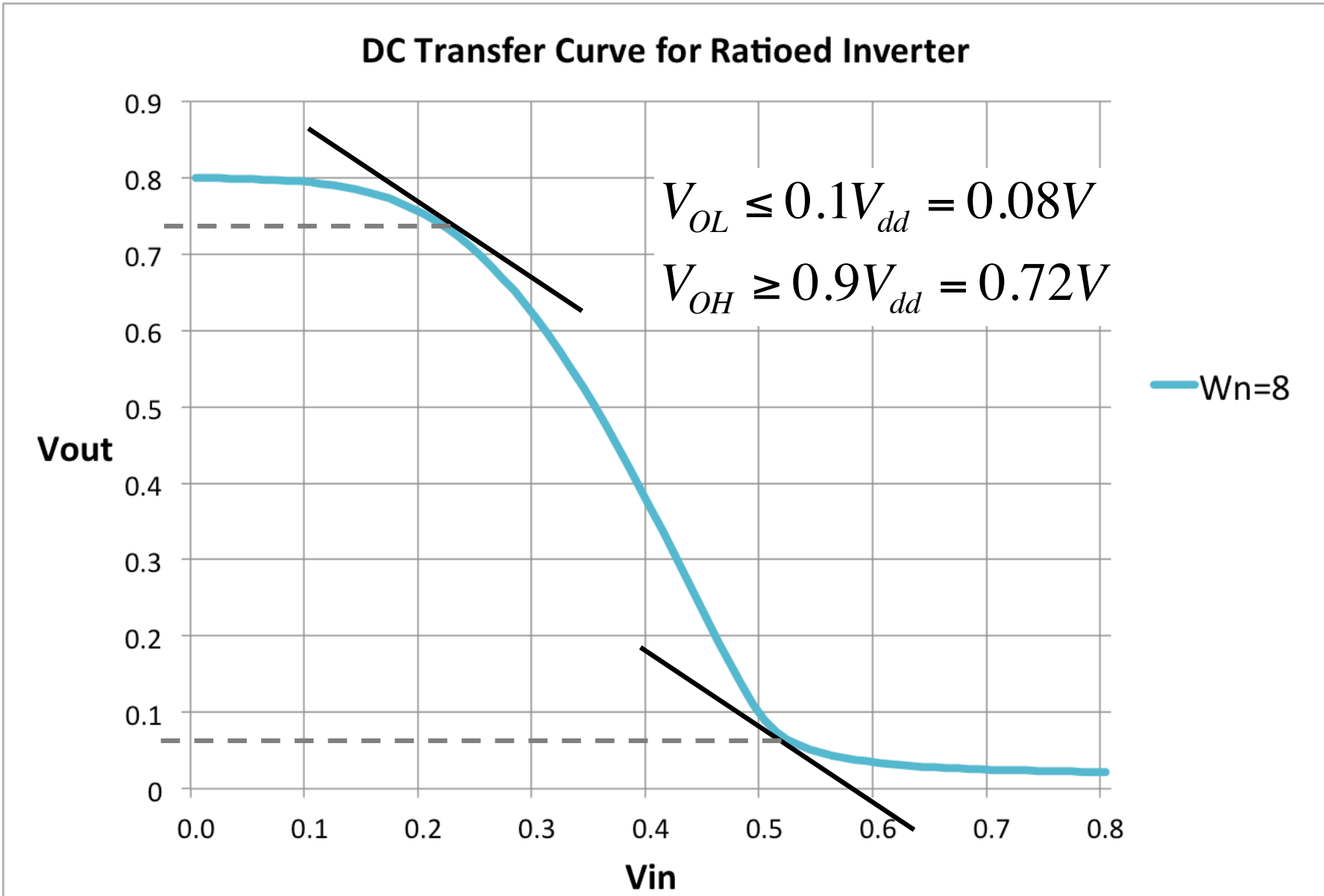


DC Transfer Function



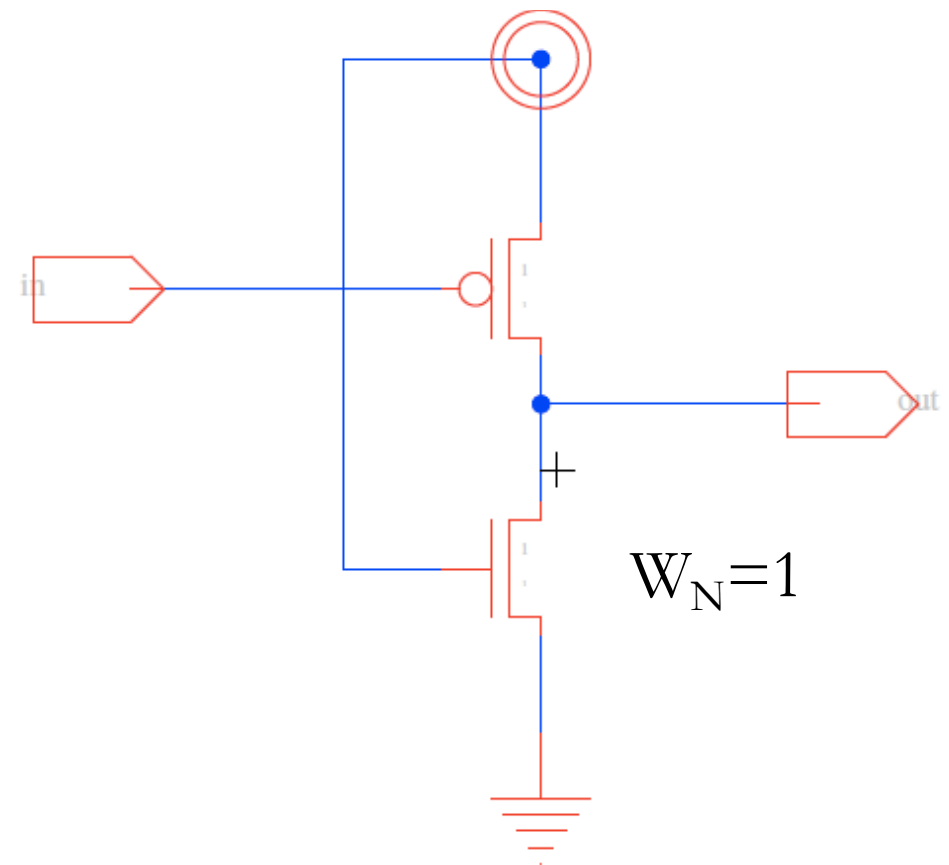


DC Transfer Function

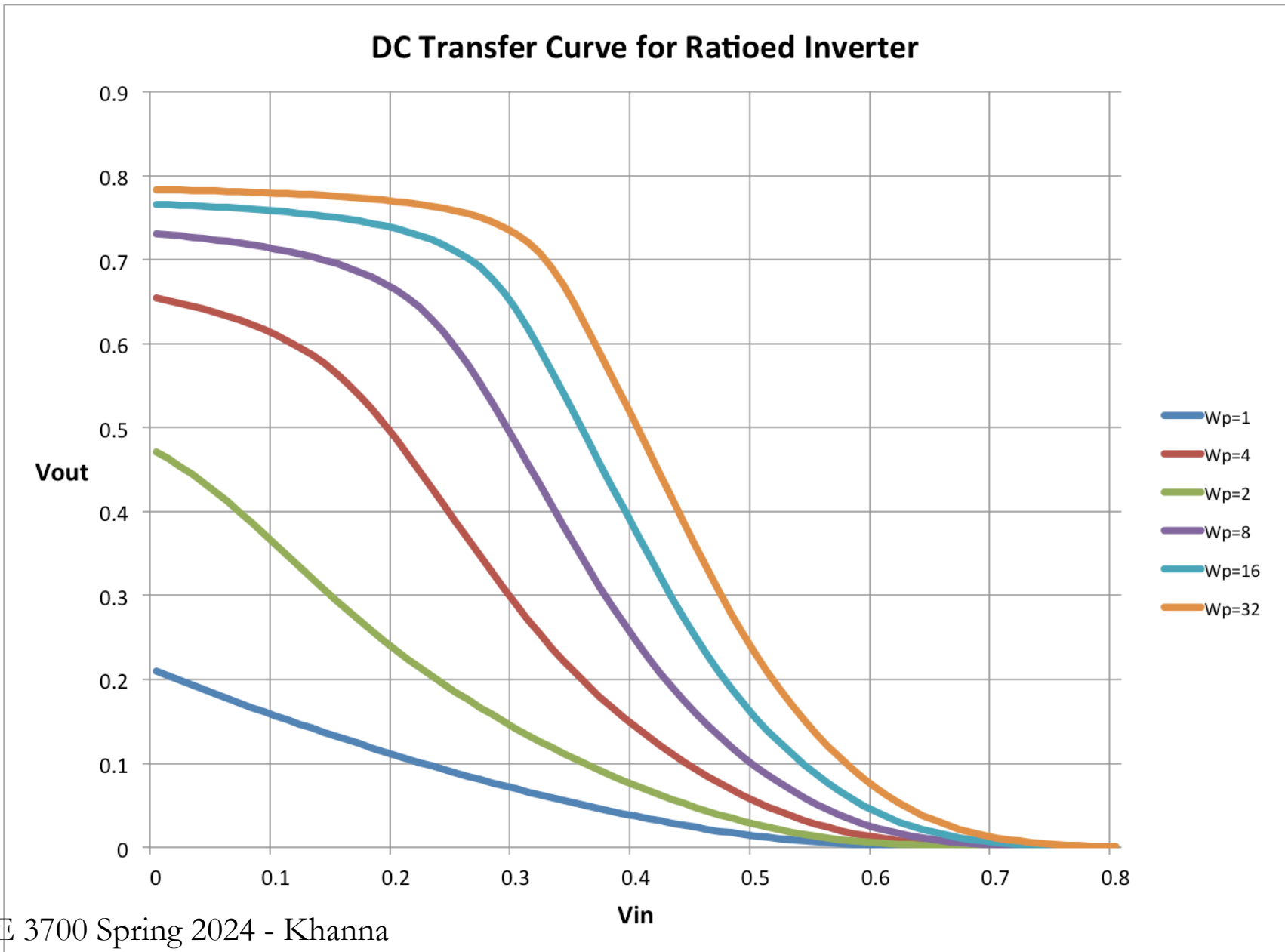


Ratioed Inverter (Preclass 1)

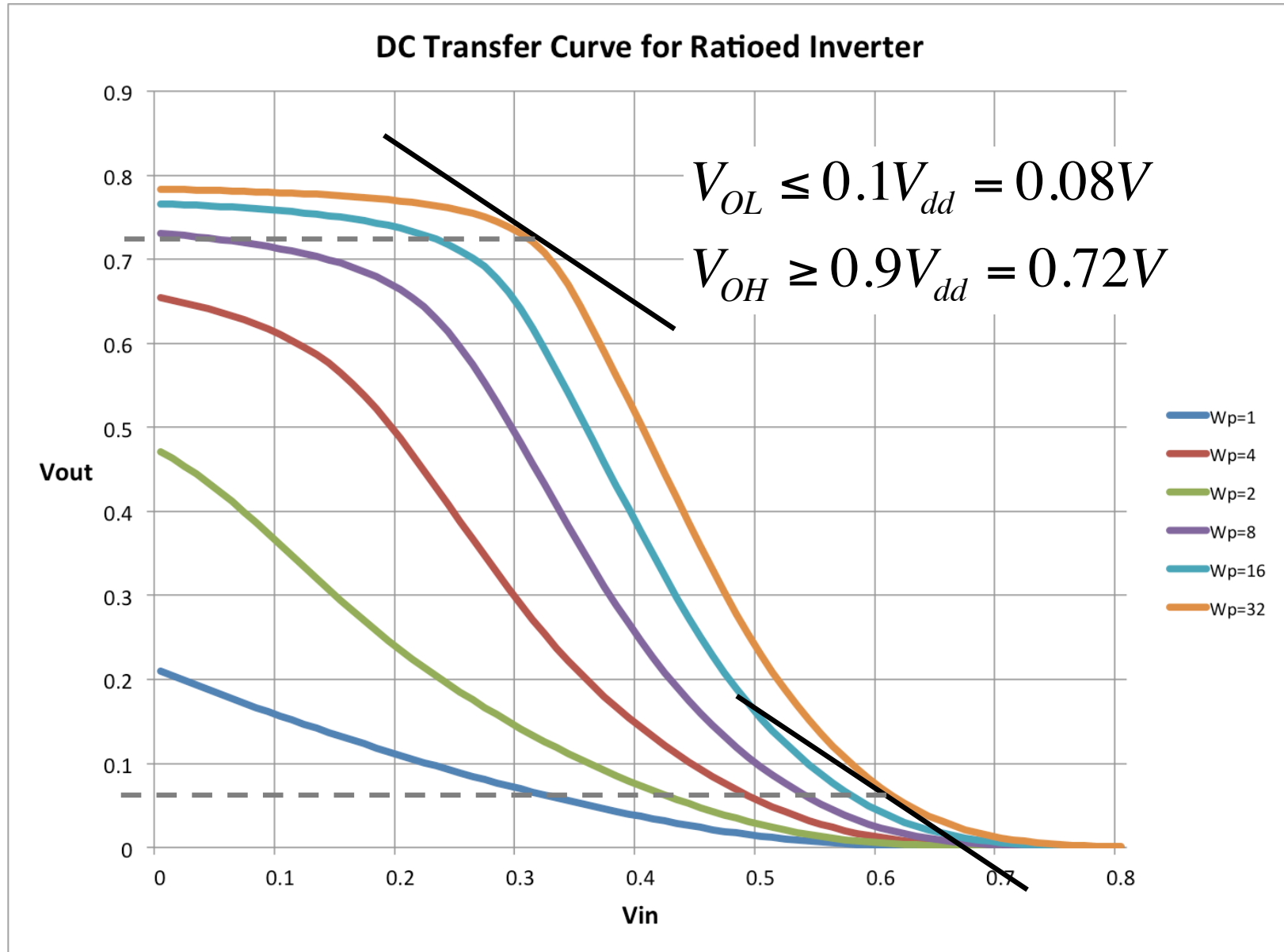
- How do we need to size P to make it work?
 - $V_{DD}=0.8$



Ratioed Inverter in 22nm



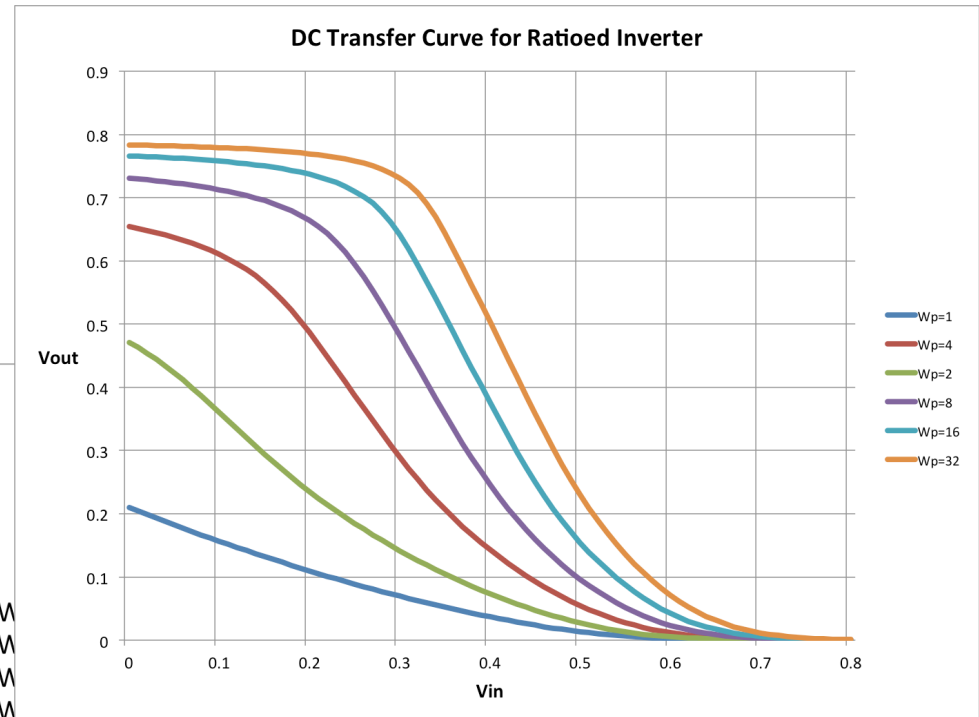
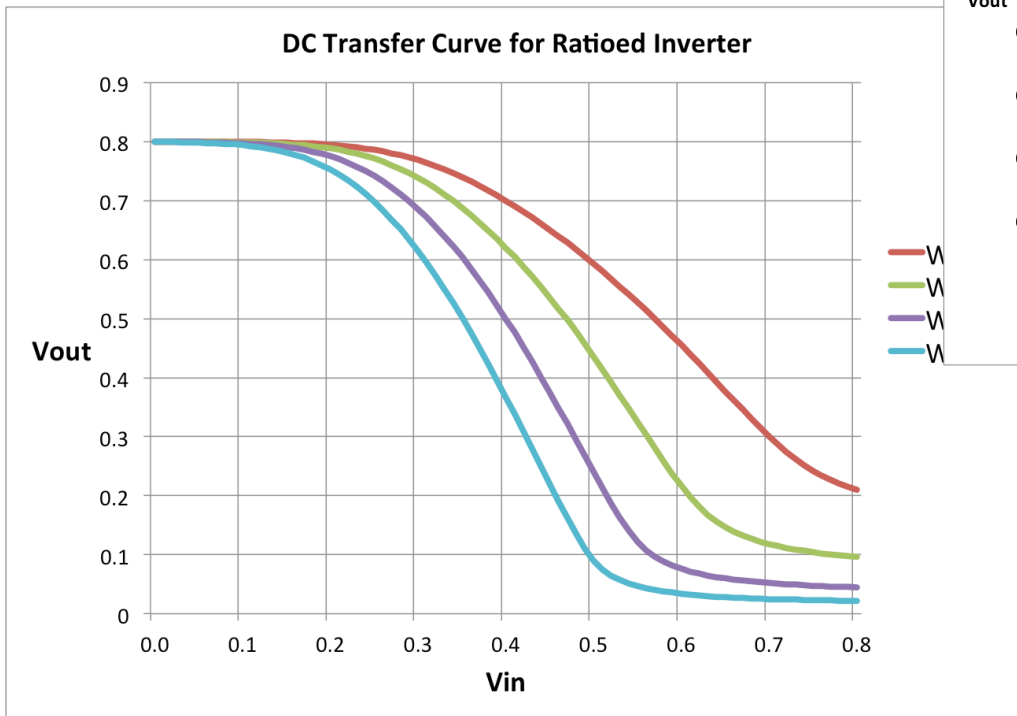
Ratioed Inverter in 22nm





P vs. N

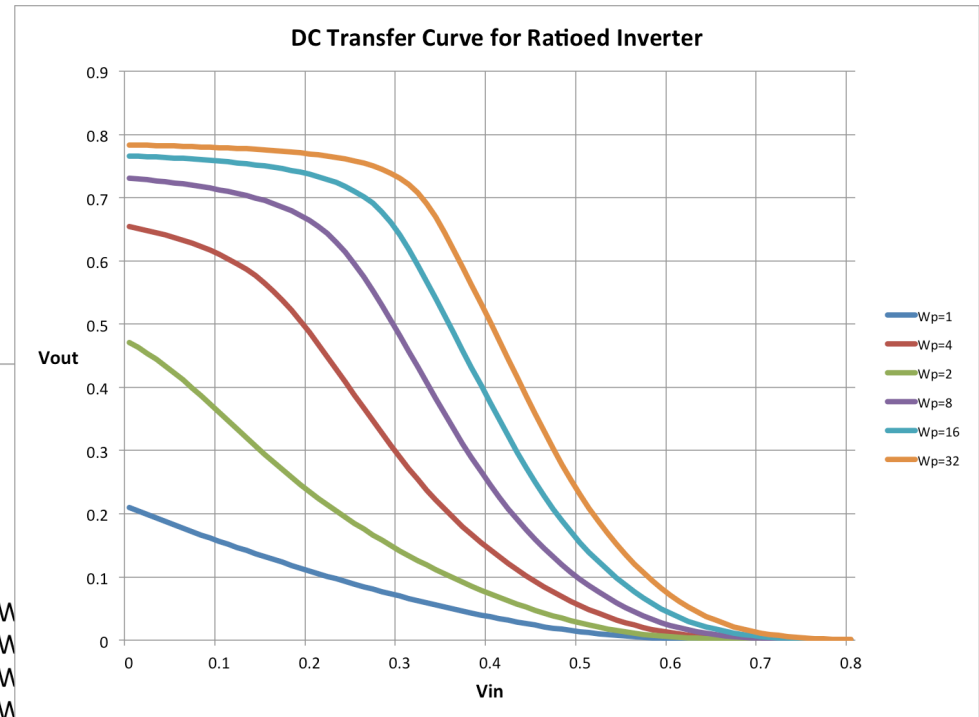
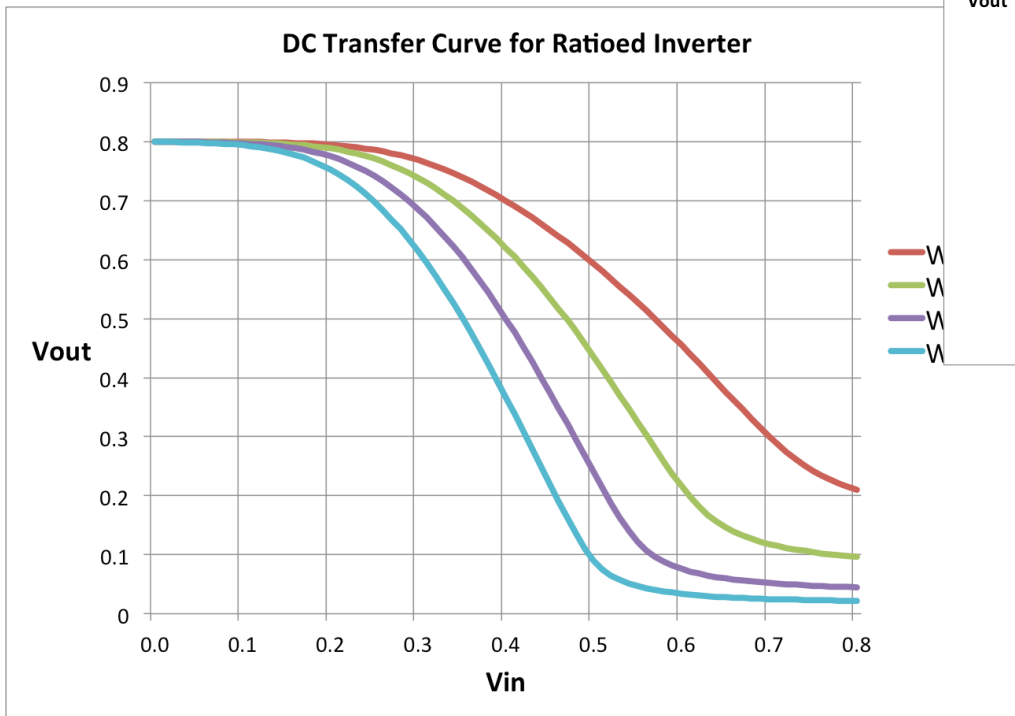
❑ **Conclude:** still prefer N to P for ratioed logic



Noise Margin Tradeoff

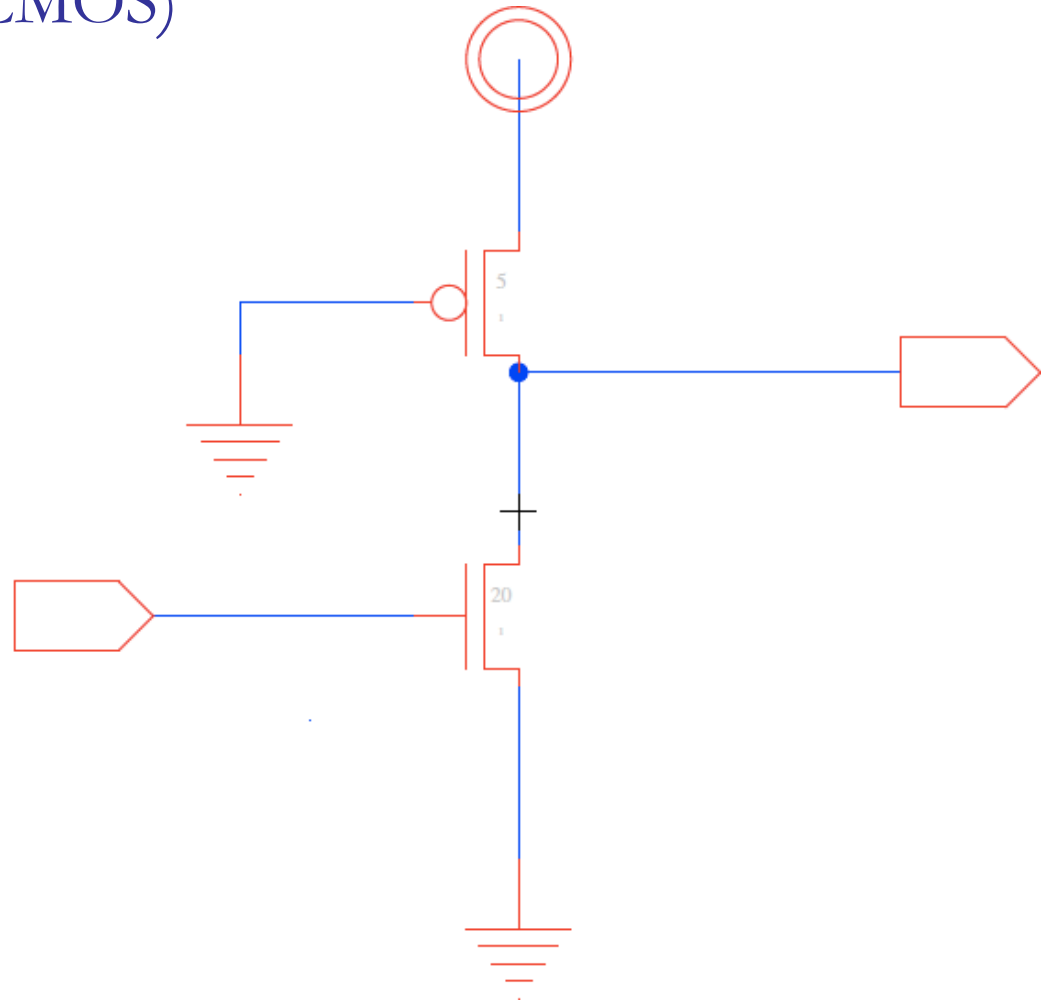
□ What is impact of increasing noise margin?

- On size
- On input capacitance



Size for $R_0/2$ drive?

- How do we size for $R_0/2$ drive?
 - (assume $R_{0p} = R_{0n}$ for CMOS)

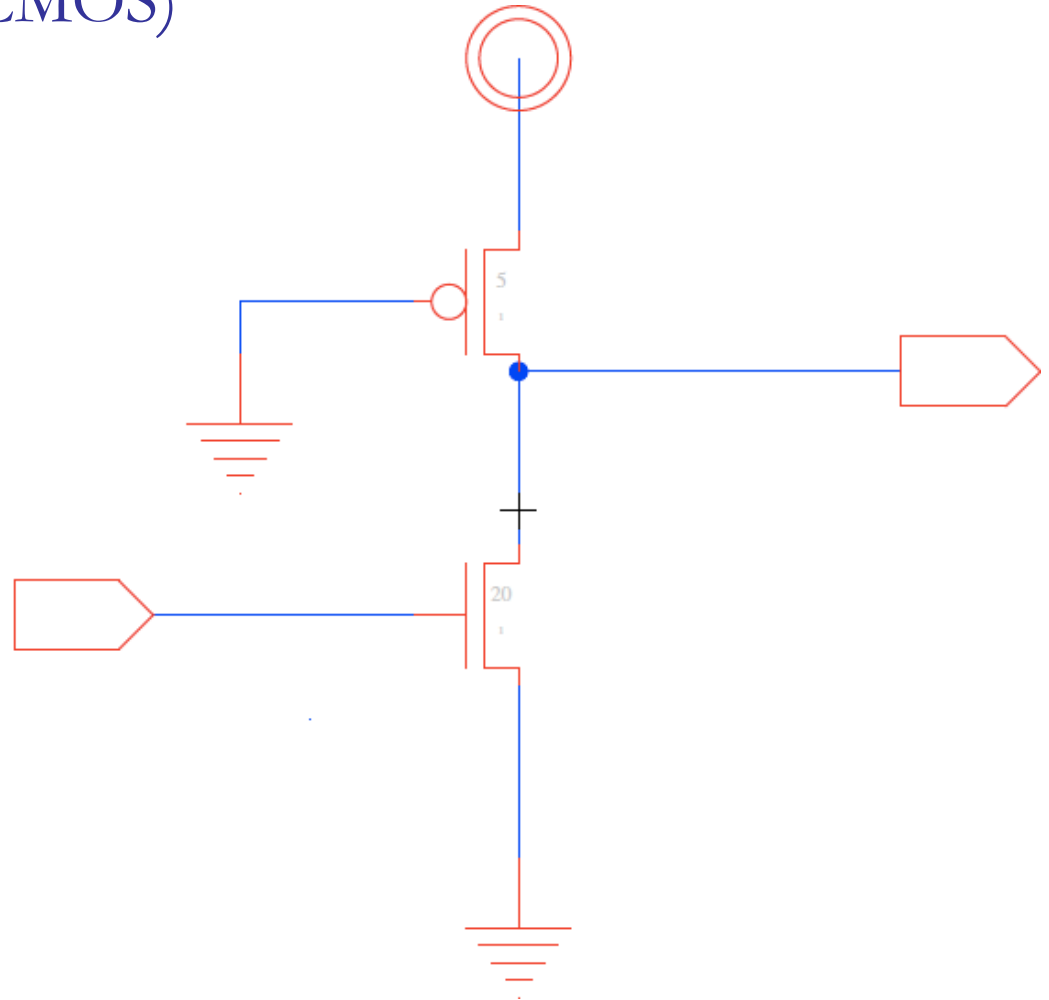


Size for $R_0/2$ drive? (Preclass 2)

- How do we size for $R_0/2$ drive?
 - (assume $R_{0p} = R_{0n}$ for CMOS)

$$R_{drive} = \frac{R_{op}}{W_p} = \frac{R_0}{W_p} = \frac{R_0}{2}$$

$$\Rightarrow W_p = 2$$



Size for $R_0/2$ drive?

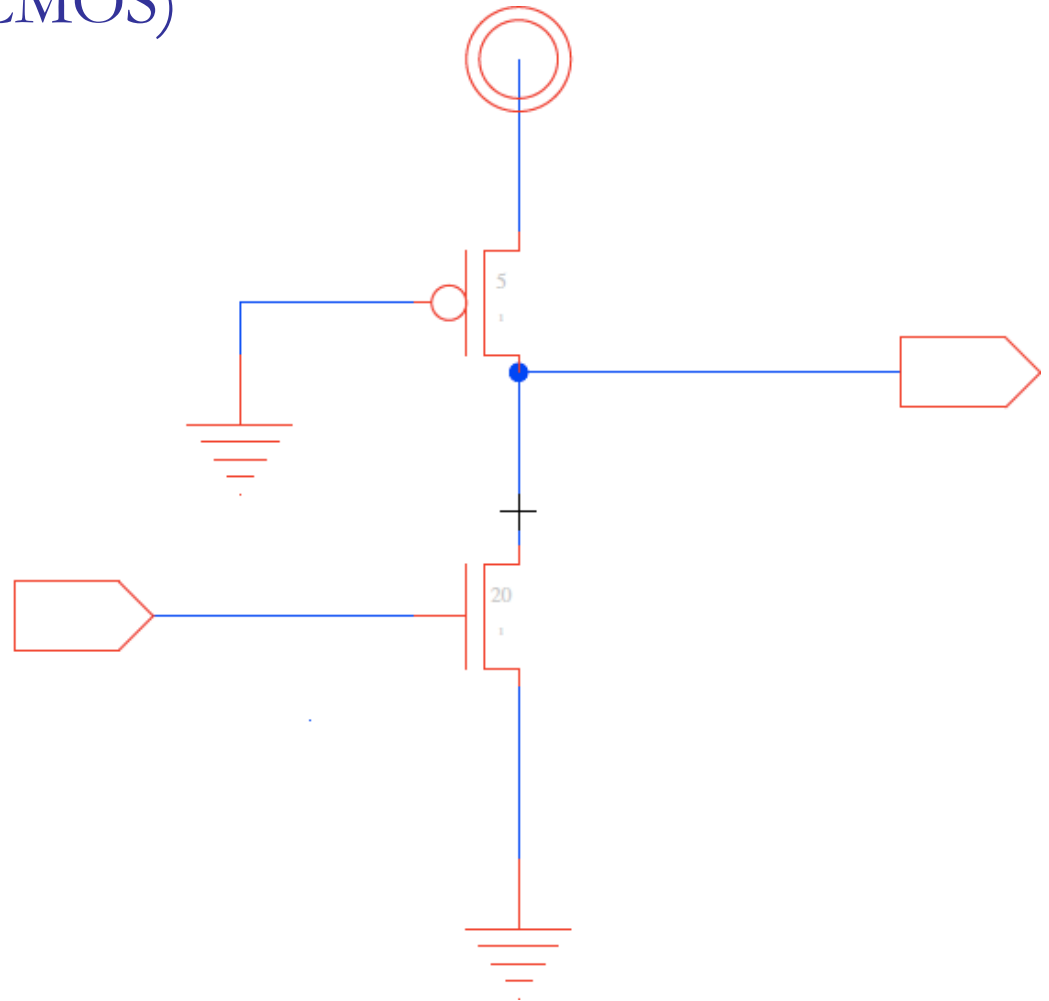
- How do we size for $R_0/2$ drive? What is C_{in} ?
 - (assume $R_{0p} = R_{0n}$ for CMOS)

$$R_{drive} = \frac{R_{op}}{W_p} = \frac{R_0}{W_p} = \frac{R_0}{2}$$

$$\Rightarrow W_p = 2$$

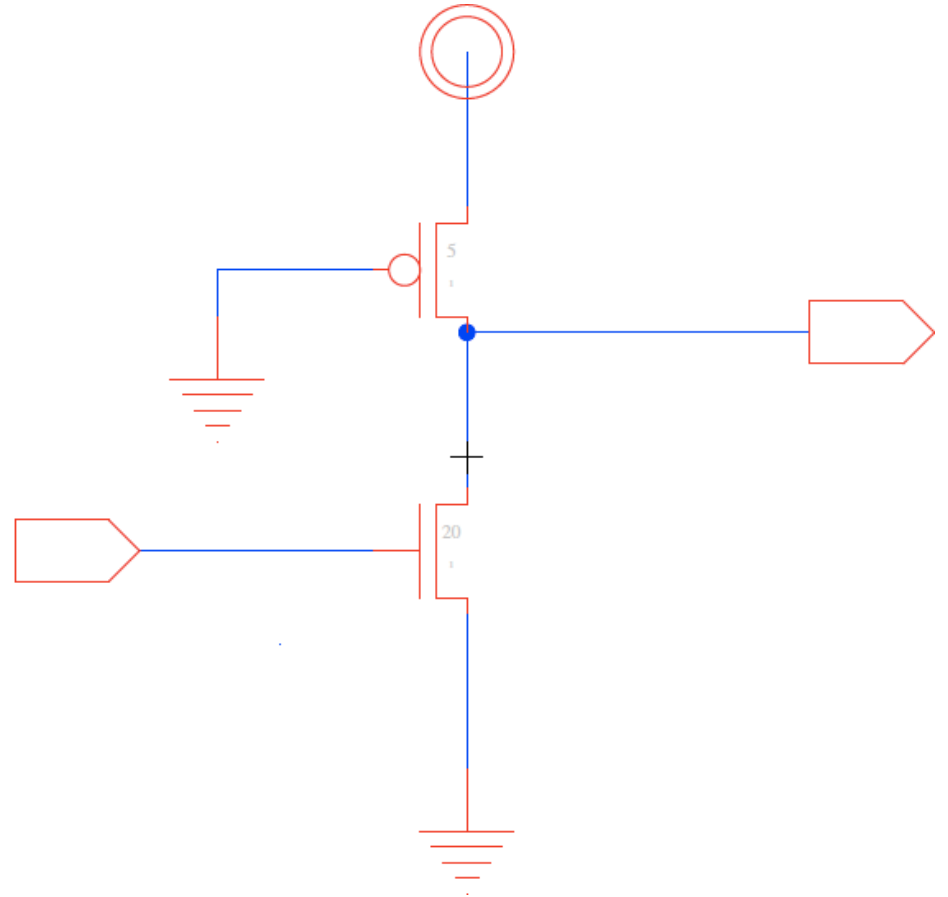
$$W_n > 8W_p$$

$$\Rightarrow W_n = 16$$



Static Power

- I_{static} ?
- Input low-Output high?
 - I_{leak}
- Input high-Output low?
 - $I_{\text{pmos_on}}$
 - $\sim V_{\text{dd}} / (R_0 / 2)$ -- for our sample case





Total Power

□ $P_{\text{tot}} \approx a(C_{\text{load}} + 2C_{\text{sc}})V^2f$



Total Power

$$\begin{aligned} \square P_{\text{tot}} &\approx a(C_{\text{load}} + 2C_{\text{sc}})V^2f \\ &\quad + p(V_{\text{out}}=\text{low})V^2/R_{\text{pon}} \\ &\quad + p(V_{\text{out}}=\text{high})VI'_s(W/L)e^{-V_t/(nkT/q)} \end{aligned}$$

$p(V_{\text{out}}=\text{low})$ – probability the output is low

$p(V_{\text{out}}=\text{high})$ – probability the output is high

$$p(V_{\text{out}}=\text{high}) = 1 - p(V_{\text{out}}=\text{low})$$



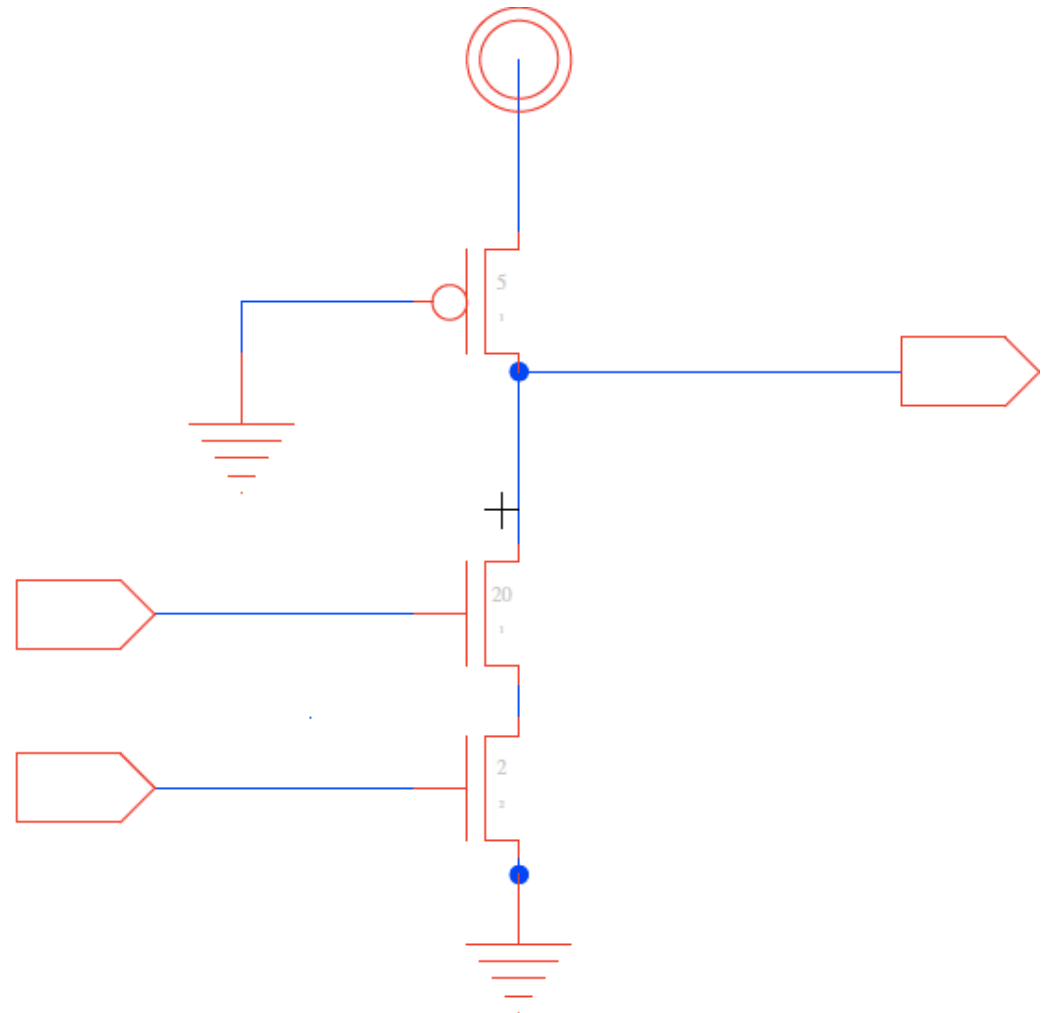
Compare Static CMOS

For $R_{\text{drive}} = R_0/2$ inverter (assume $R_{0p} = R_{0n}$ for CMOS)

- ❑ Total Transistor Width?
- ❑ Input capacitance load?

How do we size for $R_0/2$ drive?

- 2-input nand?

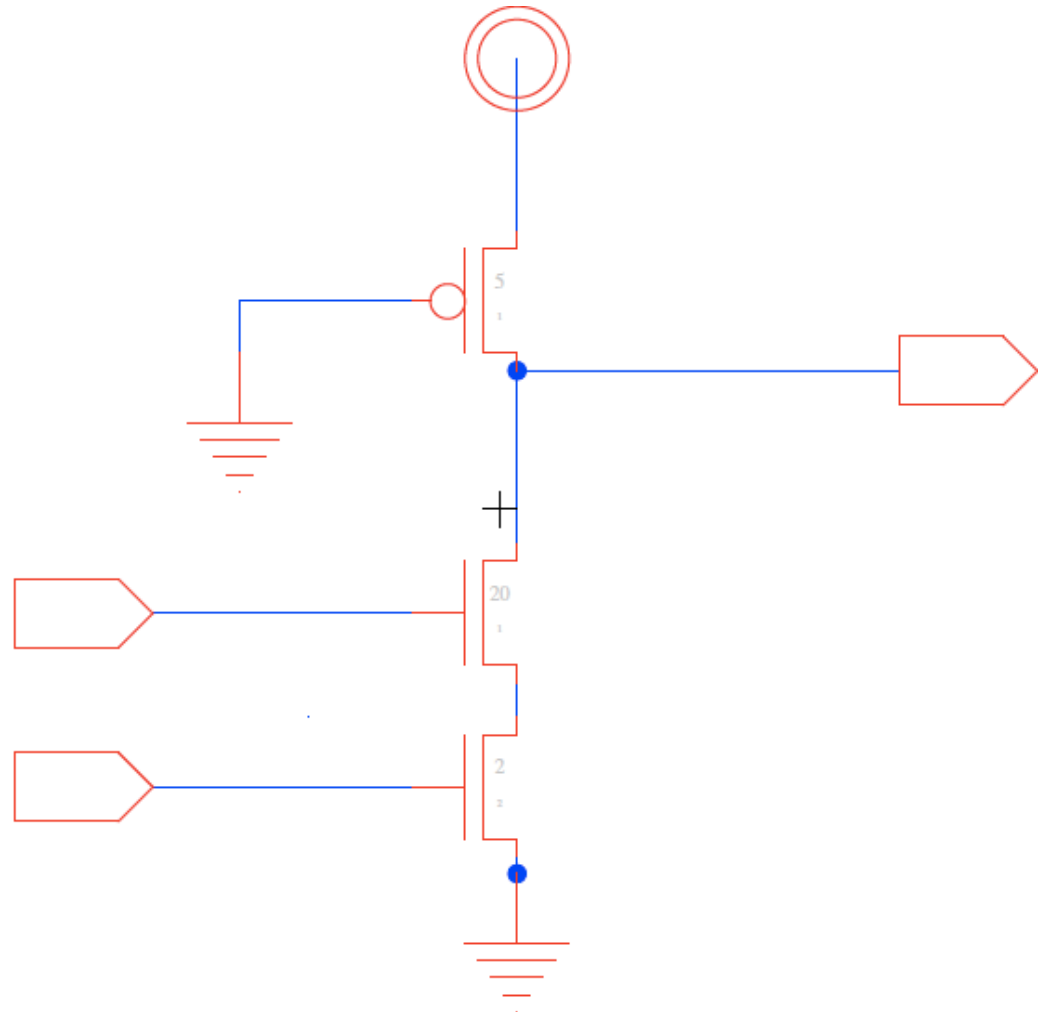


How do we size for $R_0/2$ drive?

□ 2-input nand?

$$R_{drive} = \frac{R_{op}}{W_p} = \frac{R_0}{W_p} = \frac{R_0}{2}$$

$$\Rightarrow W_p = 2$$



How do we size for $R_0/2$ drive?

□ 2-input nand? What is C_{in} ?

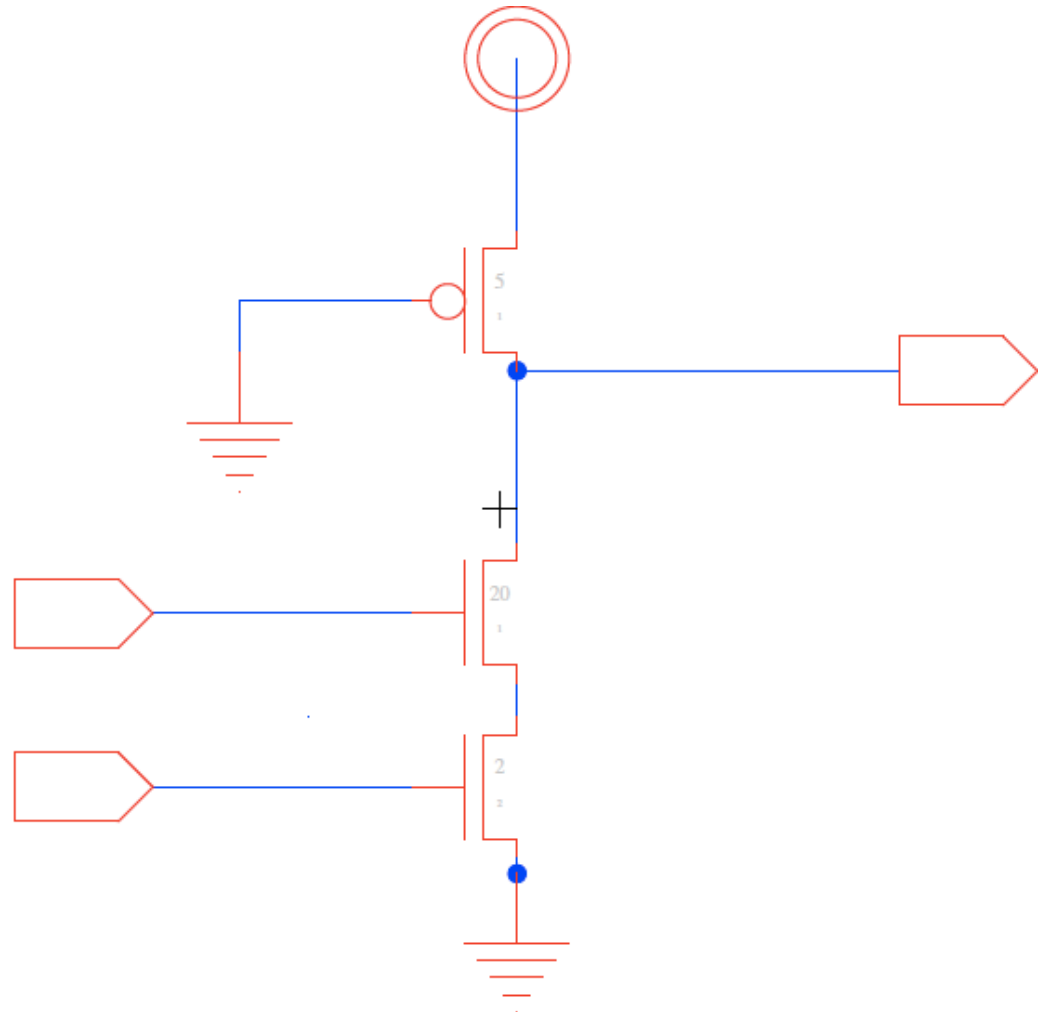
$$R_{drive} = \frac{R_{op}}{W_p} = \frac{R_0}{W_p} = \frac{R_0}{2}$$

$$\Rightarrow W_p = 2$$

$$R_{drive,pdn} = \frac{2R_0}{W_n} = \frac{R_0}{W_n/2}$$

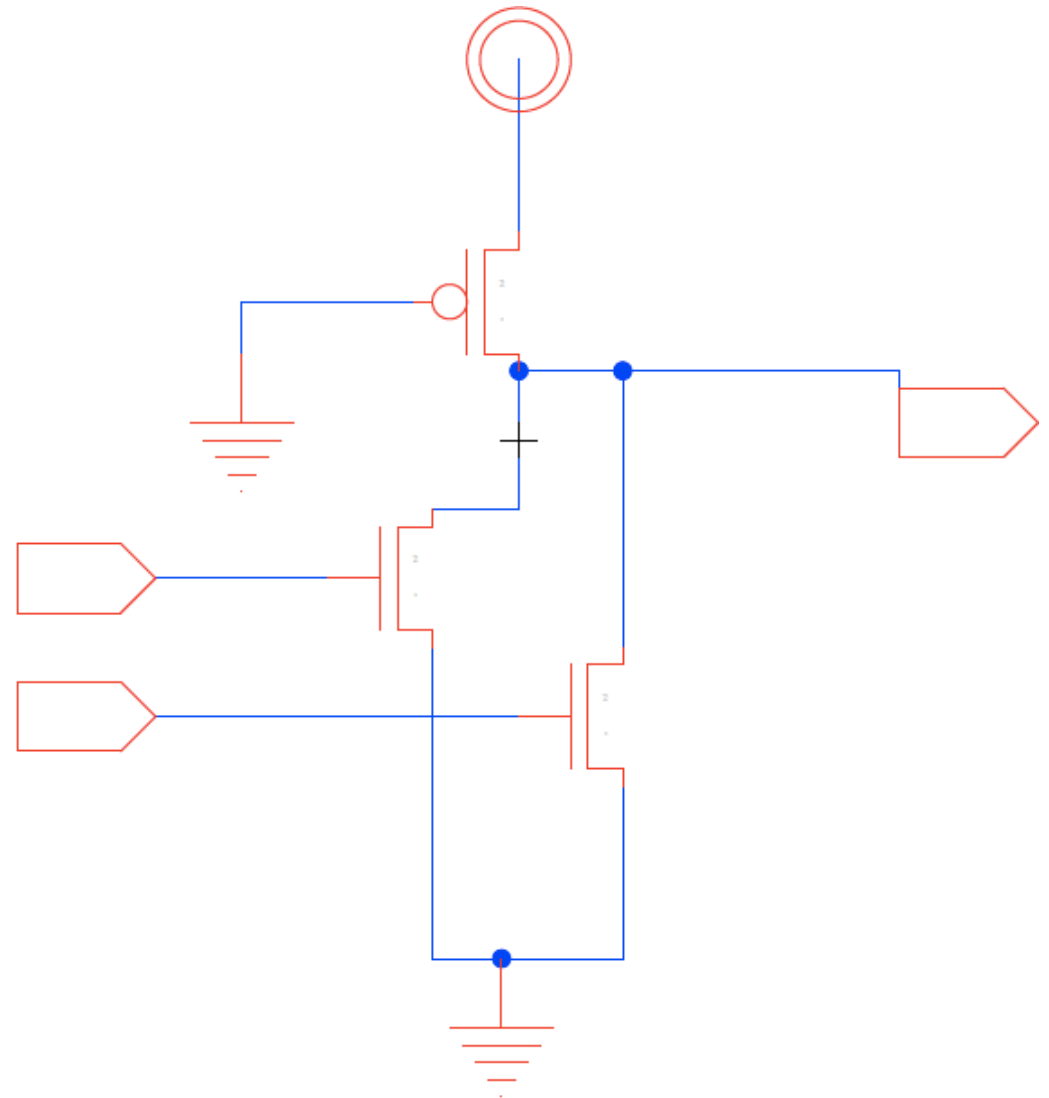
$$W_n/2 > 8W_p$$

$$\Rightarrow W_n = 32$$



How do we size for $R_0/2$ drive?

- 2-input nor?



How do we size for $R_o/2$ drive?

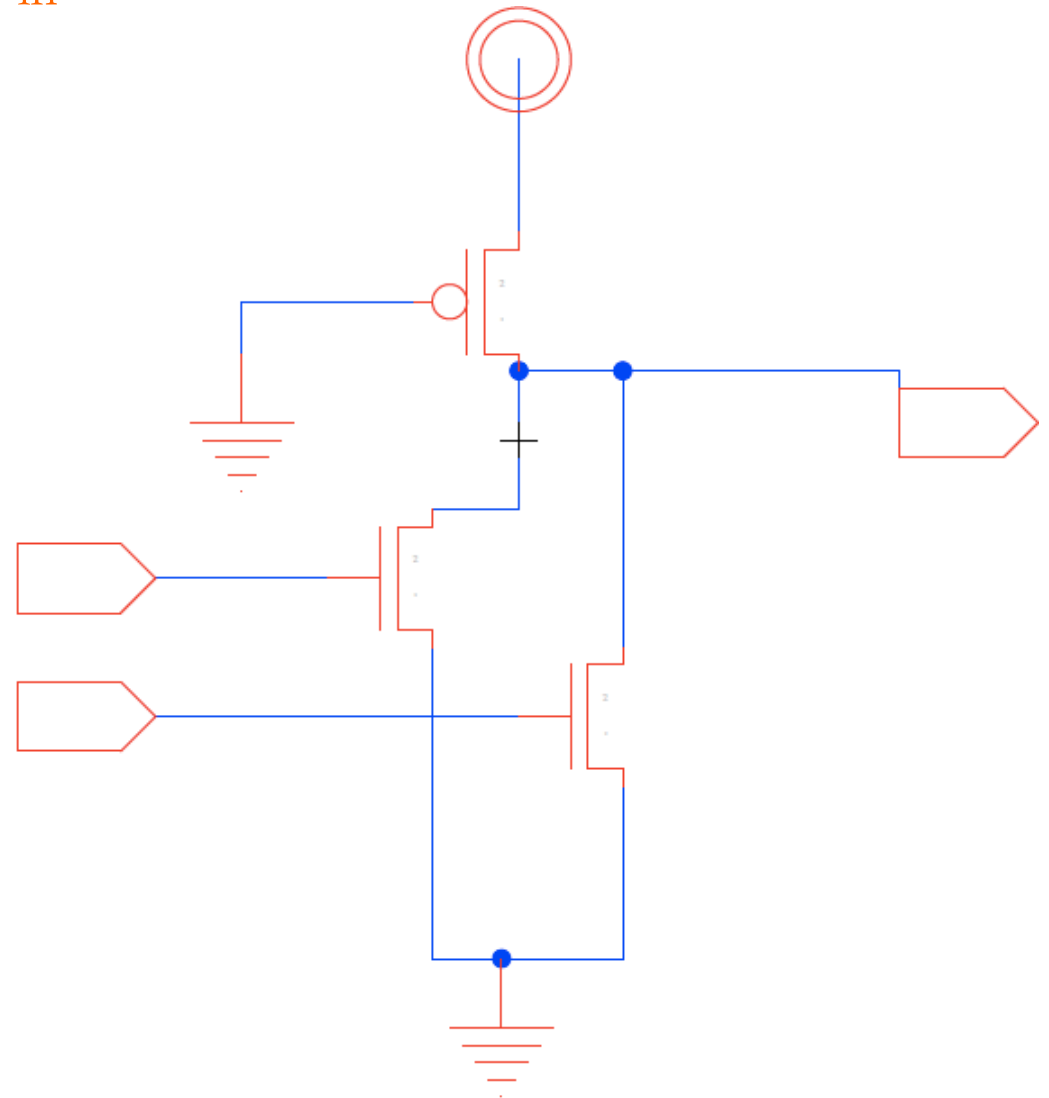
□ 2-input nor? What is C_{in} ?

$$R_{drive} = \frac{R_{op}}{W_p} = \frac{R_o}{W_p} = \frac{R_o}{2}$$

$$\Rightarrow W_p = 2$$

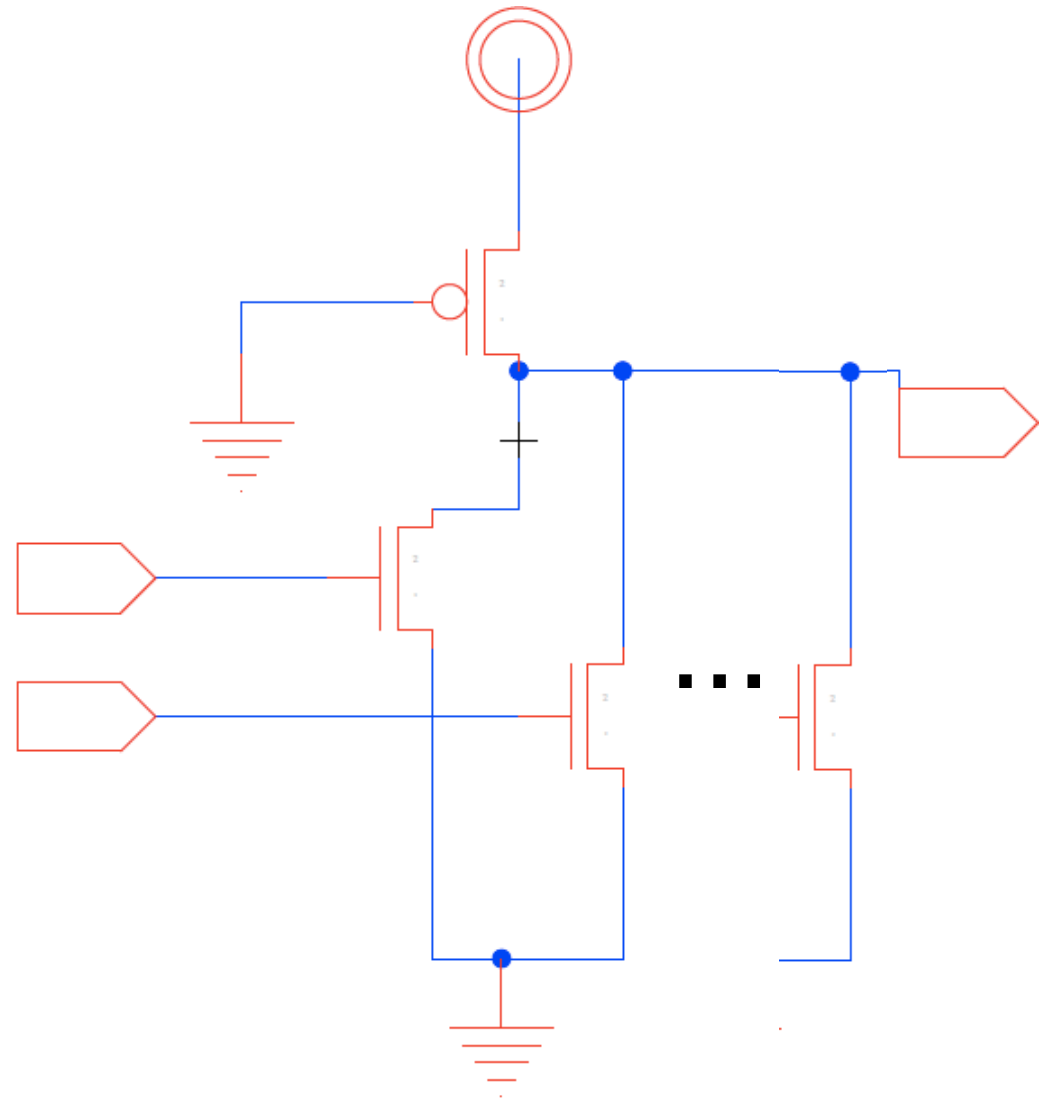
$$W_n > 8W_p$$

$$\Rightarrow W_n = 16$$

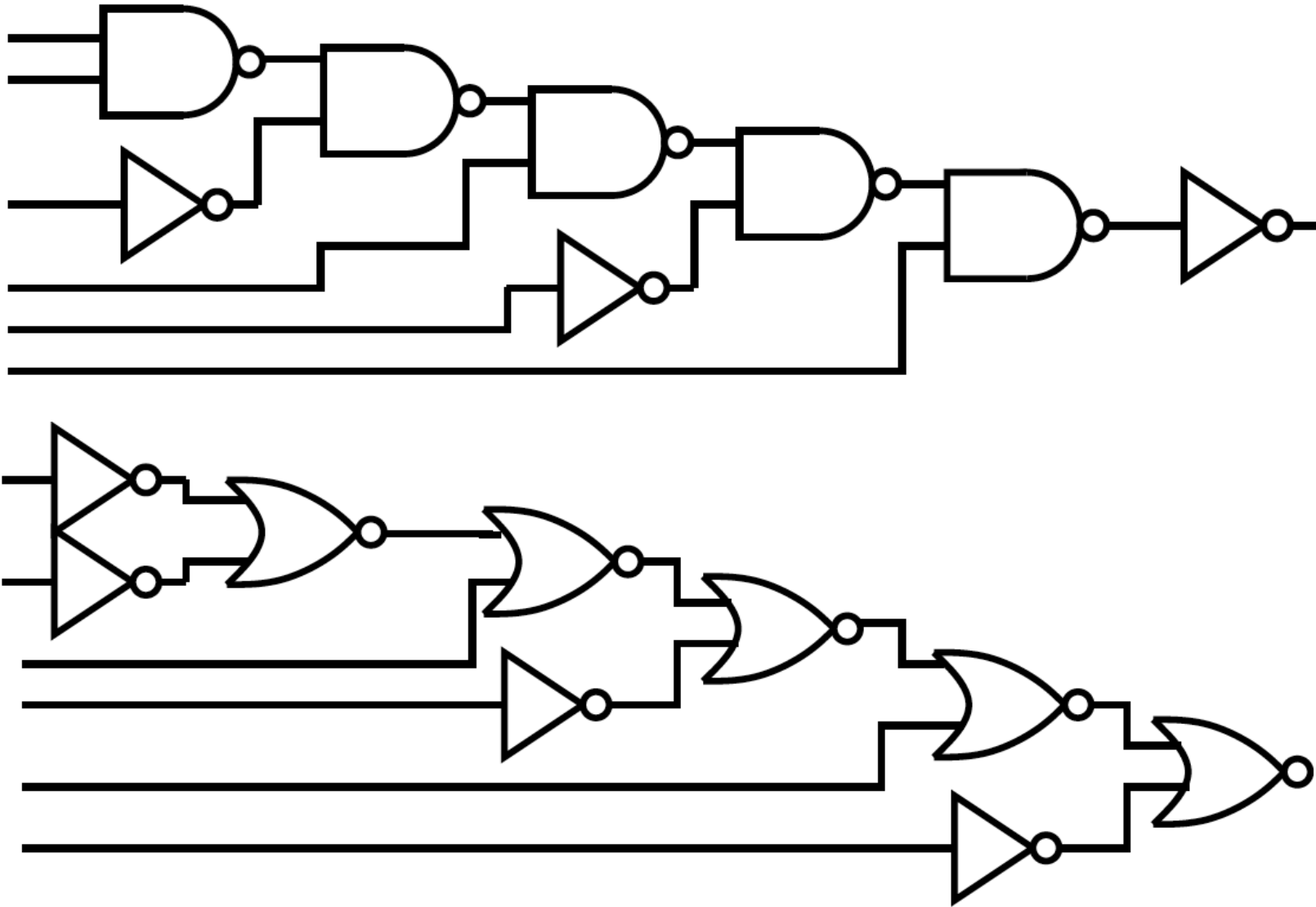


How do we size for $R_0/2$ drive? (Preclass 3)

- k-input nor?
- What is the input capacitance for k-input nor?



Which Implementation is faster in ratioed logic?



Design Space Exploration





Design Problem

- ❑ Function: Identify equivalence of two 32bit inputs
- ❑ Optimize: Minimize total energy
- ❑ Assumptions: Match case uncommon
 - Ie. Most of the time, the inputs won't be matched

- ❑ Deliberately focus on Energy to complement project
 - ...but will still talk about delay

Last page of preclass



Idea: Design Space Explore

- ❑ Identify options
 - All the knobs you can turn
- ❑ Explore space systematically
- ❑ Formulate continuum where possible
 - i.e. formulate trends and tradeoffs **quantitatively**



Problem Solvable (preclass 5a)

- ❑ Is it feasible?
 - First, make sure we have a solution so we know our main goal is optimization
- ❑ How do we decompose the problem?



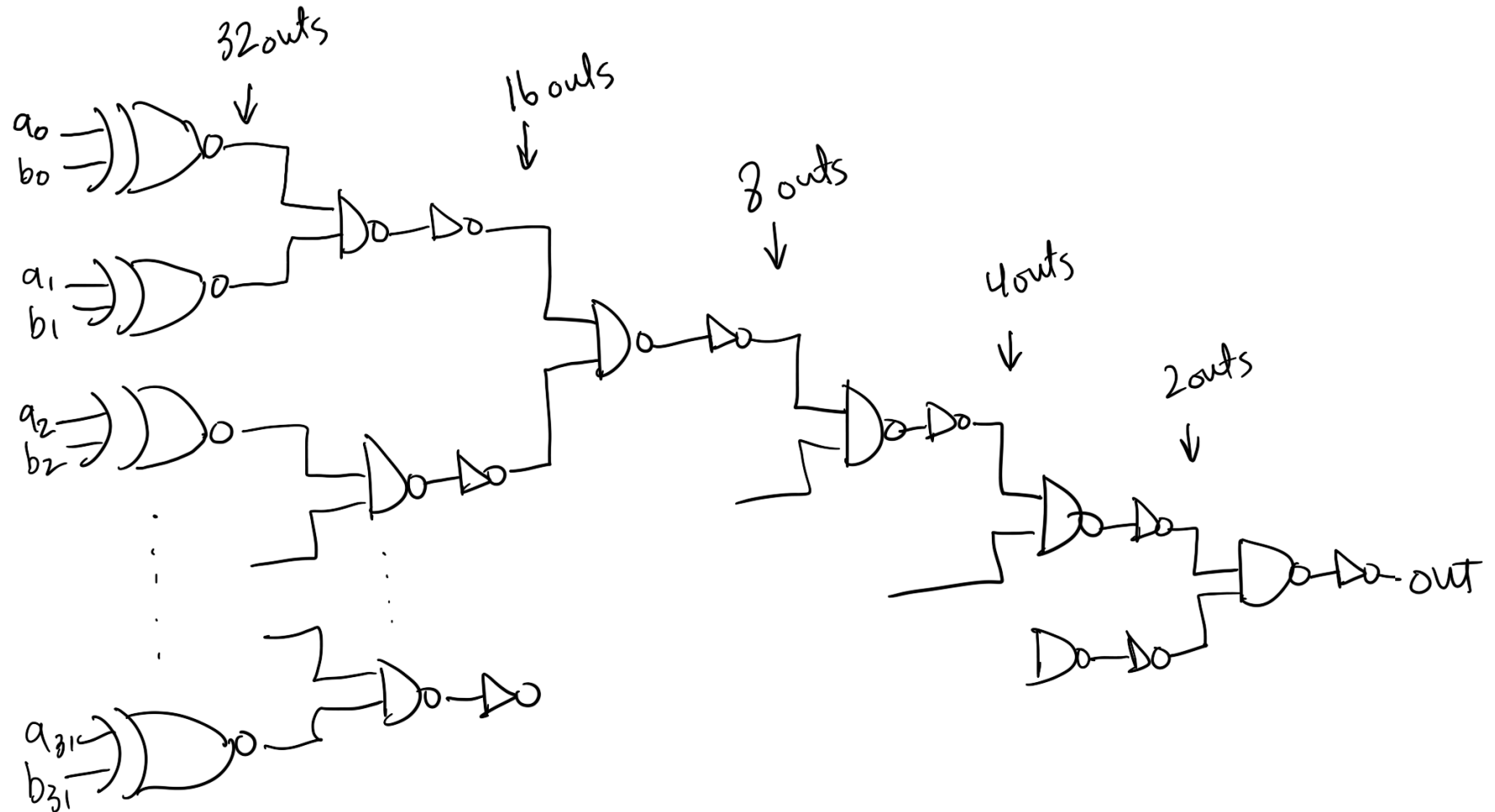
Problem Solvable (preclass 5b)

- ❑ Is it feasible?
 - First, make sure we have a solution so we know our main goal is optimization

- ❑ How do we decompose the problem?

- ❑ What look like built out of nand2 gates and inverters?

Nand2 and inverter implementation





Single Gate Match Condition (preclass 5c)

- Design a single gate for match comparison



Optimize Total Power

□ Static CMOS:

- $P_{\text{tot}} \approx a(C_{\text{load}} + 2C_{\text{sc}})V^2f + VI'_s(W/L)e^{-V_t/(nkT/q)}$

□ Ratioed Logic:

- $P_{\text{tot}} \approx a(C_{\text{load}} + 2C_{\text{sc}})V^2f$
 $+ p(V_{\text{out}} = \text{low})V^2/R_{\text{pon}}$
 $+ (1 - p(V_{\text{out}} = \text{low}))VI'_s(W/L)e^{-V_t/(nkT/q)}$

□ What can we do to reduce power?



Knobs (preclass 5d)

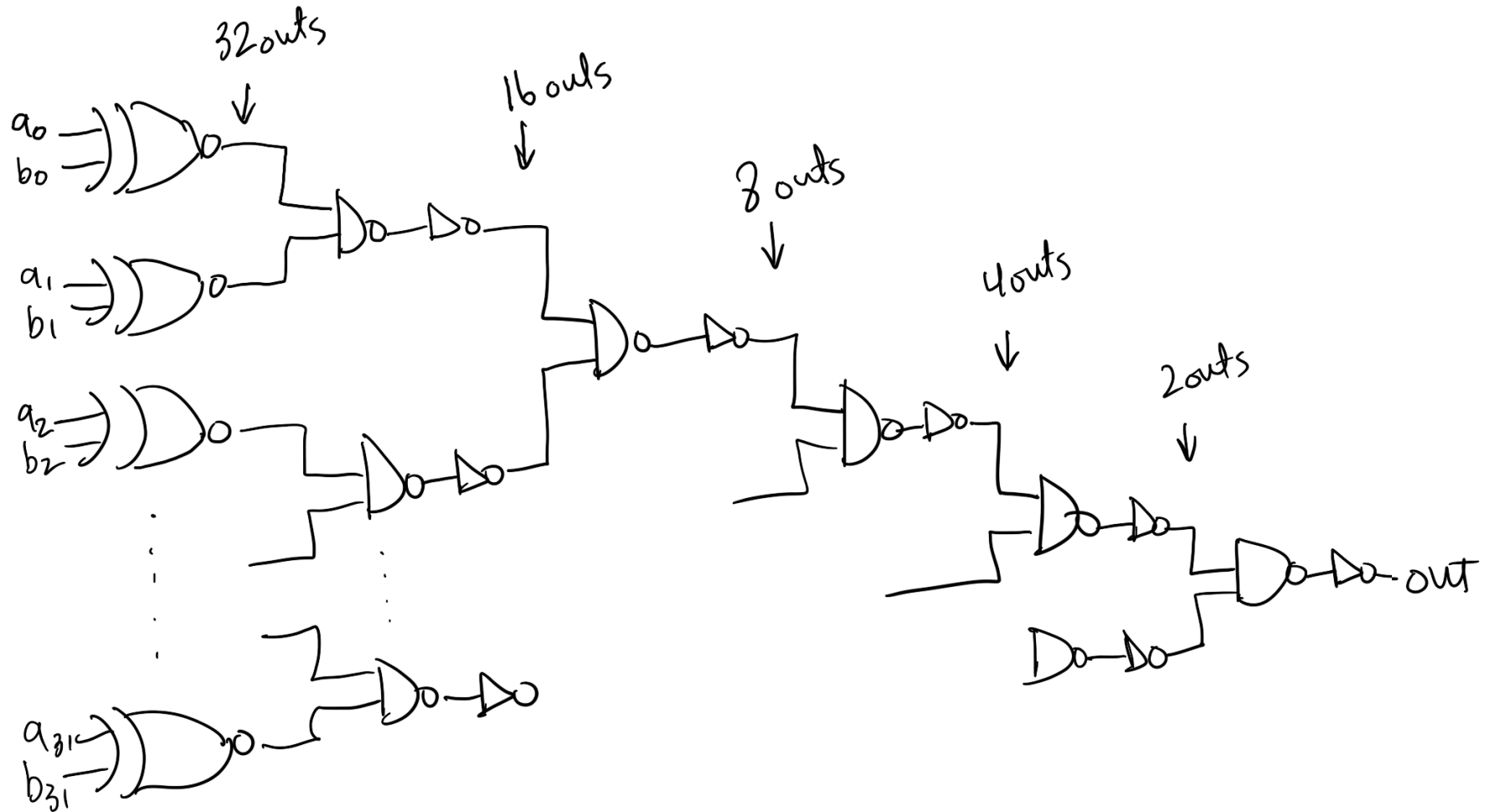
- What are the options and knobs we can turn?



Design Space Dimensions

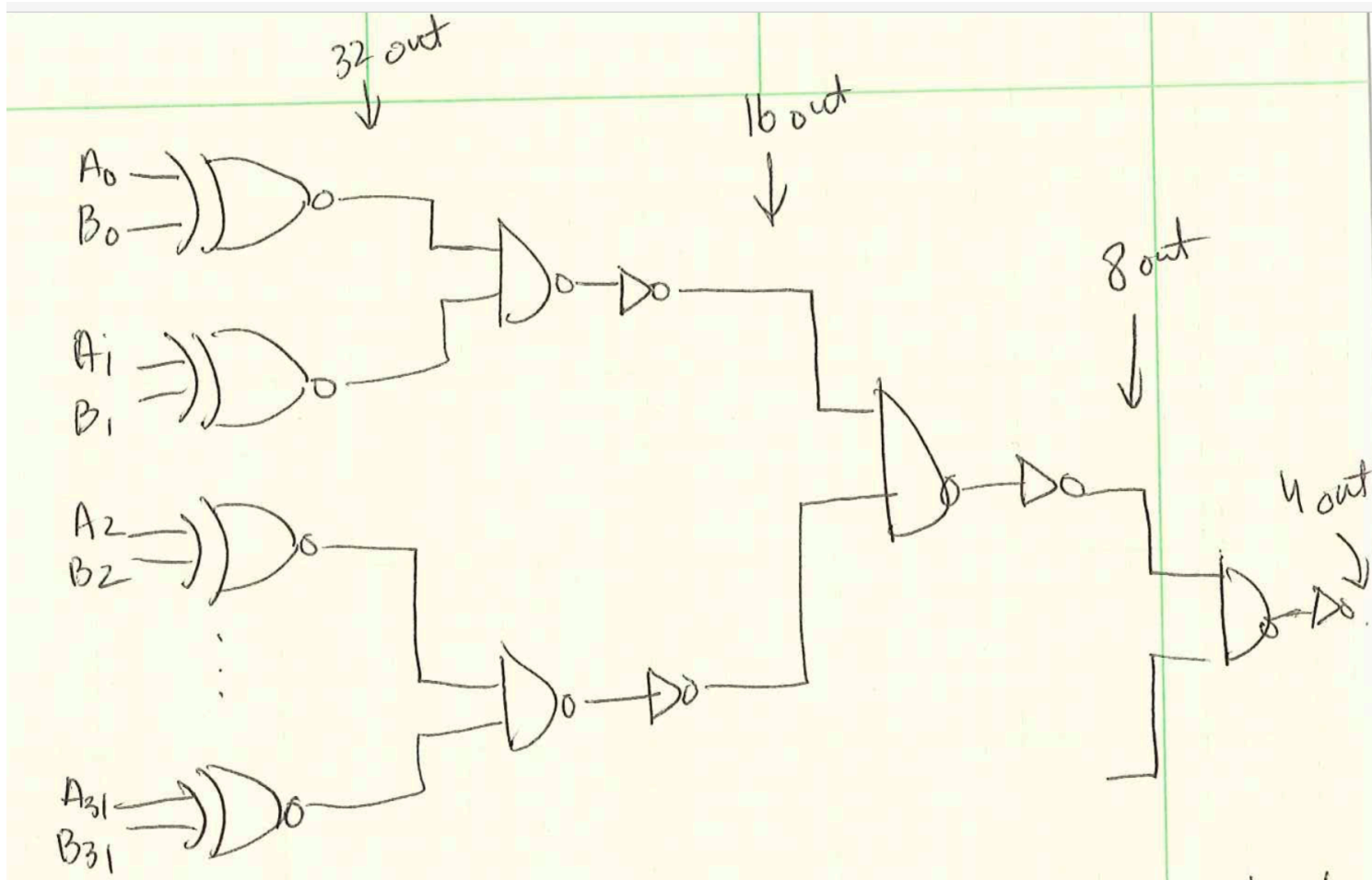
- ❑ Topology
 - (A) Gate choice, logical optimization
 - (B) Fanin, fanout, (C) Serial vs. parallel
- ❑ Gate style / logic family
 - (D) CMOS, Ratioed (N load, P load)
- ❑ (E) Transistor Sizing
- ❑ (F) Vdd
- ❑ (G) Vth

Gate



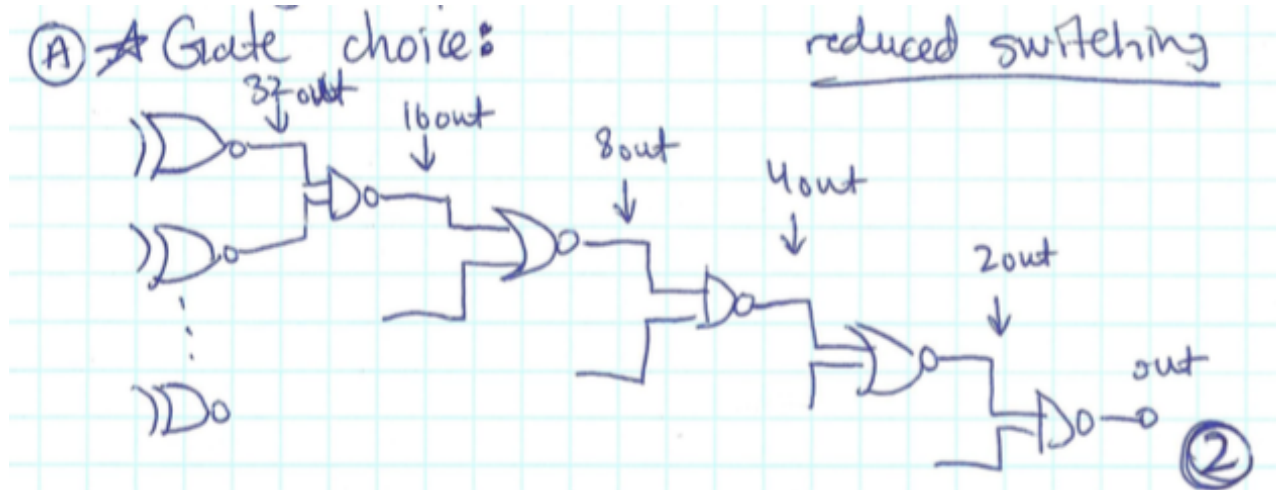
Gate Choice

- (A) What gates might we build?



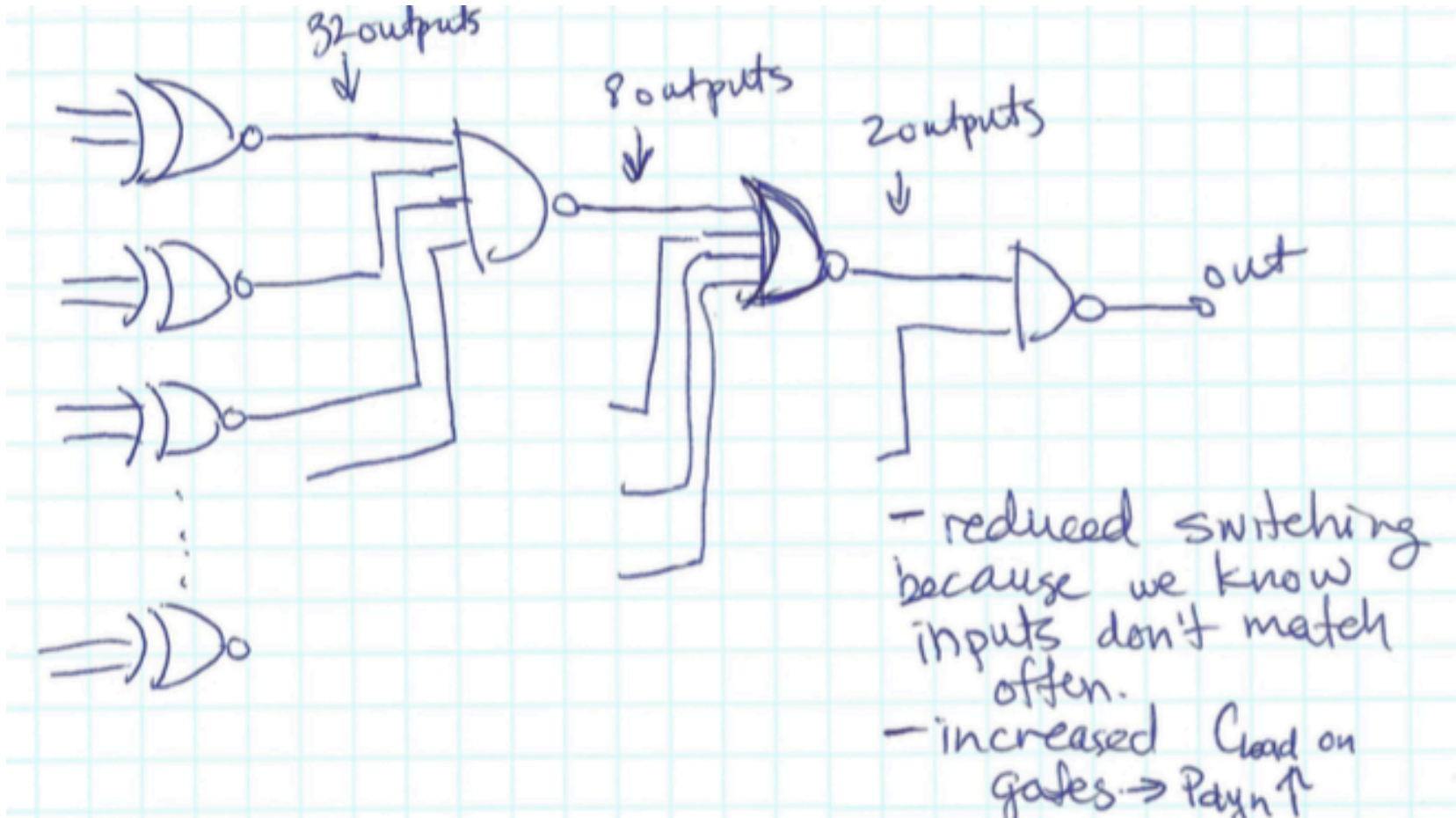
Gate Choice

- (A) What gates might we build?



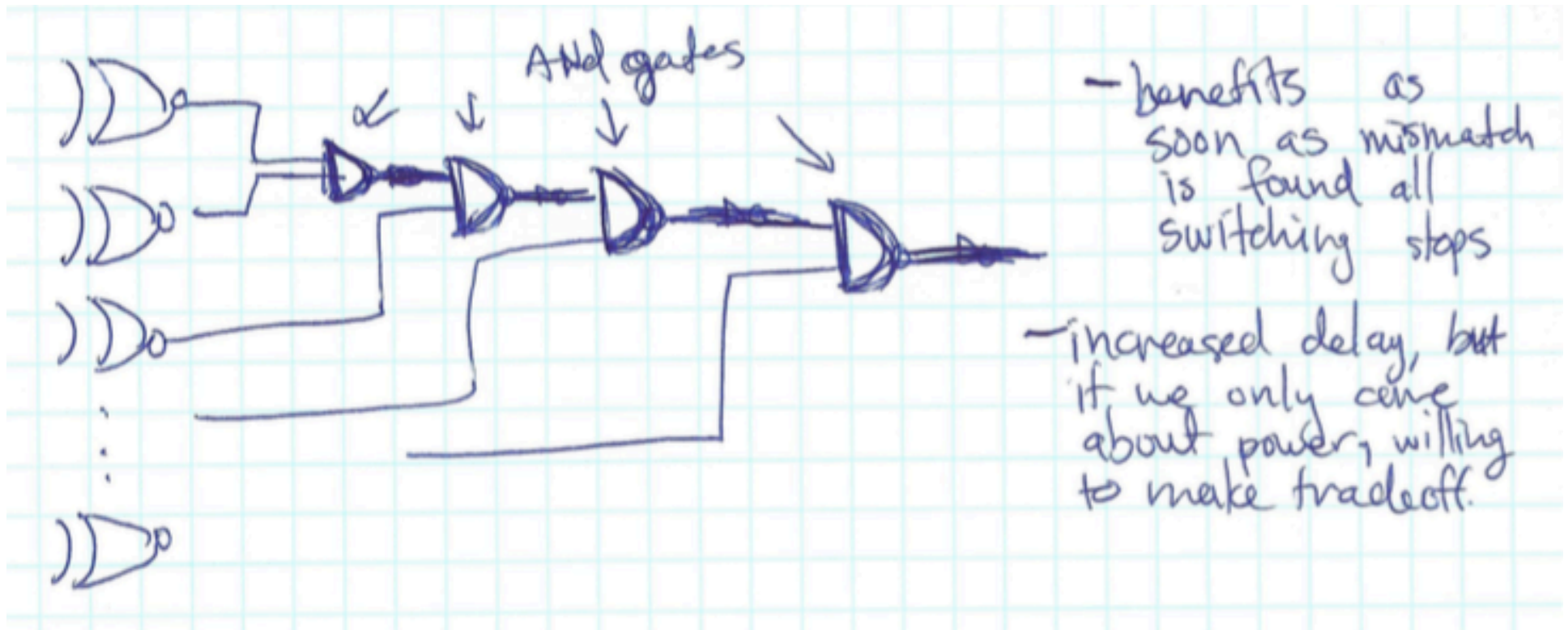
Gate Fan-in

□ (B) High fan-in?



Gate Topology

□ (C) Serial-Parallel?



(D) Logic Family

- ❑ Considerations for each logic family?
 - CMOS
 - Ratioed with PMOS load
 - Ratioed with NMOS load

- ❑ Ratioed Logic
 - Reduced C_{loads} result in lower switching power (P_{dyn} ↓)
 - Increased static power



(E) Sizing

- How do we want to size gates?
 - Sizing transistors up will reduce delay →
 - Reduces short circuit power

$$E = V_{dd} \times \left(I_{peak} \times t_{sc} \times \left(\frac{1}{2} \right) \right)$$

- Increases dynamic power

(F) Reduce Vdd

□ What happens as reduce V?

■ Energy?

■ Dynamic ↓

■ Static ↓

■ Switching Delay? ↑

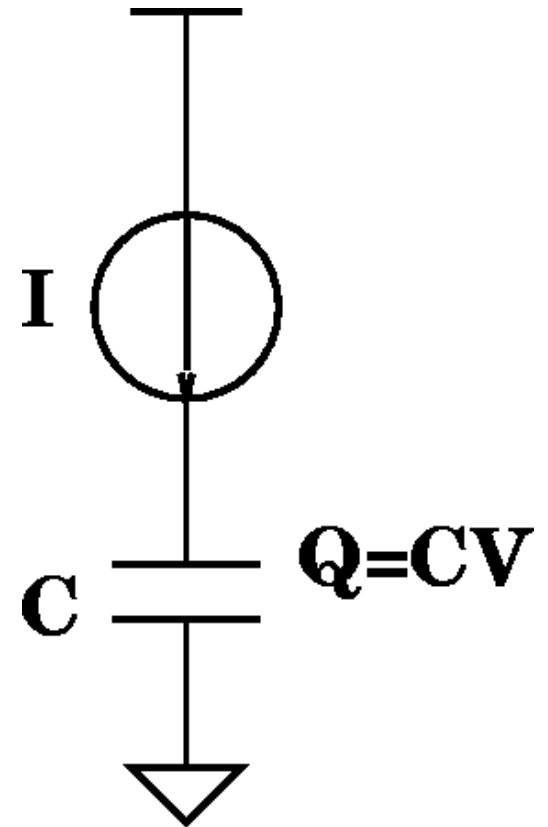
▪ $\tau_{gd} = Q/I = (CV)/I$

▪ $I_d = (\mu C_{OX}/2)(W/L)(V_{gs} - V_{TH})^2$

▪ τ_{gd} impact?

▪ $\tau_{gd} \propto 1/V$

▪ Limit on Vdd?

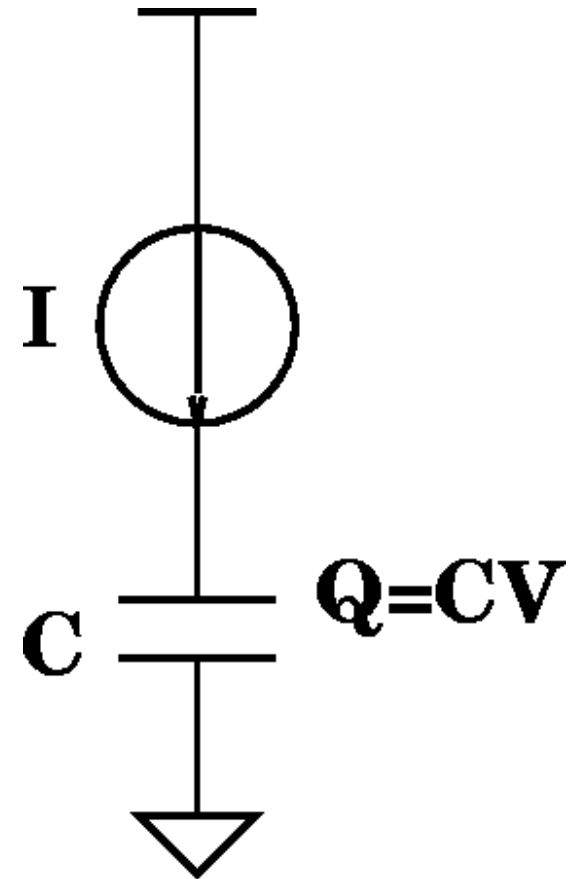


(G) Increase V_{th} ?

□ What is impact of increasing threshold on

- Dynamic Energy? ↓
- Leakage Energy? ↓
- Delay? ↑

- $\tau_{gd} = Q/I = (CV)/I$
- $I_{ds} = (\nu_{sat} C_{OX})(W)(V_{gs} - V_{TH} - V_{DSAT}/2)$





Ideas

- ❑ There are other logic disciplines
- ❑ You have the tools to analyze
- ❑ Ratioed Logic
 - Tradeoff noise margin for
 - Reduced area? Capacitive load?
 - Dissipates non-leakage static power in one input case
- ❑ We know many things we can do to our circuits
- ❑ Design space is large
- ❑ Systematically identify dimensions
- ❑ Identify continuum (trends) tuning when possible
- ❑ Watch tradeoffs ...but don't over-tune



Admin

- ❑ Project 1 out now
 - Design 8-bit ripple-carry adder
 - You already know how to do this
 - Refresh yourself on binary addition of 2 bits
 - Work **individually**
 - Full report due F 3/29
 - Milestone: Plan to have baseline built and characterized by 3/22
 - Have separate test schematic for each metric. Will save you time!!
 - Delay
 - Active energy
 - Leakage energy



Acknowledgement

- ❑ Prof. André DeHon (University of Pennsylvania)
- ❑ Prof. Jing Li (University of Pennsylvania)