ESE370: Circuit-Level Modeling, Design, and Optimization for Digital Systems

Lec 13: March 18, 2024

Pass Transistor Logic

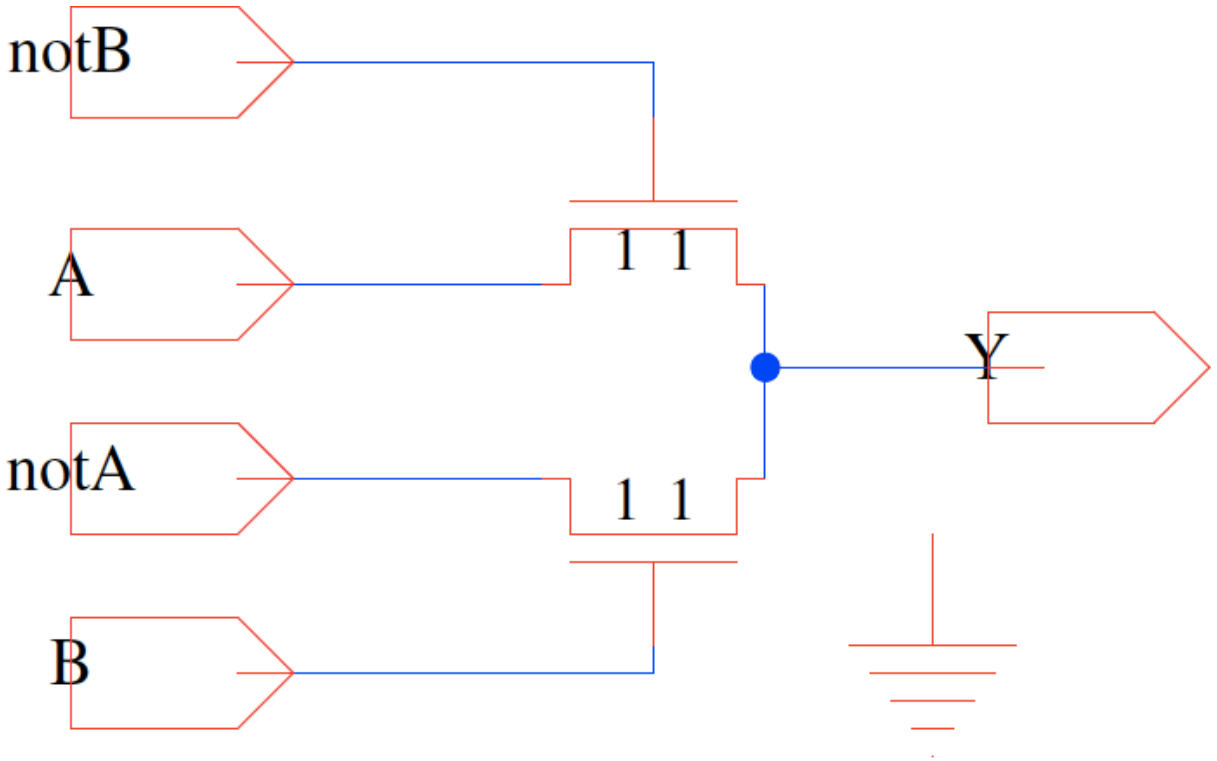
Today

- Pass Transistor Logic
- Pass Transistor Circuit
  - $C_{diff}>0$
  - Output levels
  - Cascading
    - Series pass transistors?
    - Delay

Pass Transistor Logic

Pass Transistor Logic (Preclass 1)

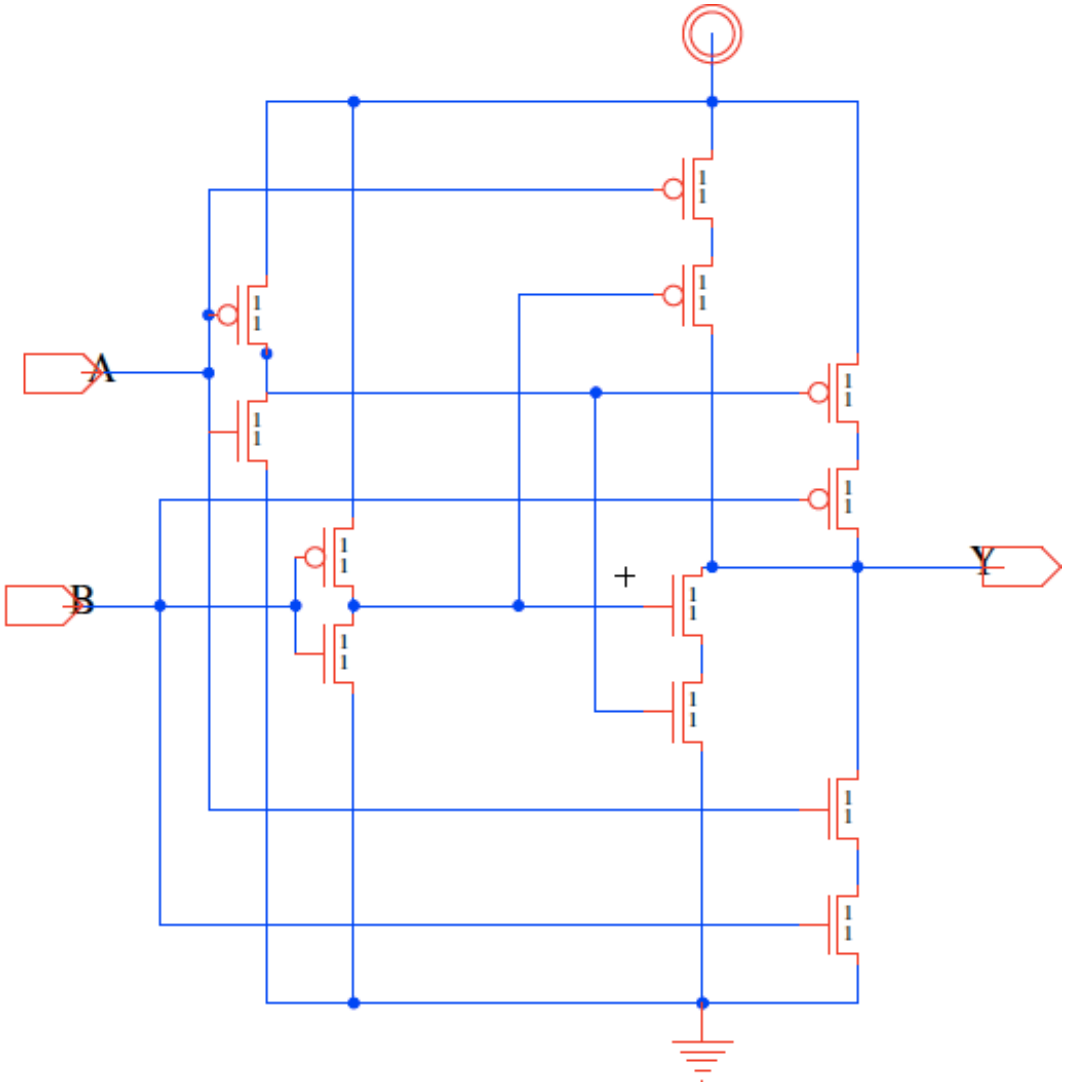
- What does this do?



A	B	Y
0	0	
0	1	
1	0	
1	1	

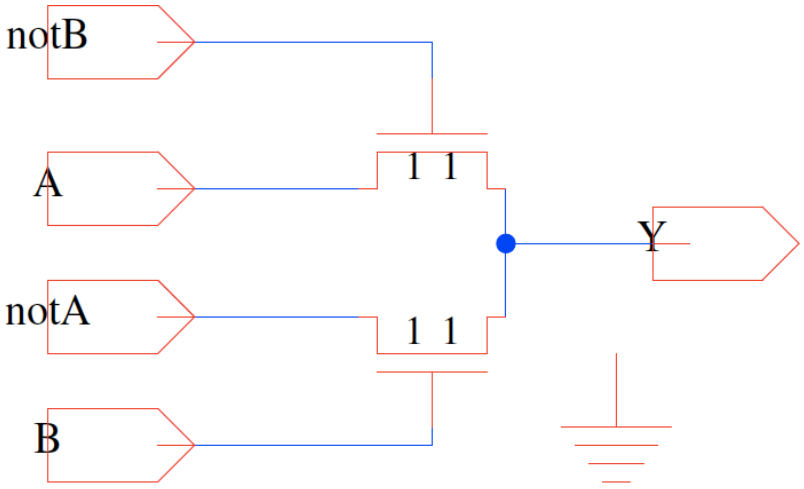
Identify Function (Preclass 2)

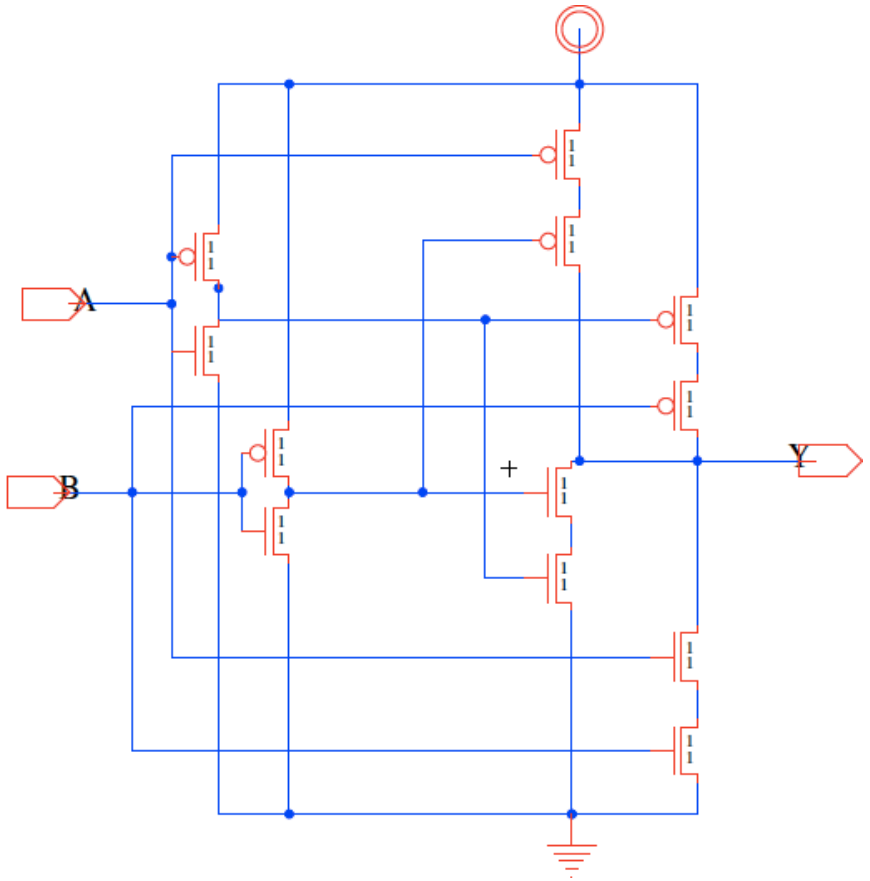
- What function is this?



Area

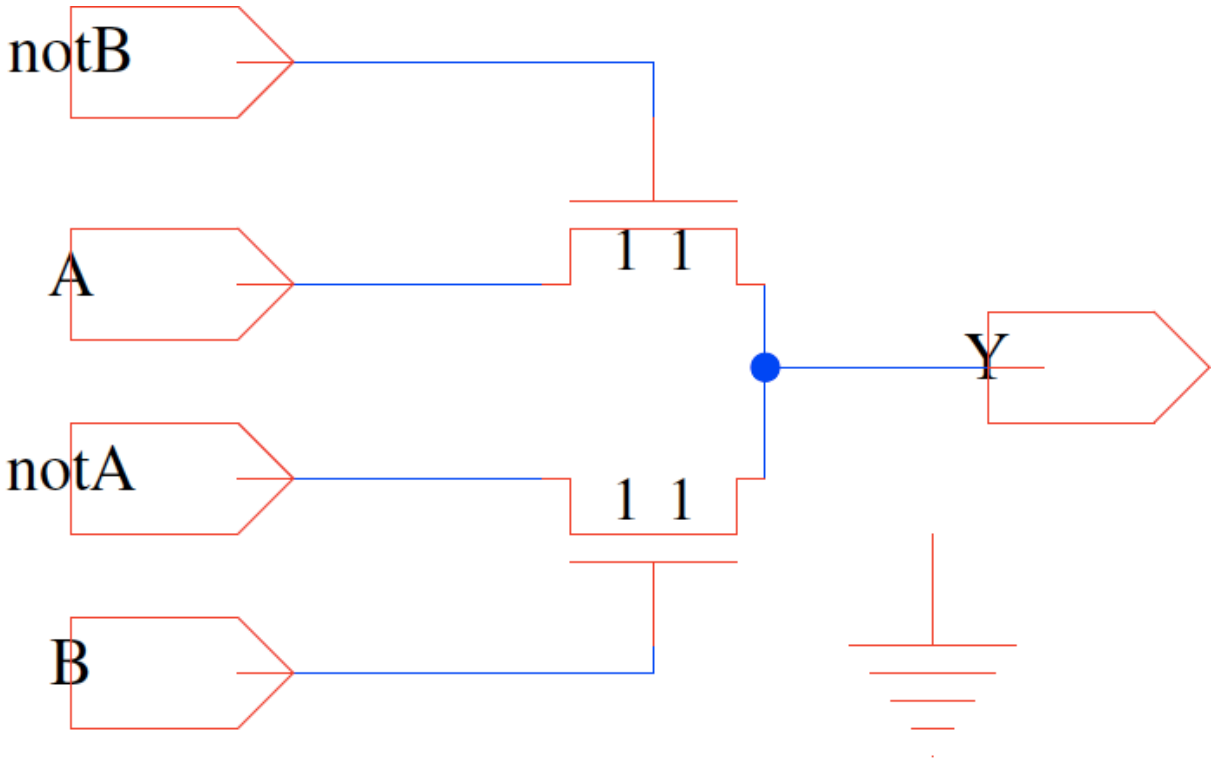
- Compare PT with CMOS circuit?





Output

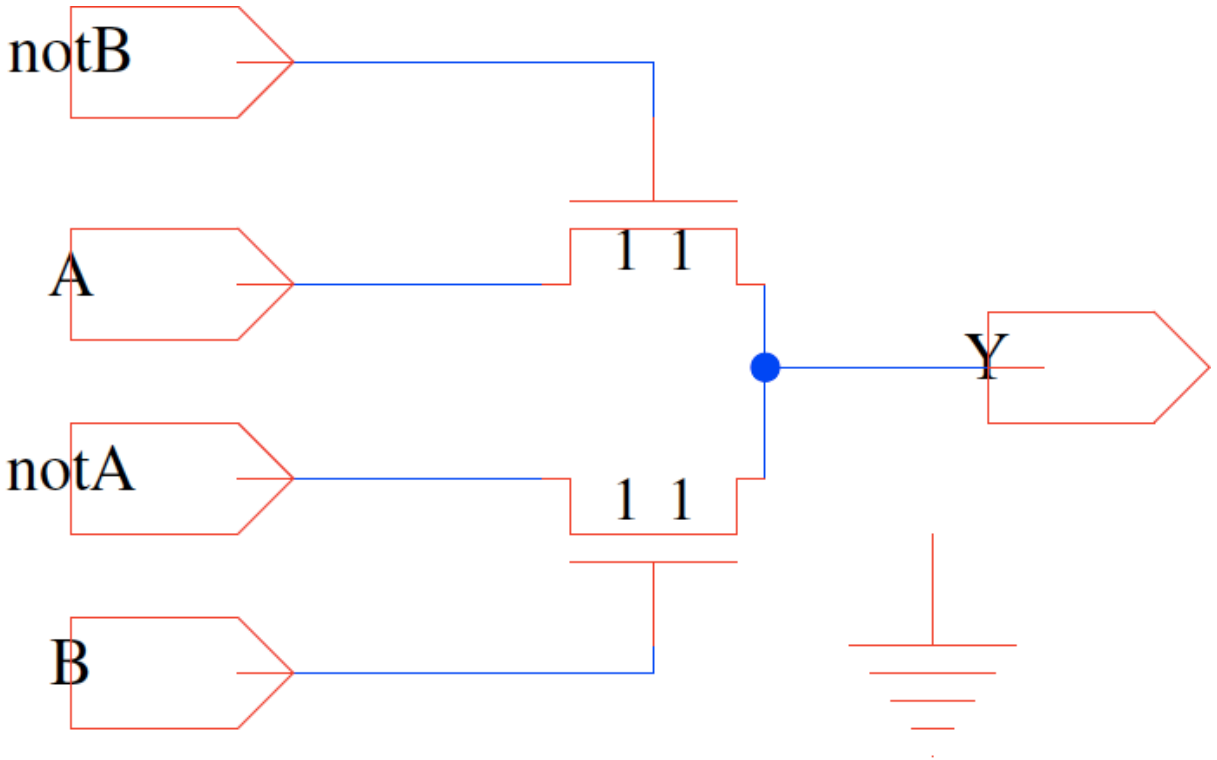
- Is this a regenerating/restoring gate?



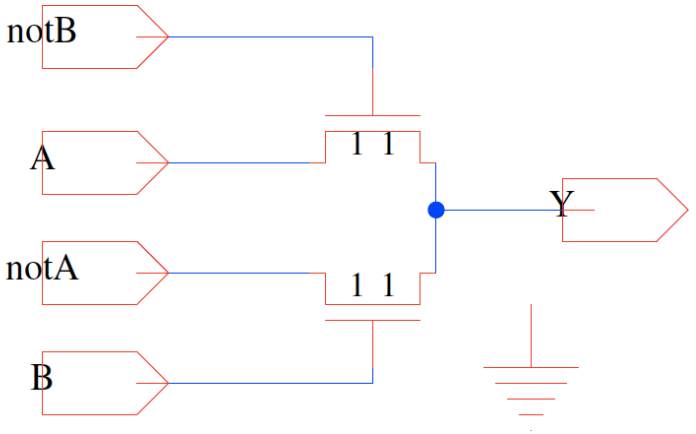
A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

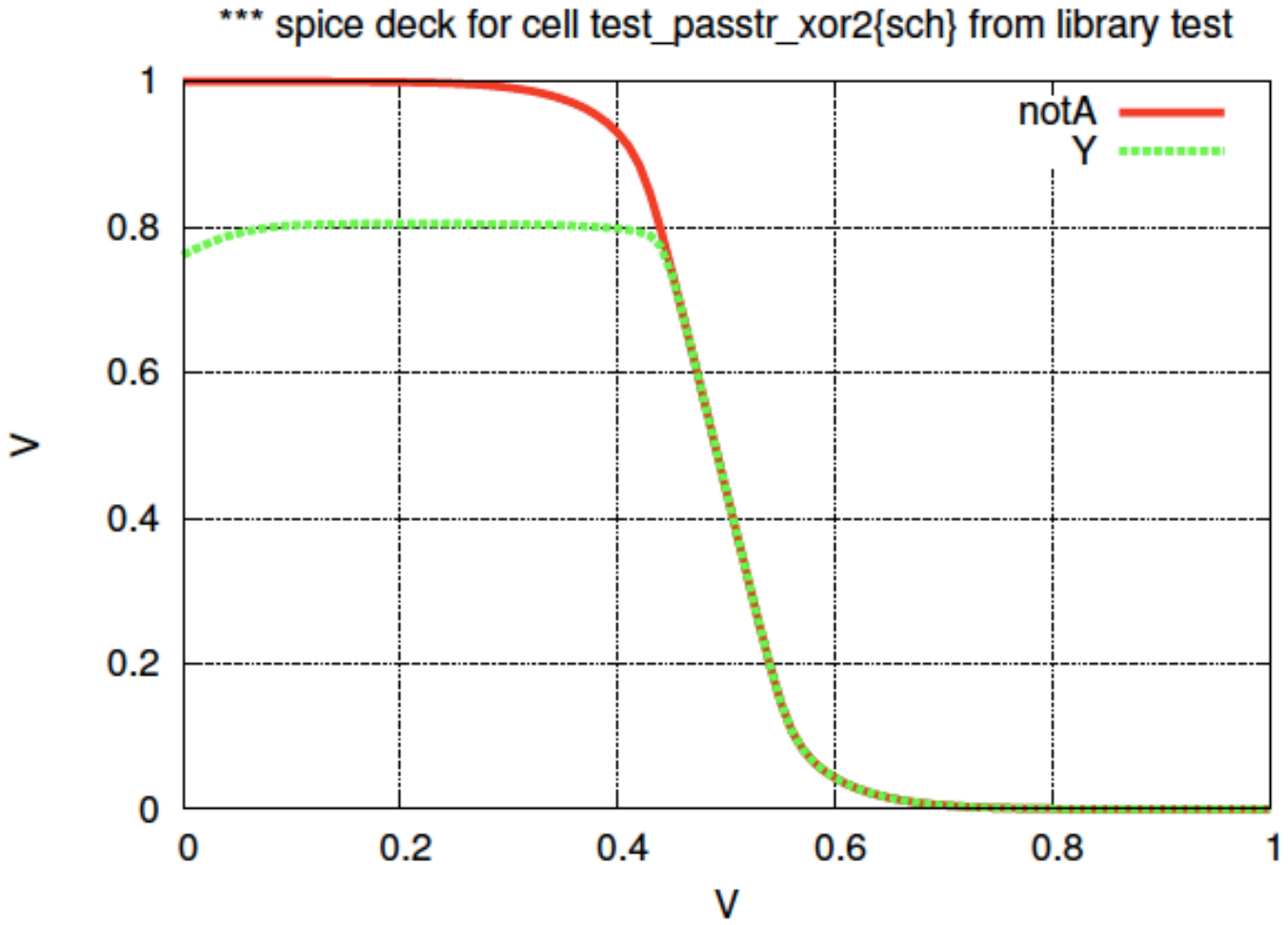
Output

- What does output look like (DC transfer)?
  - (B=1, notB=0, sweep A, notA=CMOS inv(A))



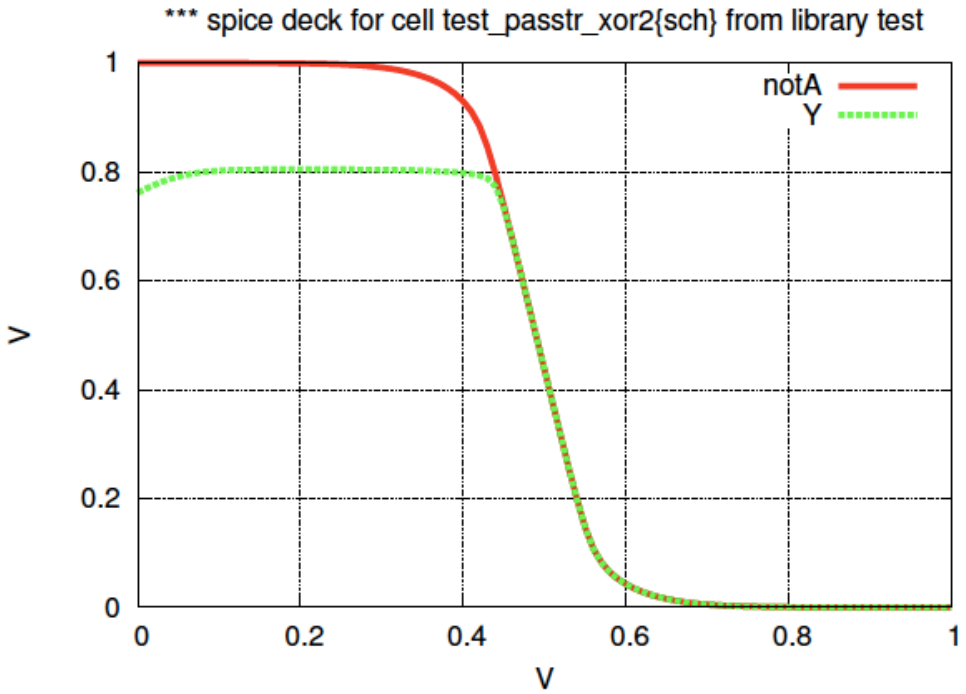
Pass TR transfer (B=1)

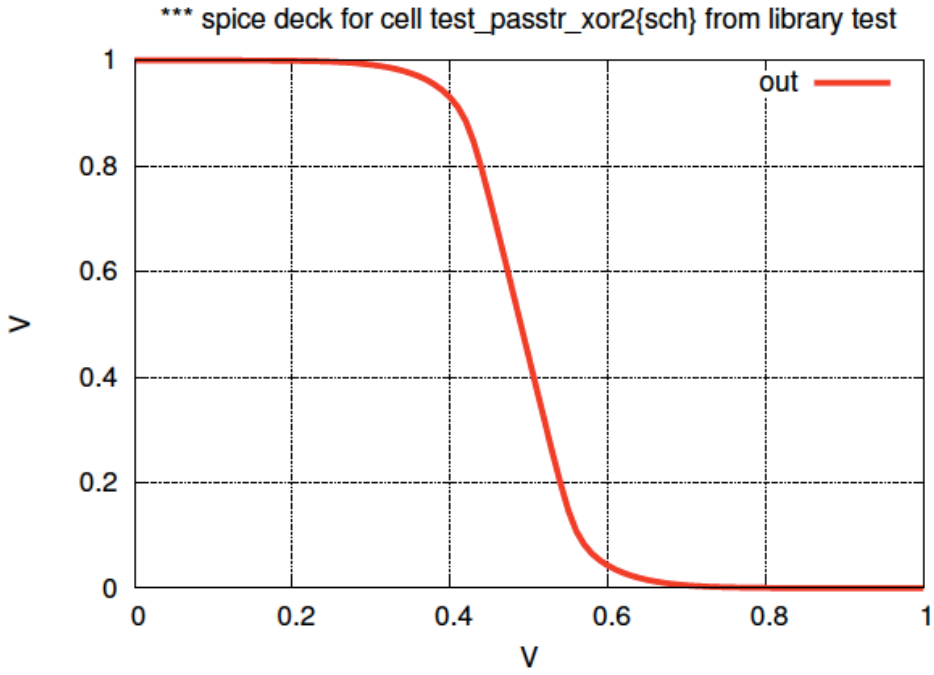




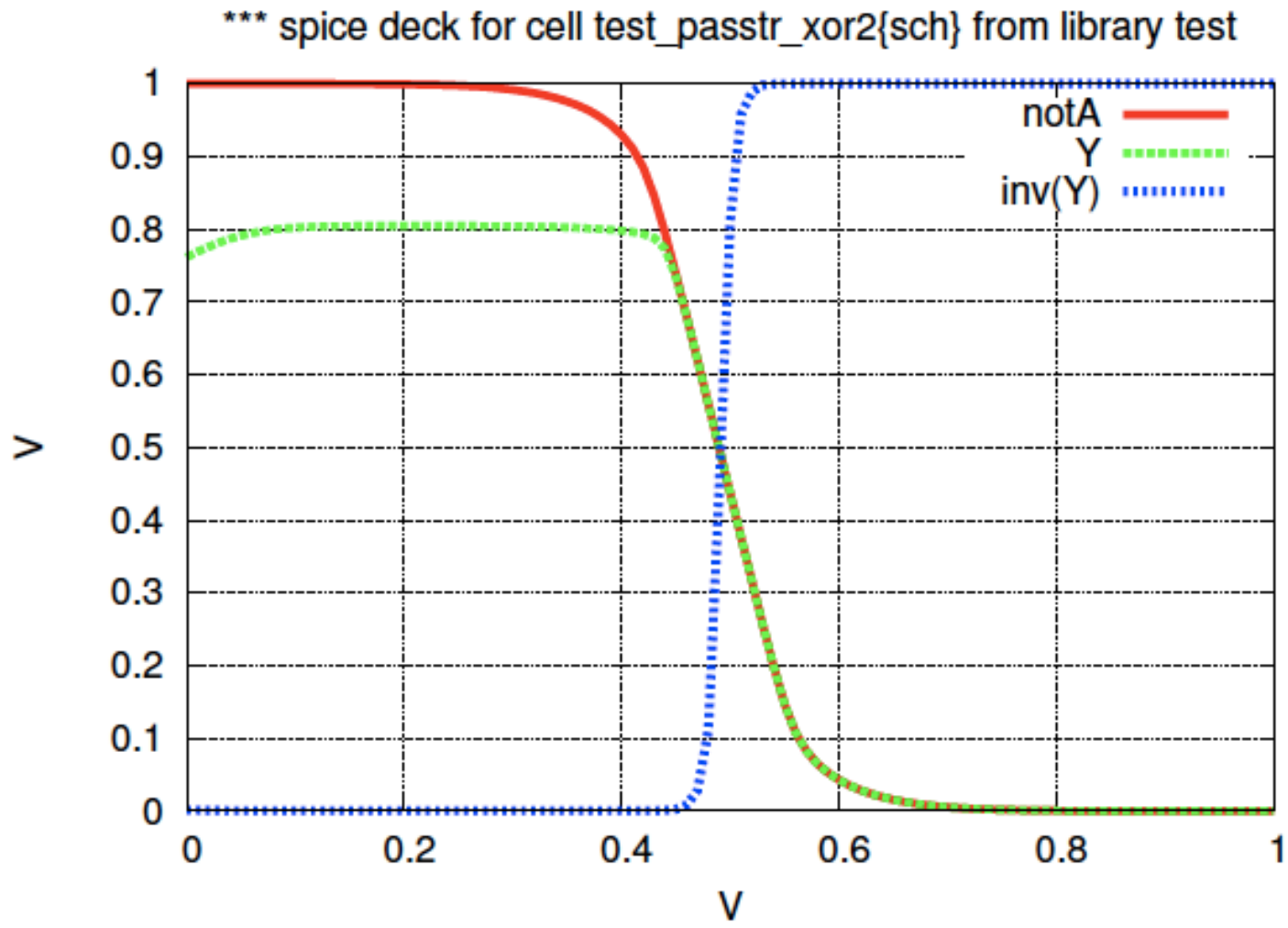
XOR Output

- Reasonable Input to CMOS Inverter?





Pass Transistor xor2 with inv restore

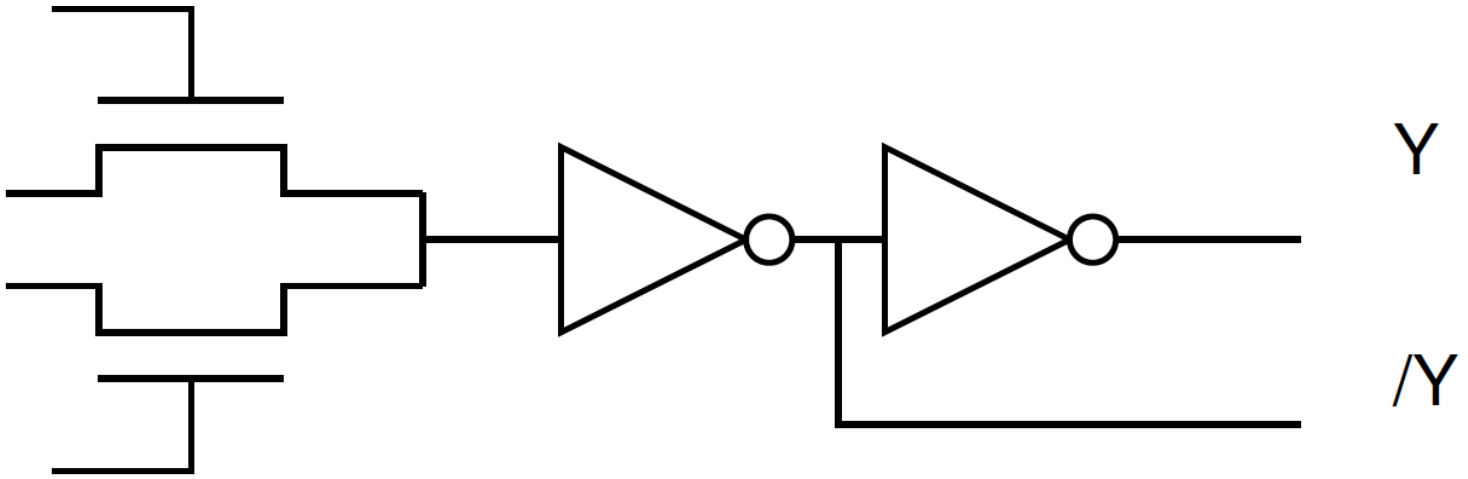


Required to use?

- What should we add to make suitable comparison with CMOS?

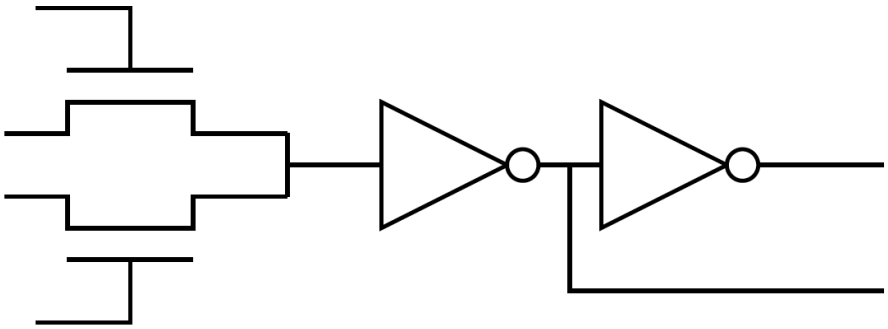
Restore Output

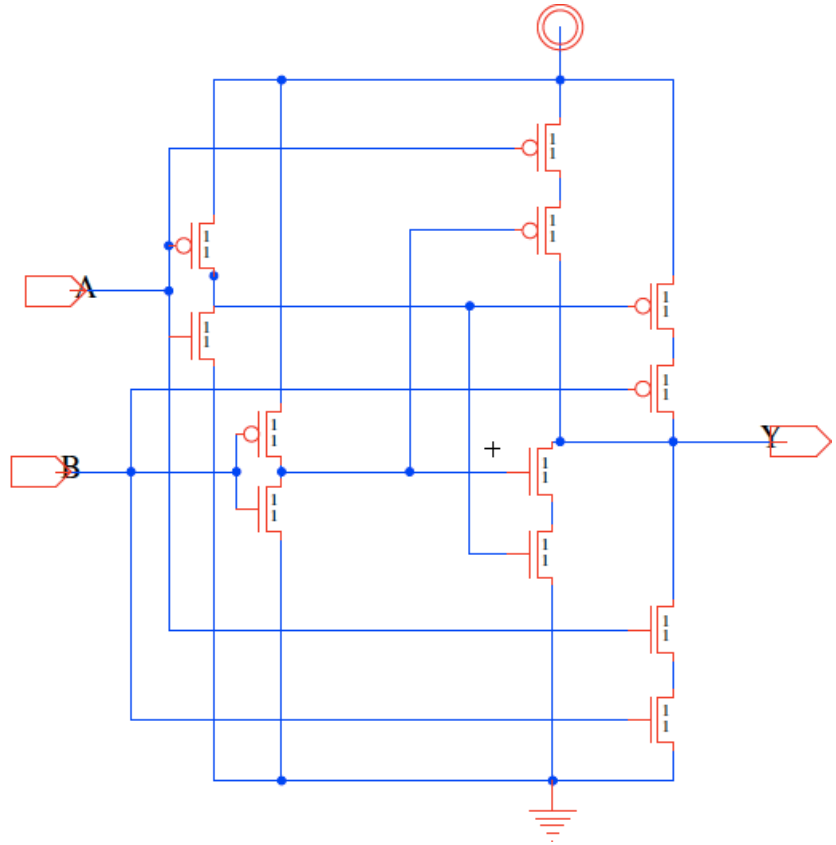
- What should we add to make suitable comparison with CMOS?



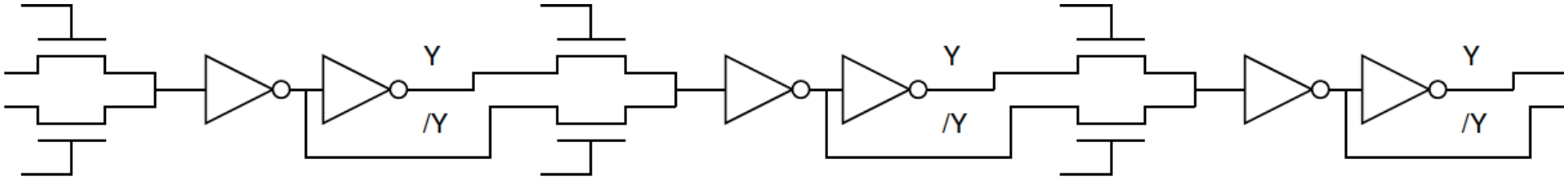
Restore Output

- Area? (compare to CMOS)

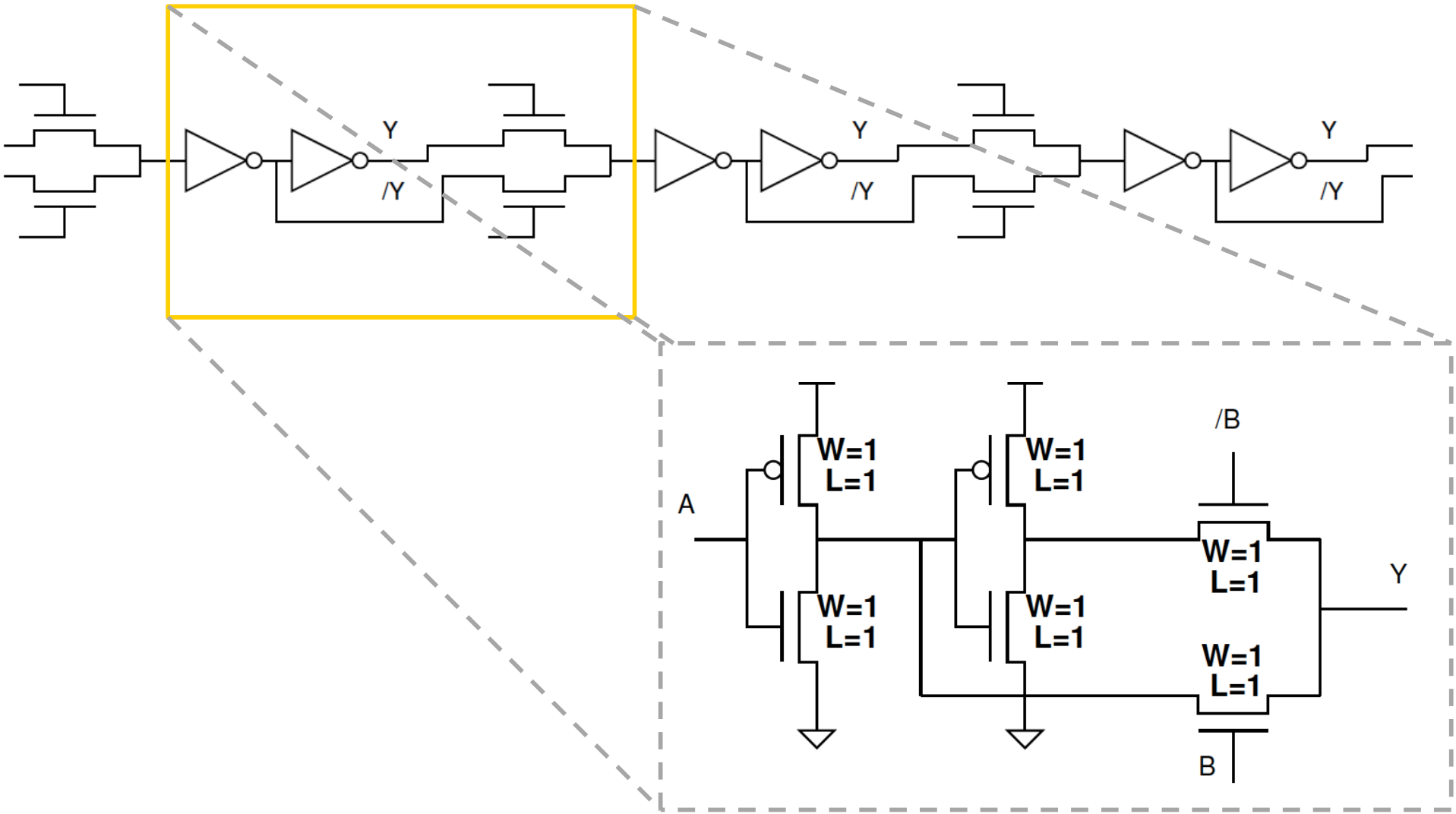




Chain Together

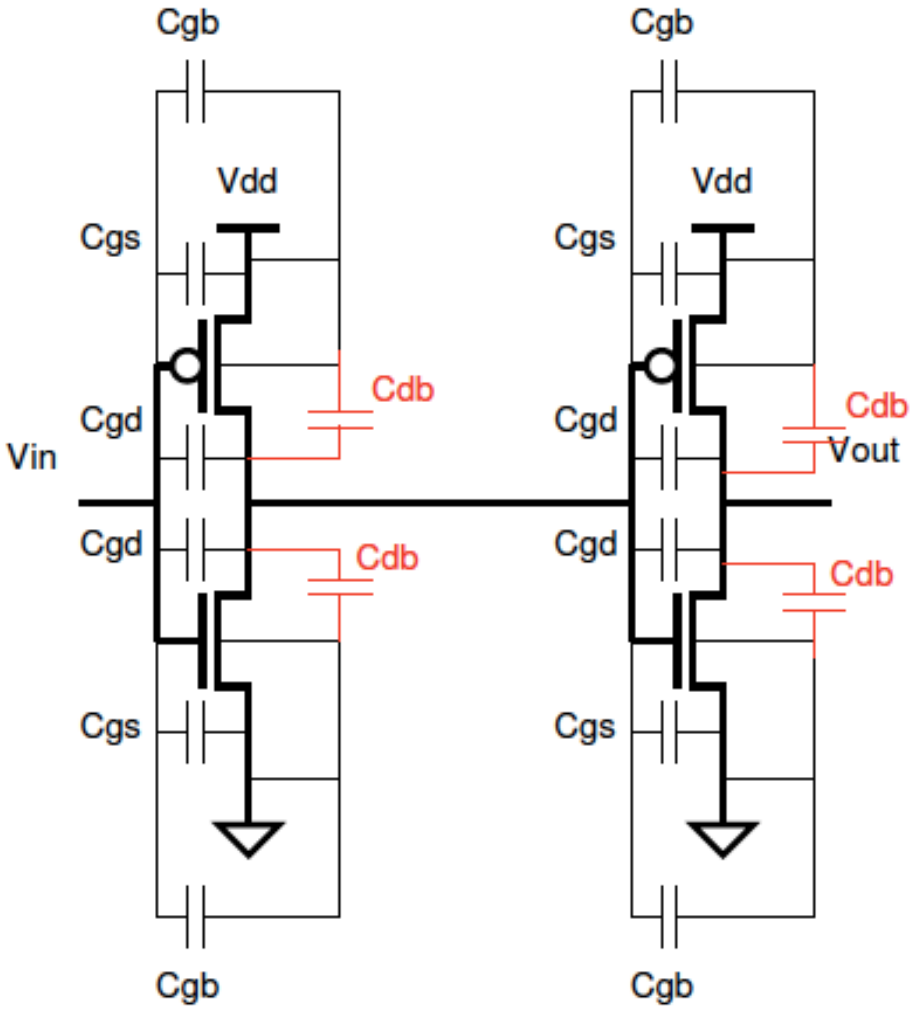


Analyze Stage



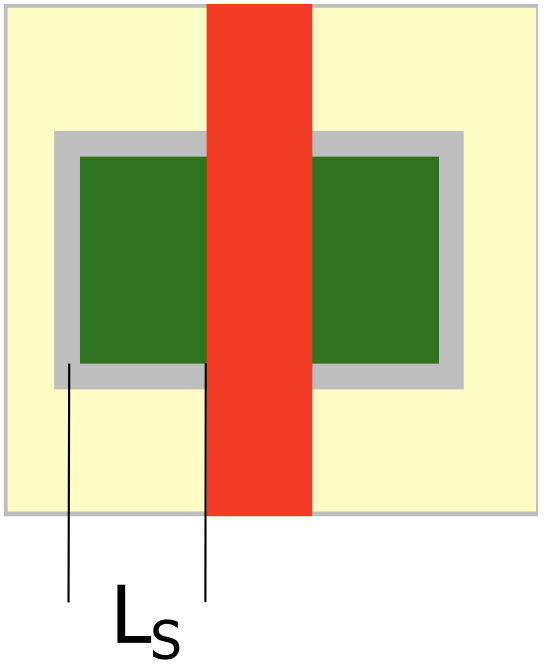
Impact of Capacitance

- $C_{GS}=C_{GCS}+C_{GSO}$
- $C_{GD}=C_{GCD}+C_{GDO}$
- $C_{GB}=C_{GCB}$
- $C_{SB}=C_{diff}$
- $C_{DB}=C_{diff}$



Contact/Diffusion Capacitance

- C_j – diffusion depletion
- C_{jsw} – sidewall capacitance
- L_S – length of diffusion

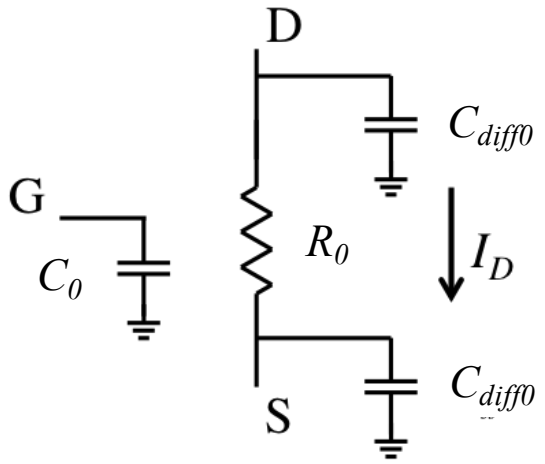


$$C_{diff} = C_j L_S W + C_{jsw}\left(2L_S + W\right)$$

Define: $C_{diff\,0} \approx \gamma C_0$

$$C_{diff} \approx W C_{diff\,0} = W \cdot \gamma C_0$$

First Order Model



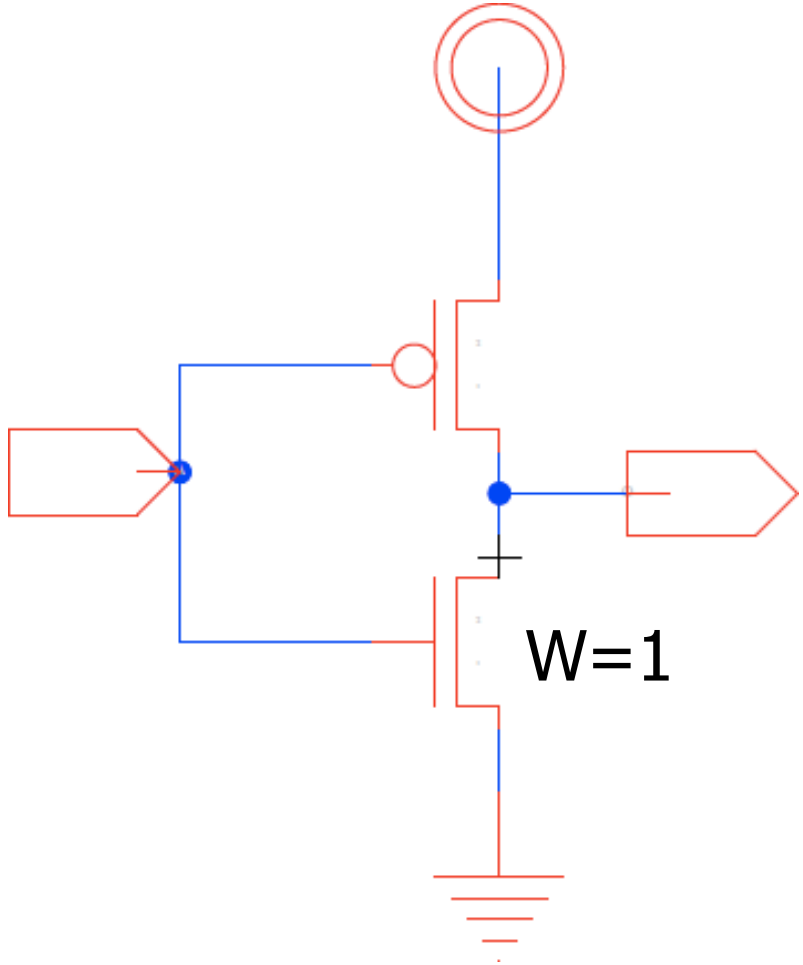
- Switch
  - Loads all terminals capacitively
    - Draw no steady-state current for a CMOS gate
    - Does not impact steady-state output voltage
    - Impacts Settling time/Delay
  - Has finite drive strength
    - Could form voltage divider with resistive load
    - Impacts Settling time/Delay

First Order Delay

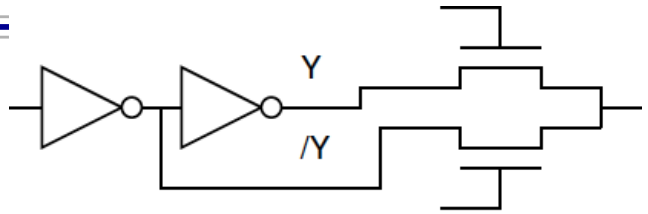
- R_0 = Resistance of minimum size NMOS device
- C_0 = gate capacitance of minimum size NMOS device
- C_{diff0} = diffusion capacitance on minimum size NMOS
  - $C_{diff0} = \gamma C_0$
- $R_{drive} = R_0/W$
- $C_g = WC_0$
- $C_{diff} = WC_{diff0} = \gamma WC_0$

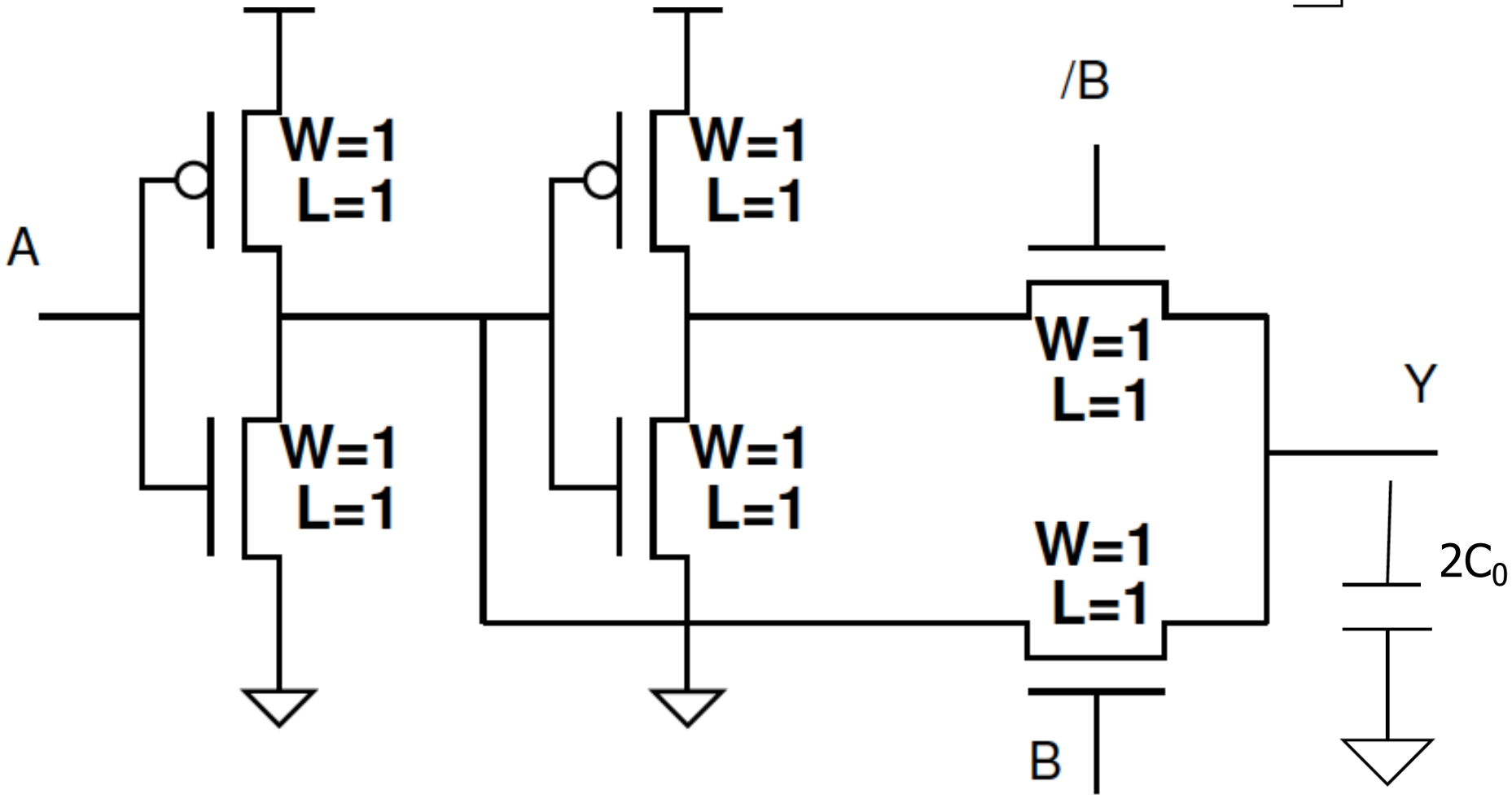
Inverter Delay

- Delay driving another (min size) inverter?
  - Include $C_{diff}=\gamma C_g=\gamma W C_0$



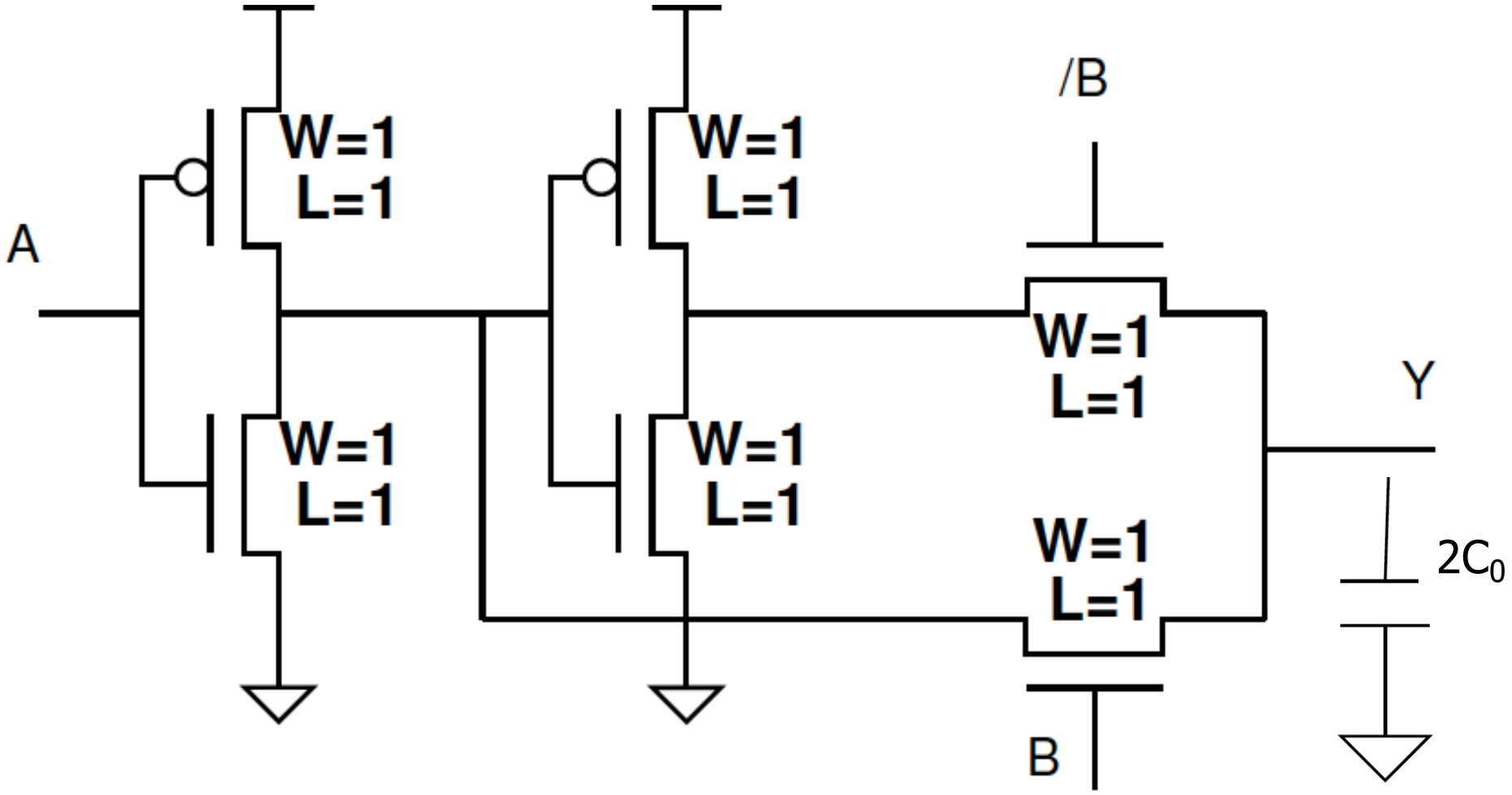
Delay A=1, B=0, $C_{diff0}=\gamma C_0$? (Preclass 3)





Delay A=1, B=0, $C_{diff0}=\gamma C_0$? (Preclass 3)

- What's the equivalent RC circuit?



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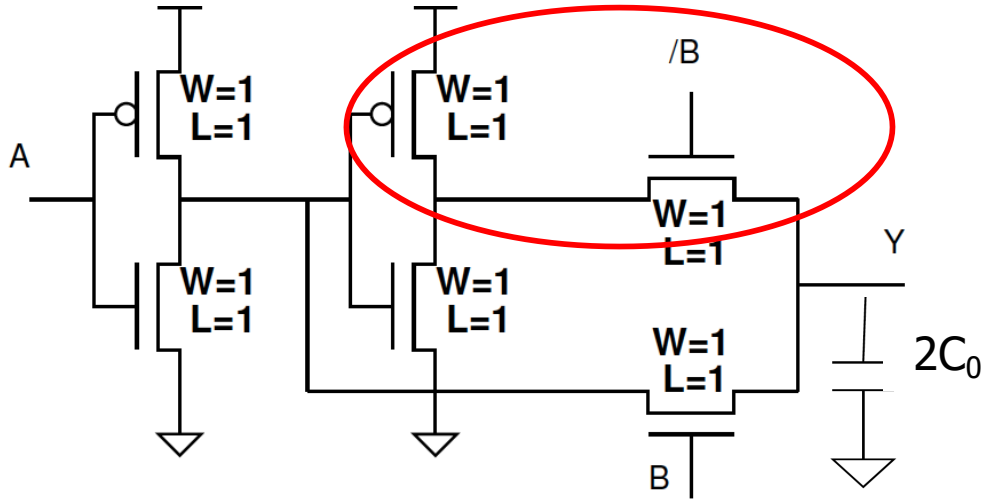

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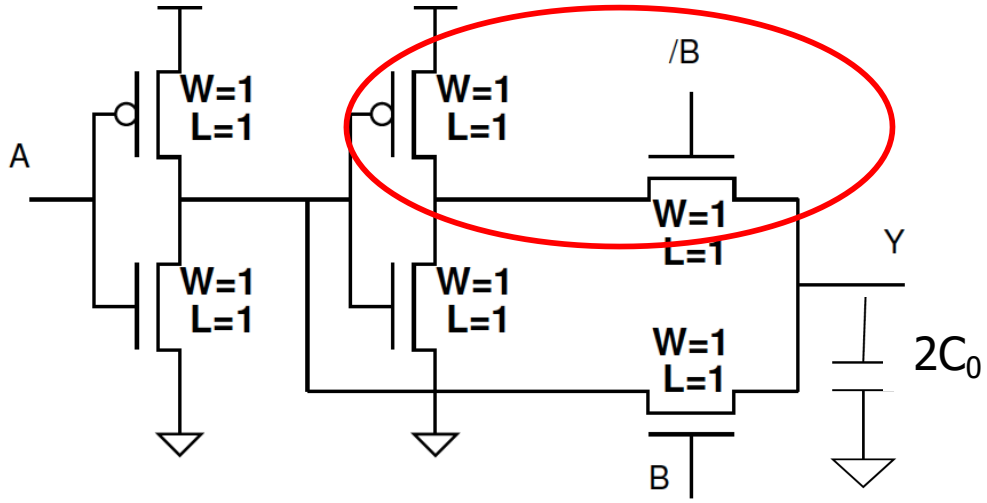
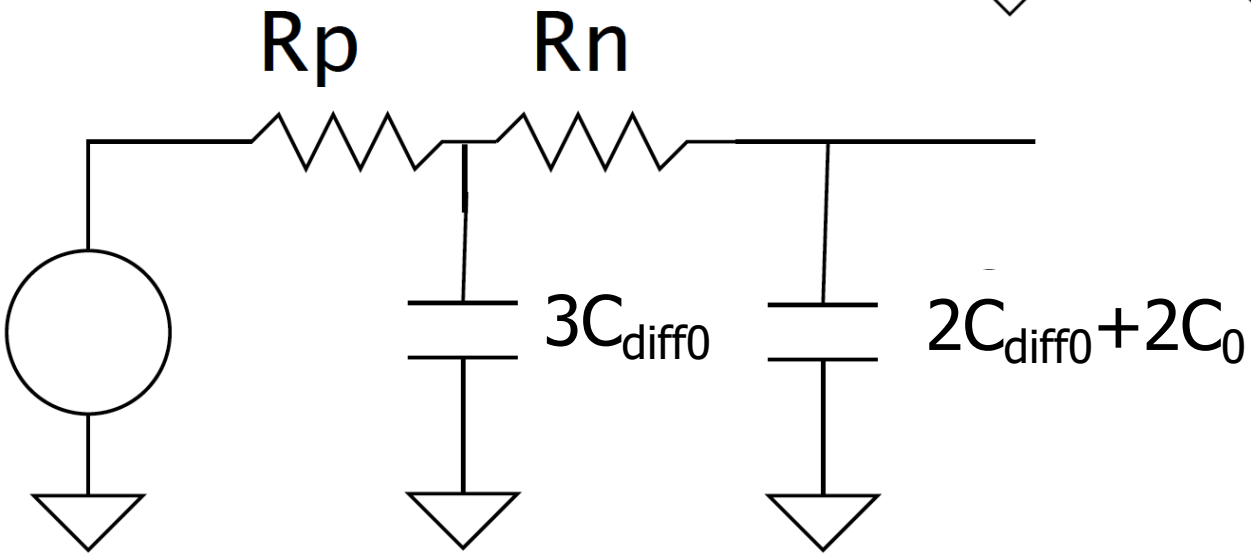
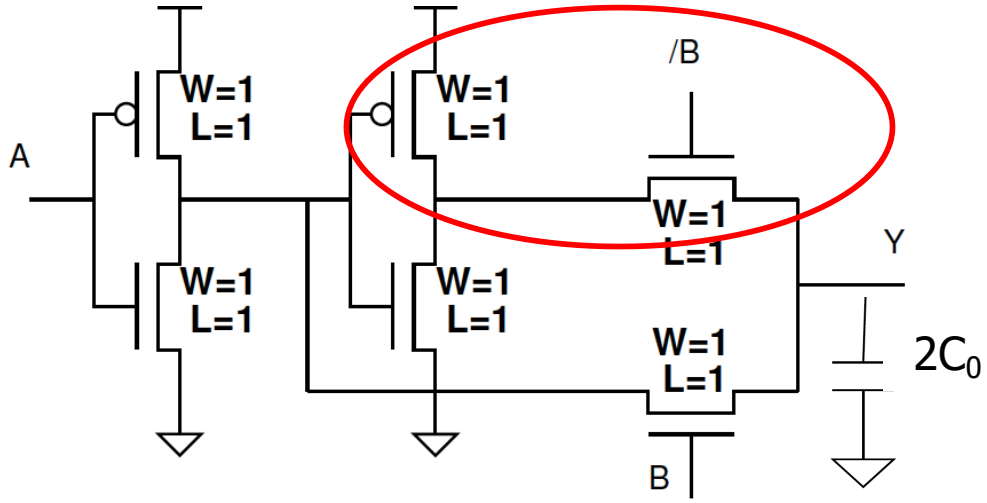
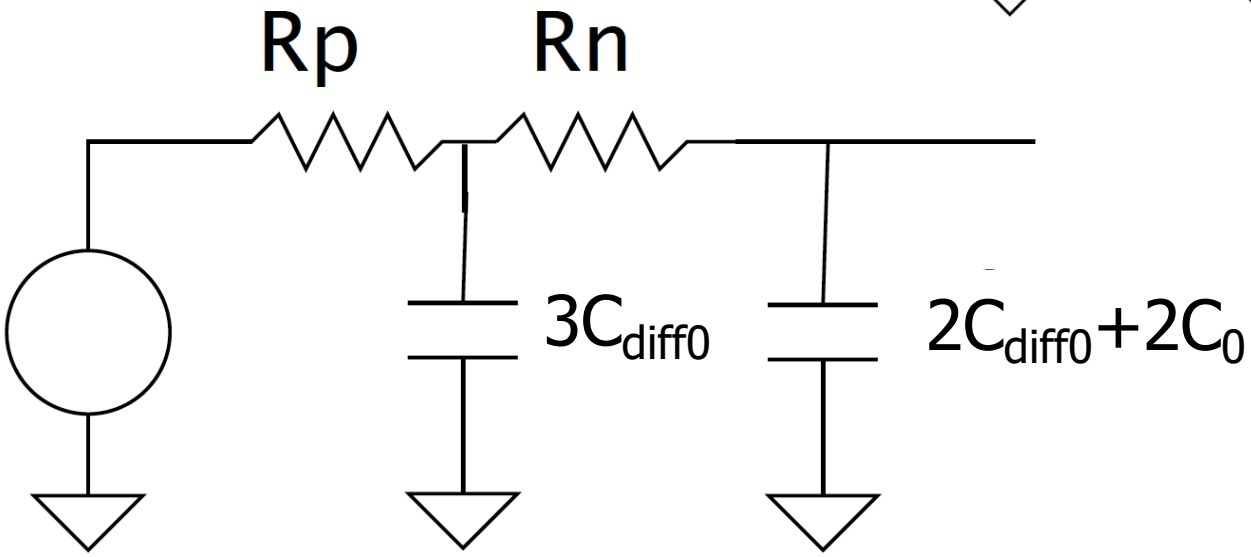




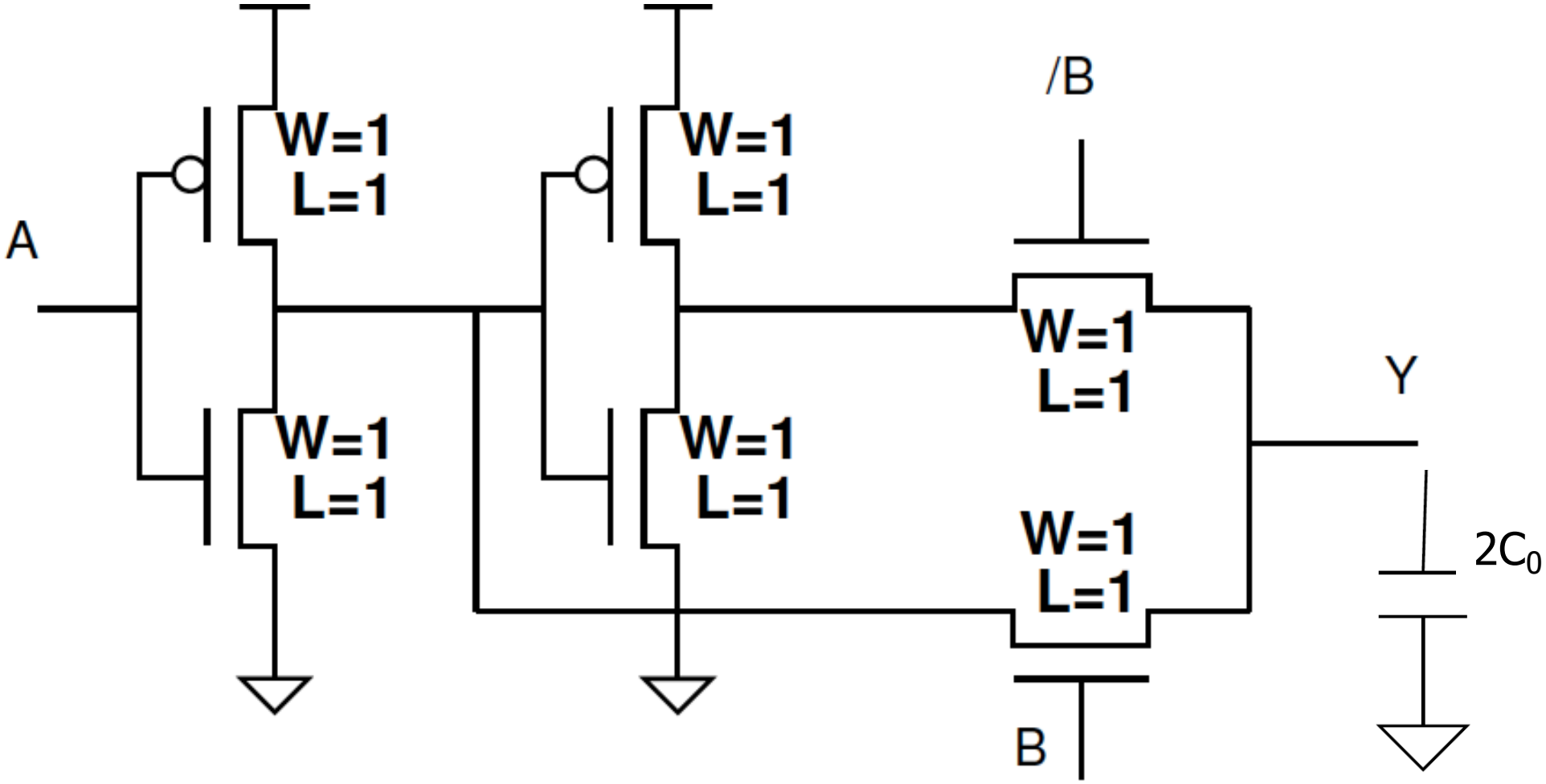
Delay A=1, B=0, $C_{diff0}=\gamma C_0$? (Preclass 3)

- What's the equivalent RC circuit?
  - Delay from A to Y?



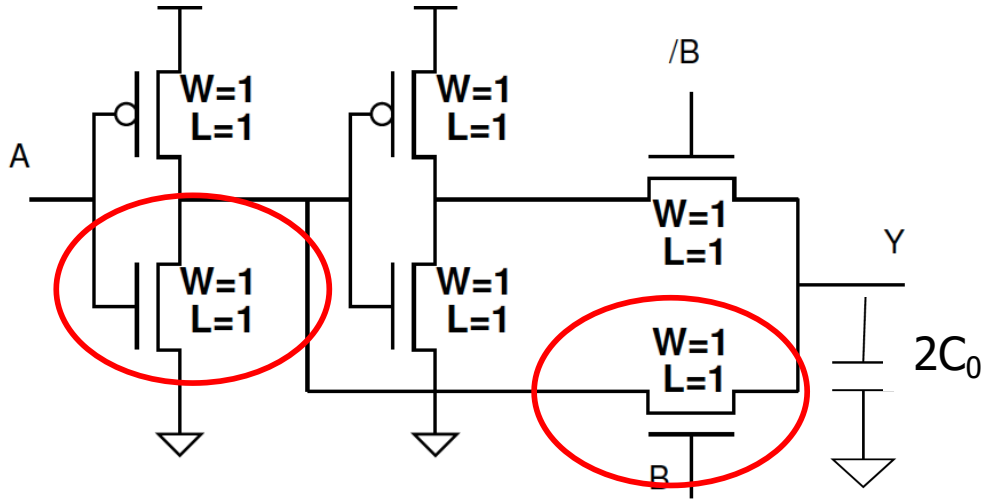


Delay A=1, B=1, $C_{diff0}=\gamma C_0$? (Preclass 3)



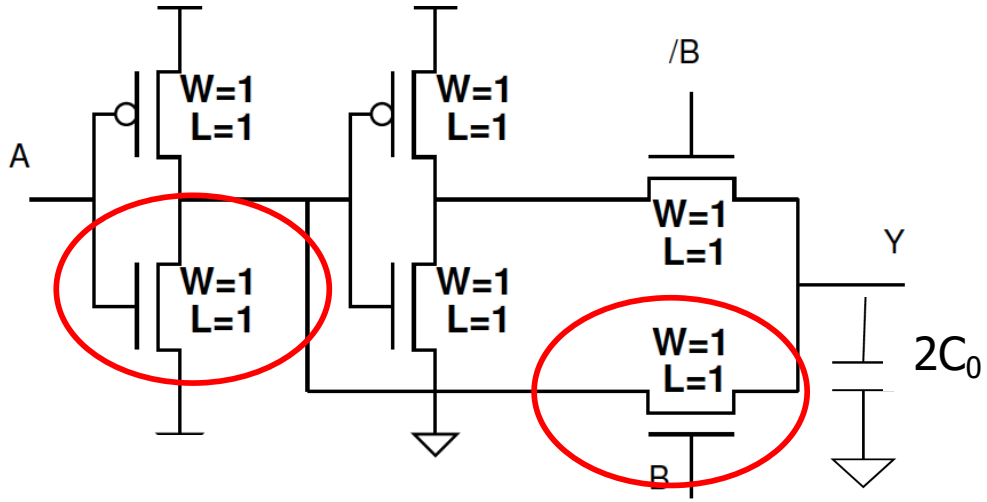
Delay A=1, B=1, $C_{diff0}=\gamma C_0$? (Preclass 3)

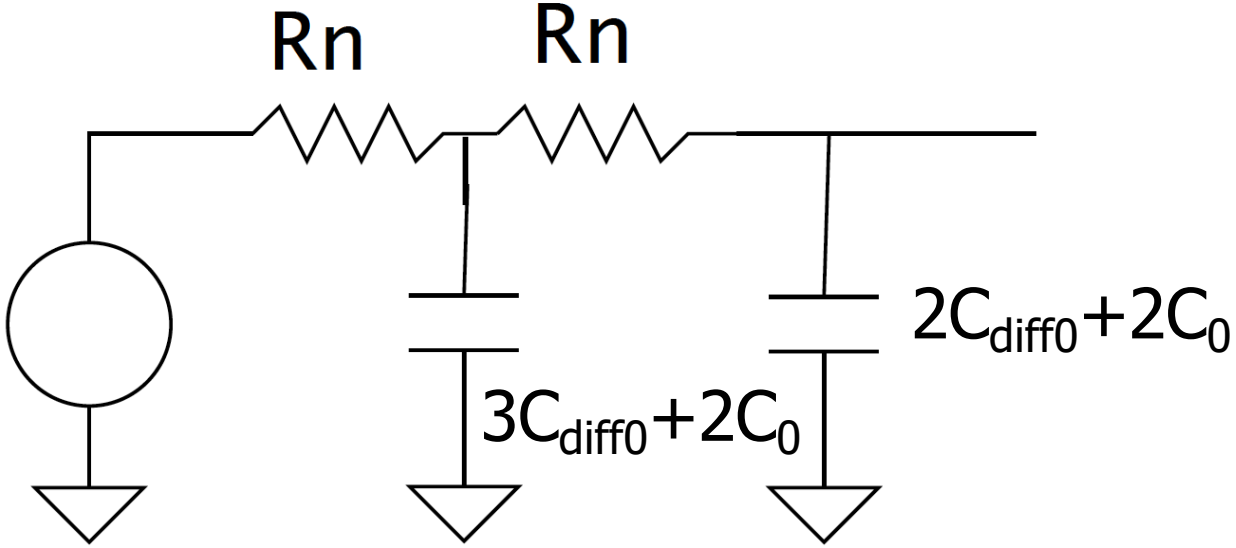
- What's the equivalent RC circuit?



Delay A=1, B=1, $C_{diff0}=\gamma C_0$? (Preclass 3)

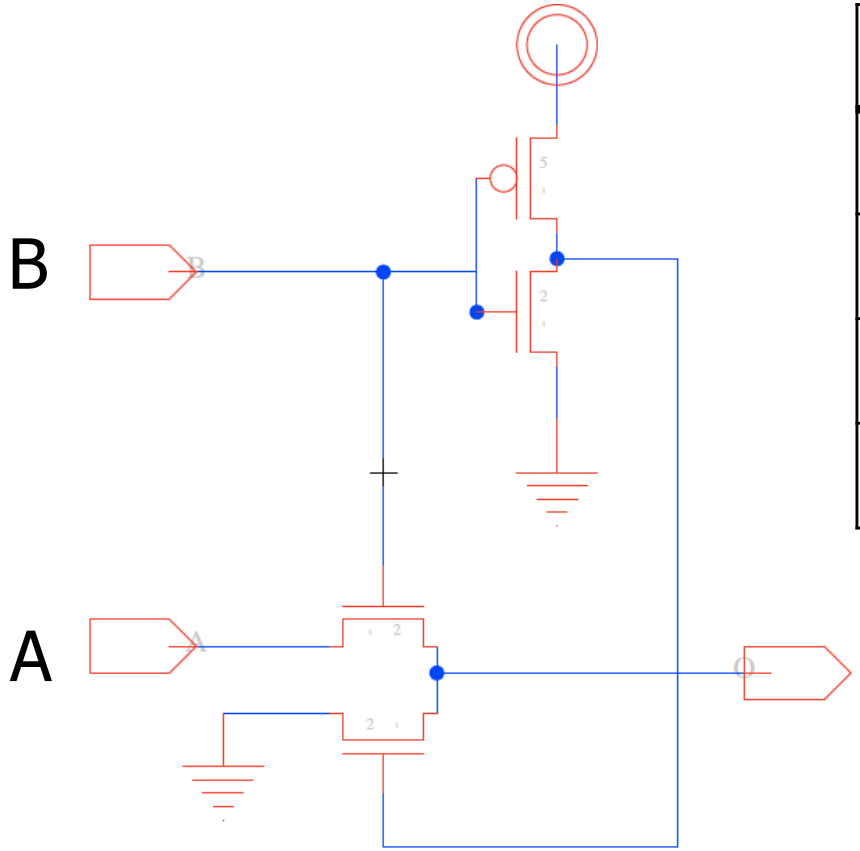
- What's the equivalent RC circuit?





Bonus

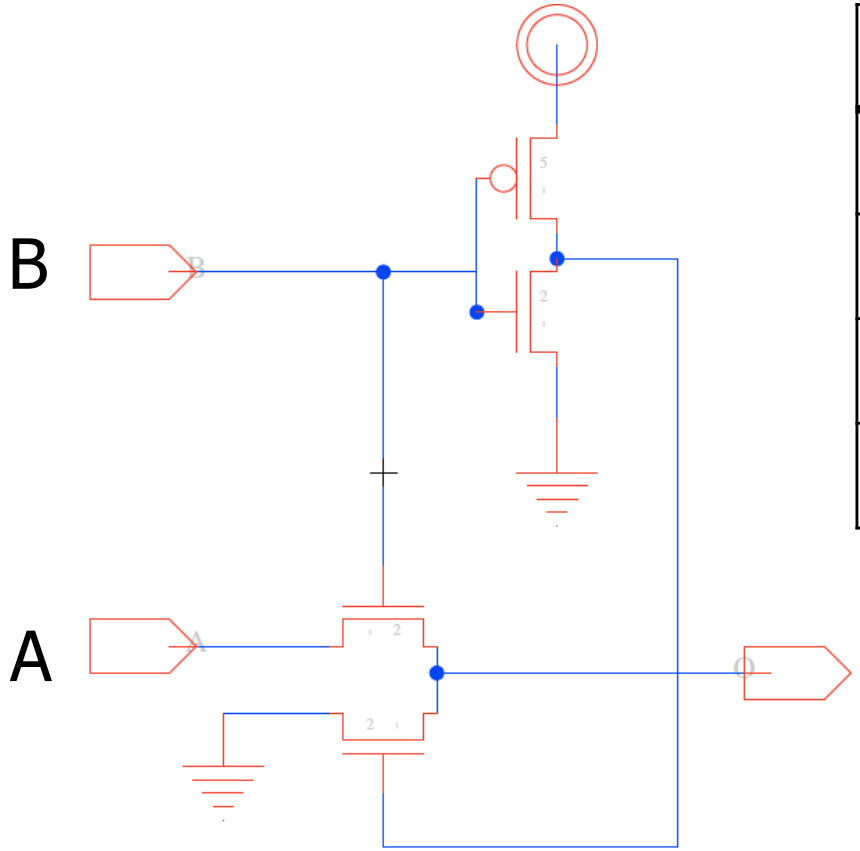
- What does this do?



A	B	Y
0	0	
0	1	
1	0	
1	1	

Bonus

- What does this do?



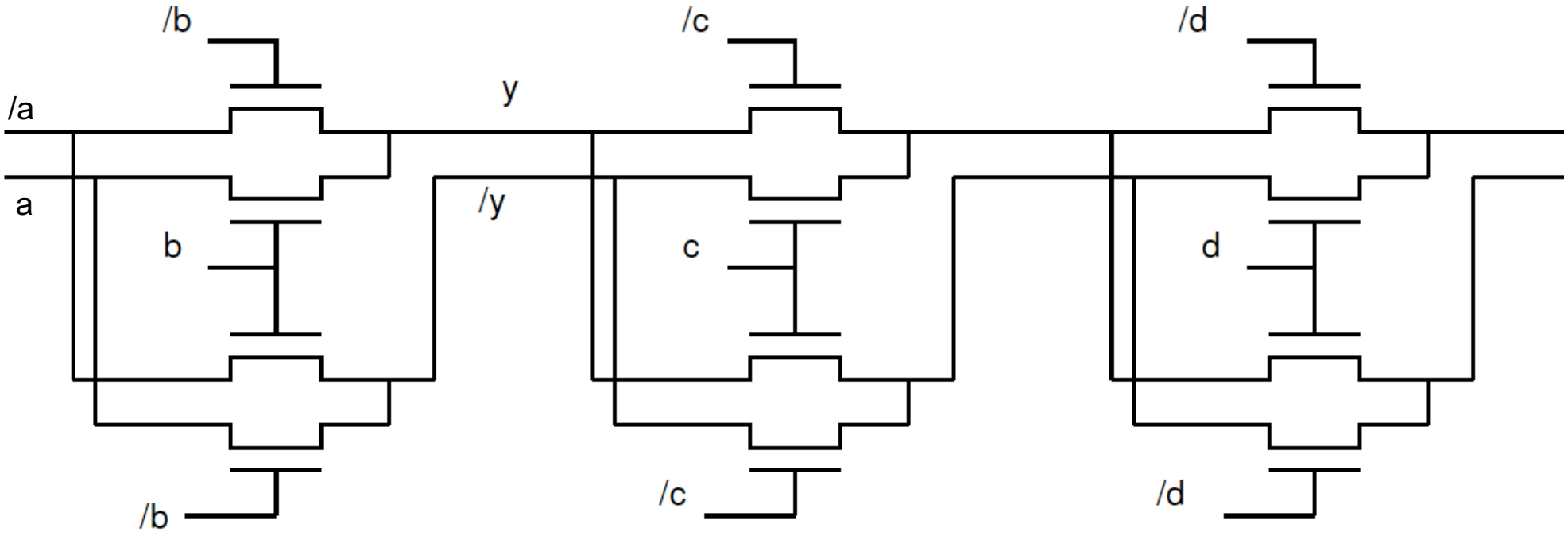
A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

More examples in the text

Cascading Pass Transistors

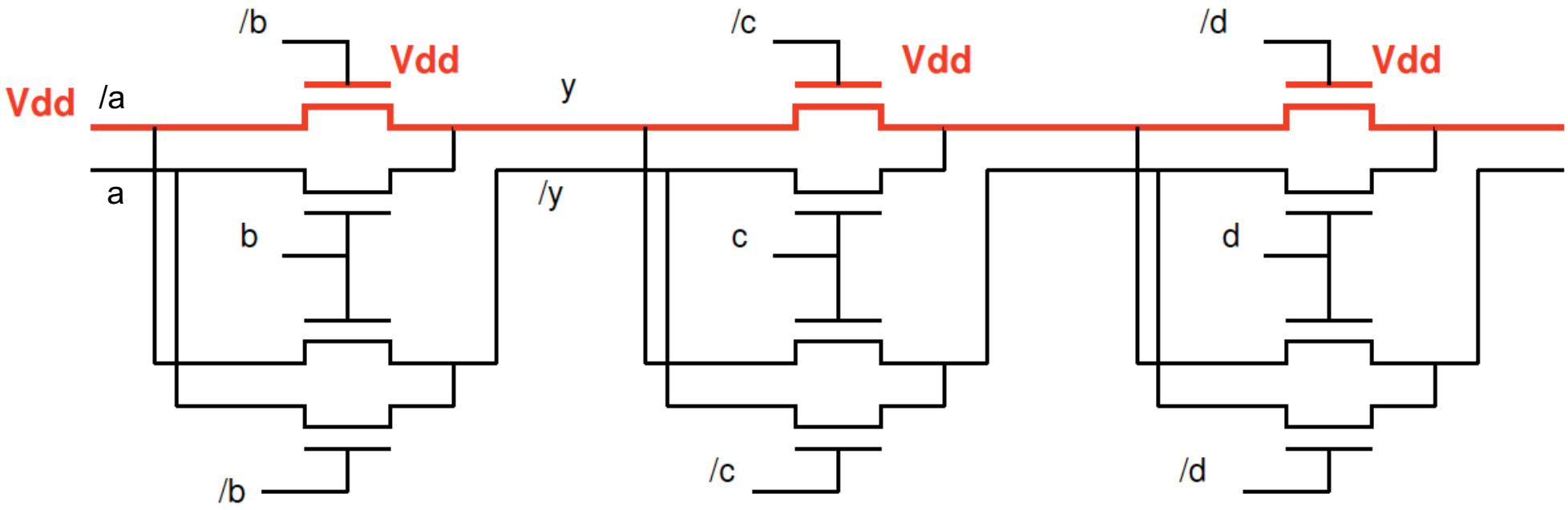
Chain without Inverters

- What if we did this?



Chain without Inverters

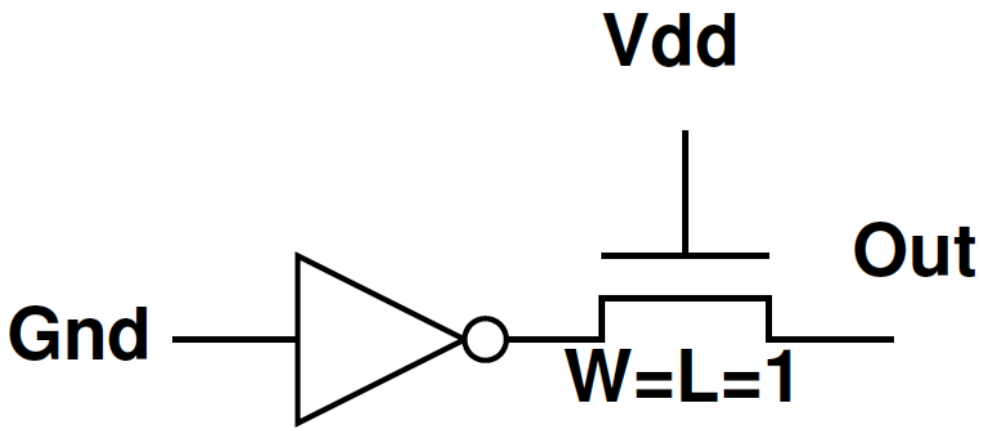
- Extract key path



Voltage of Chain (Preclass 4)

- What is voltage at output?

V_{dd}=1V
V_{thn}=-V_{thp}=0.3V



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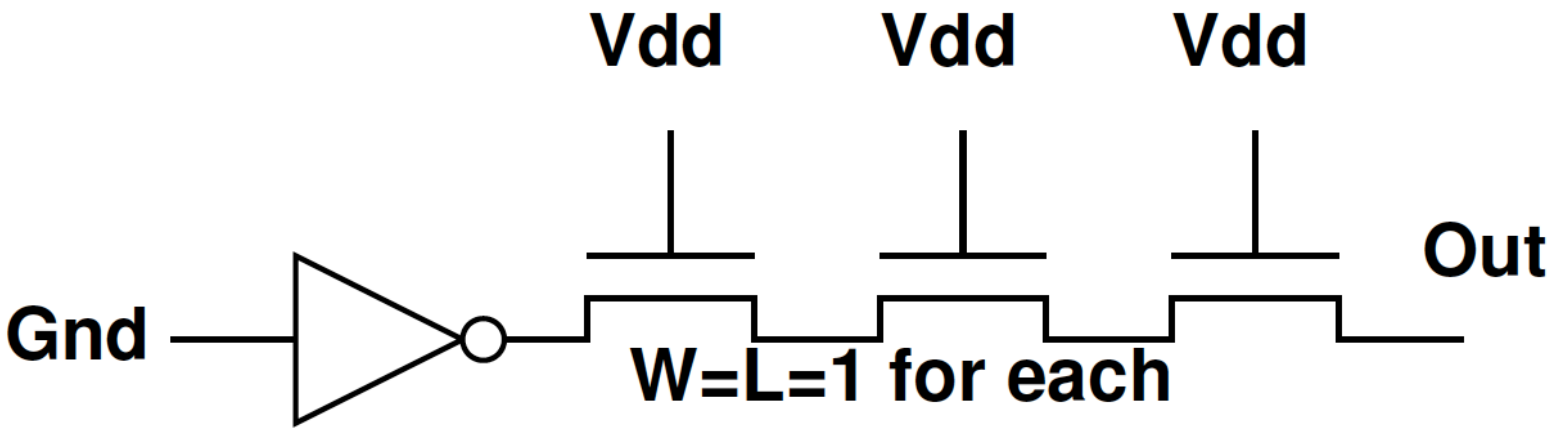
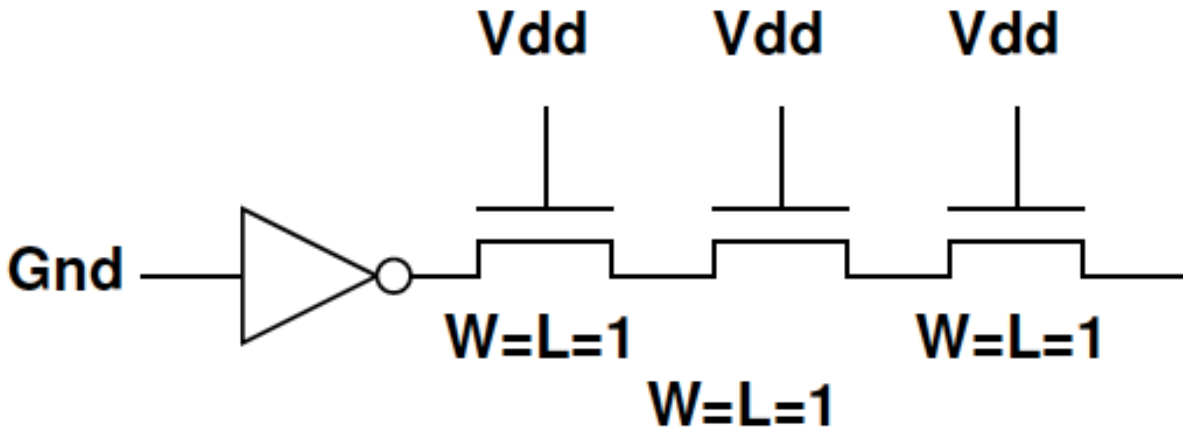
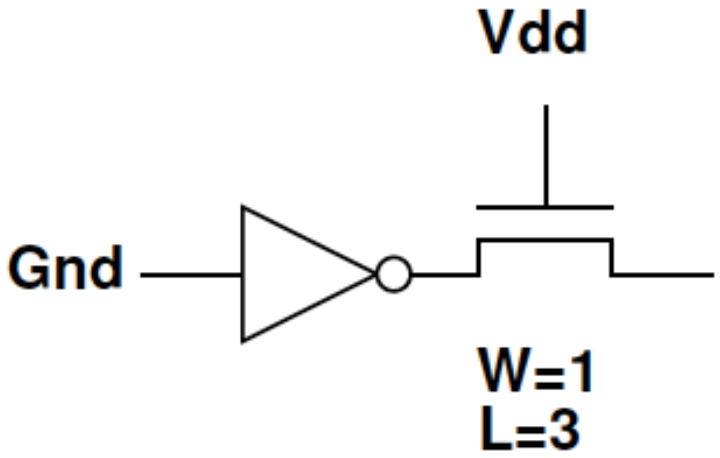


How compare (Preclass 4)

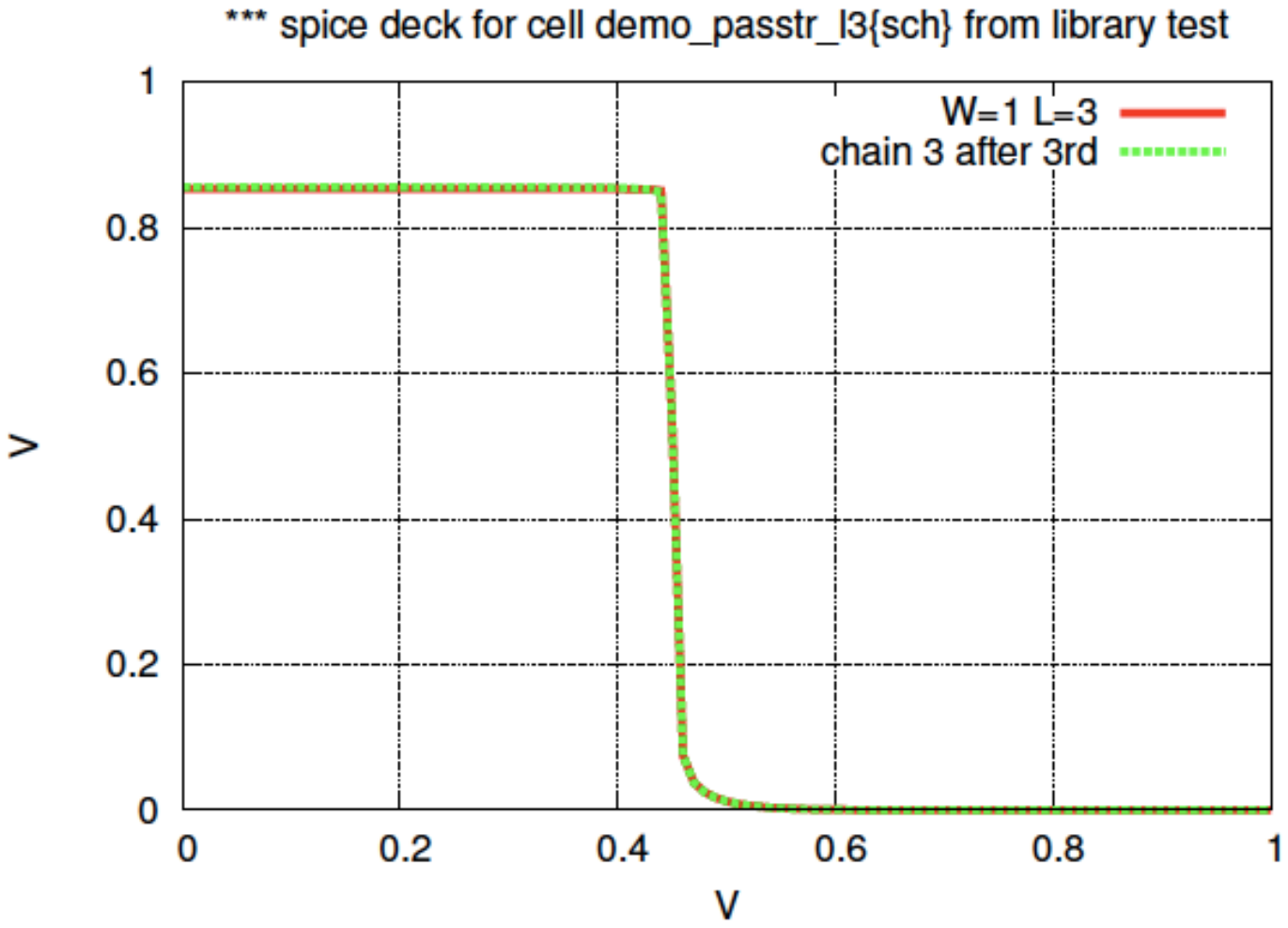
- Compare

V_{dd}=1V
V_{thn}=-V_{thp}=0.3V



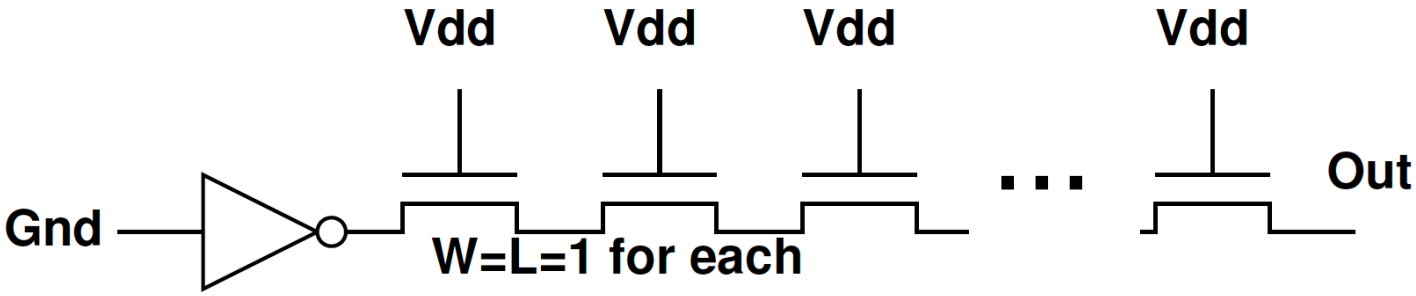


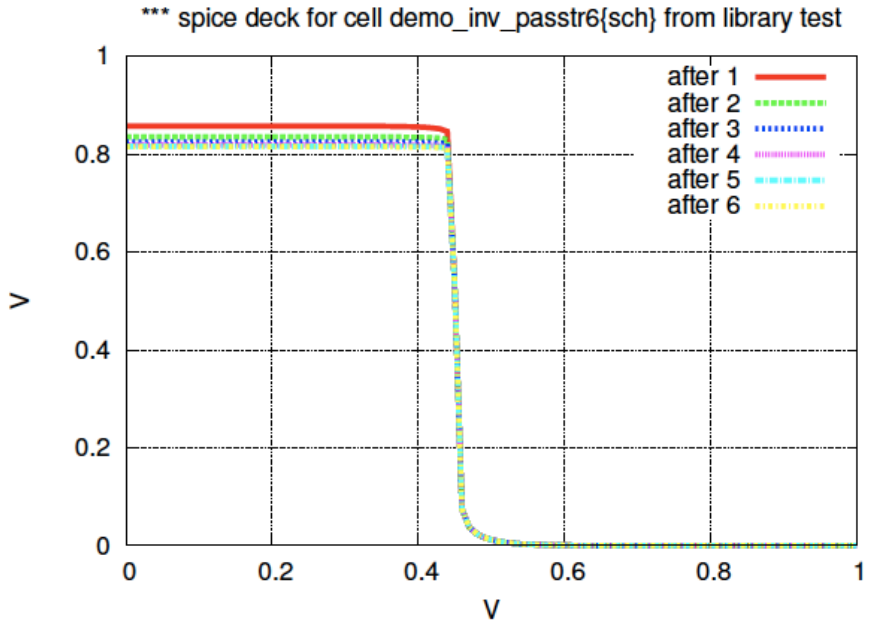
DC Analysis – chain of 3 vs length of 3



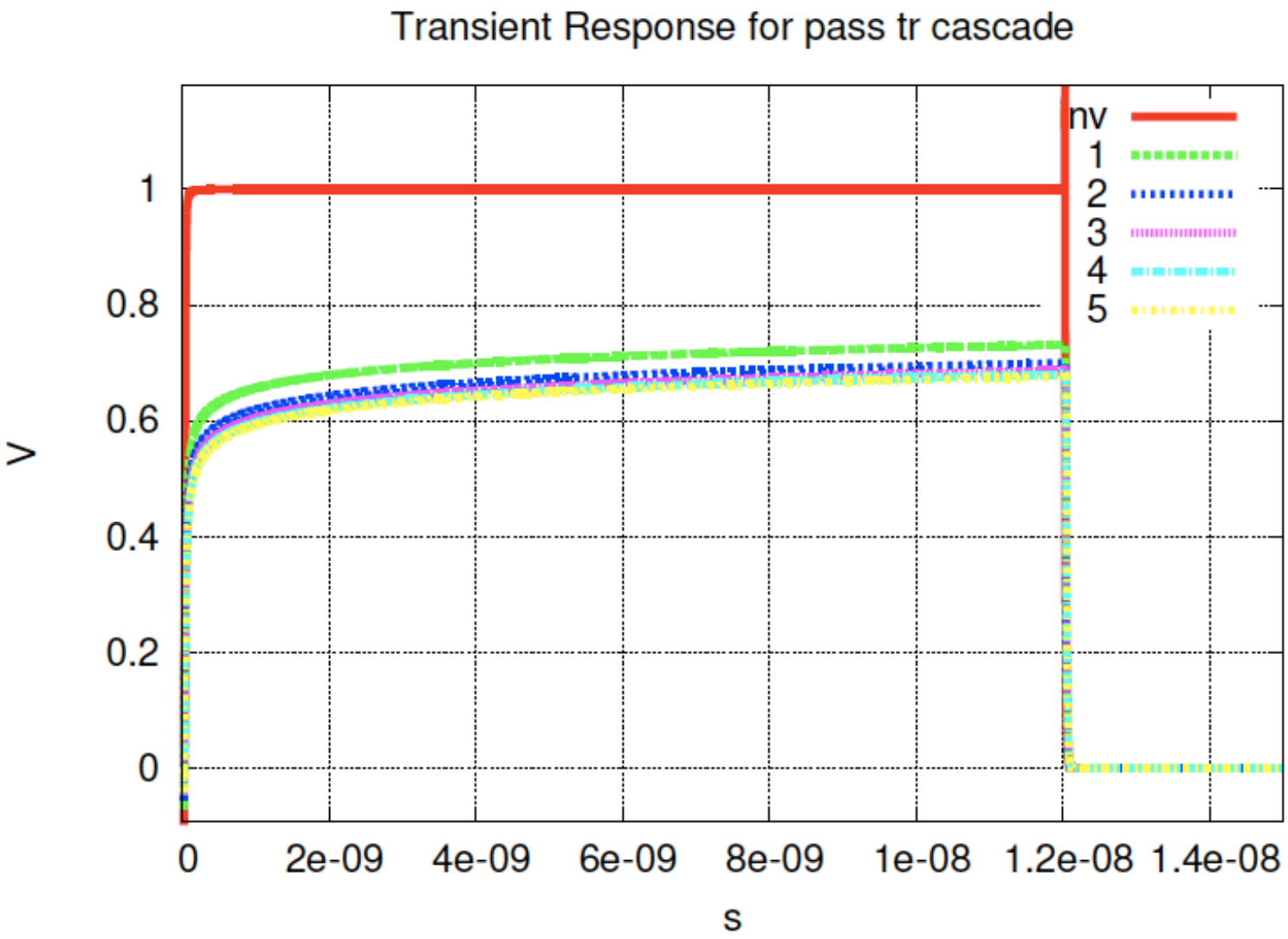
Conclude

- Can chain any number of pass transistors and only drop a single V_{th}

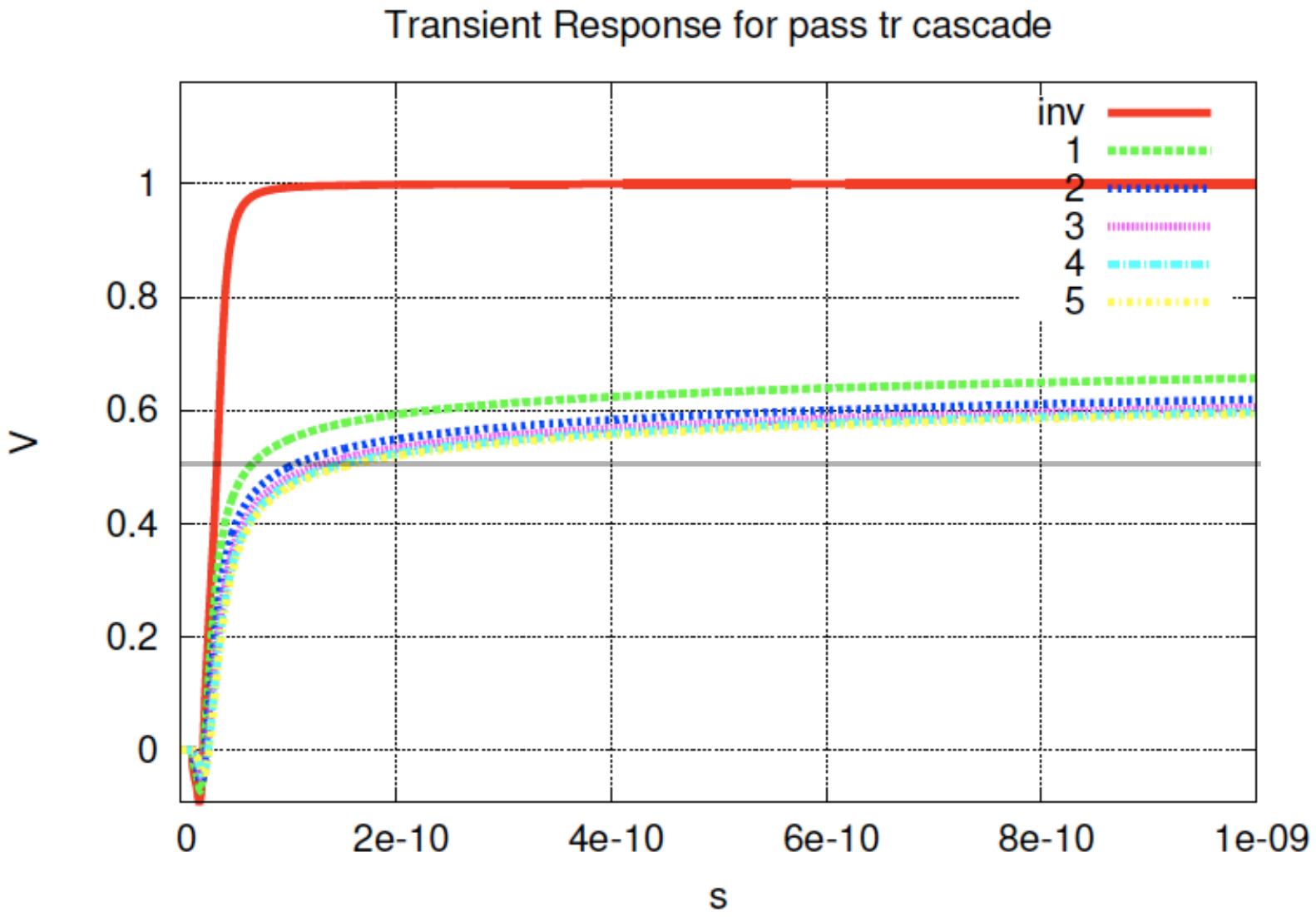




Transient

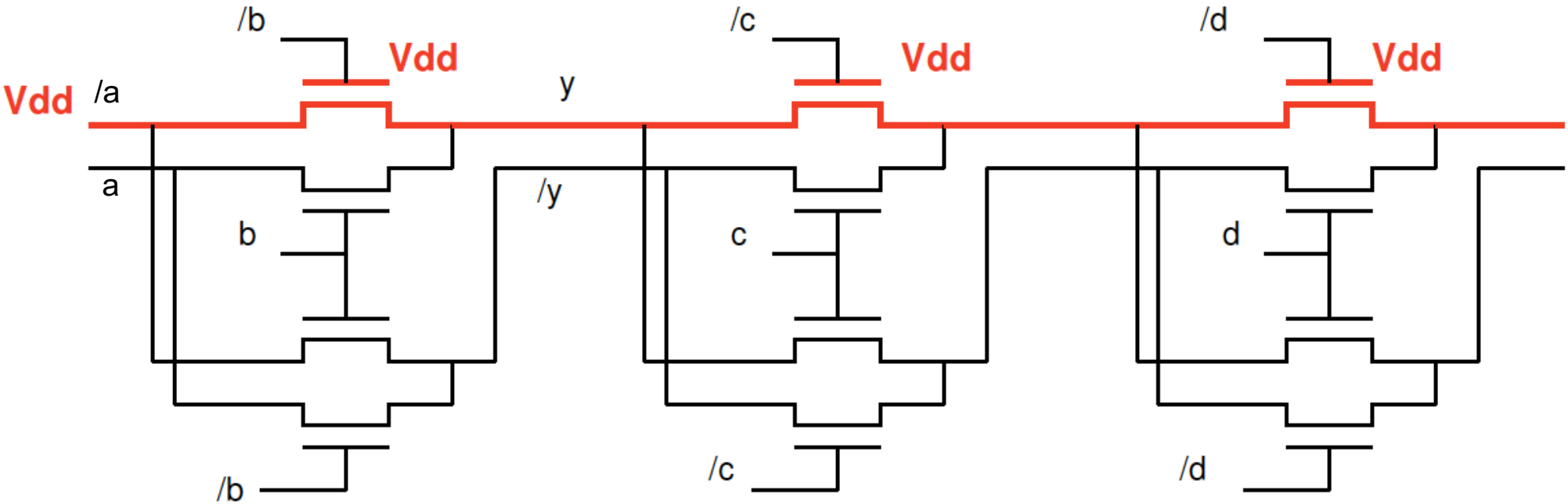

Transient Response for pass tr cascade
nv
1
2
3
4
5
V
1
0.8
0.6
0.4
0.2
0
0
2e-09
4e-09
6e-09
8e-09
1e-08
1.2e-08
1.4e-08
s

Transient: Zoomed Closeup



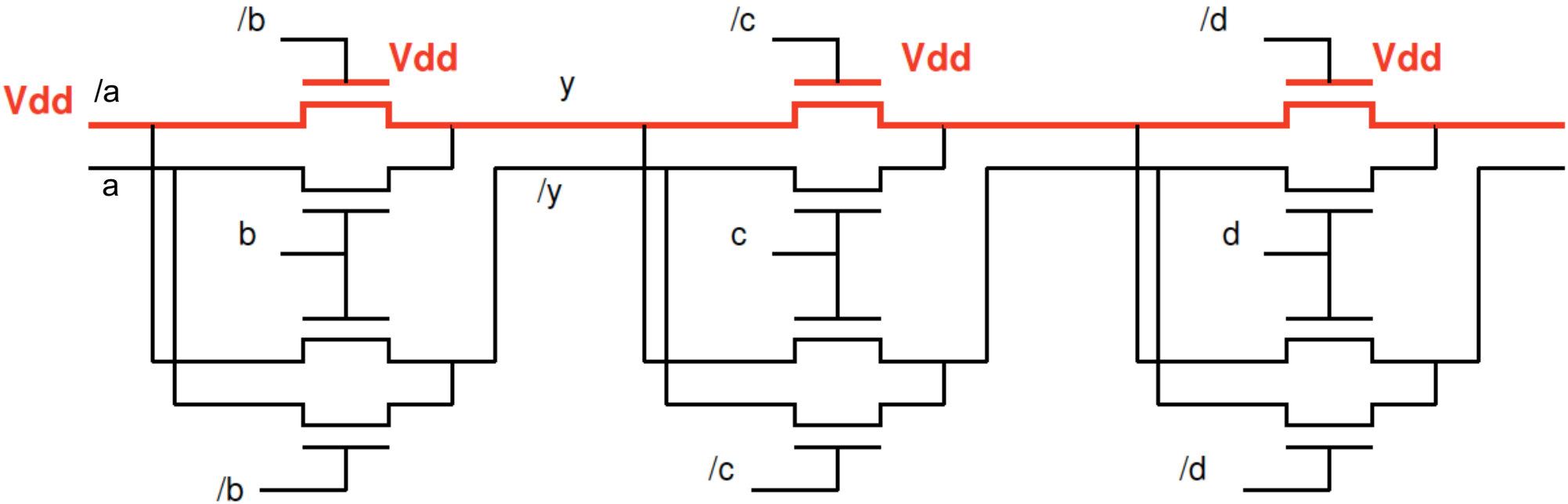
Capacitance

- What is output capacitance per stage?
  - I.e. What is the capacitance at output y?



Delay Setup

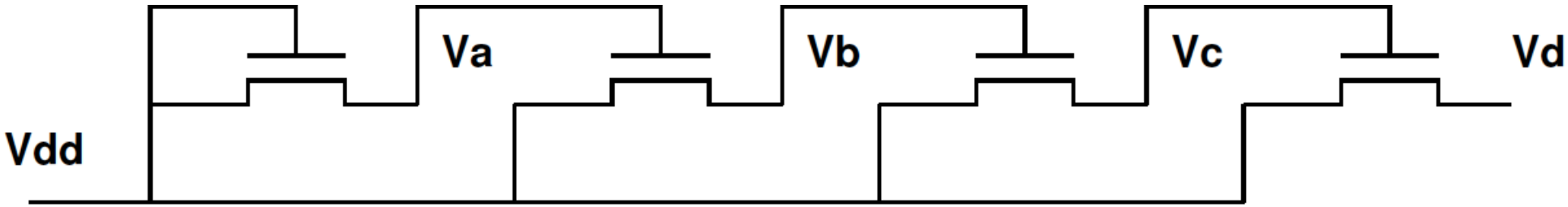
- What does RC circuit look like?



Gate Cascade? (Preclass 5)

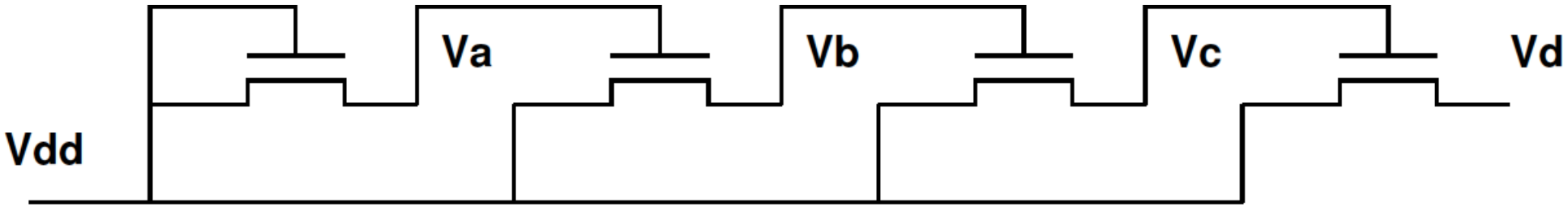
- What are the voltages?

V_{dd}=1V
V_{thn}=-V_{thp}=0.3V



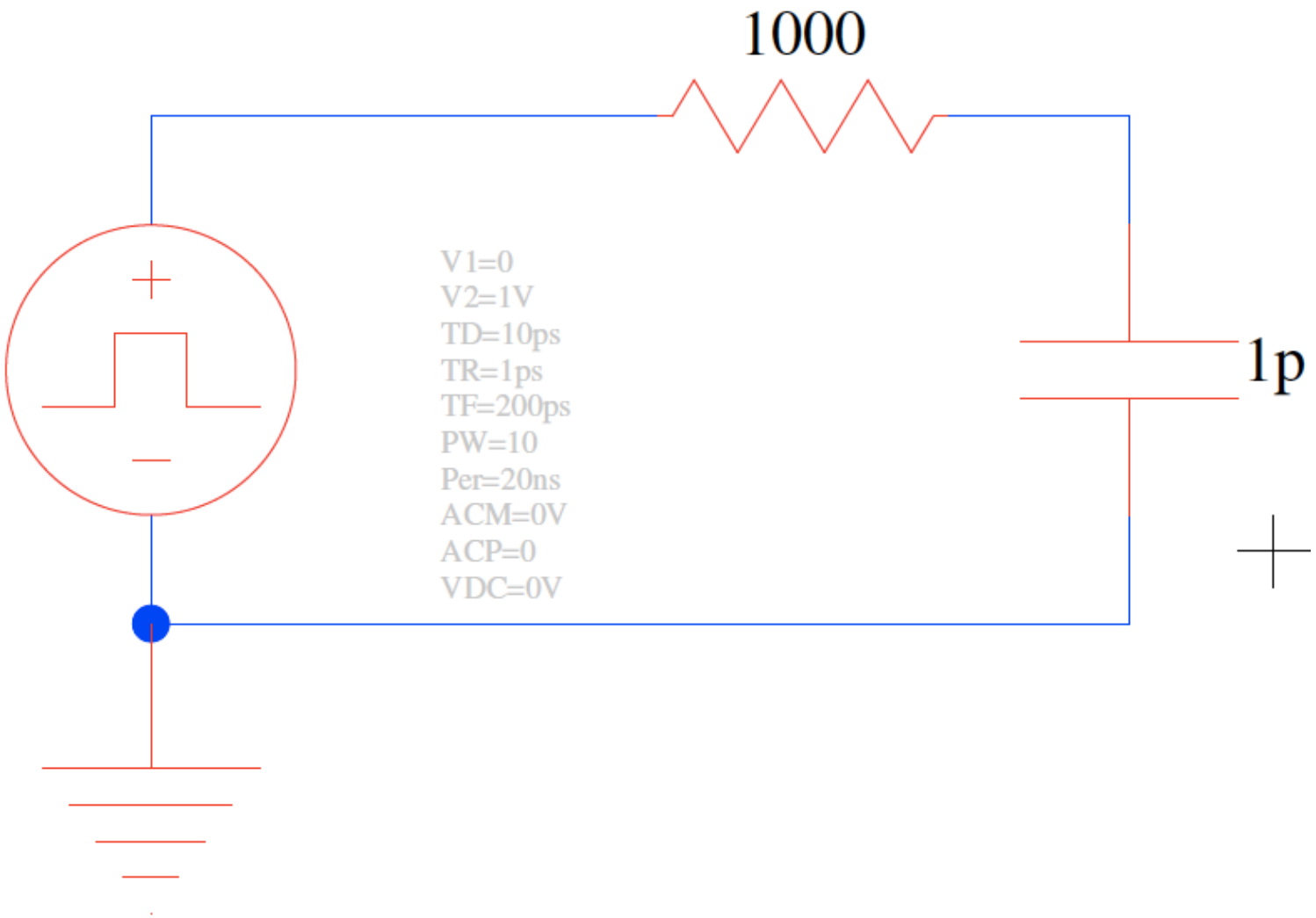
Conclude

- Cannot cascade degraded inputs into **gates**.

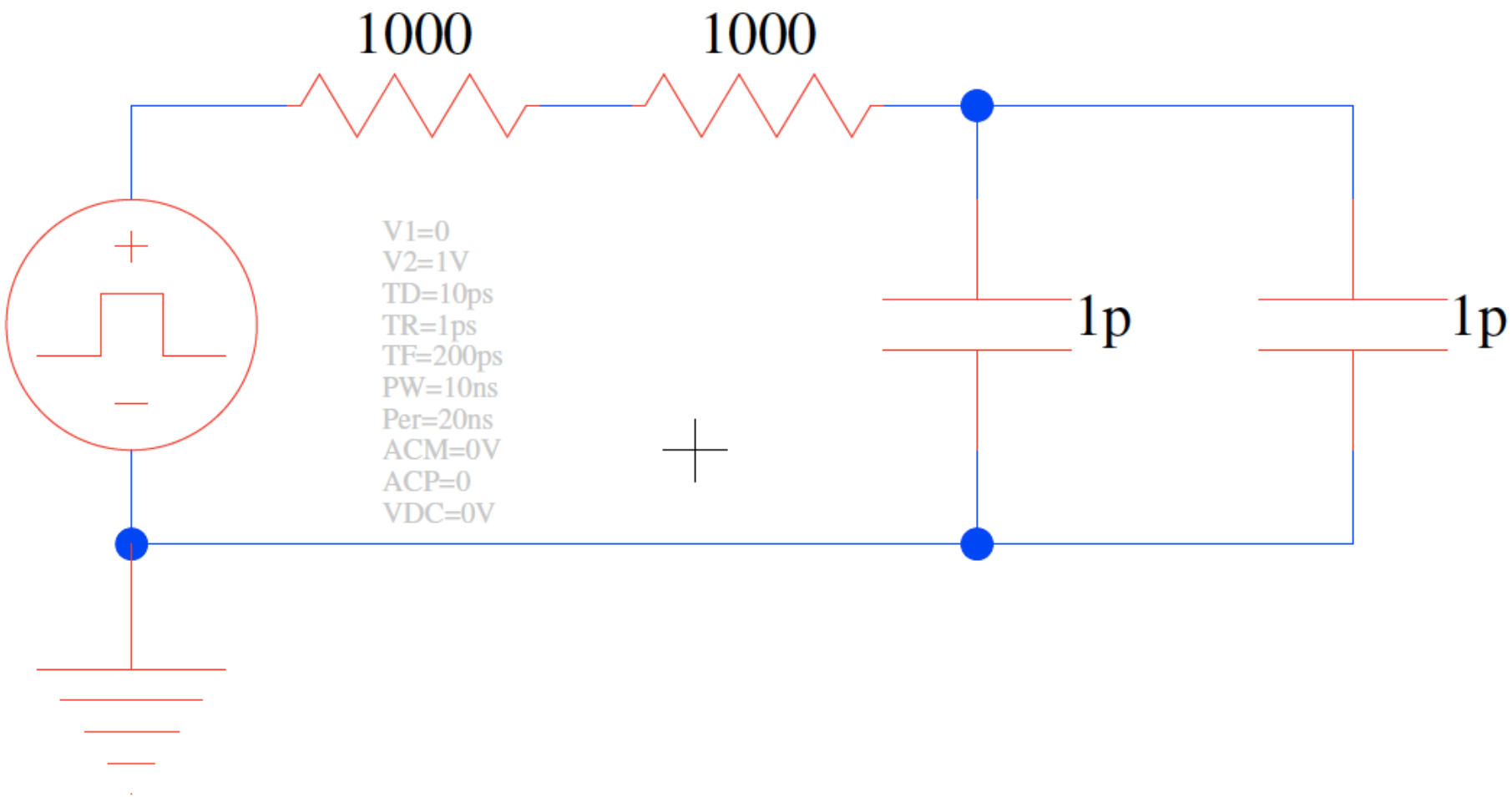


Distributed RC (setup)

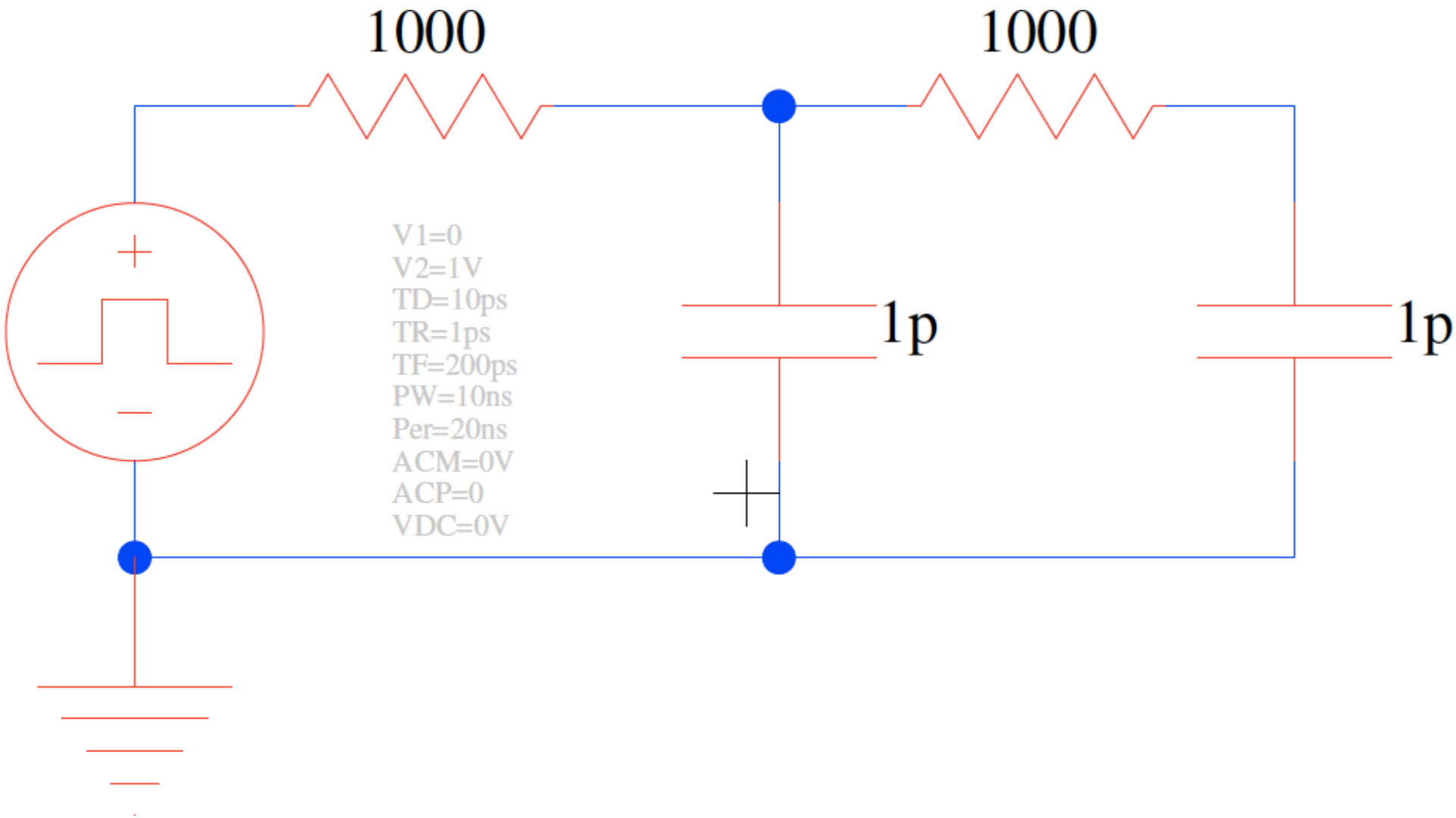
What is response? (Preclass 6)



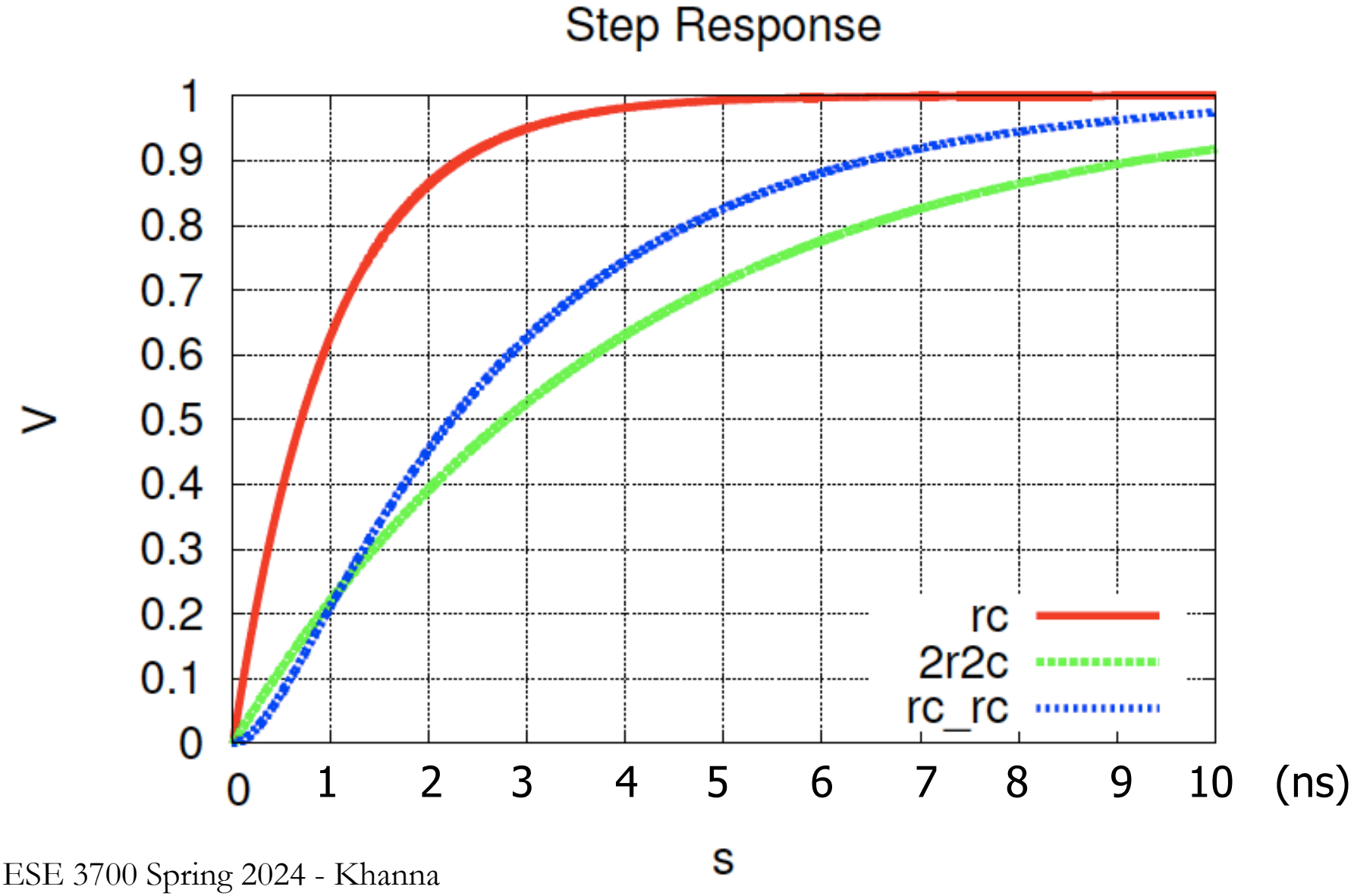
What is response? (Preclass 6)



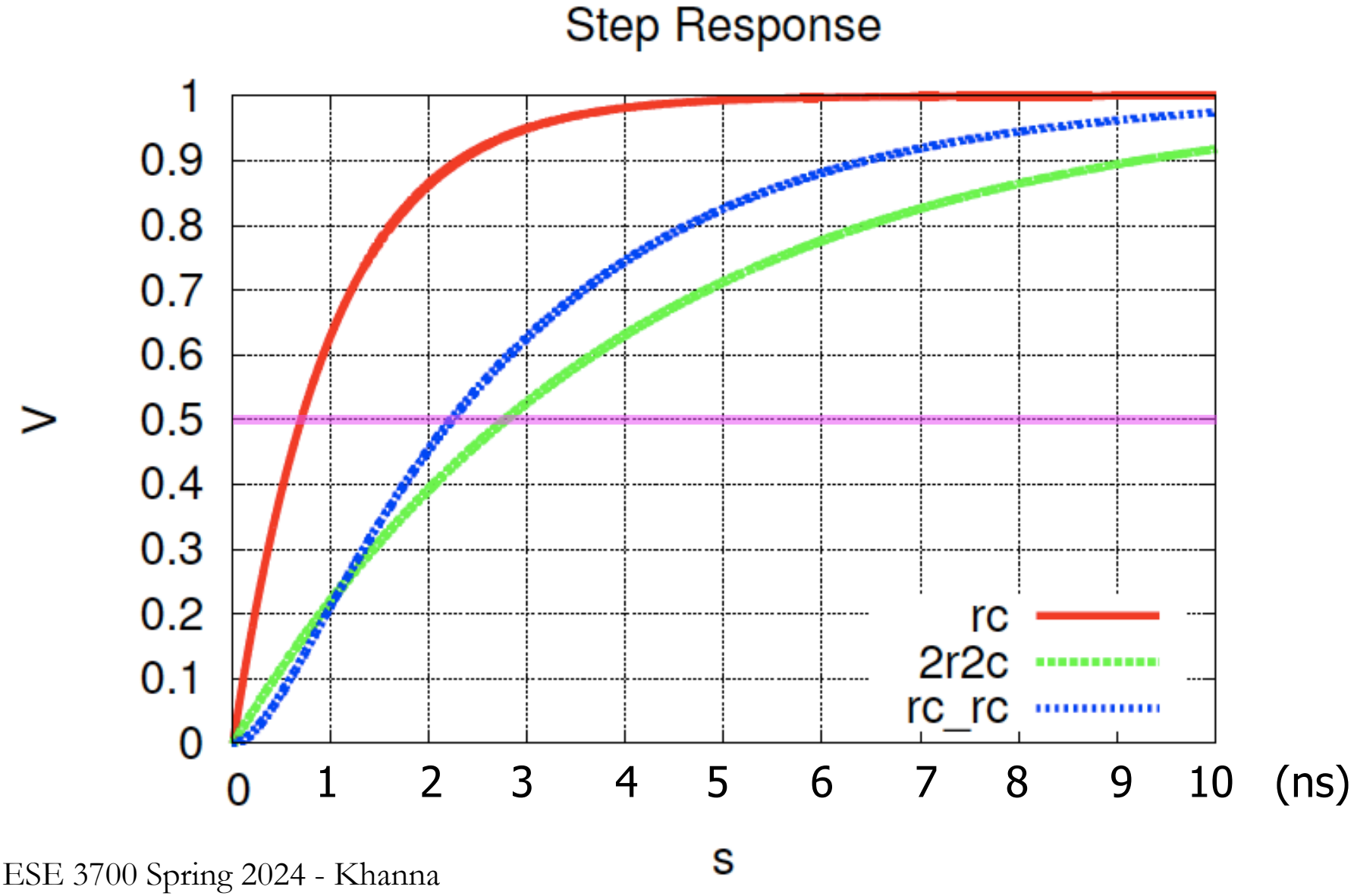
What is response? (Preclass 6)



SPICE Response

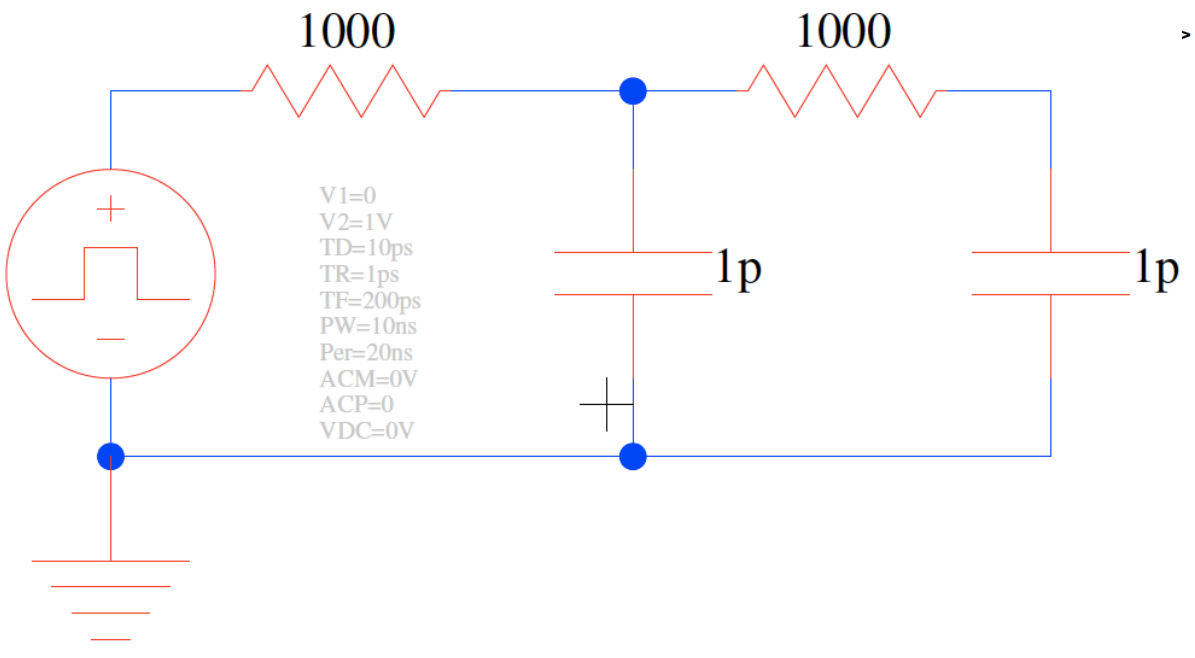


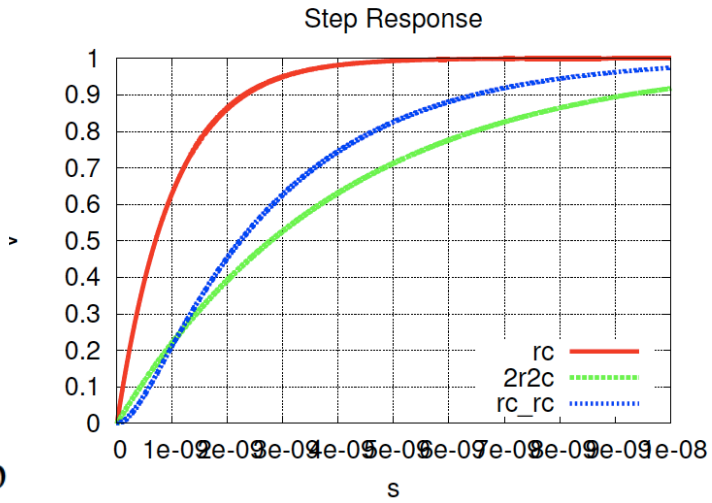
SPICE Response



Intuition

- Look at series of R's on path
  - Must move Q=V(ΣC) across each R





Idea

- There are other circuit disciplines
- Can use pass transistors for logic
  - Even chains of pass transistors
  - Mostly gives area win, sometimes gives delay win
    - Will talk more about delay on Wednesday
- Do not cascade as easily as CMOS

Admin

- Project 1 out now
  - Design 8-bit ripple-carry adder
    - You already know how to do this
    - Refresh yourself on binary addition of 2 bits
  - Work individually
  - Full report due F 3/29
    - Milestone: Plan to have baseline built and characterized by 3/22
      - Have separate test schematic for each metric. Will save you time!!
        - Delay
        - Active energy
        - Leakage energy

Logic Types

- CMOS Gates
  - Dual pull-down and pull-up networks, only one enabled at a time
  - Performance of gate is strong function of the fanin of gate
    - Techniques to improve performance include sizing, input reordering, and buffering (staging)
- Ratioed Gates
  - Have active pull-down (-up) network connected to load device
  - Reduced gate complexity at expense of static power asymmetric transfer function
    - Techniques to improve performance include sizing to improve noise margins and reduce static power
- Pass Gates
  - Implement logic gate as switch network for reduced area and load capacitance
  - Long cascades of switches result in quadratic increase in delay
  - Also suffer from reduced noise margins (V_T drop)
    - Use level-restoring buffers to improve noise margins

- Dynamic logic … coming up soon

Acknowledgement

- Prof. André DeHon (University of Pennsylvania)
- Prof. Jing Li (University of Pennsylvania)