

# ESE3700: Circuit-Level Modeling, Design and Optimization for Digital Systems

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Lec 14: March 20, 2024

Distributed RC Wire and Elmore Delay,  
CMOS Worst Case Delay (if time)





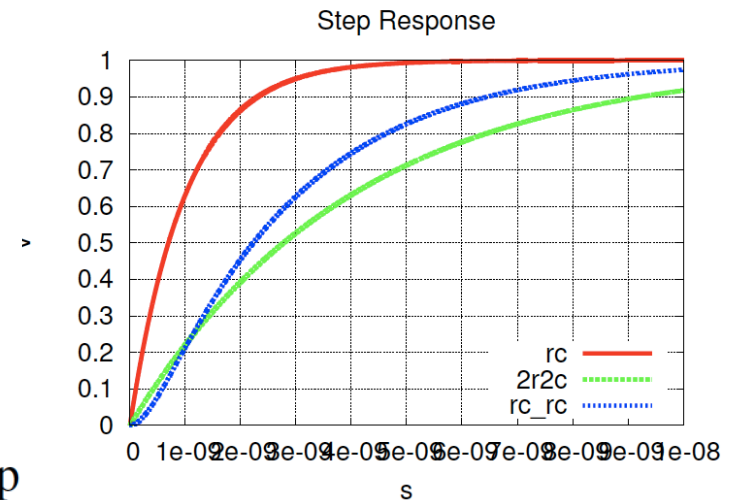
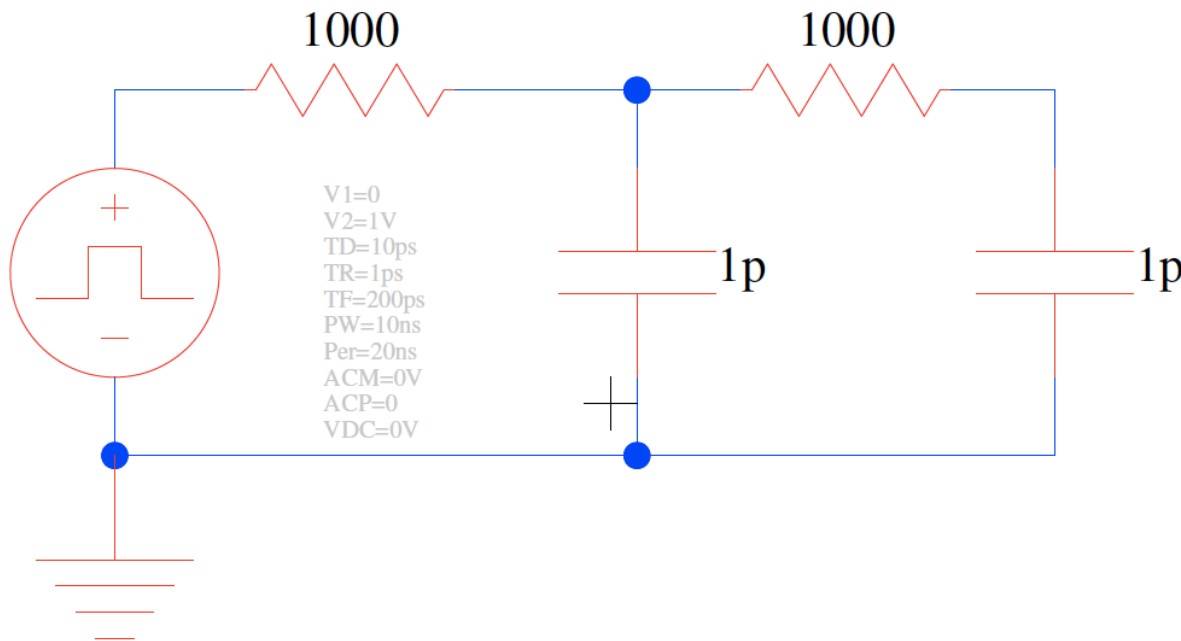
# Today

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- ❑ Estimate delay in RC Network
  - Elmore delay calculation
- ❑ Apply to wire delay
- ❑ Apply to pass transistor circuits
- ❑ Apply to CMOS gates
- ❑ CMOS Worst Case Delay (if time)

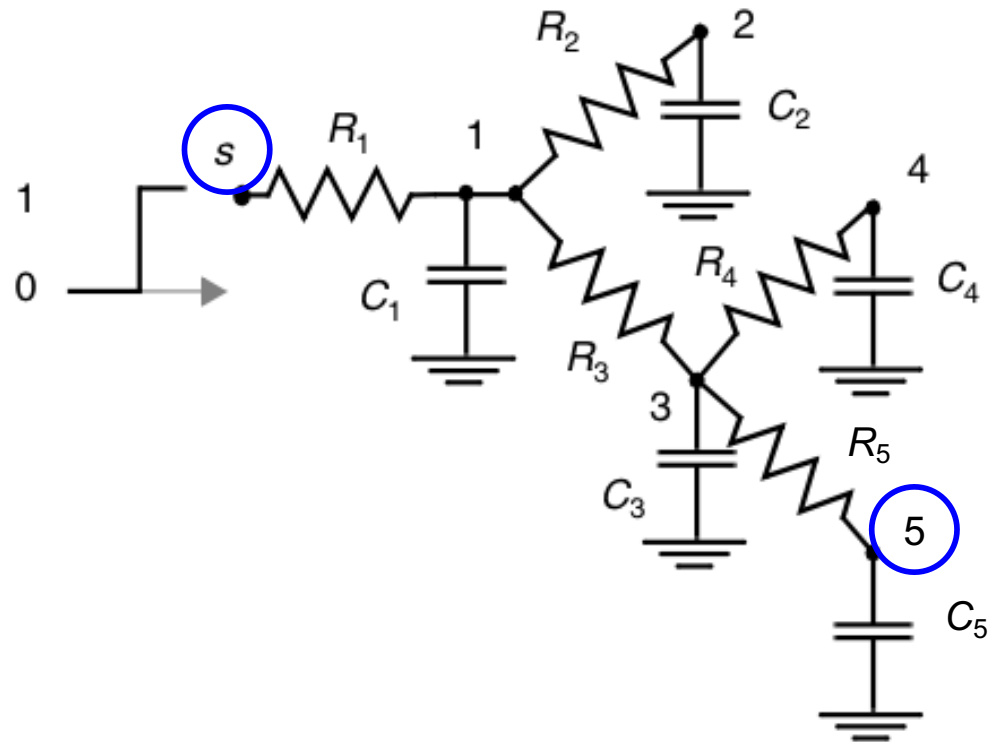
# Intuition (Preclass 1)

- Look at series of R's on path
  - Must move  $Q=V(\Sigma C)$  across each R



# Elmore Delay: Distributed RC network

- The delay from source  $s$  to node 5
  - $N$  = number of nodes in circuit

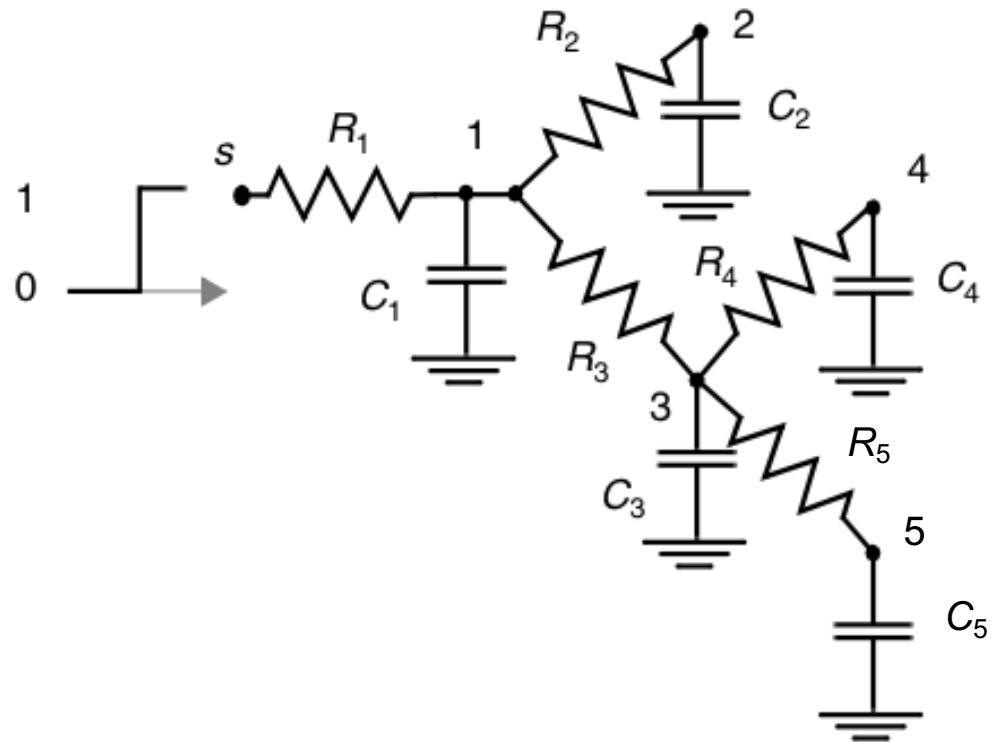


# Elmore Delay: Distributed RC network

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$$R_{5k} = \sum R_j \Rightarrow (R_j \in [\text{path}(s \rightarrow 5) \cap \text{path}(s \rightarrow k)])$$

$$\tau_{D5} = \sum_{k=1}^N C_k R_{5k}$$

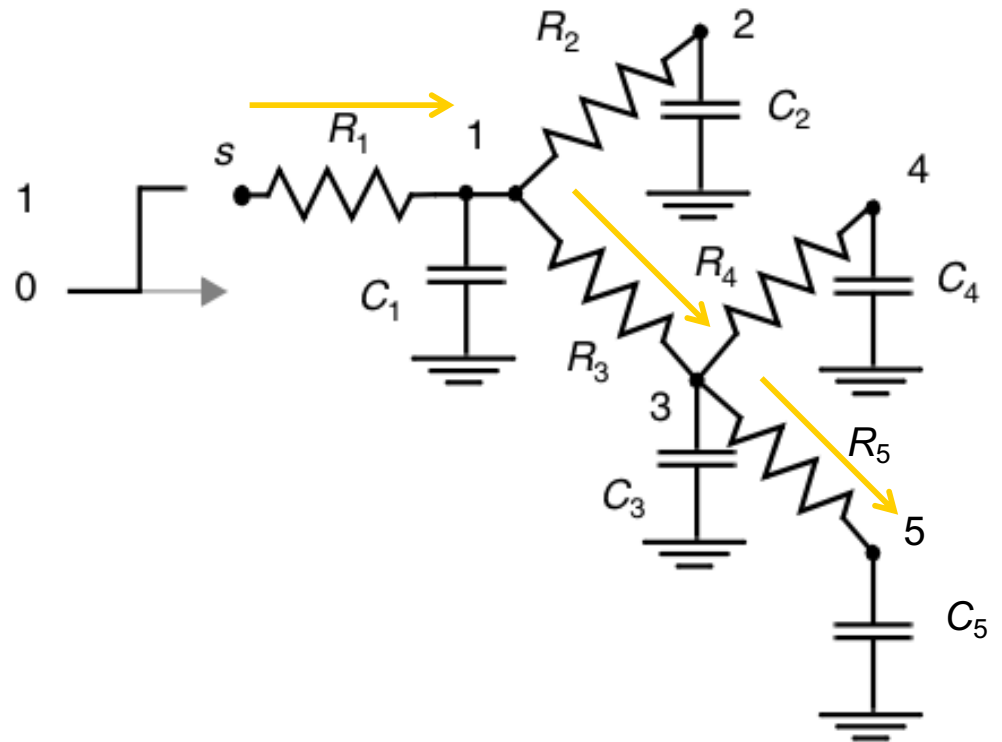


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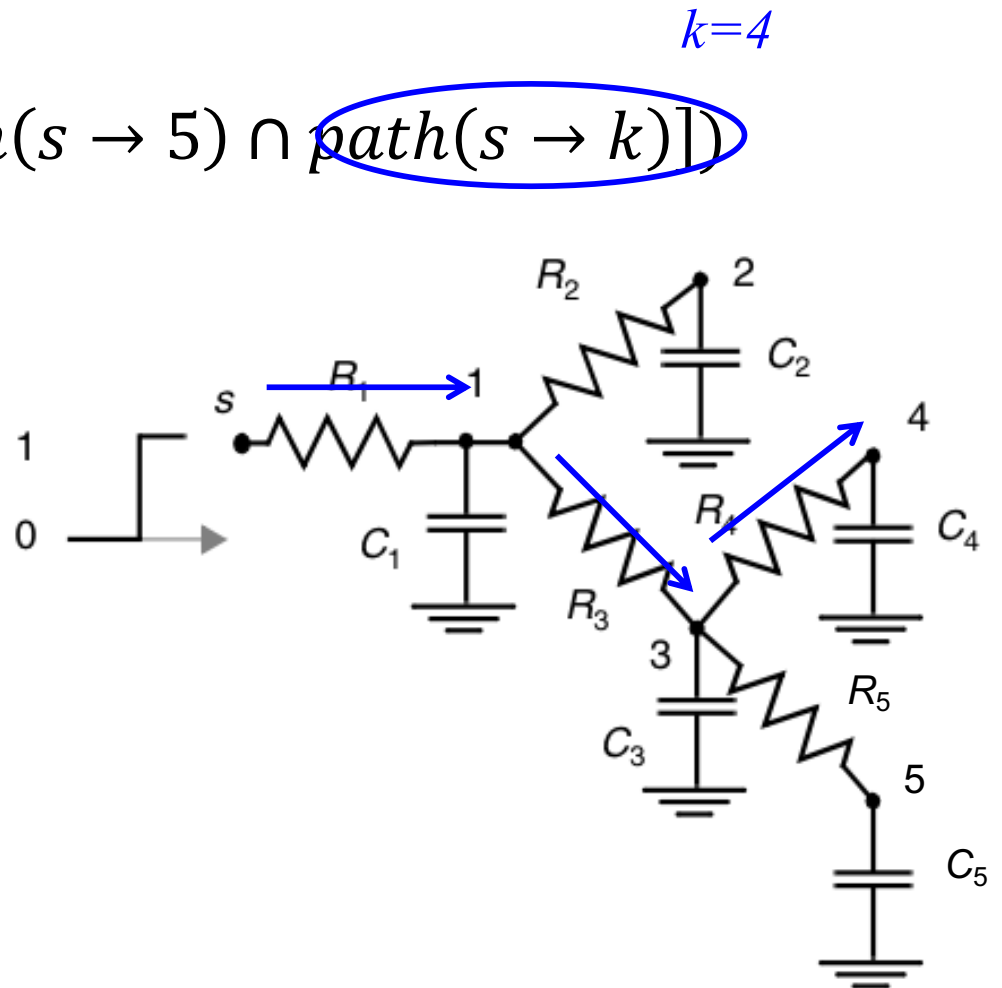


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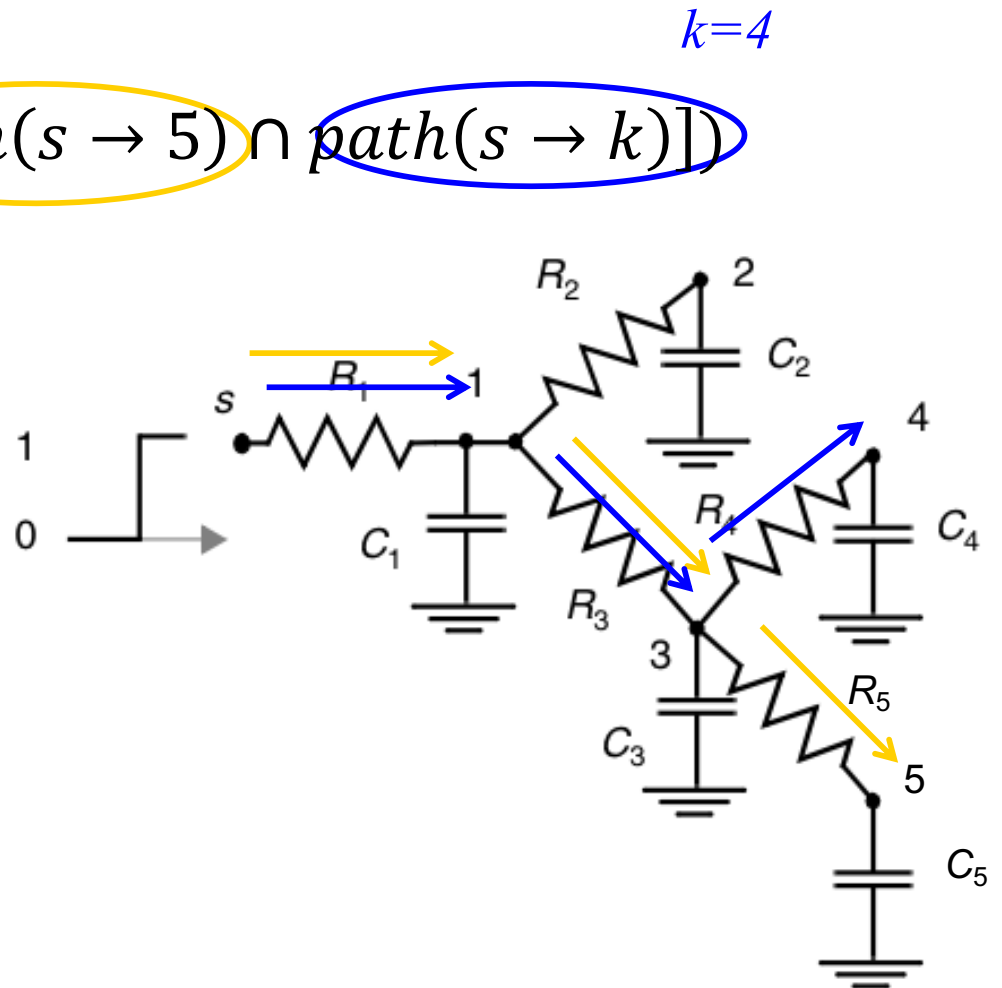
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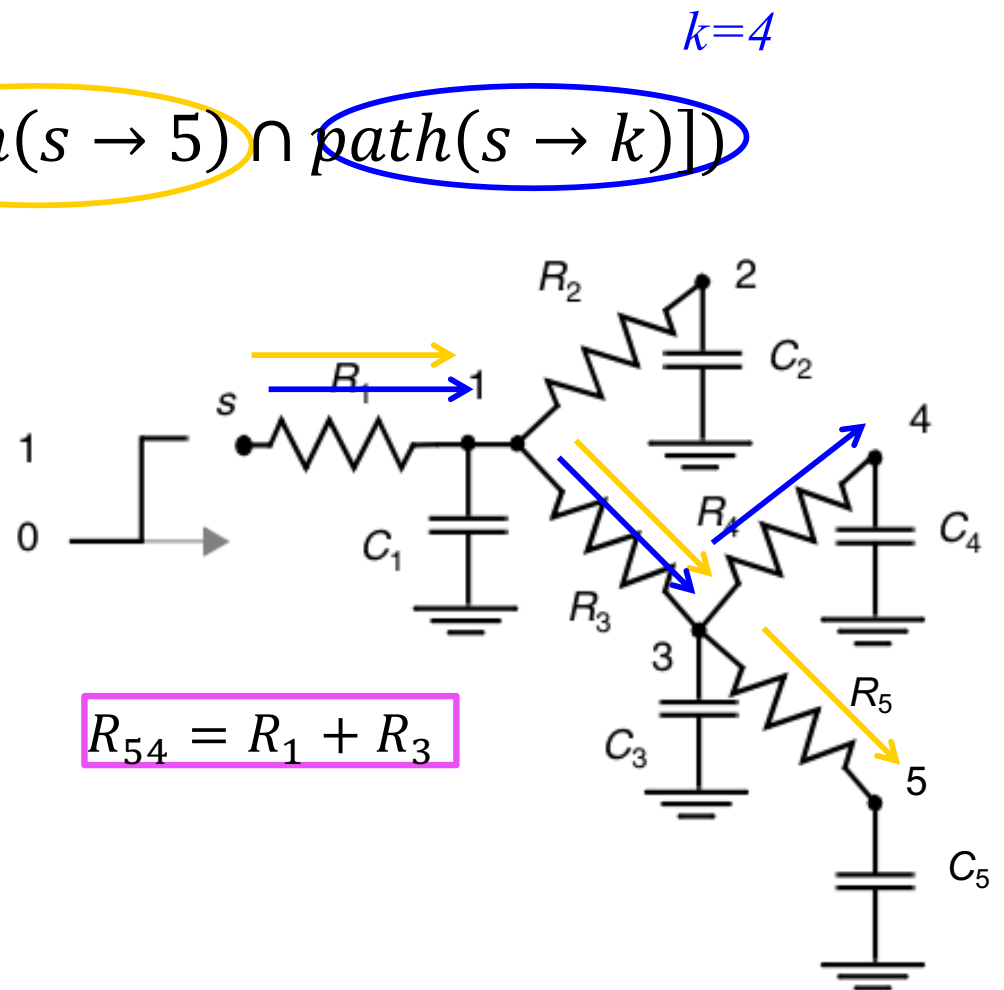
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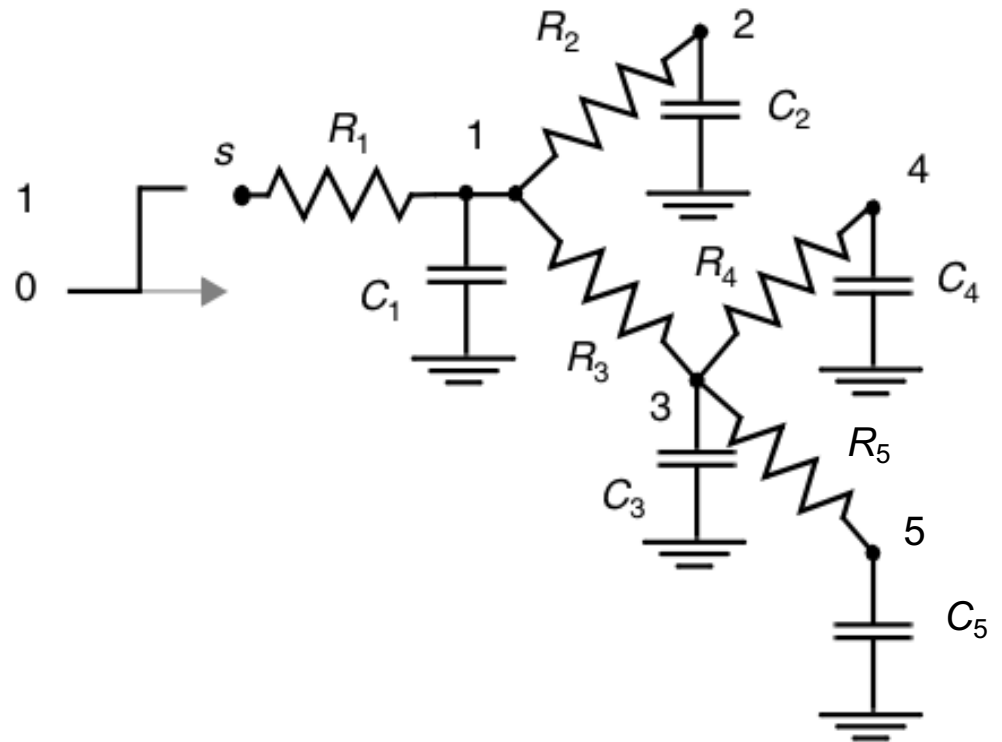


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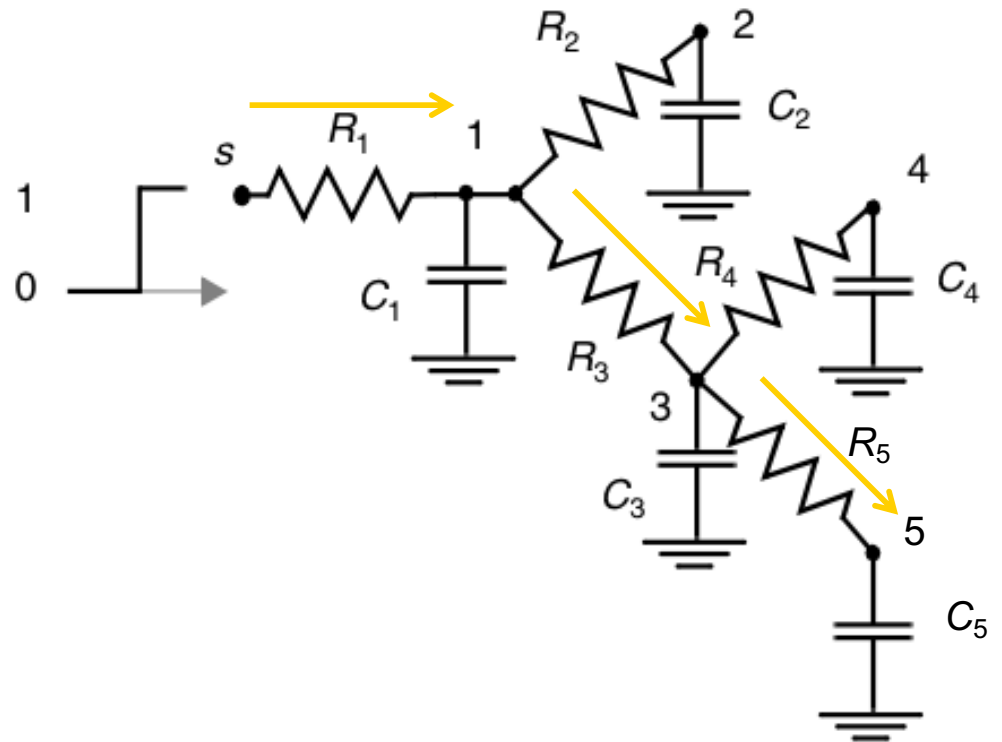


# Elmore Delay: Distributed RC network

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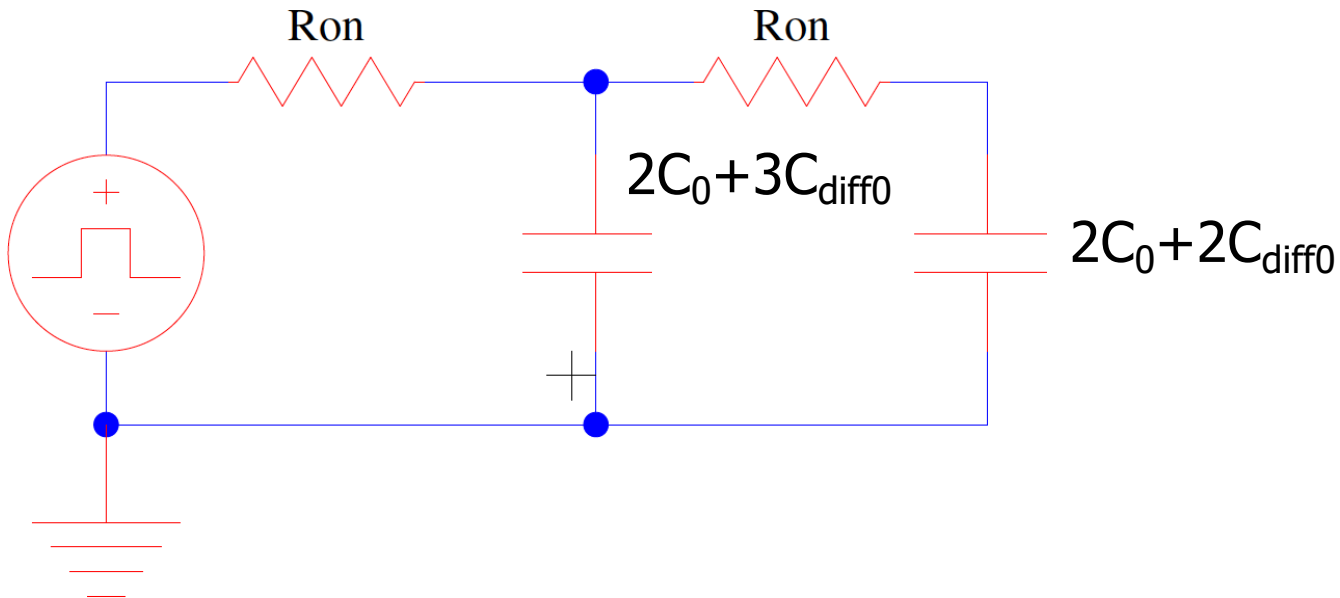
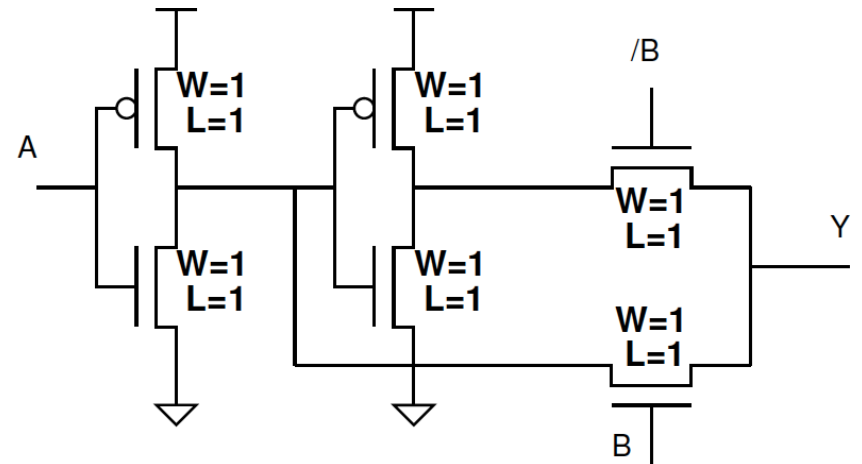
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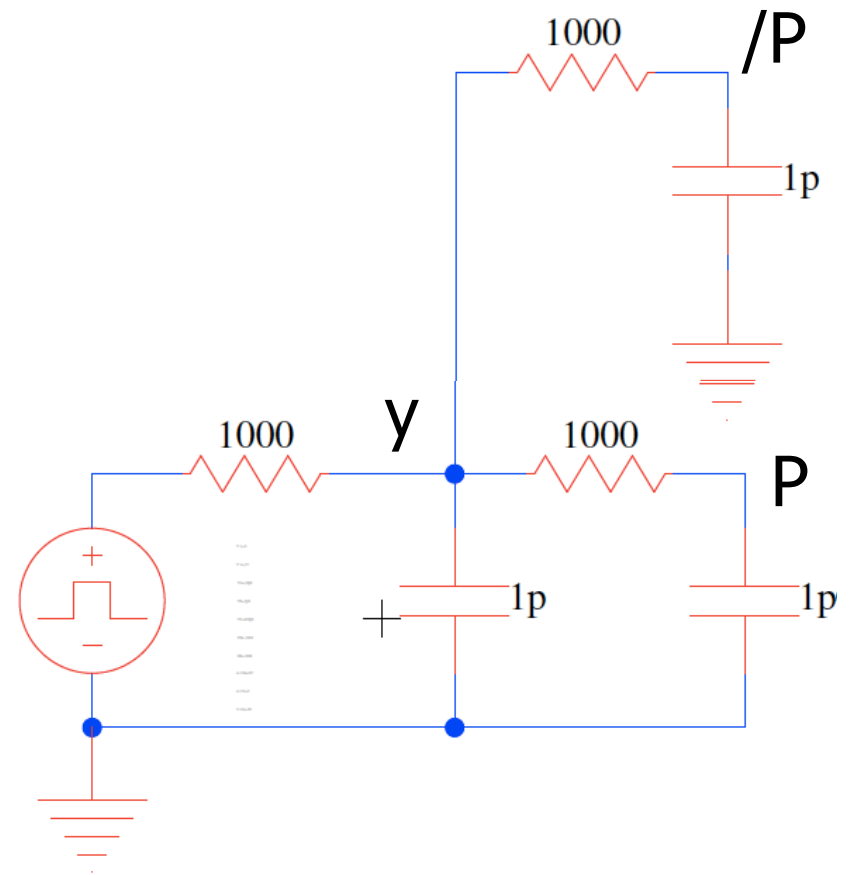
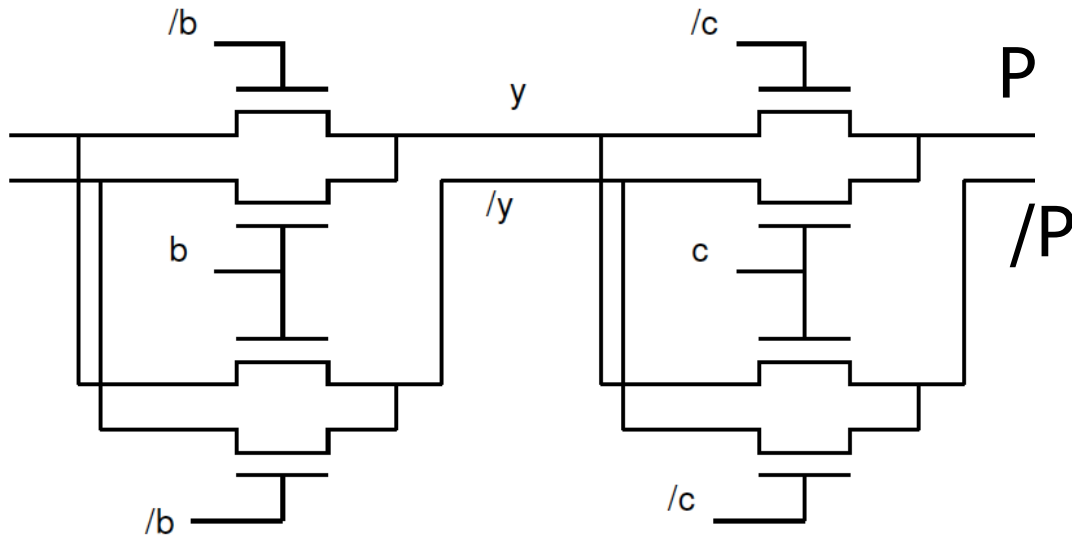




# Previously: Equivalent RC



# What is response?

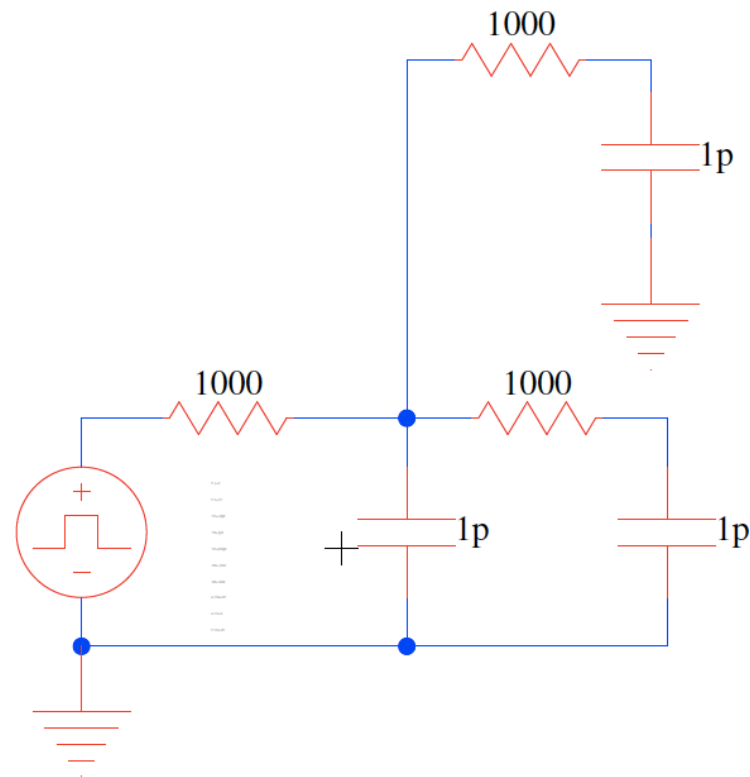


# Elmore Delay: Practice (preclass 1)

- The delay from source  $s$  to node  $i$ 
  - $N$  = number of nodes in circuit

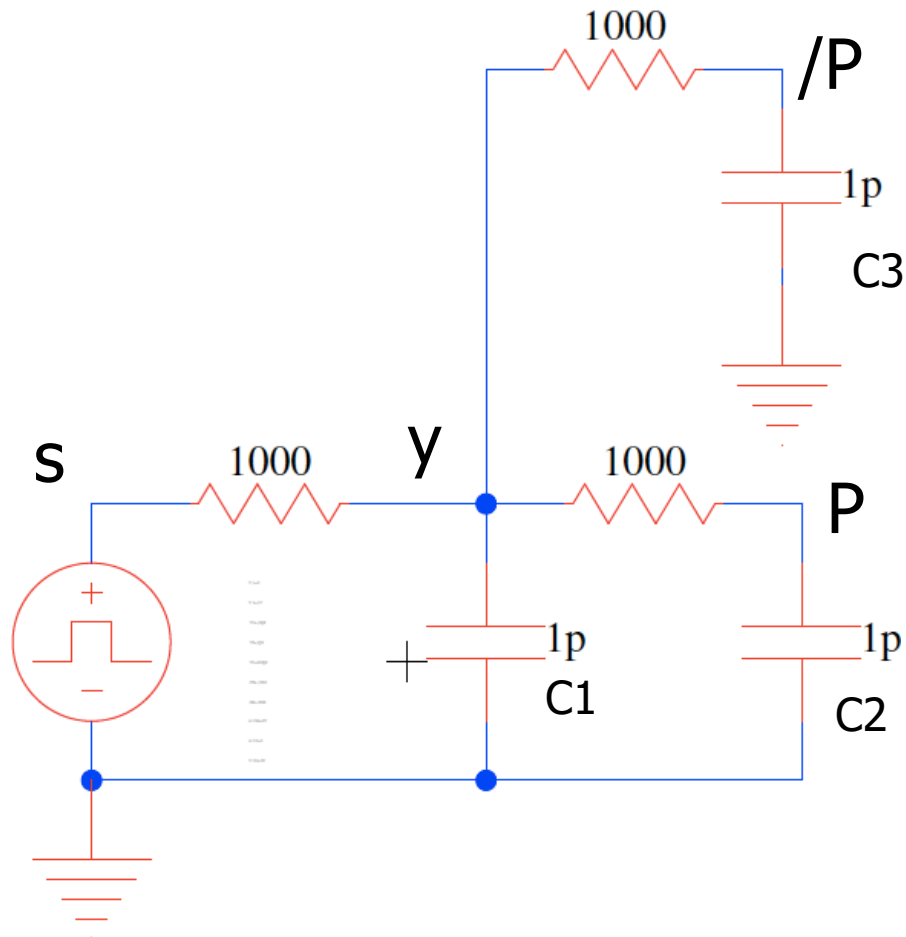
$$R_{ik} = \sum R_j \Rightarrow (R_j \in [path(s \rightarrow i) \cap path(s \rightarrow k)])$$

$$\tau_{Di} = \sum_{k=1}^N C_k R_{ik}$$



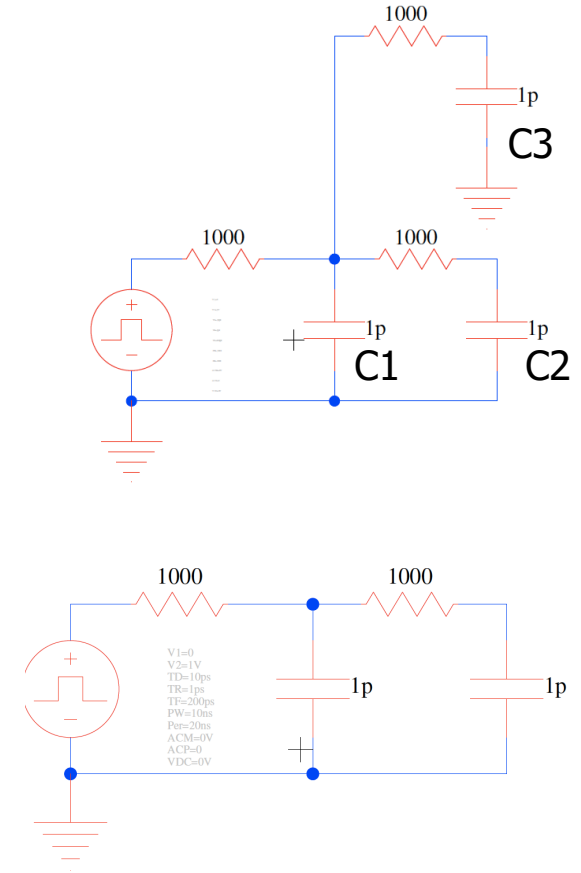
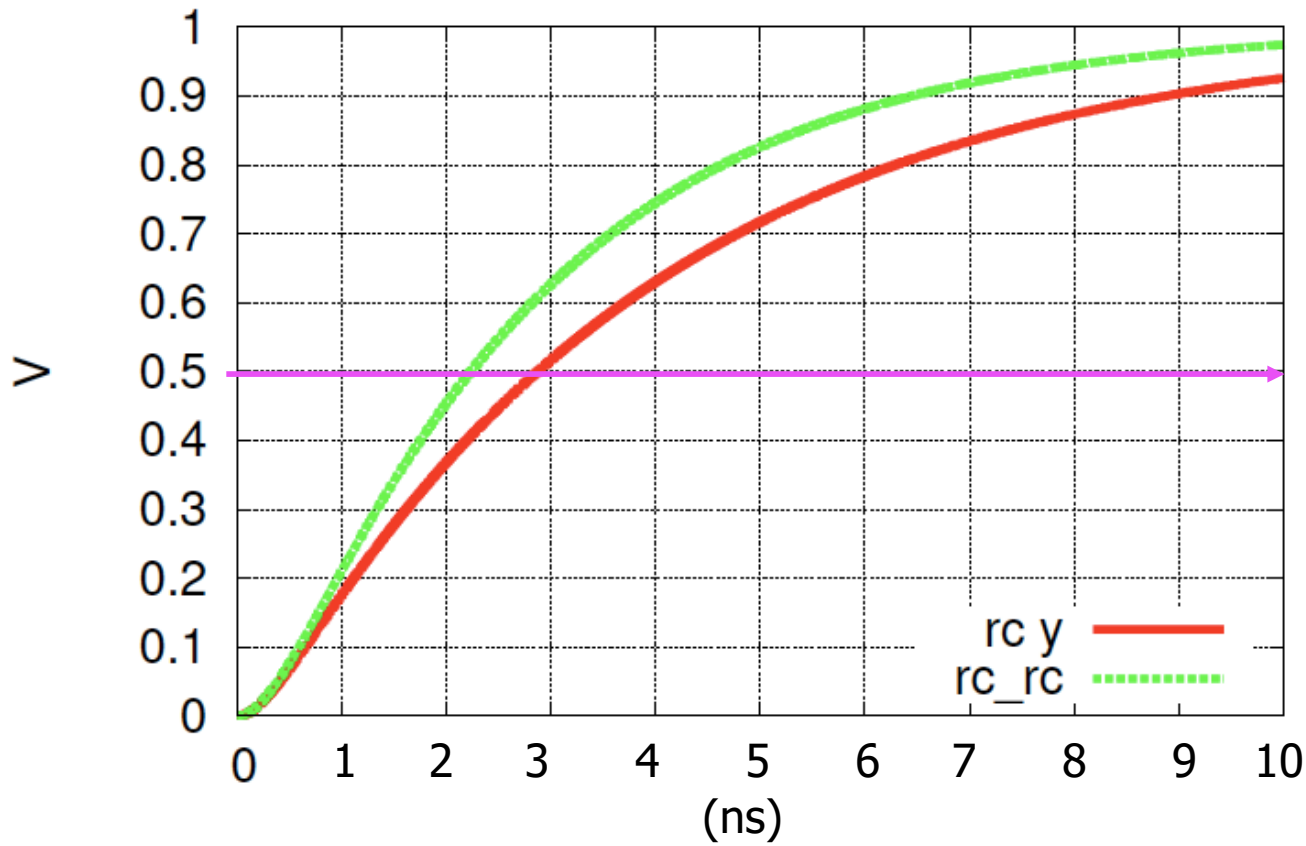
# Apply (preclass 1)

- What is Elmore delay?
  - $S \rightarrow P$



# SPICE Response

## Step Response

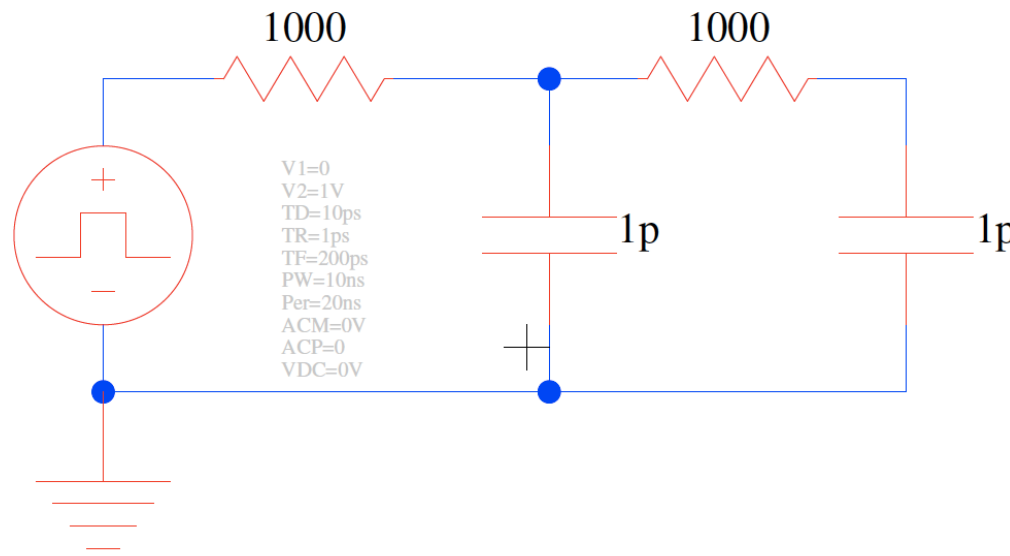




# Elmore Delay: Special Ladder Case

- For each resistor  $C_k$  in path
  - Compute  $R_{kk} =$  sum of all  $R$ s upstream of  $C_k$

$$\tau_{DN} = \sum_{k=1}^N C_k \sum_{j=1}^k R_j = \sum_{k=1}^N C_k R_{kk}$$

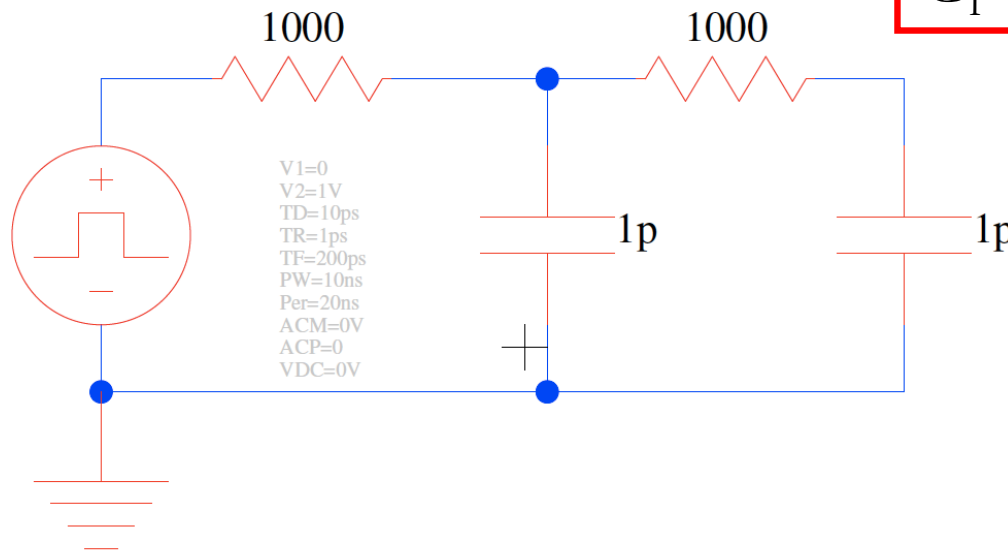


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$$C_1 * (R_1) + C_2 * (R_1 + R_2)$$

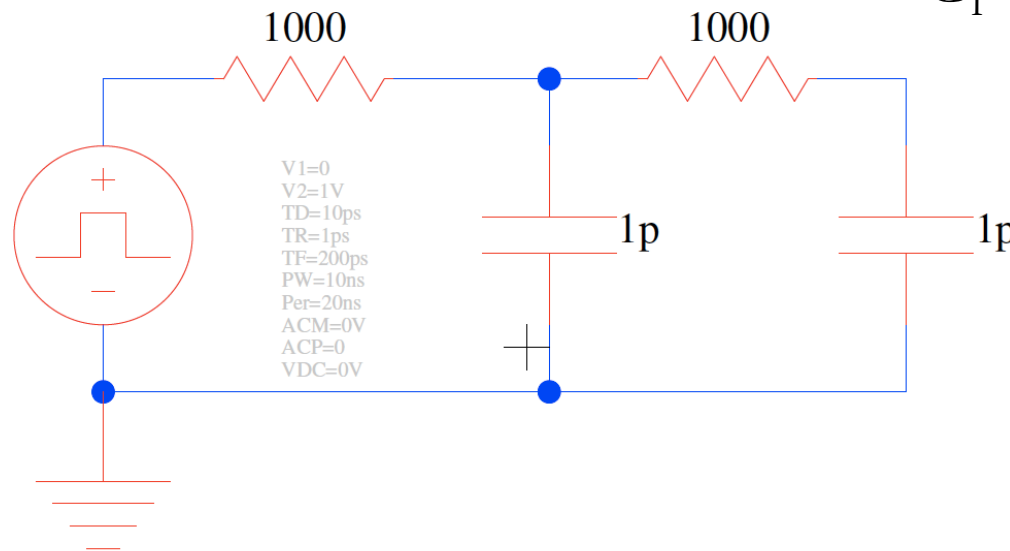


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$$C_1 * (R_1) + C_2 * (R_1 + R_2)$$



$$=3RC$$

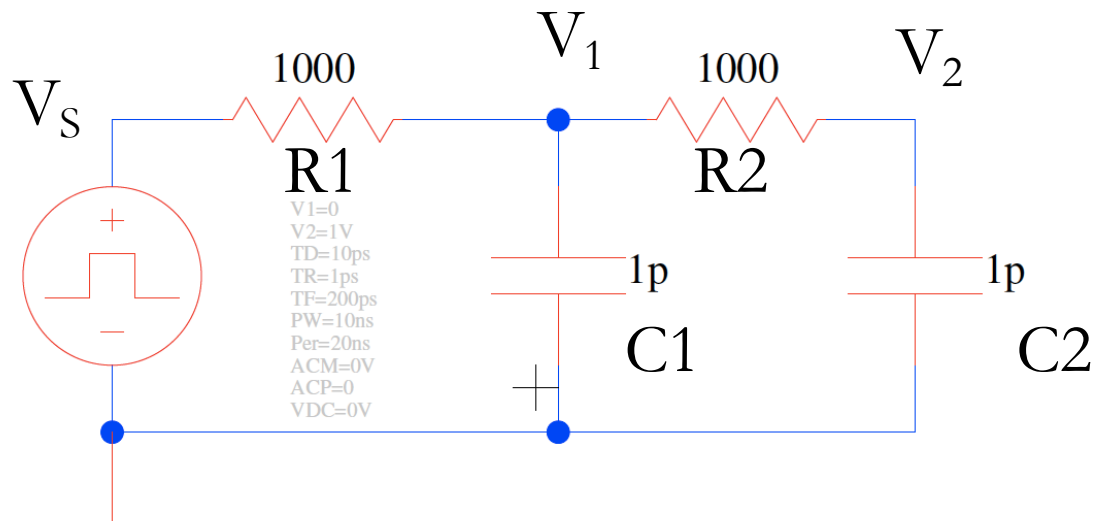
$$=3ns$$

# Compare KCL: Setup

## □ Equations from KCL?

$$\text{@}V_1: \frac{V_S - V_1}{R_1} = \frac{V_1 - V_2}{R_2} + C_1 \frac{dV_1}{dt}$$

$$\text{@}V_2: \frac{V_1 - V_2}{R_2} = C_2 \frac{dV_2}{dt}$$



# Compare KCL: Math

@ $V_1$ :

$$\frac{V_S - V_1}{R_1} = \frac{V_1 - V_2}{R_2} + C_1 \frac{dV_1}{dt}$$

$$\frac{V_S}{R_1} = \frac{V_1}{R_1} + \frac{V_1}{R_2} - \frac{V_2}{R_2} + C_1 \frac{dV_1}{dt}$$

$$V_S = V_1 \left( 1 + \frac{R_1}{R_2} \right) - \frac{R_1 V_2}{R_2} + R_1 C_1 \frac{dV_1}{dt}$$

@ $V_2$ :

$$\frac{V_1 - V_2}{R_2} = C_2 \frac{dV_2}{dt}$$

$$\frac{V_1}{R_2} = \frac{V_2}{R_2} + C_2 \frac{dV_2}{dt}$$

$$V_1 = V_2 + R_2 C_2 \frac{dV_2}{dt}$$

$$\frac{dV_1}{dt} = \frac{dV_2}{dt} + R_2 C_2 \frac{d^2 V_2}{dt^2}$$

# Compare KCL: Math

$$V_S = V_1 \left( 1 + \frac{R_1}{R_2} \right) - \frac{R_1}{R_2} V_2 + R_1 C_1 \frac{dV_1}{dt}$$

$$V_S = \left( V_2 + R_2 C_2 \frac{dV_2}{dt} \right) \left( 1 + \frac{R_1}{R_2} \right) - \frac{R_1}{R_2} V_2 + R_1 C_1 \left( \frac{dV_2}{dt} + R_2 C_2 \frac{d^2 V_2}{dt^2} \right)$$

$$V_S = V_2 + \left( R_2 C_2 \left( 1 + \frac{R_1}{R_2} \right) + R_1 C_1 \right) \frac{dV_2}{dt} + R_1 C_1 R_2 C_2 \frac{d^2 V_2}{dt^2}$$

$$V_S = V_2 + (R_2 C_2 + R_1 C_2 + R_1 C_1) \frac{dV_2}{dt} + R_1 C_1 R_2 C_2 \frac{d^2 V_2}{dt^2}$$



# Compare KCL: Math

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$$R_1 = R_2 = R$$

$$C_1 = C_2 = C$$

$$V_S = V_2 + (R_2 C_2 + R_1 C_2 + R_1 C_1) \frac{dV_2}{dt} + R_1 C_1 R_2 C_2 \frac{d^2 V_2}{dt^2}$$

$$V_S = V_2 + 3RC \frac{dV_2}{dt} + R^2 C^2 \frac{d^2 V_2}{dt^2}$$

# Compare KCL: Math

$$R_1 = R_2 = R$$

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$$V_S = V_2 + 3RC \frac{dV_2}{dt} + R^2 C^2 \frac{d^2 V_2}{dt^2}$$

$$V_2 = A(1 + e^{-\alpha t}) \rightarrow$$

$$V_S = A(1 + e^{-\alpha t}) - 3RC \cdot \alpha A e^{-\alpha t} + R^2 C^2 \cdot \alpha^2 A e^{-\alpha t}$$





# Compare KCL: Math

---

$$V_2 = A(1 + e^{-\alpha t}) \rightarrow$$

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$$t = \infty \rightarrow V_2 = V_S = A$$

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$$V_S = V_S(1 + e^{-\alpha t}) - 3RC \cdot \alpha V_S e^{-\alpha t} + R^2 C^2 \cdot \alpha^2 V_S e^{-\alpha t}$$

$$0 = e^{-\alpha t} - 3RC \cdot \alpha e^{-\alpha t} + R^2 C^2 \cdot \alpha^2 e^{-\alpha t}$$

$$0 = e^{-\alpha t} (1 - 3RC\alpha + R^2 C^2 \cdot \alpha^2)$$

$$0 = 1 - 3RC\alpha + R^2 C^2 \cdot \alpha^2$$

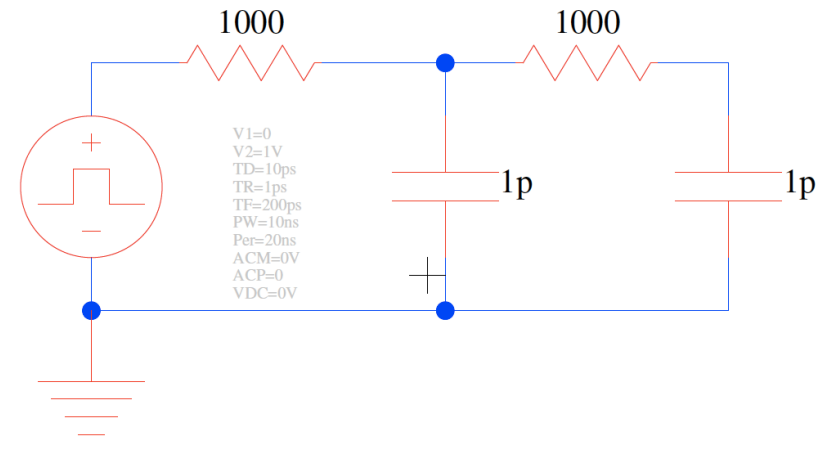
# Compare KCL: Math

$$V_2 = V_S(1 + e^{-\alpha t})$$

$$0 = 1 - 3RC\alpha + R^2C^2 \cdot \alpha^2$$

$$\alpha = \frac{3RC \pm \sqrt{9(RC)^2 - 4(RC)^2}}{2(RC)^2} = \frac{3RC \pm \sqrt{5}RC}{2(RC)^2} = \frac{3 \pm \sqrt{5}}{2RC}$$

$$\rightarrow \tau = \frac{2}{3 \pm \sqrt{5}} RC \approx 2.6RC$$



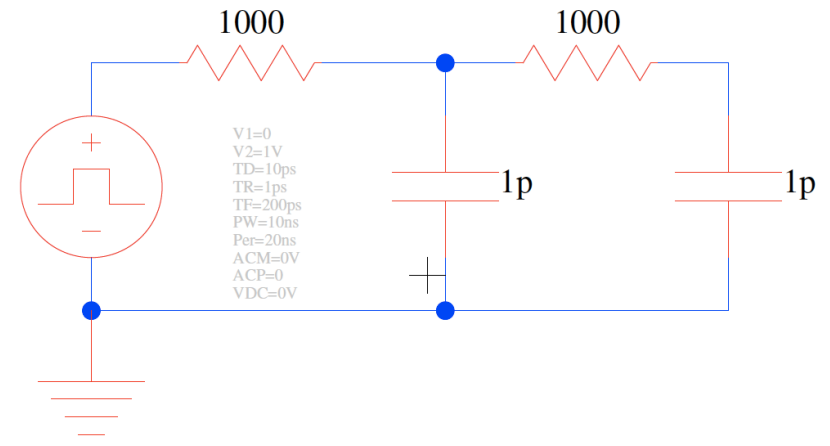
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$$\begin{aligned} &= 3RC \\ &= 3\text{ns} \end{aligned}$$

# Elmore Delay: Distributed RC network

- The delay from source to node  $i$ 
  - $N$  = number of nodes in circuit

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$$\tau_{Di} = \sum_{k=1}^N C_k R_{ik}$$

- Special ladder case

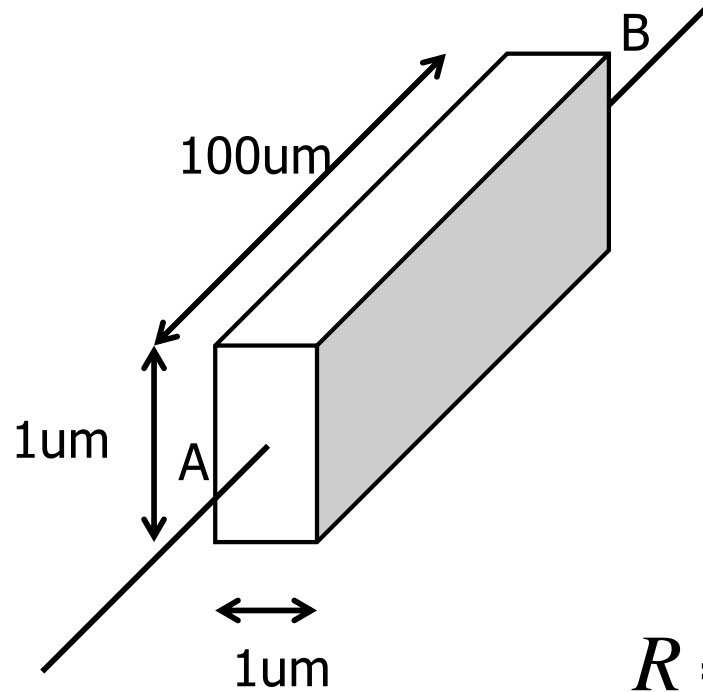
$$\tau_{DN} = \sum_{k=1}^N C_k \sum_{j=1}^k R_j = \sum_{k=1}^N C_k R_{kk}$$

# Wire Delay

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# Wire Resistance

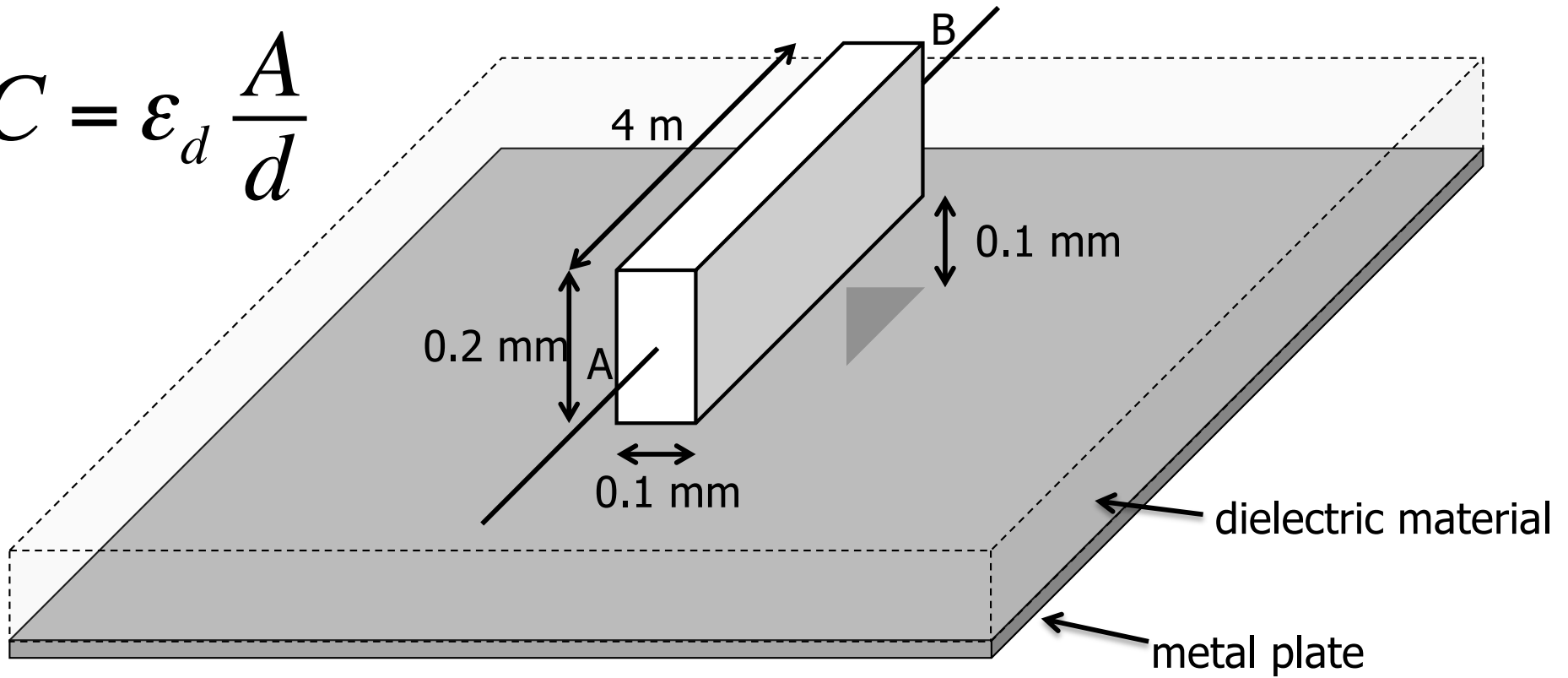


$$R = \frac{\rho L}{A}$$

$$R = \frac{10^{-7} \Omega \cdot m \cdot 100 \mu m}{1 \mu m \cdot 1 \mu m} = 10 \Omega$$

# Wire Capacitance

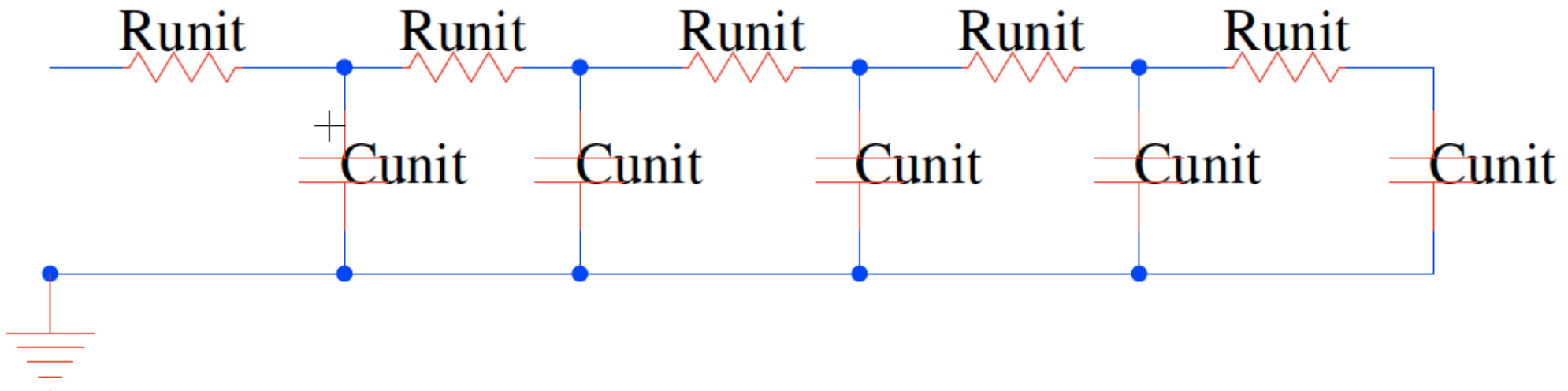
$$C = \epsilon_d \frac{A}{d}$$





# Wire as Distributed RC Ladder

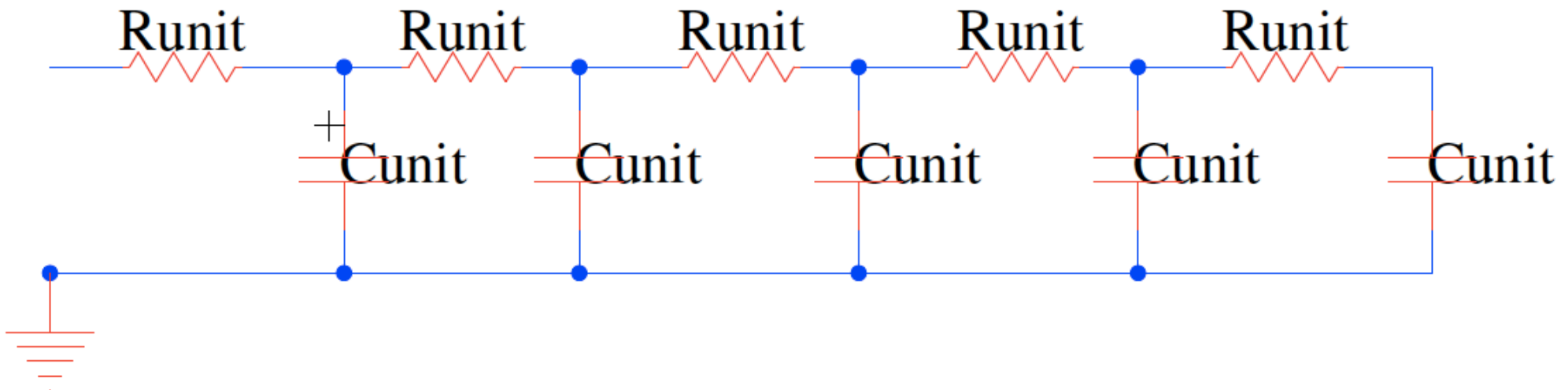
- Measure wire length in units
  - Say  $\lambda$
  - Each  $\lambda$  unit has  $C_{\text{unit}}$ ,  $R_{\text{unit}}$ 
    - Unit capacitance and resistance of wire of length  $\lambda$





# Wire Delay

- Delay of Wire  $N$  units long:

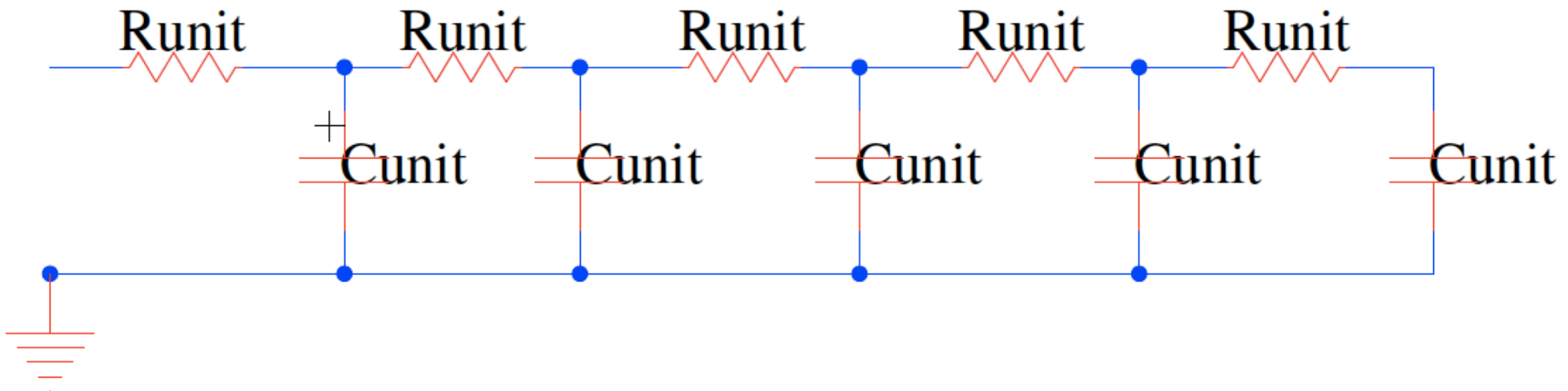




# Wire Delay

□ Delay of Wire N units long:

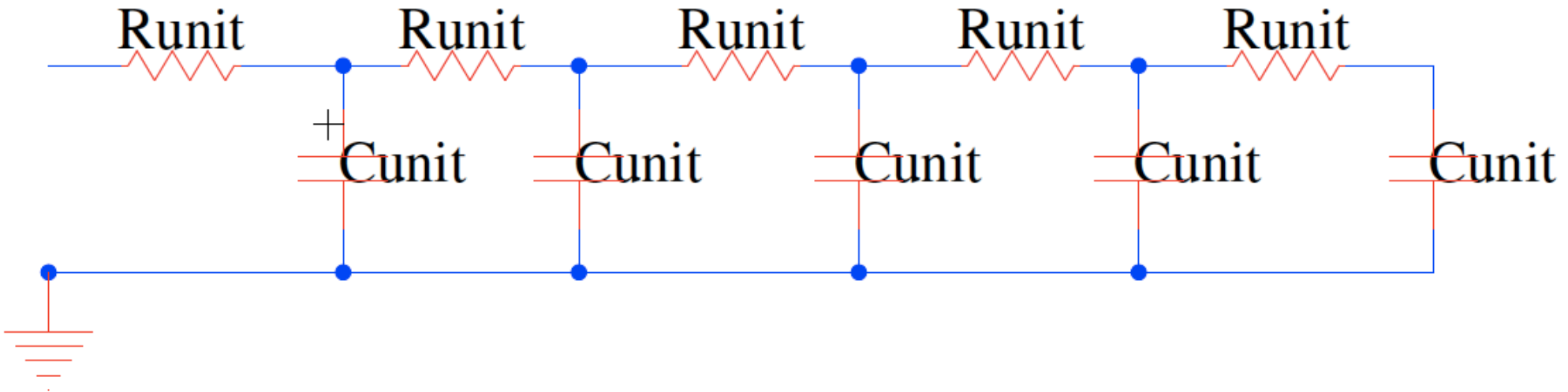
$$R_{\text{unit}}C_{\text{unit}}$$



# Wire Delay

□ Delay of Wire N units long:

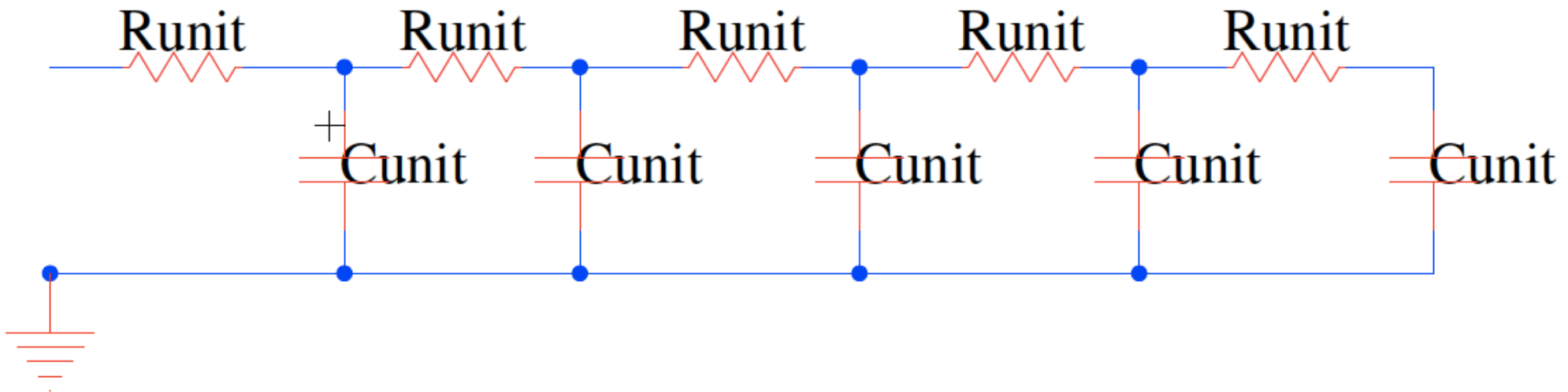
$$R_{\text{unit}}C_{\text{unit}} + 2R_{\text{unit}}C_{\text{unit}}$$



# Wire Delay

□ Delay of Wire N units long:

$$\begin{aligned} & R_{\text{unit}}C_{\text{unit}} \\ & + 2R_{\text{unit}}C_{\text{unit}} \\ & + 3R_{\text{unit}}*C_{\text{unit}} + \dots + NR_{\text{unit}}*C_{\text{unit}} \\ & = (R_{\text{unit}}*C_{\text{unit}})*(1 + 2 + 3 + \dots(N-1) + N) \end{aligned}$$





# Sum of integers (preclass 2)

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- What's the sum of the integer 1 to N?

$$\sum_{k=0}^N k =$$



# Sum of integers

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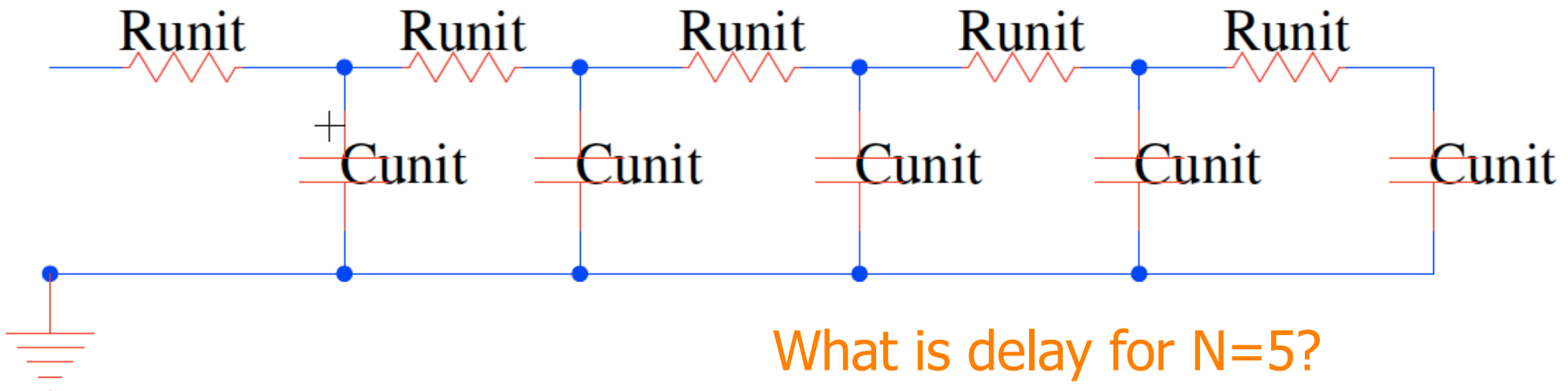
- What's the sum of the integer 1 to N?

$$\sum_{k=0}^N k = \frac{N(N+1)}{2} \approx \frac{N^2}{2}$$

# Wire Delay (preclass 3)

□ Delay of Wire N units long:

$$\begin{aligned} & R_{\text{unit}} C_{\text{unit}} \\ & + 2R_{\text{unit}} C_{\text{unit}} \\ & + 3R_{\text{unit}} * C_{\text{unit}} + \dots + NR_{\text{unit}} * C_{\text{unit}} \\ & = (R_{\text{unit}} * C_{\text{unit}}) * (1 + 2 + 3 + \dots (N-1) + N) \\ & \sim R_{\text{unit}} C_{\text{unit}} * N^2 / 2 \end{aligned}$$



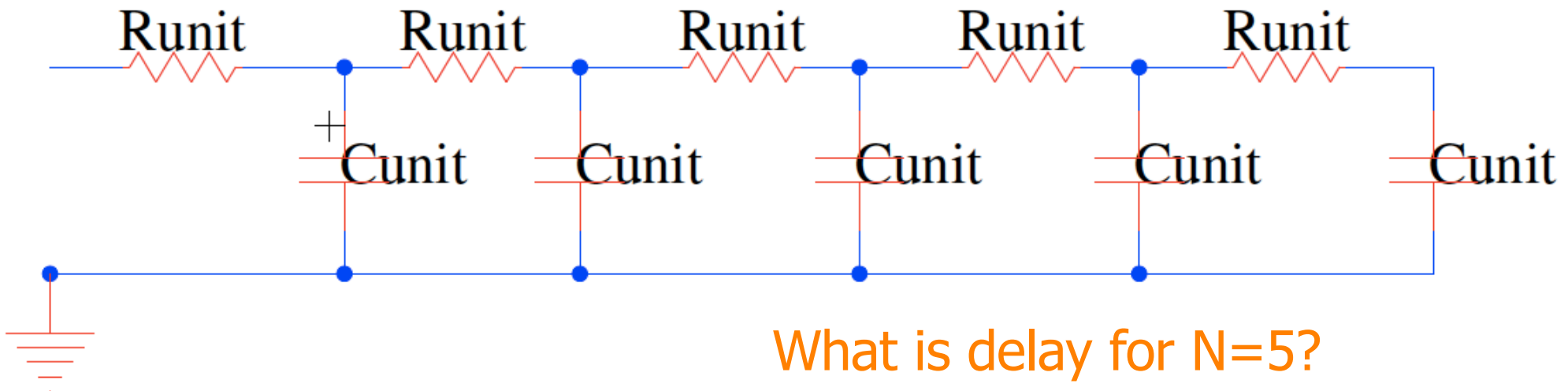


# Lumped RC Wire? (preclass 4)

- What would the delay be if we treated the wire as lumped R and C?

$$R_{\text{wire}} = N \times R_{\text{unit}}$$

$$C_{\text{wire}} = N \times C_{\text{unit}}$$



What is delay for  $N=5$ ?



# Wire Delay

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- ❑  $R_{\text{wire}} = N * R_{\text{unit}}$
- ❑  $C_{\text{wire}} = N * C_{\text{unit}}$
- ❑ Lumped RC wire delay =  $R_{\text{unit}} * C_{\text{unit}} * N^2$
- ❑ Distributed RC Wire delay =  $R_{\text{unit}} * C_{\text{unit}} * N^2 / 2$
  
- ❑ Distributed has half the delay of lumped RC product
- ❑ Delay is quadratic in length of wire in both cases

# Apply to Gates

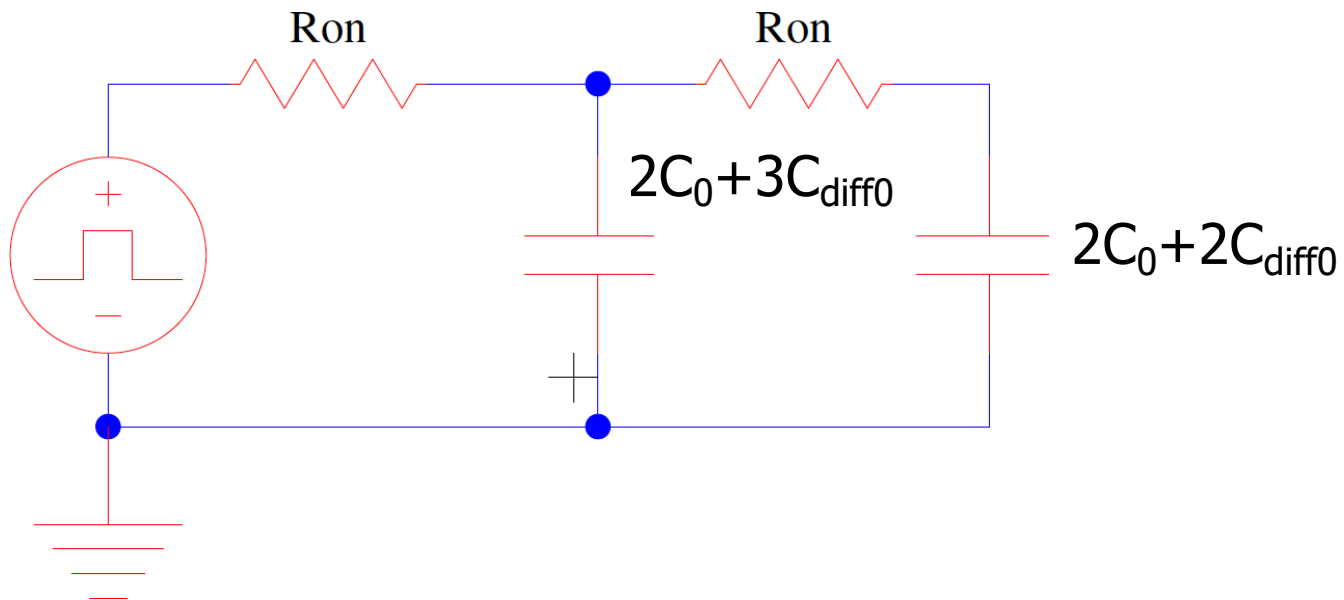
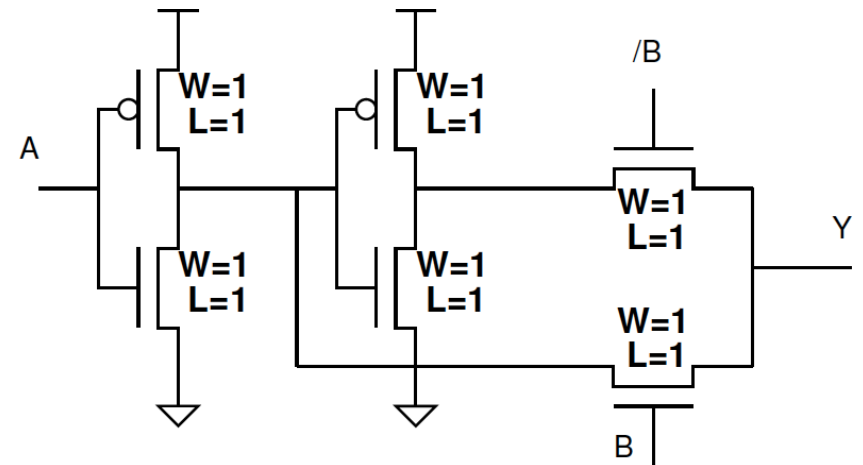
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Pass Transistor and CMOS



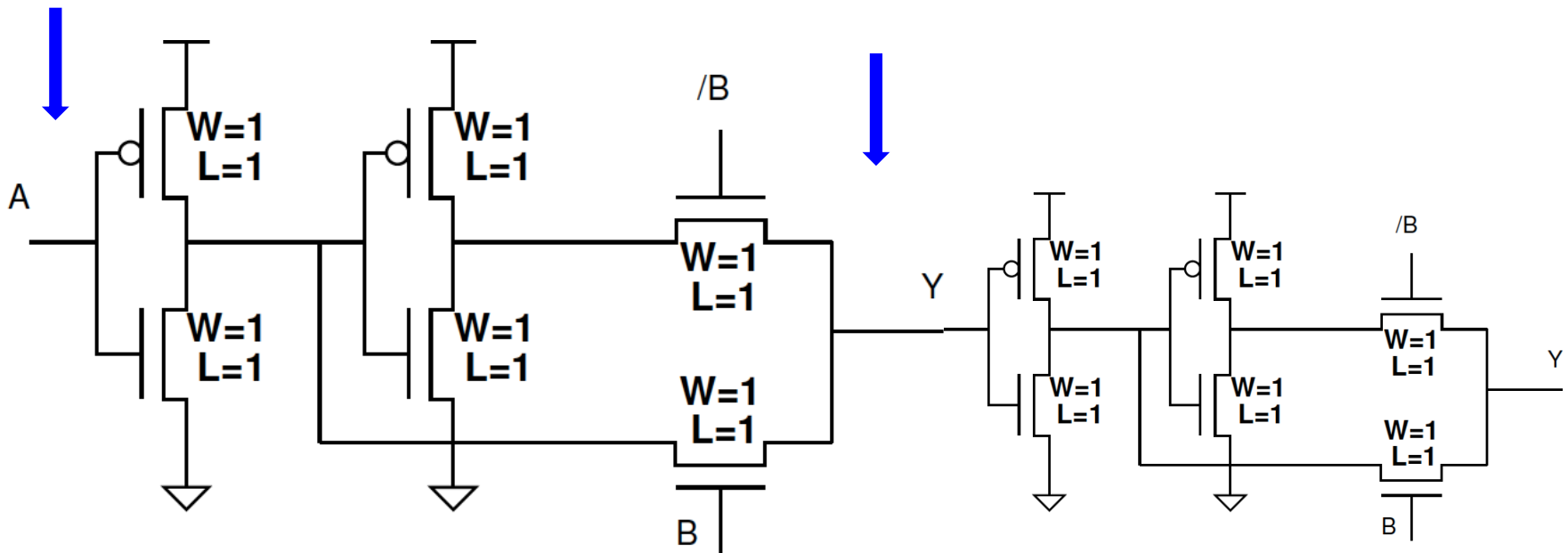
# Pass Transistor XOR

□ Delay when  $A=B=1$



# Pass Transistor XOR (preclass 5)

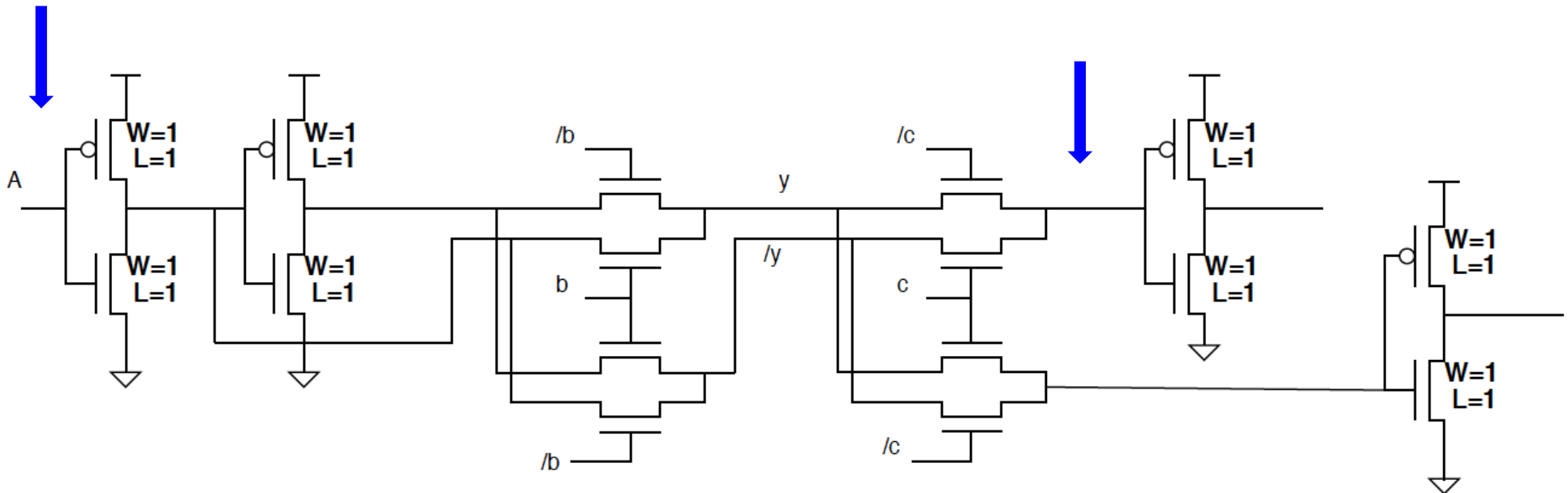
- Delay when  $A=1, B=0$ ?
  - Start with equivalent RC circuit



# Unbuffered (preclass 6)

□ Circuit → Delay?

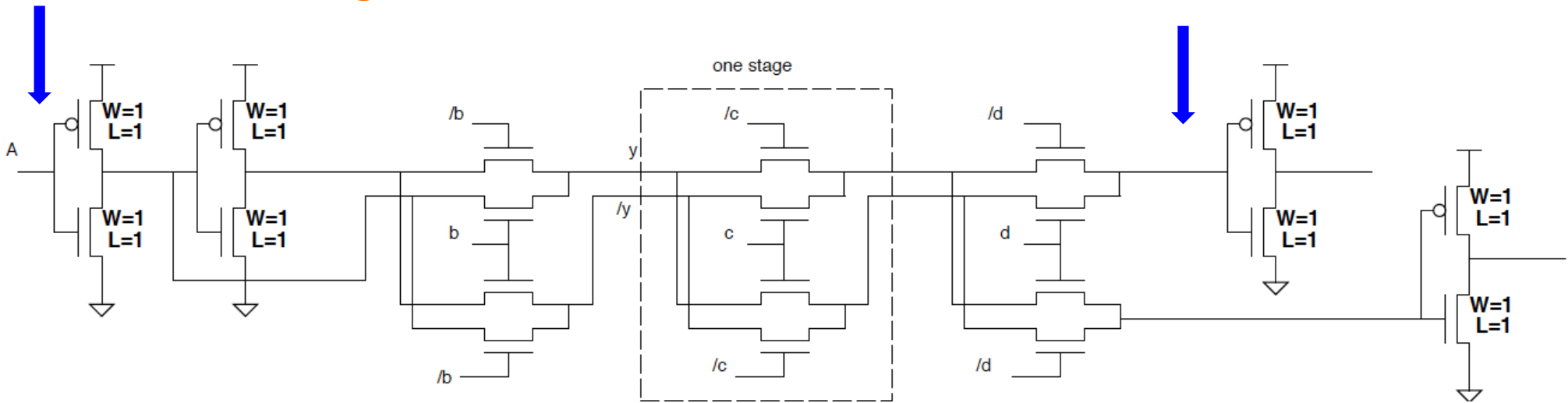
■ 2 stages



# Unbuffered (preclass 7)

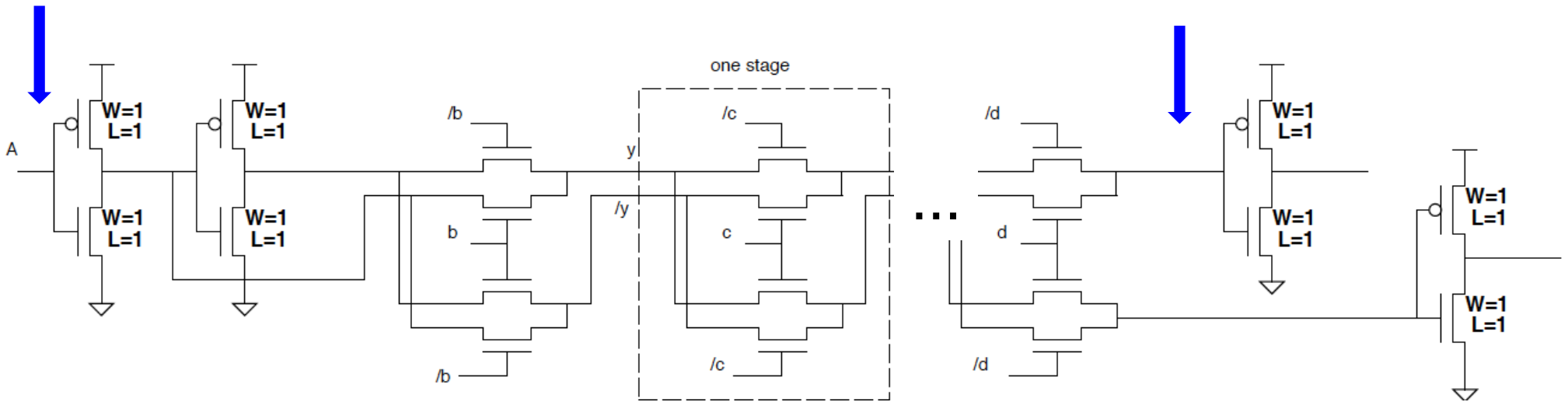
□ Circuit → Delay?

■ 3 stages



# Unbuffered (preclass 8)

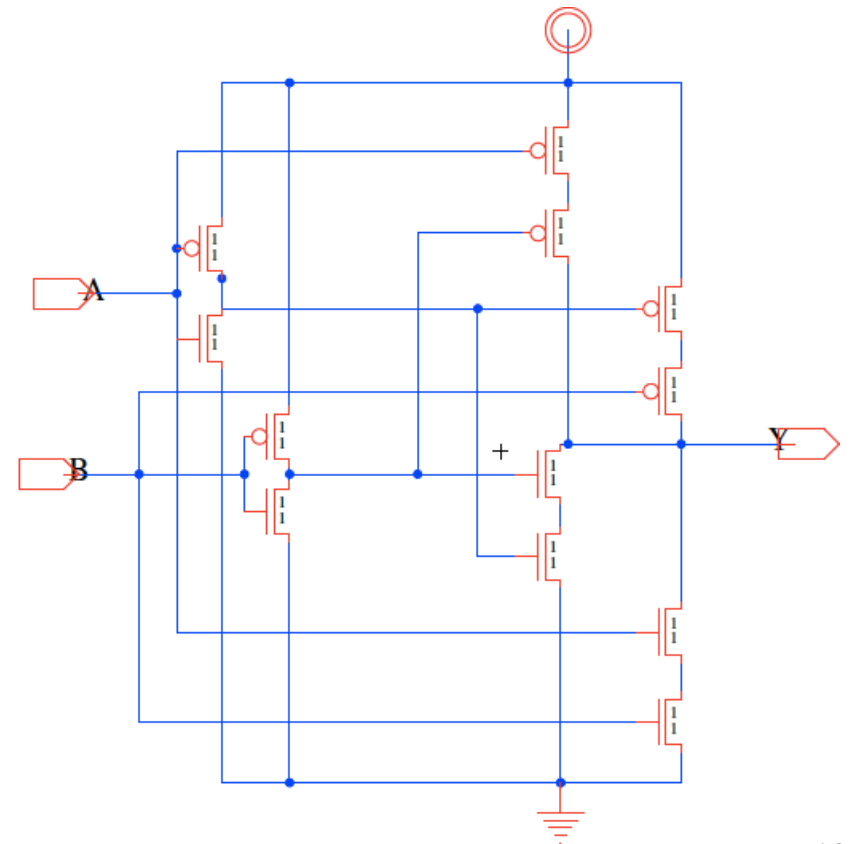
□ Delay as a function of number of stages,  $k$ ?



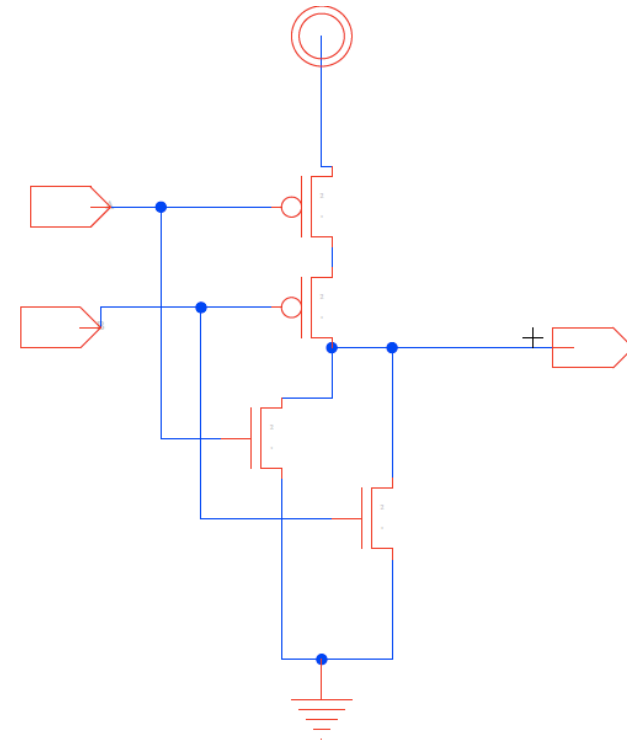
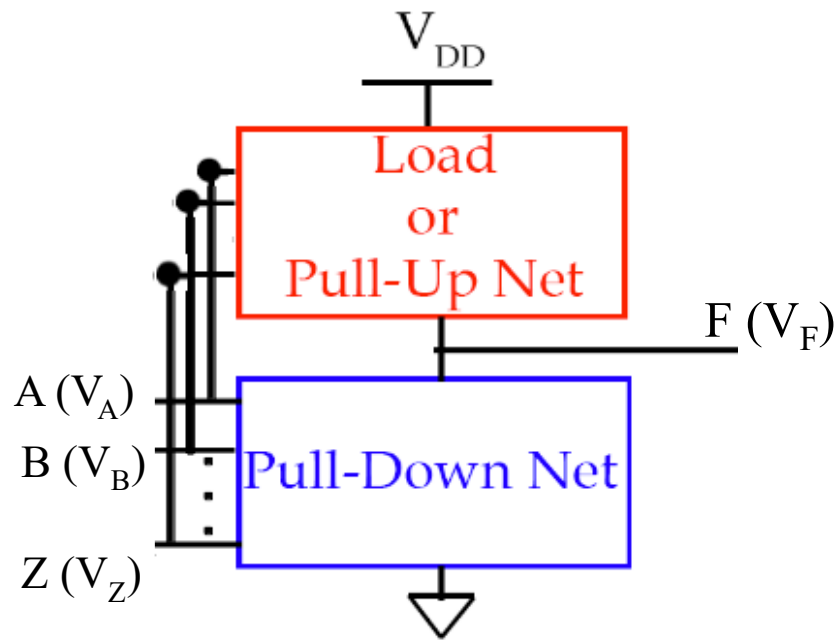


# CMOS XOR (preclass 9)

- Delay with  $C_{diff} > 0$ ?



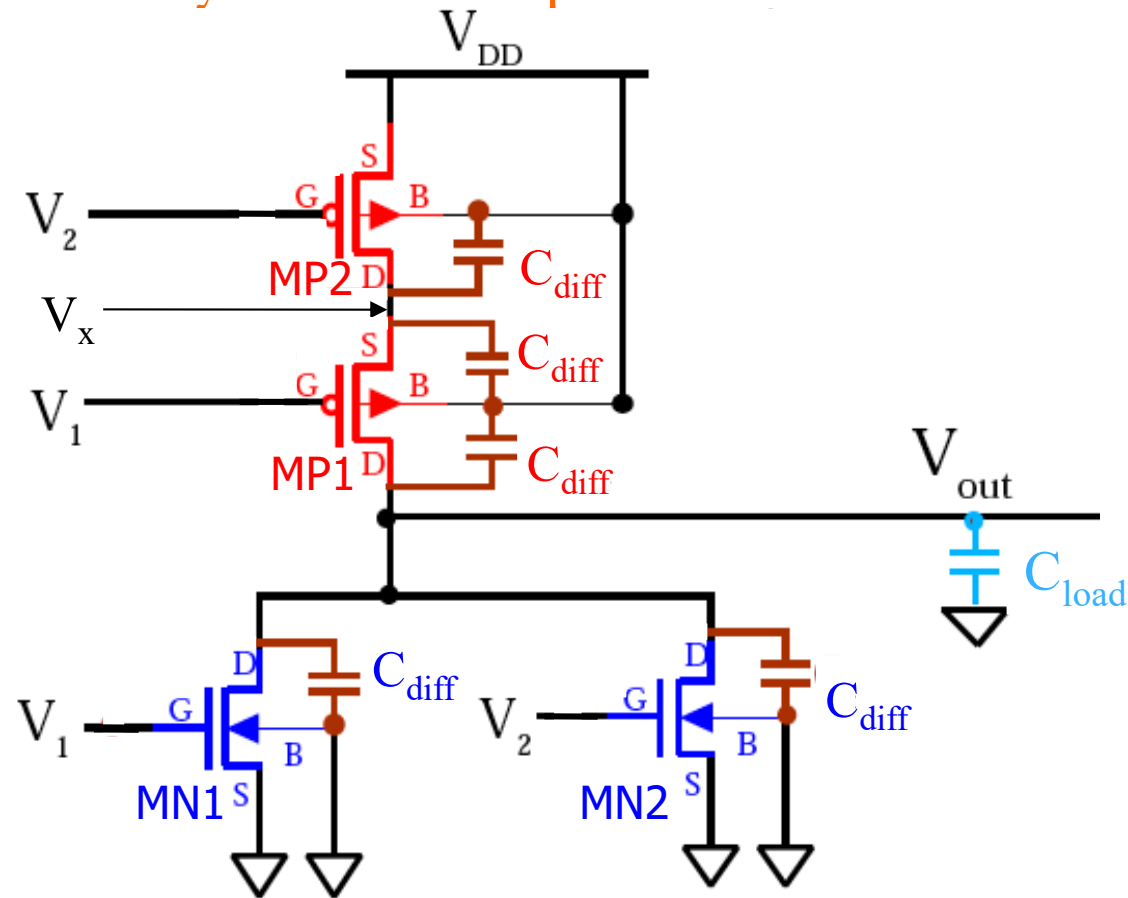
# Review: Two-Input NOR Gate (NOR2)



- ❑ Worst case delay of NOR2?
  - Minimum size, Loaded with itself

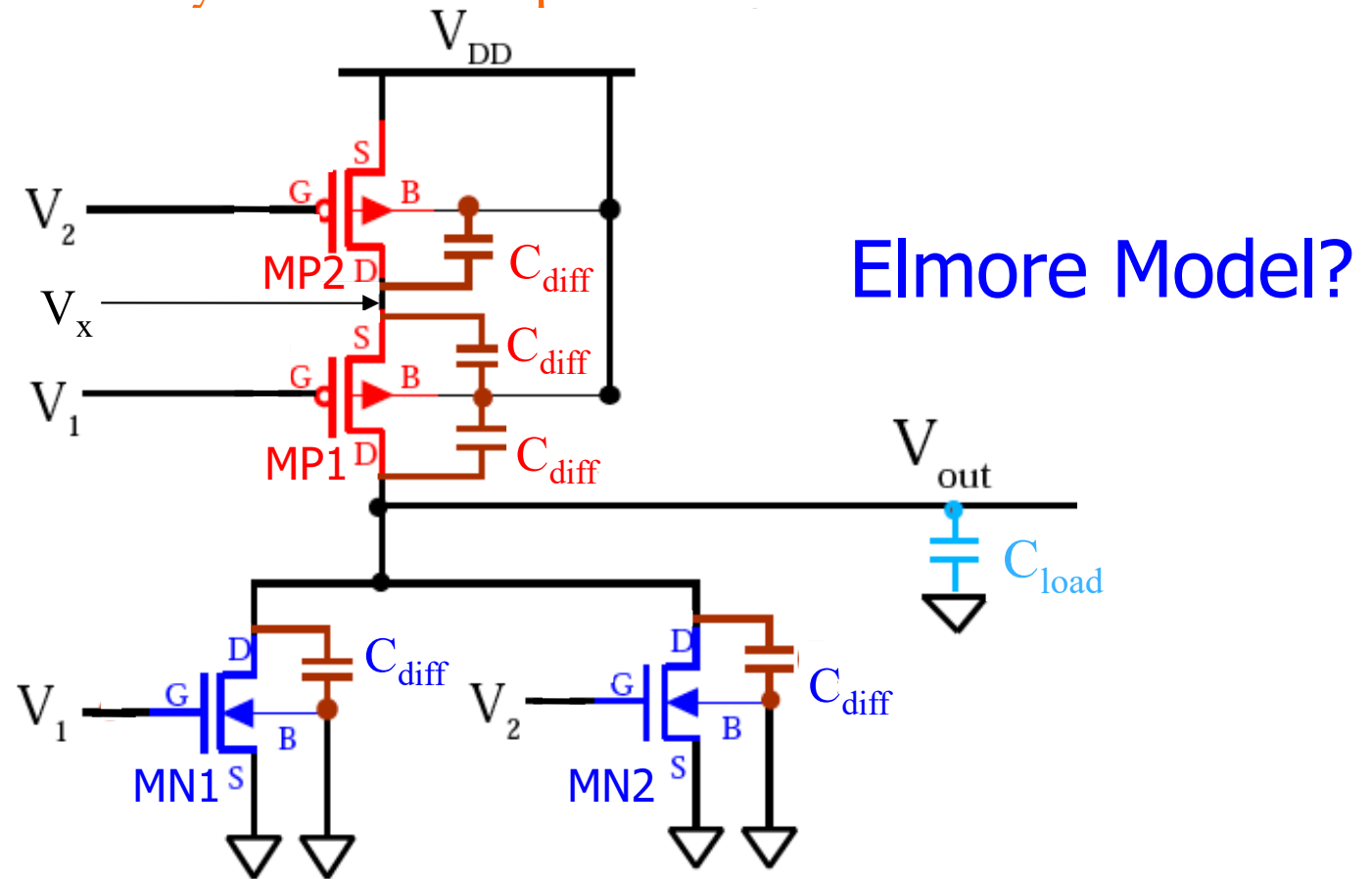
# NOR2 Delay (preclass 10)

- Worst case delay for Pull-up?



# NOR2 Delay

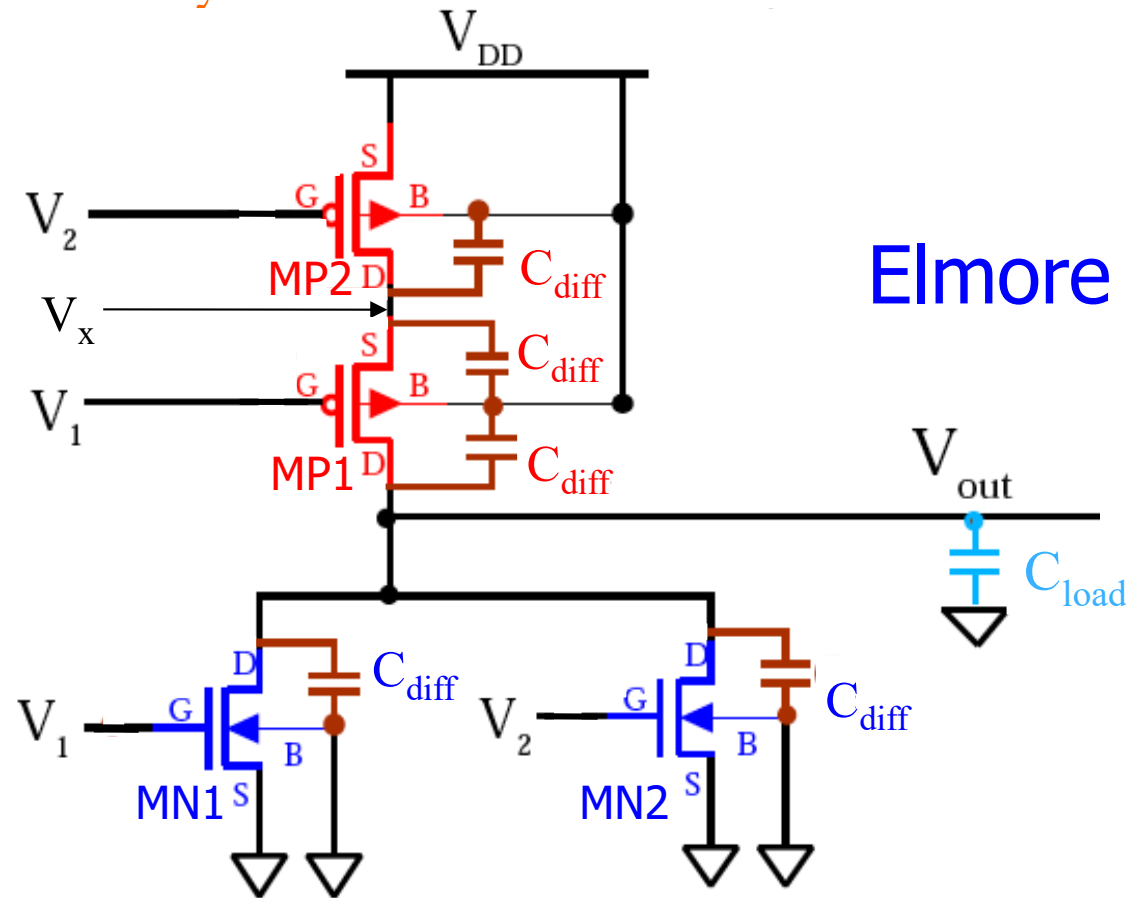
- Worst case delay for Pull-up?



Worst Case for Pull-up  $\rightarrow V_1 = 0, V_2 = V_{DD} \rightarrow 0$  @ $t=0$  &  $V_x \approx V_{out} = 0 \rightarrow V_{DD}$

# NOR2 Delay

□ Worst case delay?

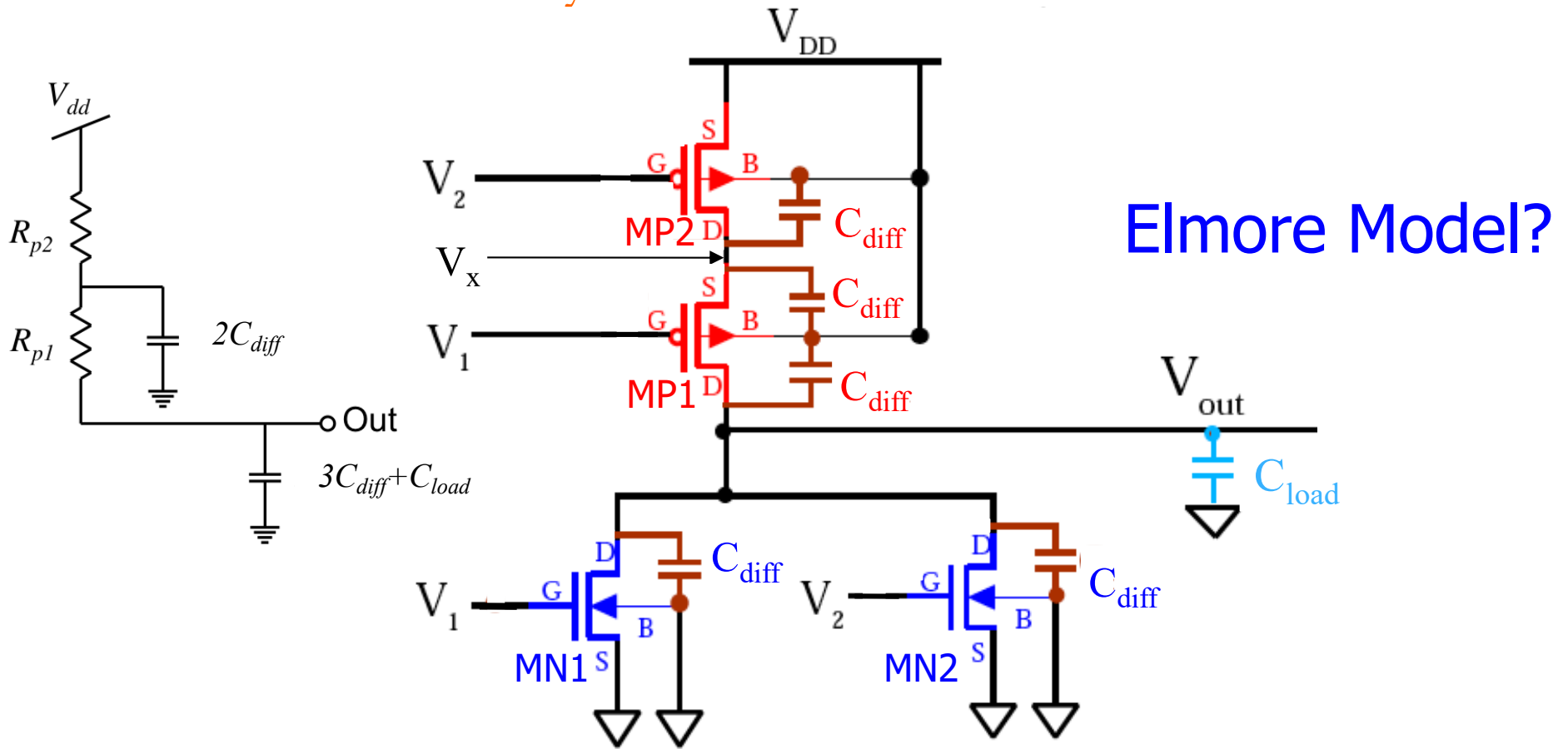


Elmore Model?

Worst Case for Pull-up  $\rightarrow V_1 = 0, V_2 = V_{DD} \rightarrow 0$  @  $t=0$  &  $V_x \approx V_{out} = 0 \rightarrow V_{DD}$

# NOR2 Delay

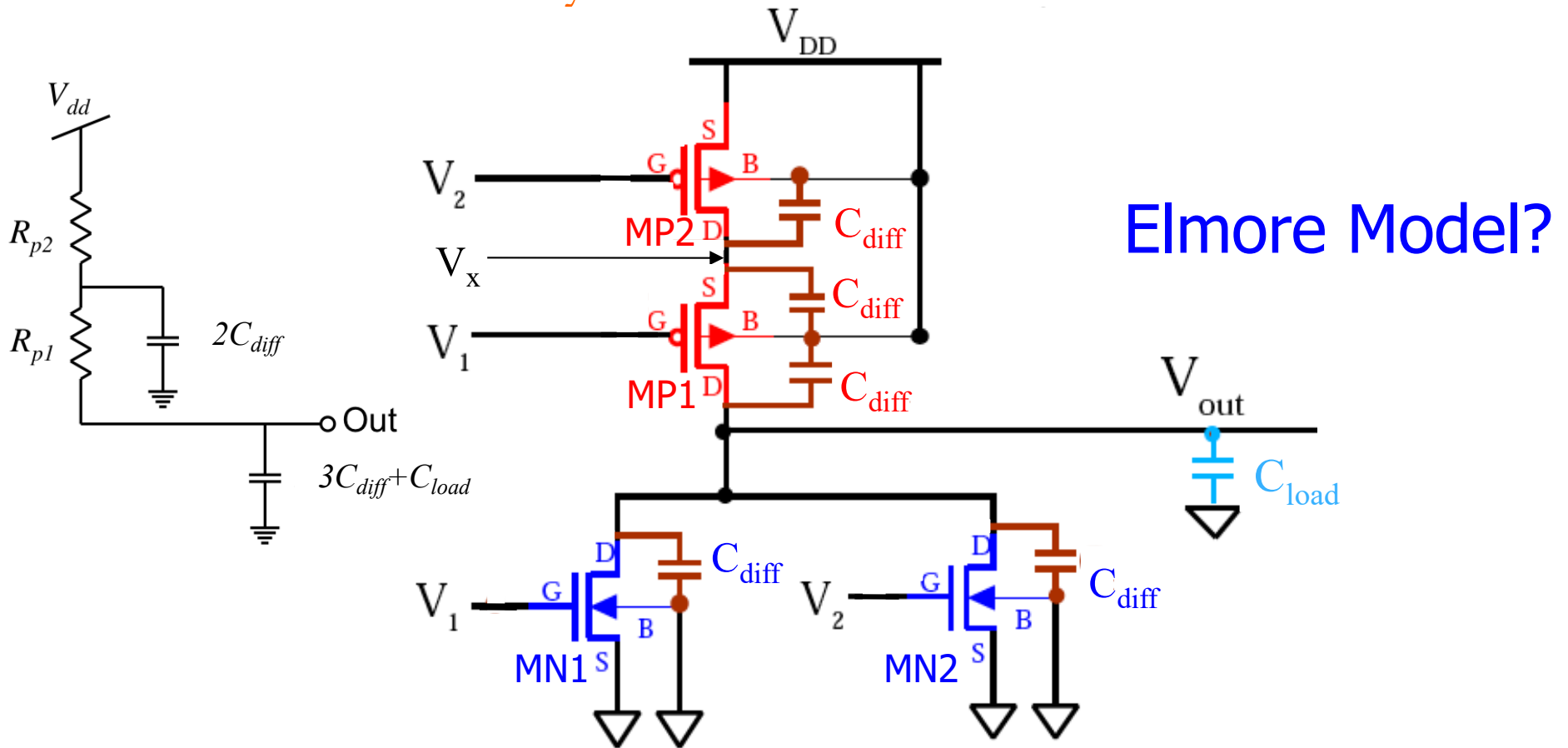
□ Worst case delay?



Worst Case for Pull-up  $\rightarrow V_1 = 0, V_2 = V_{DD} \rightarrow 0$  @  $t=0$  &  $V_x \approx V_{out} = 0 \rightarrow V_{DD}$

# NOR2 Delay

□ Worst case delay?

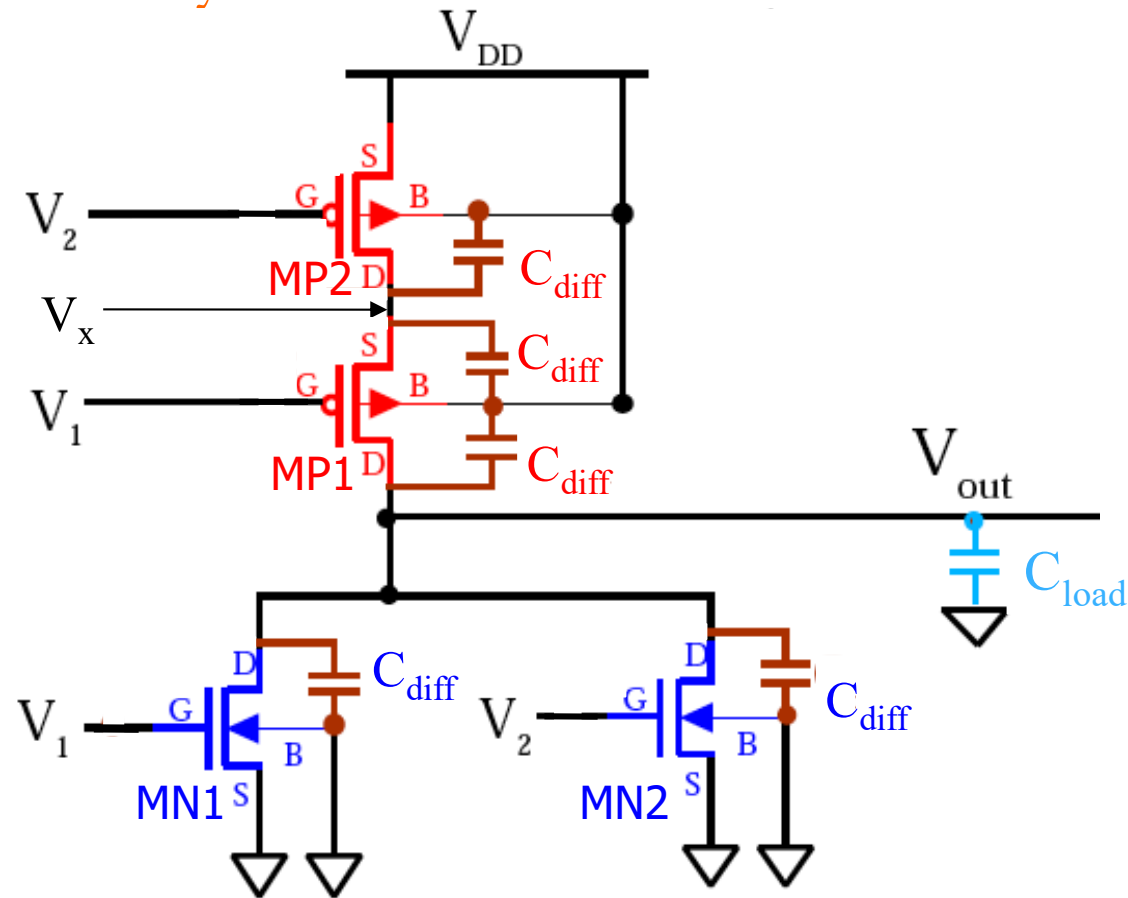


Worst Case for Pull-up  $\rightarrow V_1 = 0, V_2 = V_{DD} \rightarrow 0 @t=0$  &  $V_x \approx V_{out} = 0 \rightarrow V_{DD}$

$$\text{delay} = (2C_{diff})(R_{p2}) + (3C_{diff} + C_{load})(R_{p1} + R_{p2}) = (8\gamma + 4)\tau$$

# NOR2 Delay

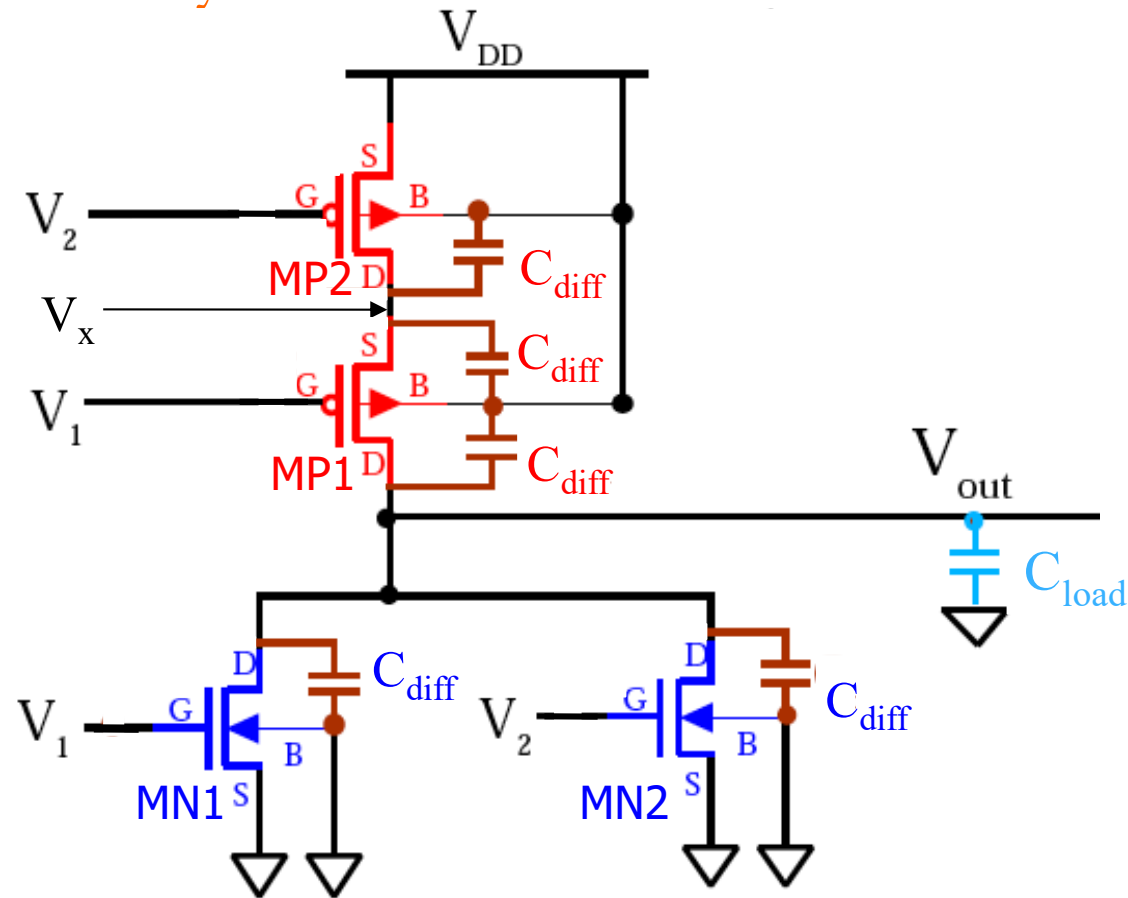
□ Worst case delay Pull-down?





# NOR2 Delay

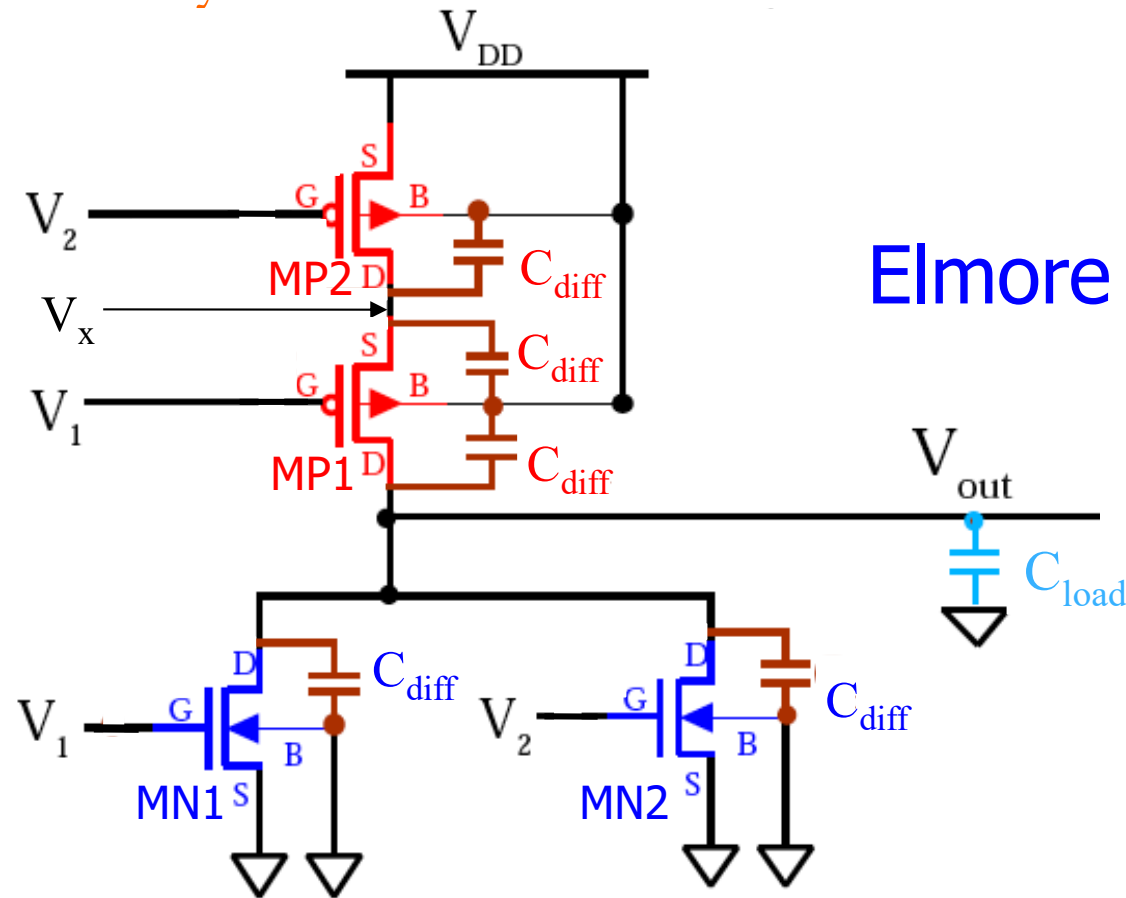
- Worst case delay Pull-down?



Worst case for Pull-down  $\rightarrow V_1 = 0, V_2 = 0 \rightarrow V_{DD} @ t=0$  &  $V_x \approx V_{out} = V_{DD} \rightarrow 0$

# NOR2 Delay

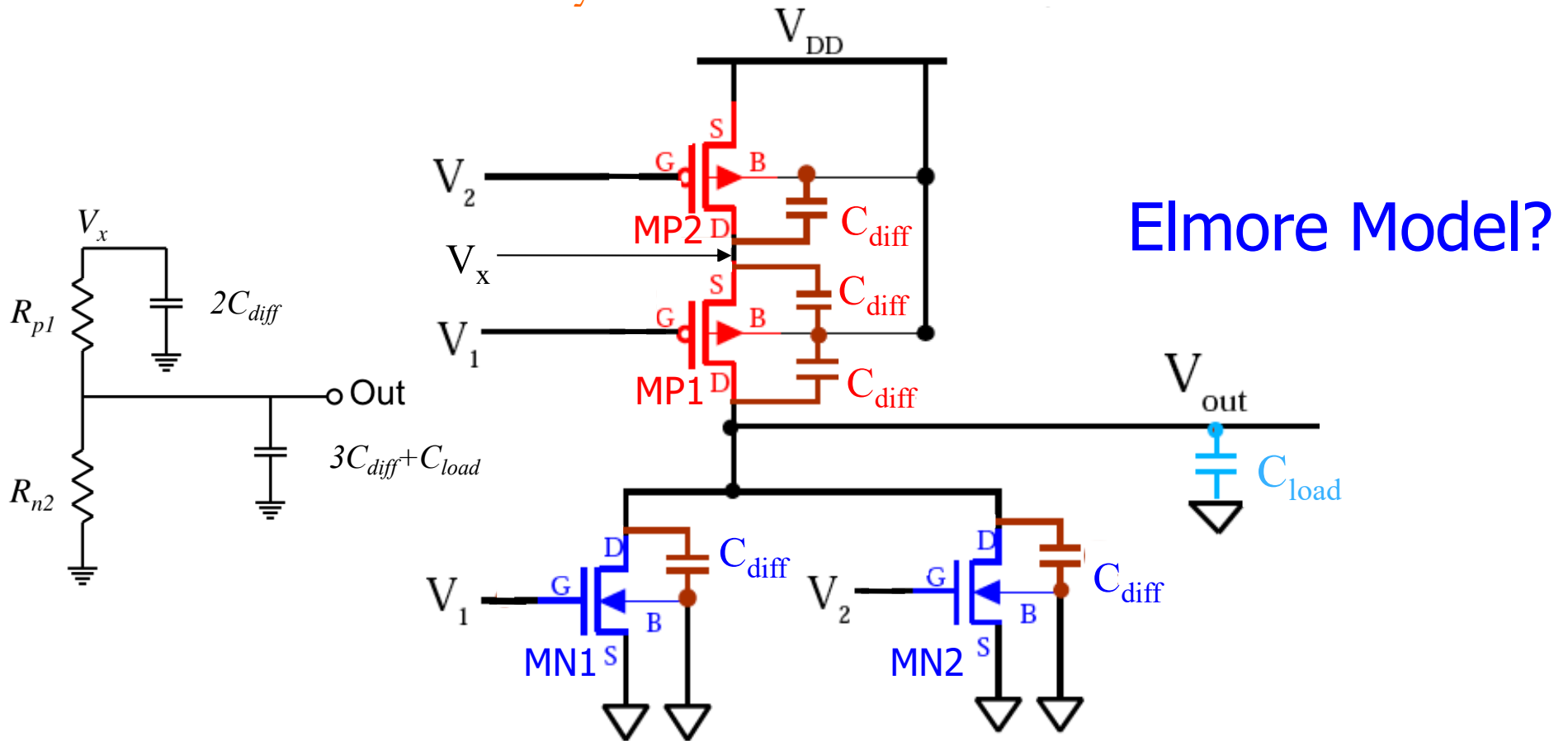
- Worst case delay Pull-down?



Worst case for Pull-down  $\rightarrow V_1 = 0, V_2 = 0 \rightarrow V_{DD} @ t=0$  &  $V_x \approx V_{out} = V_{DD} \rightarrow 0$

# NOR2 Delay

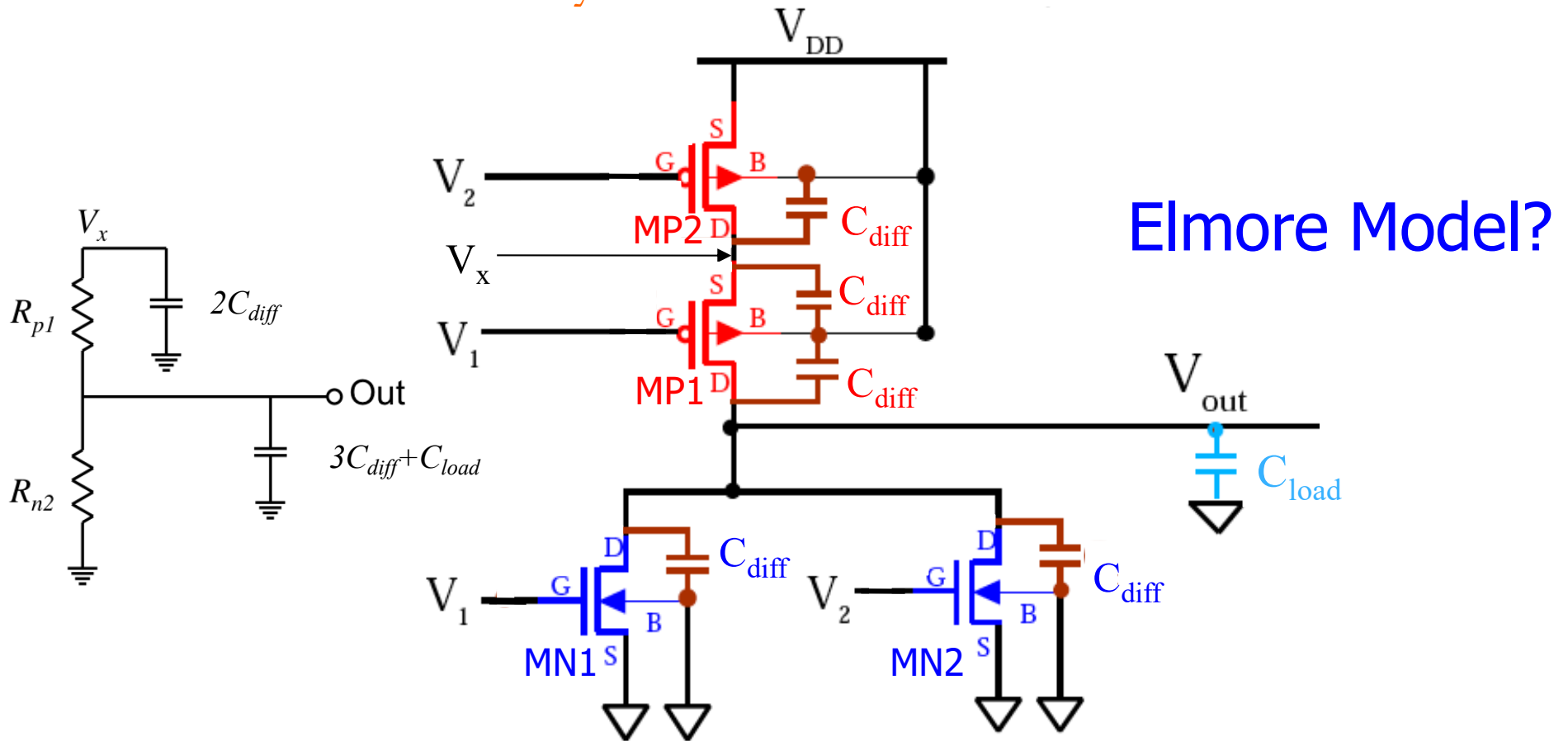
Worst case delay Pull-down?



Worst case for Pull-down  $\rightarrow V_1 = 0, V_2 = 0 \rightarrow V_{DD} @ t=0$  &  $V_x \approx V_{out} = V_{DD} \rightarrow 0$

# NOR2 Delay

Worst case delay Pull-down?

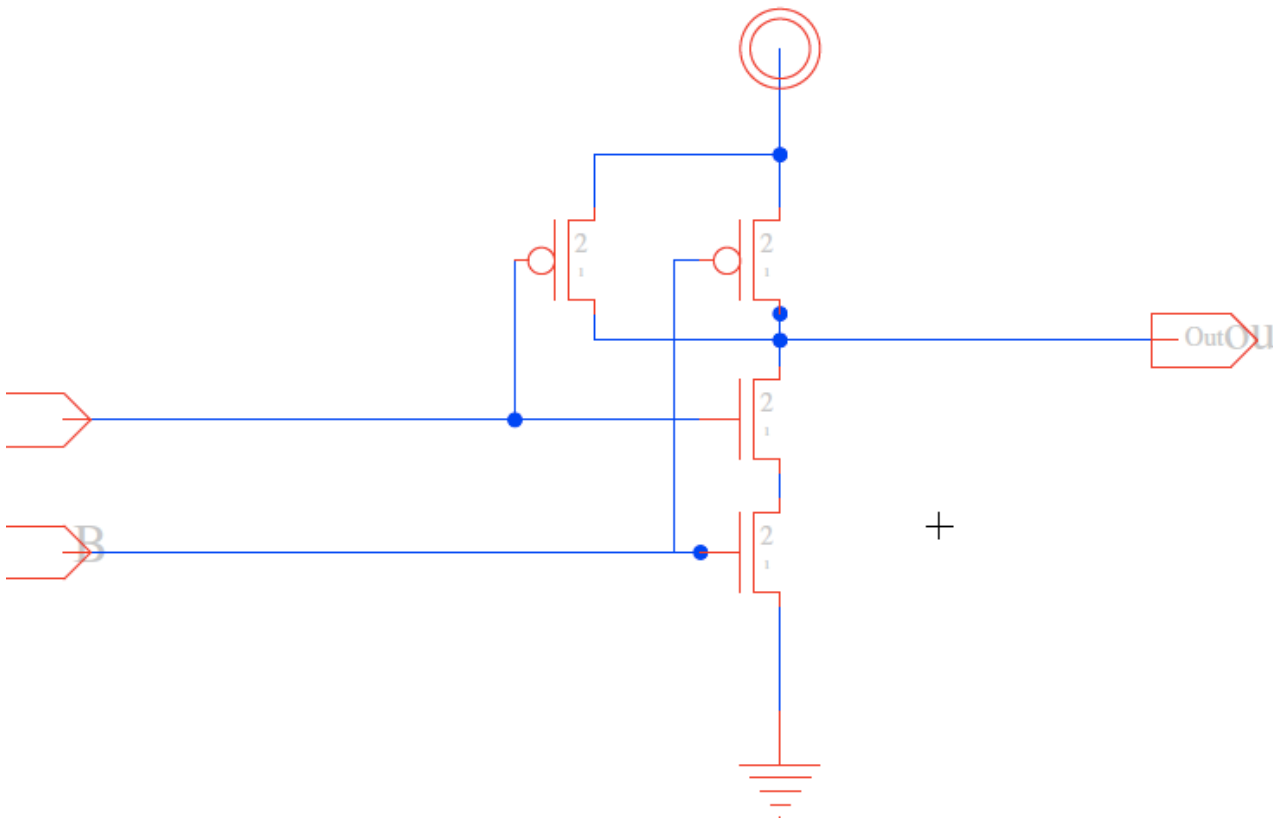


Worst case for Pull-down  $\rightarrow V_1 = 0, V_2 = 0 \rightarrow V_{DD} @ t=0$  &  $V_x \approx V_{out} = V_{DD} \rightarrow 0$

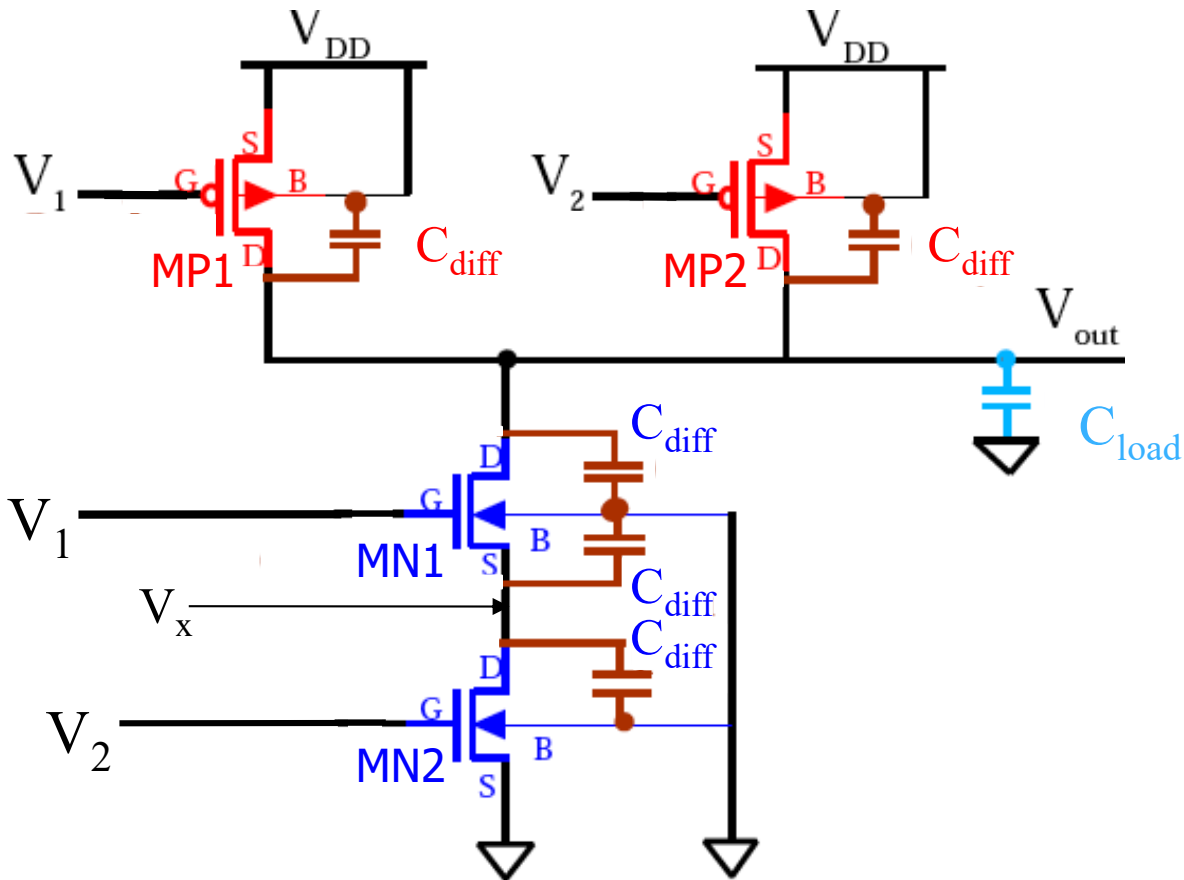
$$\text{delay} = (2C_{diff})(R_{p1} + R_{n2}) + (3C_{diff} + C_{load})(R_{n2}) = (7\gamma + 2)\tau$$



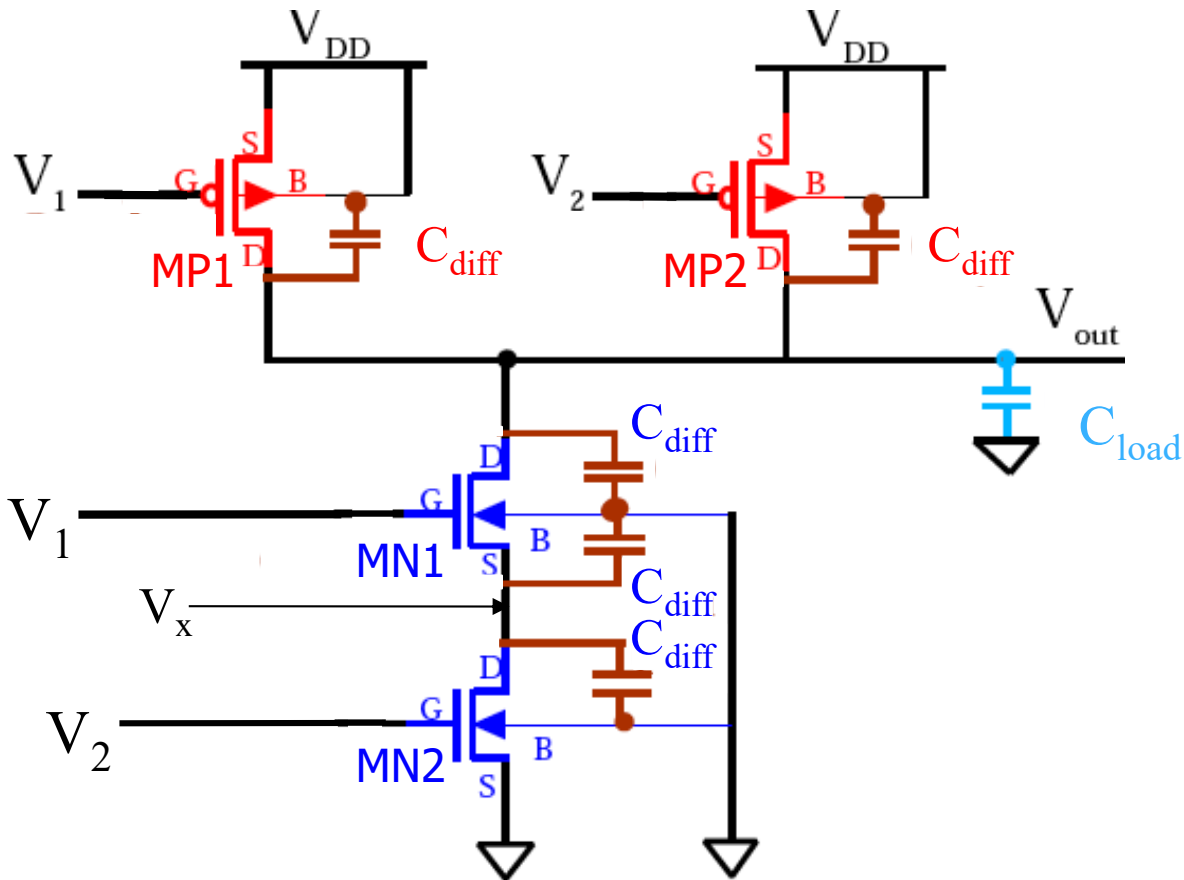
# NAND2 Delay (preclass 11)



# Parasitic Caps for NAND2 (worst case)

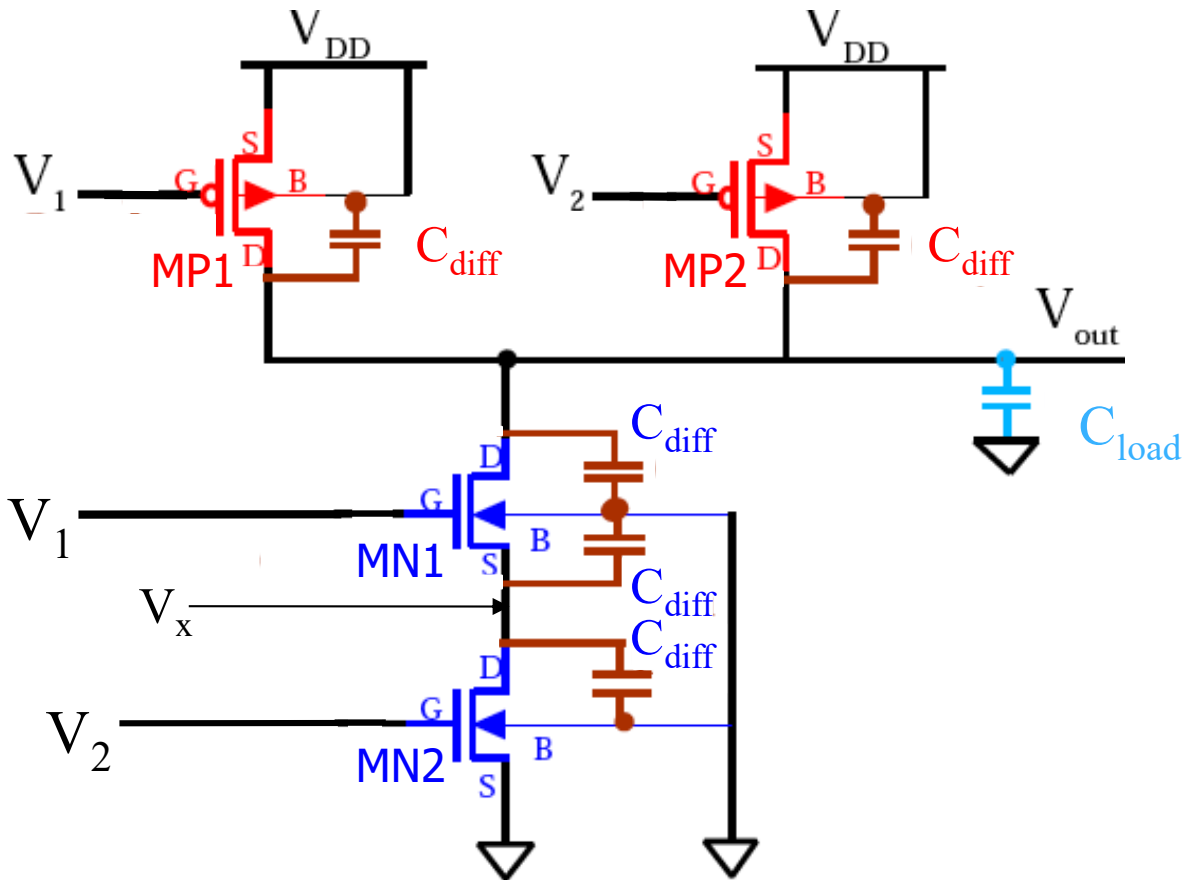


# Parasitic Caps for NAND2 (worst case)



Worst case for Pull-up →

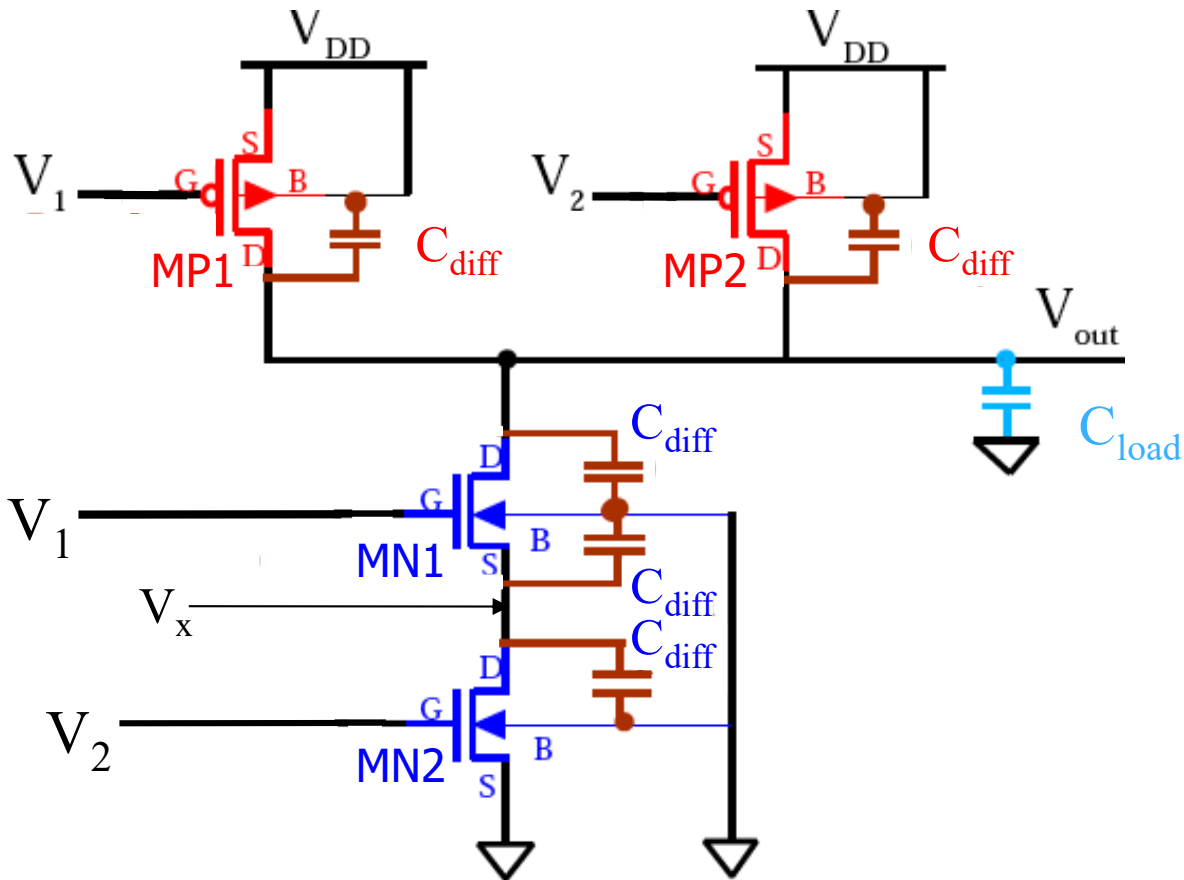
# Parasitic Caps for NAND2 (worst case)



Worst case for Pull-up  $\rightarrow V_1 = V_{DD}, V_2 = V_{DD} \rightarrow 0$  @  $t=0$  &  $V_x \approx V_{out} = 0 \rightarrow V_{DD}$

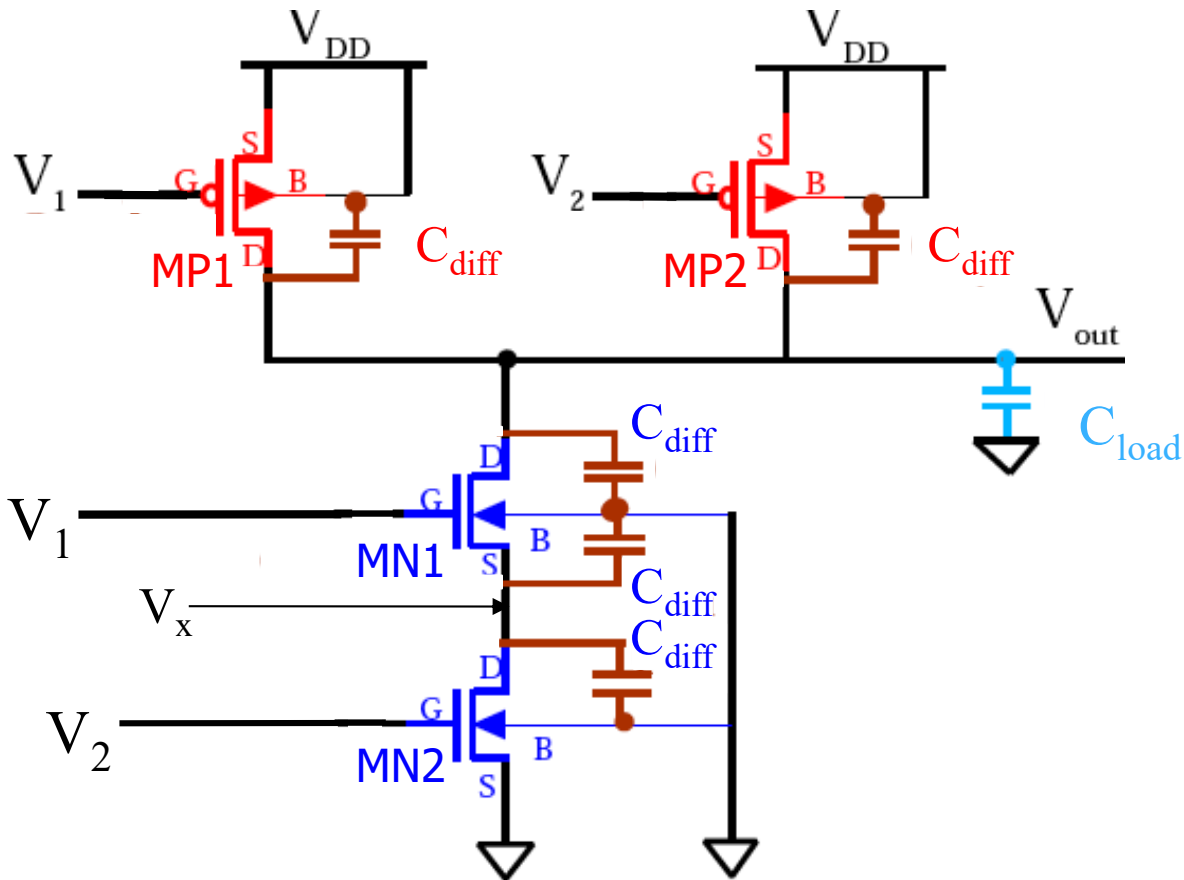


# Parasitic Caps for NAND2 (worst case)



Worst case for pull down →

# Parasitic Caps for NAND2 (worst case)



Worst case for pull down  $\rightarrow V_1 = V_{DD}, V_2 = 0 \rightarrow V_{DD} @ t=0$  &  $V_x \approx V_{out} = V_{DD} \rightarrow 0$



# Logic Types

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- ❑ CMOS Gates
  - Dual pull-down and pull-up networks, only one enabled at a time
  - Performance of gate is strong function of the fanin of gate
    - Techniques to improve performance include sizing, input reordering, and buffering (staging)
- ❑ Ratioed Gates
  - Have active pull-down (-up) network connected to load device
  - Reduced gate complexity at expense of static power asymmetric transfer function
    - Techniques to improve performance include sizing to improve noise margins and reduce static power
- ❑ Pass Gates
  - Implement logic gate as switch network for area and often delay win
  - Long cascades of switches result in quadratic increase in delay
  - Also suffer from reduced noise margins ( $V_T$  drop)
    - Use level-restoring buffers to improve noise margins
- ❑ Dynamic logic ... next time



# Idea

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- ❑ Elmore delay calculation allows us to estimate delay for distributed RC network
  - Necessary for pass transistors
- ❑ Wires are distributed RC
  - Half delay lumped calculation
  - Still quadratic in length
- ❑ Worst delay switching case
  - Put early inputs closer to supply rails



# Admin

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- Project 1
  - Final report due **Friday 3/29** midnight
  - Can use max one late day



# Acknowledgement

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- ❑ Prof. André DeHon (University of Pennsylvania)
- ❑ Prof. Jing Li (University of Pennsylvania)