**Today's Question:** How do we drive a large load  $(e.g. C_{load} = 4 \times 10^4 C_0)$  with minimum delay? Detail buffer count and sizing.

Assume:

- velocity saturated sizing for gate drive; inverter sizing is:  $W_n=2, W_p=2$
- Start with  $C_{diff} = 0$  case (for simplicity)
- 1. If we had one inverter stage to size, how should it be sized?



- (a) Write delay equation from  $R_0/2$  drive through driving  $C_{load}$ .
- (b) Symbolic expression for delay-minimizing  $W_N$ .
- (c) Concrete size,  $W_N$ , for  $C_{load} = 4 \times 10^4 C_0$ .
- 2. If we had k inverter stages to size, how should the each be sized?



- (b) Symbolic expression for delay-minimizing  $W_{Ni}$ .
- (c) Symbolic expression for total delay using solution above.



(**Hint:** solve for  $\gamma$  in terms of  $\rho$ )

ρ	$\gamma$
3	
4	

Assume:

- $R_u$ =60K $\Omega$  per 1mm length of wire;  $C_u$ =0.16pF per 1mm length of wire
- $R_{wire} = L \times R_u; C_{wire} = L \times C_u;$
- $R_0 = 25 \text{K}\Omega; C_0 = 0.01 \text{fF}$
- velocity saturated;  $\gamma = C_{diff}/C_{gate} = 1$
- initial, minimum size buffer has  $W_p = W_n = 1$
- 5. What is the delay of an unbuffered wire of length L=1mm driven and loaded by a minimum size buffer  $(W_p = 1, W_n = 1)$ ? Draw the equivalent RC network and write a symbolic equation.



v	0		÷ 1
wire.			
Wire of Length	Delay (ns)	Number in 1mm	Total Delay for 1mm (ns)
1mm		1	
0.5mm		2	
0.1mm		10	
0.01mm		100	
0.001mm		1000	

6. What is the delay of a length L = 1mm, when we add N evenly spaced buffers to the wire.

7. What is the delay of a length L, when we add N evenly spaced buffers to the wire.

- Symbolic Equation:
- 8. How many buffers do we use to minimize delay?
  - Symbolic Equation:
  - Number of buffers to minimize delay on 1mm wire:
  - Delay at this buffer count:
  - Optimum segment length between buffers:
- 9. How should we size the buffers?
  - Symbolic Equation:
    W to minimize delay:
    Delay of 1mm wire at optimal buffer size: