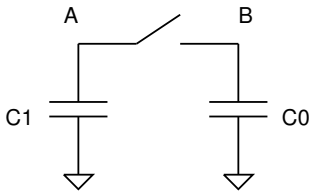
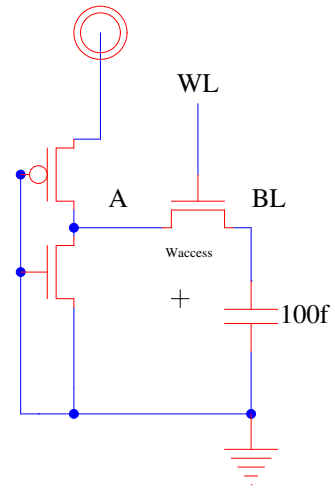
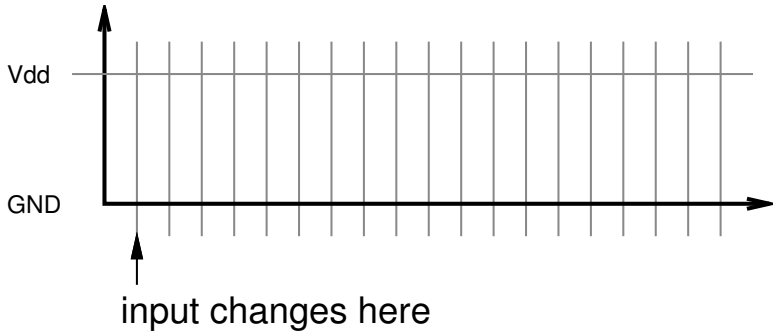
1. Initially: The switch is open and node A is charged to 1V and node B is charged to 0V.
   What is the voltage at node A in steady state after the switch is closed?



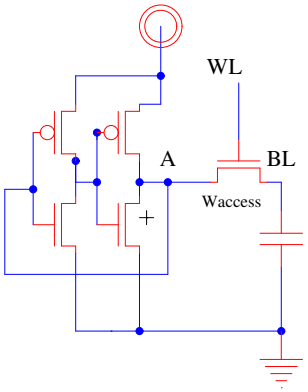
2. What is the waveform on A after WL transitions from 0 to 1?

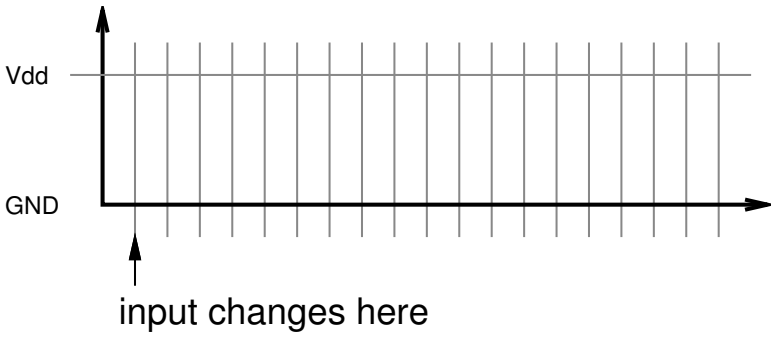




   Assume BL initially at 0. How does it depend on W_{access}?

3. What is the waveform on A after WL transitions from 0 to 1?



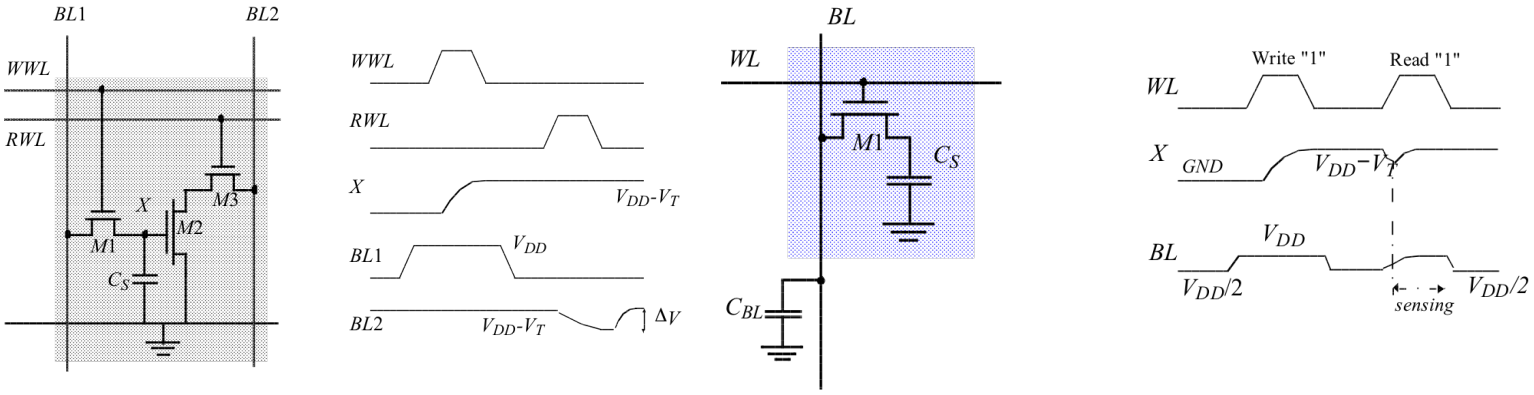


   Assume:

   - BL initially at 0
   - A initially at 1

   How does it depend on W_{access}?

4. Below is the 3T DRAM and 1T DRAM cell with waveform for writing a '1' into the cell and then reading the cell.



5. What is capacitance of the bit line? In terms of access transistor width W_{access}, number of words on bit line, d, γ, and C_0.

6. Delay of memory cell driving bit line? (Read operation) In terms of variables above plus buffer size, W_{buf}, and R_0.

7. Concrete delay for $W_{access} = W_{buf} = 1$, $\gamma = 0.5$? In terms of $\tau = R_0 C_0$.

Unit	Delay in τ
d=32 (register file)	
d=512 (BRAM or small L1 Cache)	

8. What is the capacitance of the word line? In terms of access transistor width W_{access}, number of bits on the word line, w, γ, and C_0.

9. Delay driving word line, assuming driven by a driver with equivalent drive strength to $W_{wldrive}$ inverter? (other parameters as above)