ESE3700: Circuit-Level Modeling, Design and Optimization for Digital Systems

Lec 20: April 24, 2024

Inductive Noise and Crosstalk

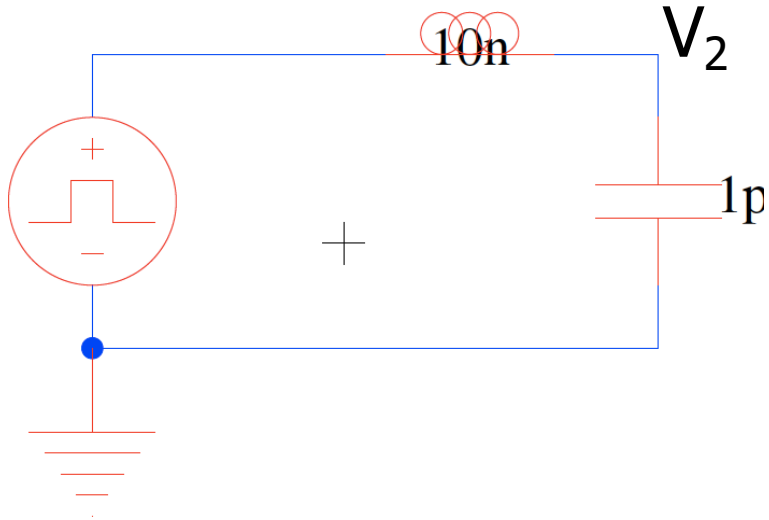
Today

- Inductive Responses
- Calculating L
- Where inductances show up
- Impact of inductance on digital circuits
- How to address inductive noise

LC Response (preclass 1)

- What happens here?

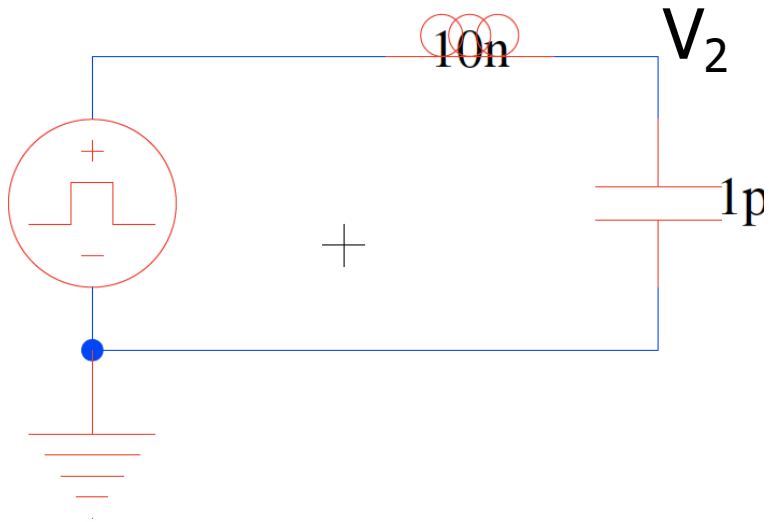
$$L\frac{dI_L}{dt} = V_L \qquad I_C = C\frac{dV_C}{dt}$$



LC Response

- What happens here?

$$L\frac{dI_L}{dt} = V_L \qquad I_C = C\frac{dV_C}{dt}$$



$$L\frac{dI}{dt} + V_2 = V_S$$

$$I = C\frac{dV_2}{dt} \Rightarrow \frac{dI}{dt} = C\frac{d^2V_2}{dt^2}$$

$$LC\frac{d^2V_2}{dt^2} + V_2 = V_S$$

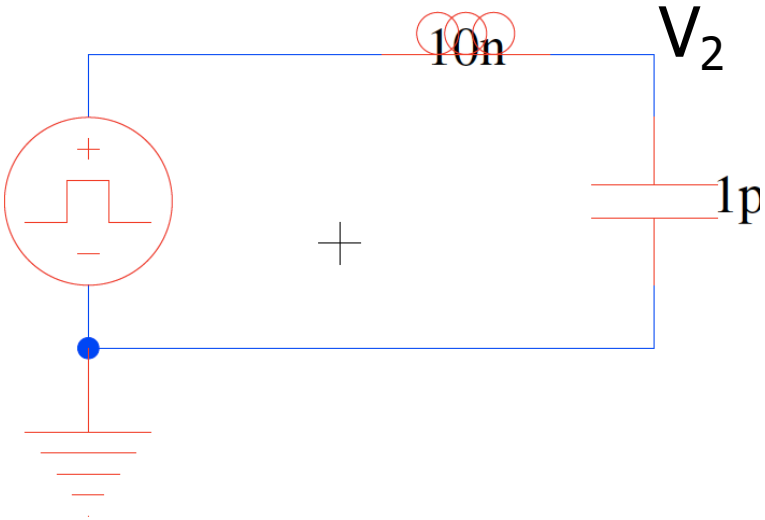
LC Response

- What happens here?

$$\omega = \sqrt{\frac{1}{LC}}$$

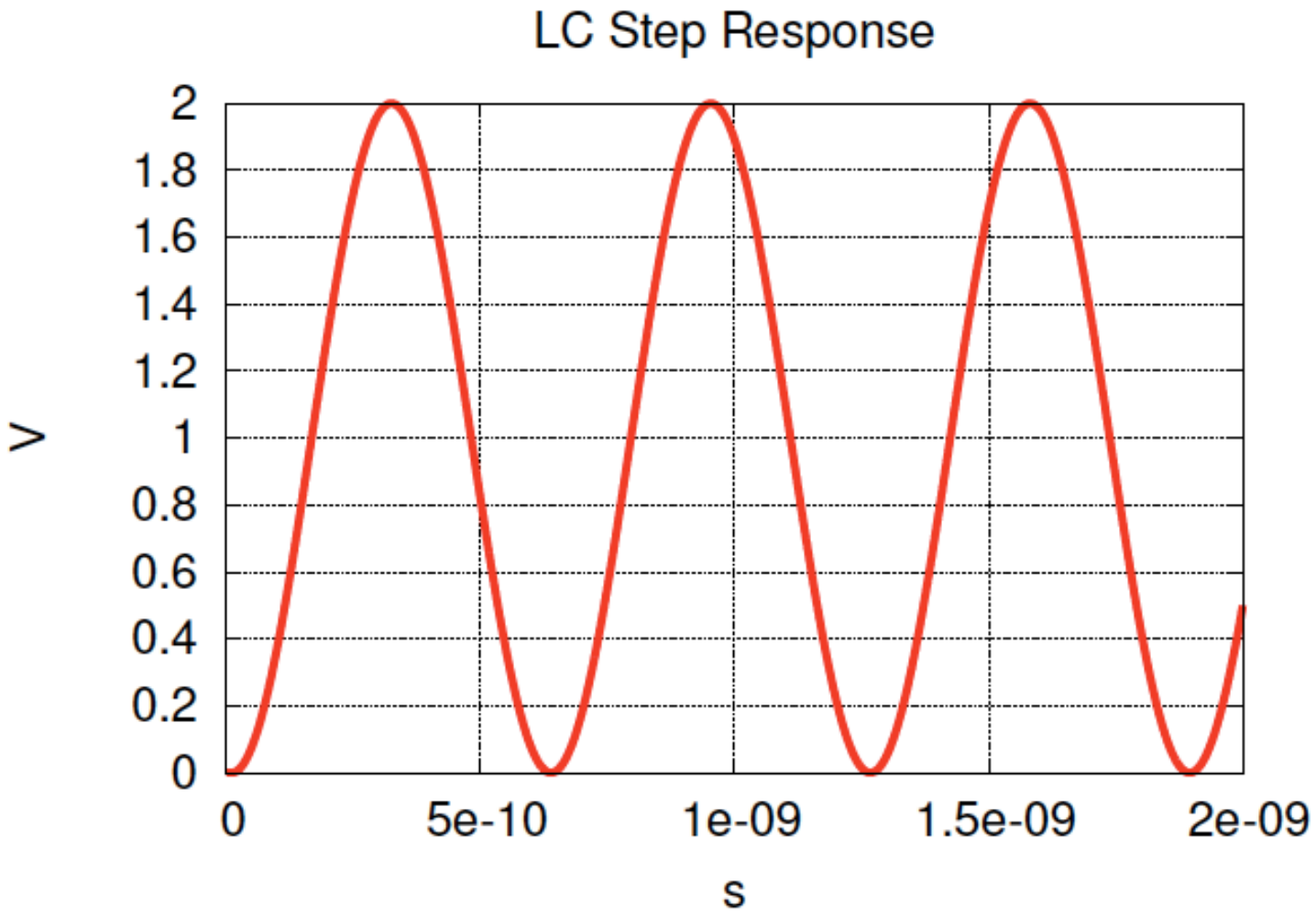
$$V_2 = A + Be^{j\omega t}$$

$$V_2 = V + Be^{j\left(\sqrt{\frac{1}{LC}}\right)t}$$

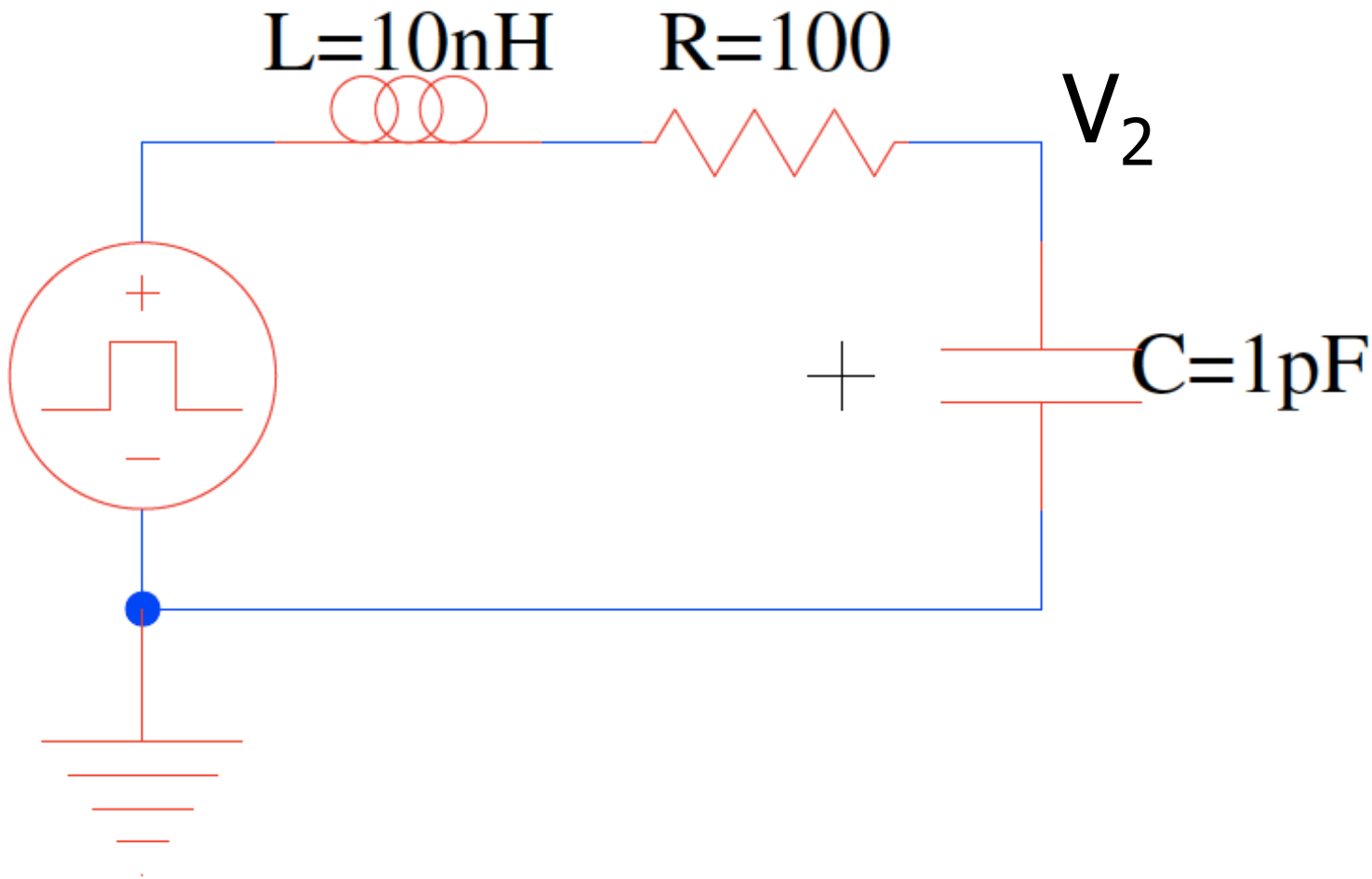


$$e^{j\theta} = \cos(\theta) + j\sin(\theta)$$

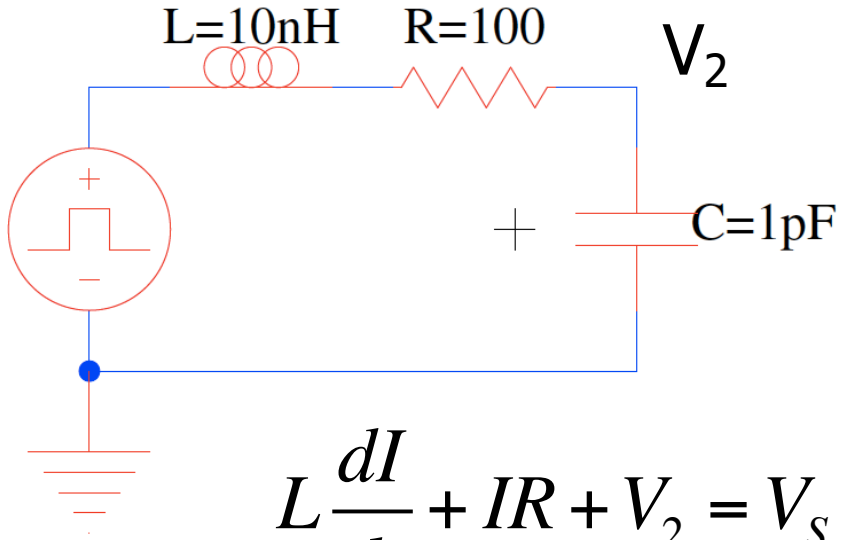
LC Response


LC Step Response
2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0
V
0
5e-10
1e-09
1.5e-09
2e-09
s

Response? (preclass 1)



RLC Response



$$L\frac{dI}{dt} + IR + V_2 = V_S$$

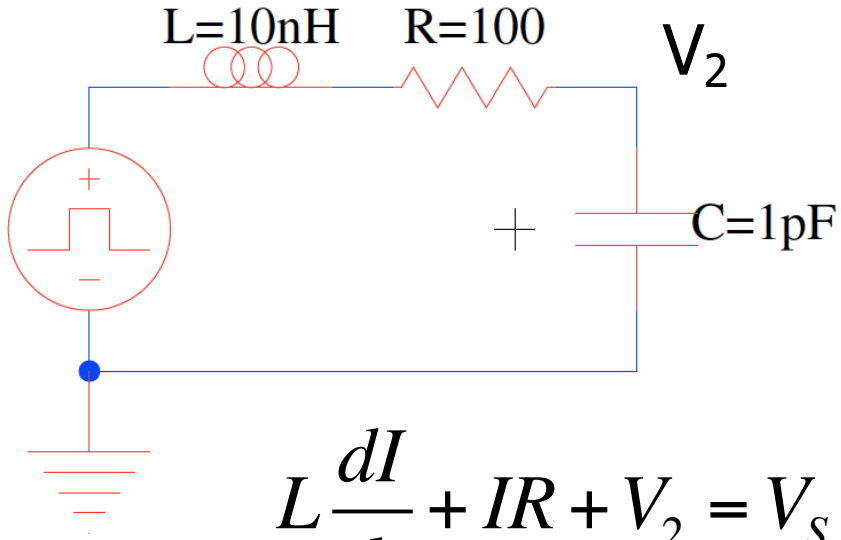
$$I = \frac{CdV_2}{dt}$$

RLC Response

$$V_2 = A + Be^{j\omega t}$$

$$\frac{dV_2}{dt} = j\omega Be^{j\omega t}$$

$$\frac{d^2V_2}{dt^2} = -\omega^2 Be^{j\omega t}$$



$$L\frac{dI}{dt} + IR + V_2 = V_S$$

$$LC\left(\frac{d^2V_2}{dt^2}\right) + RC\left(\frac{dV_2}{dt}\right) + V_2 = V_S$$

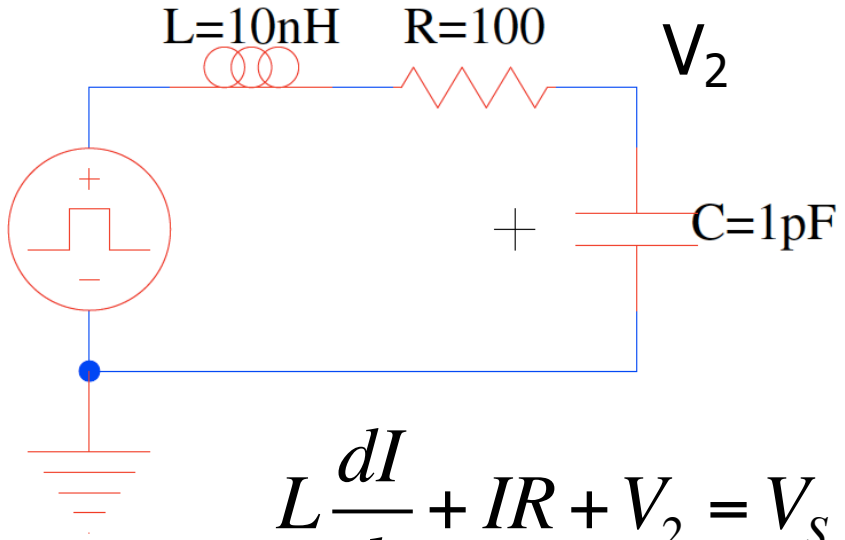
$$LC\left(-\omega^2 Be^{j\omega t}\right) + RC\left(j\omega Be^{j\omega t}\right) + A + Be^{j\omega t} = V_S$$

RLC Response

$$V_2 = A + Be^{j\omega t}$$

$$\frac{dV_2}{dt} = j\omega Be^{j\omega t}$$

$$\frac{d^2V_2}{dt^2} = -\omega^2 Be^{j\omega t}$$



$$L\frac{dI}{dt} + IR + V_2 = V_S$$

$$LC\left(-\omega^2 Be^{j\omega t}\right) + RC\left(j\omega Be^{j\omega t}\right) + A + Be^{j\omega t} = V_S$$

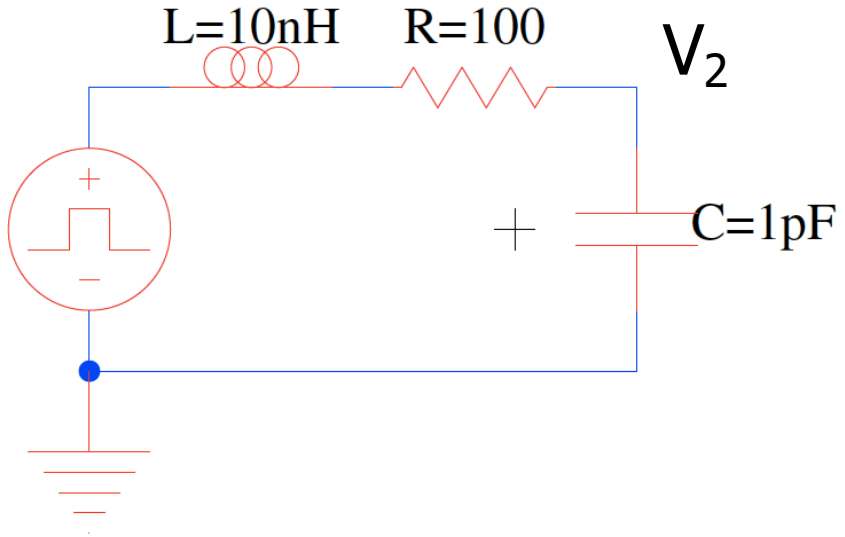
$$A = V_S$$

$$LC\left(-\omega^2\right) + RC\left(j\omega\right) + 1 = 0$$

RLC Response

$$LC\left(-\omega^2\right)+RC\left(j\omega\right)+1=0$$

$$\omega^2-j\omega\frac{R}{L}-\frac{1}{LC}=0$$



$$\omega=\frac{j\frac{R}{L}\pm\sqrt{\left(-j\frac{R}{L}\right)^2+\frac{4}{LC}}}{2}$$

$$\omega=j\frac{R}{2L}\pm\sqrt{\frac{1}{LC}-\left(\frac{R}{2L}\right)^2}$$

RLC Response

$$LC\left(-\omega^2\right)+RC\left(j\omega\right)+1=0$$

$$\omega^2-j\omega\frac{R}{L}-\frac{1}{LC}=0$$

$$\omega=\frac{j\frac{R}{L}\pm\sqrt{\left(-j\frac{R}{L}\right)^2+\frac{4}{LC}}}{2}$$

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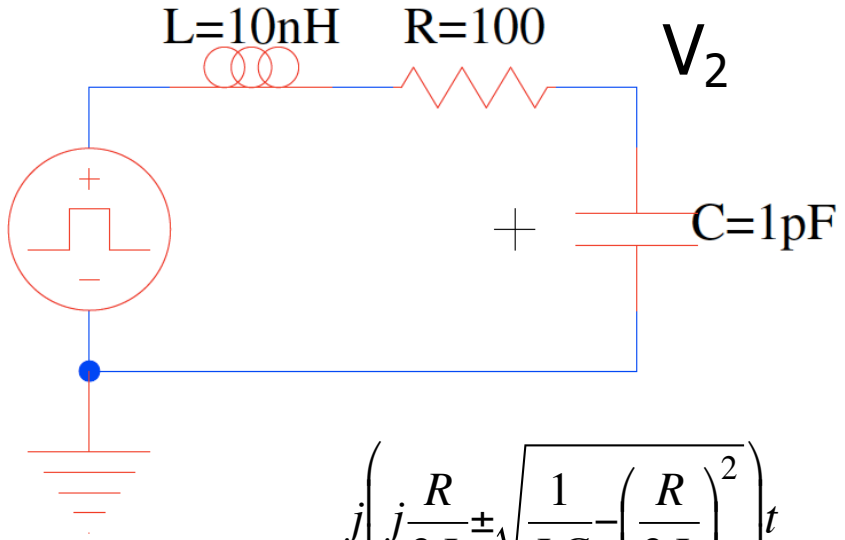


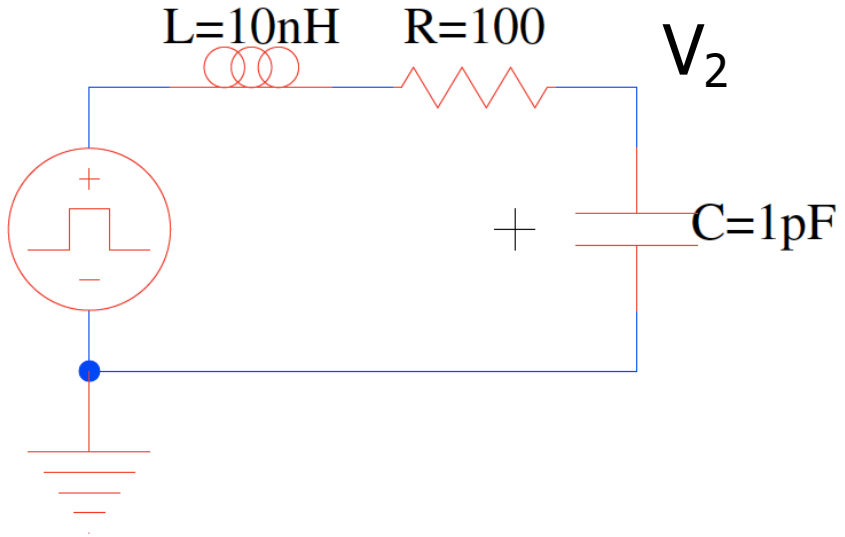
$$V_2=V_S+Be^{\left(j\frac{R}{2L}\pm\sqrt{\frac{1}{LC}-\left(\frac{R}{2L}\right)^2}\right)t}$$

$$V_2=V_S+Be^{\left(-\frac{R}{2L}\pm j\sqrt{\frac{1}{LC}-\left(\frac{R}{2L}\right)^2}\right)t}$$

$$V_2=V_S+Be^{\left(-\frac{R}{2L}\right)t}e^{\left(j\sqrt{\frac{1}{LC}-\left(\frac{R}{2L}\right)^2}\right)t}$$

RLC Response (preclass 2)

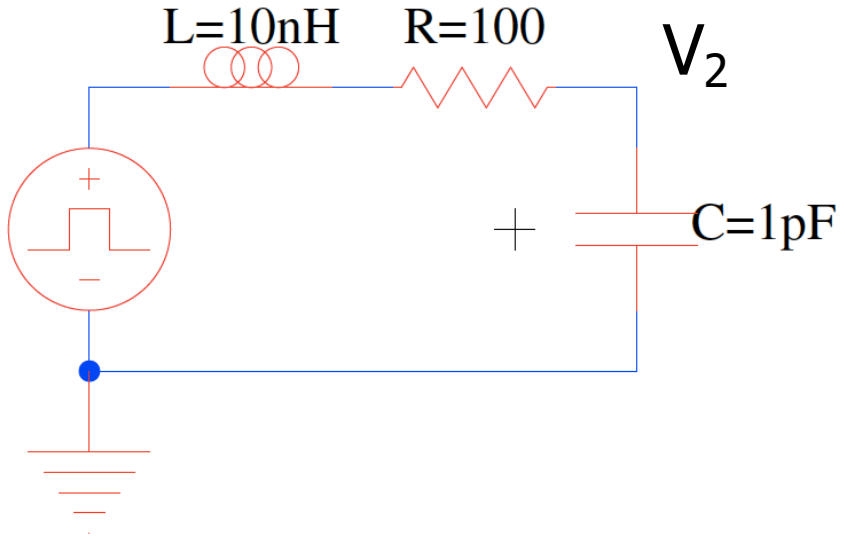
$$V_2 = V_S + Be^{\left(-\frac{R}{2L}\right)t} e^{\left(j\sqrt{\frac{1}{LC}-\left(\frac{R}{2L}\right)^2}\right)t}$$



- For what R does this circuit oscillate?

RLC Response

$$V_2 = V_S + Be^{\left(-\frac{R}{2L}\right)t} e^{\left(j\sqrt{\frac{1}{LC}-\left(\frac{R}{2L}\right)^2}\right)t}$$



- For what R does this circuit oscillate?

$$\frac{1}{LC} - \left(\frac{R}{2L}\right)^2 > 0$$

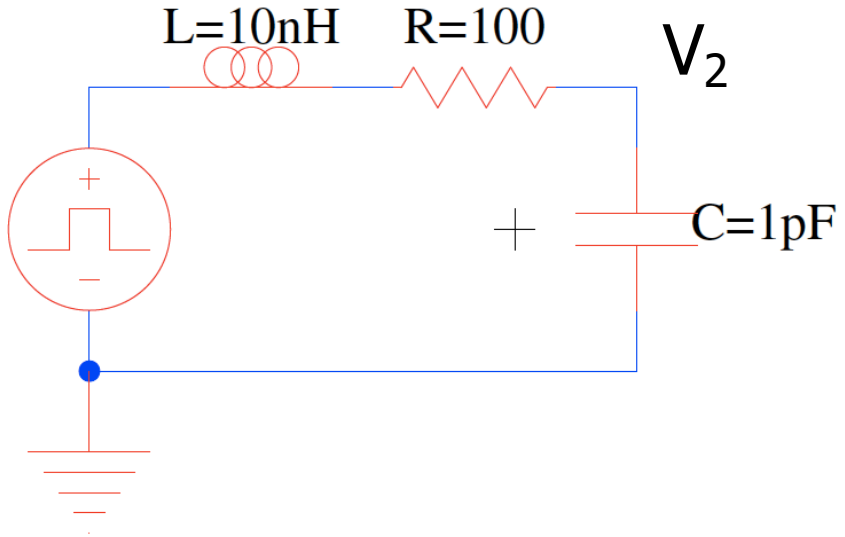
$$\frac{1}{LC} > \left(\frac{R}{2L}\right)^2 \Rightarrow \sqrt{\frac{4L}{C}} > R$$

RLC Response

$$V_2 = V_S + Be^{\left(-\frac{R}{2L}\right)t} e^{\left(j\sqrt{\frac{1}{LC}-\left(\frac{R}{2L}\right)^2}\right)t}$$

Decay

Oscillation



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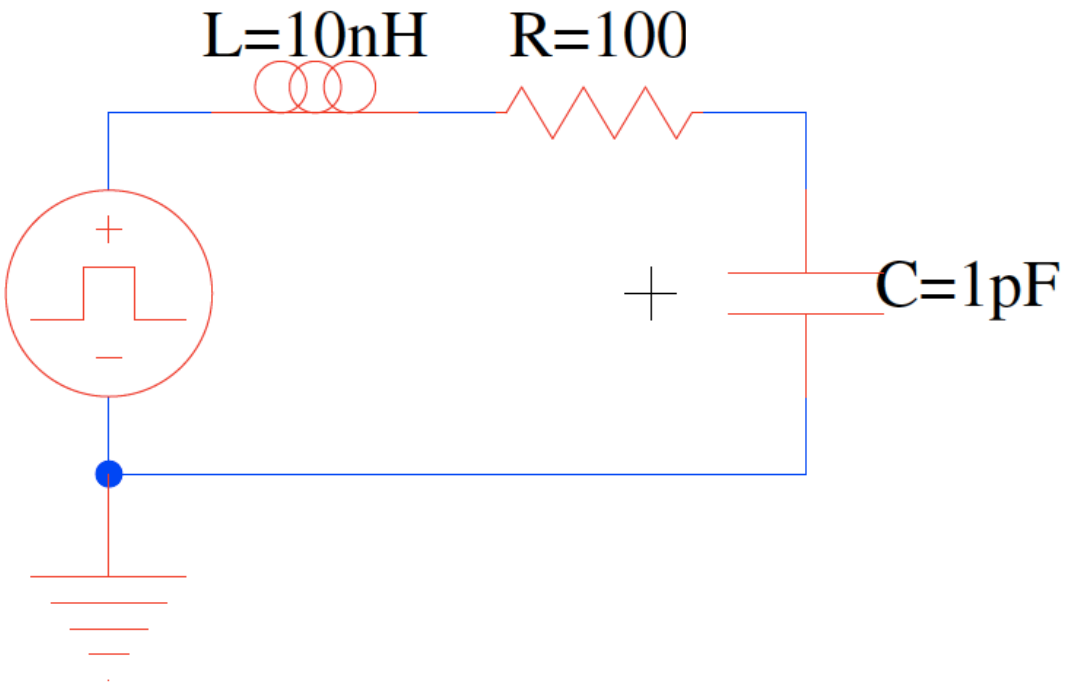
When Oscillate

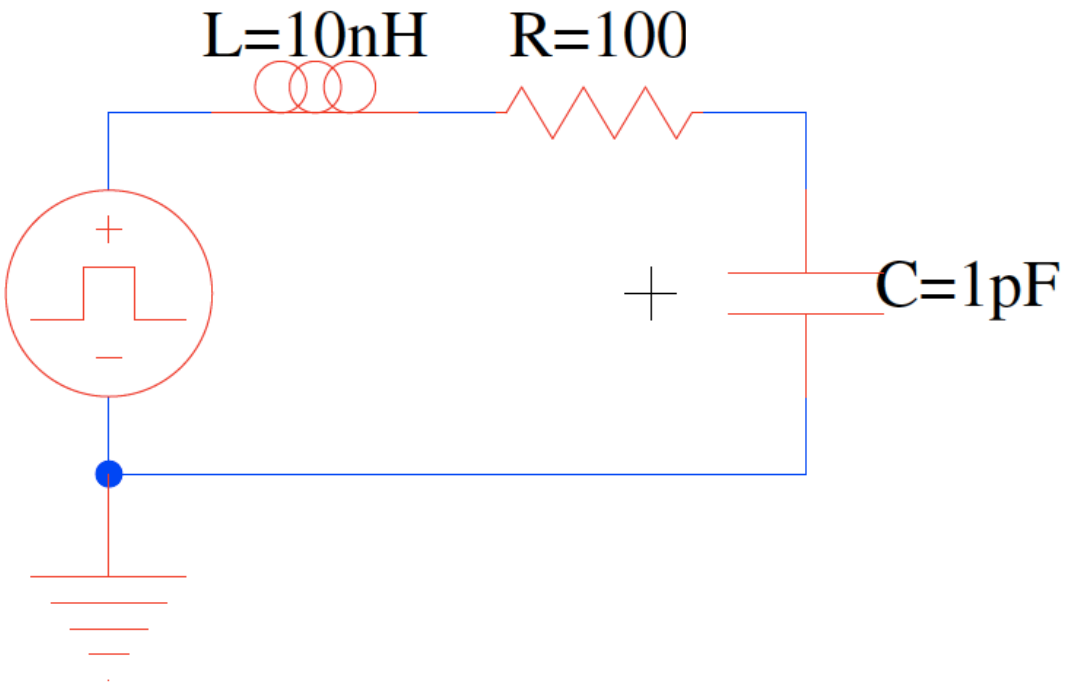
- For what R does this particular circuit oscillate?



When Oscillate

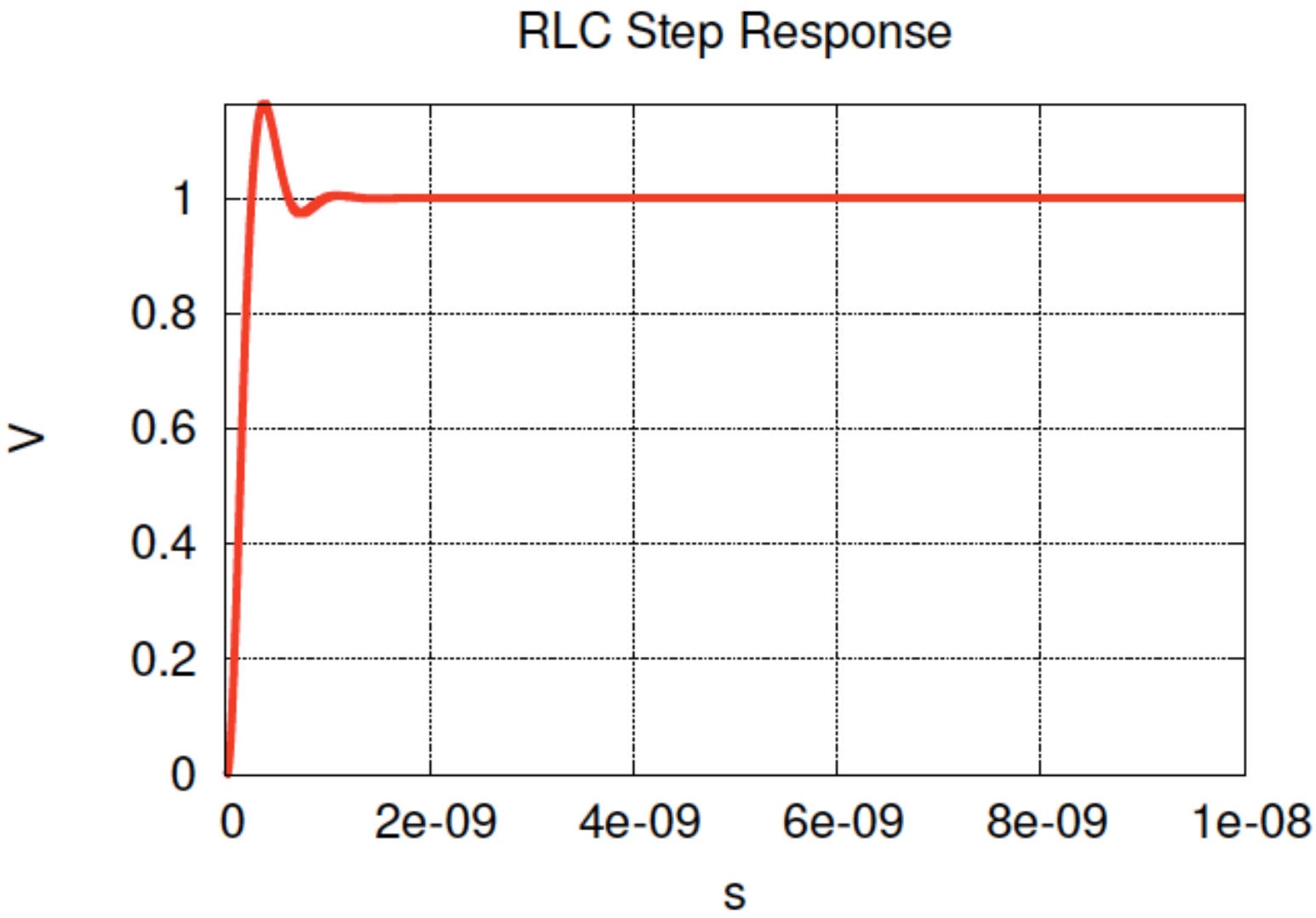
- For what R does this particular circuit oscillate?

$$R < \sqrt{\frac{4L}{C}}$$

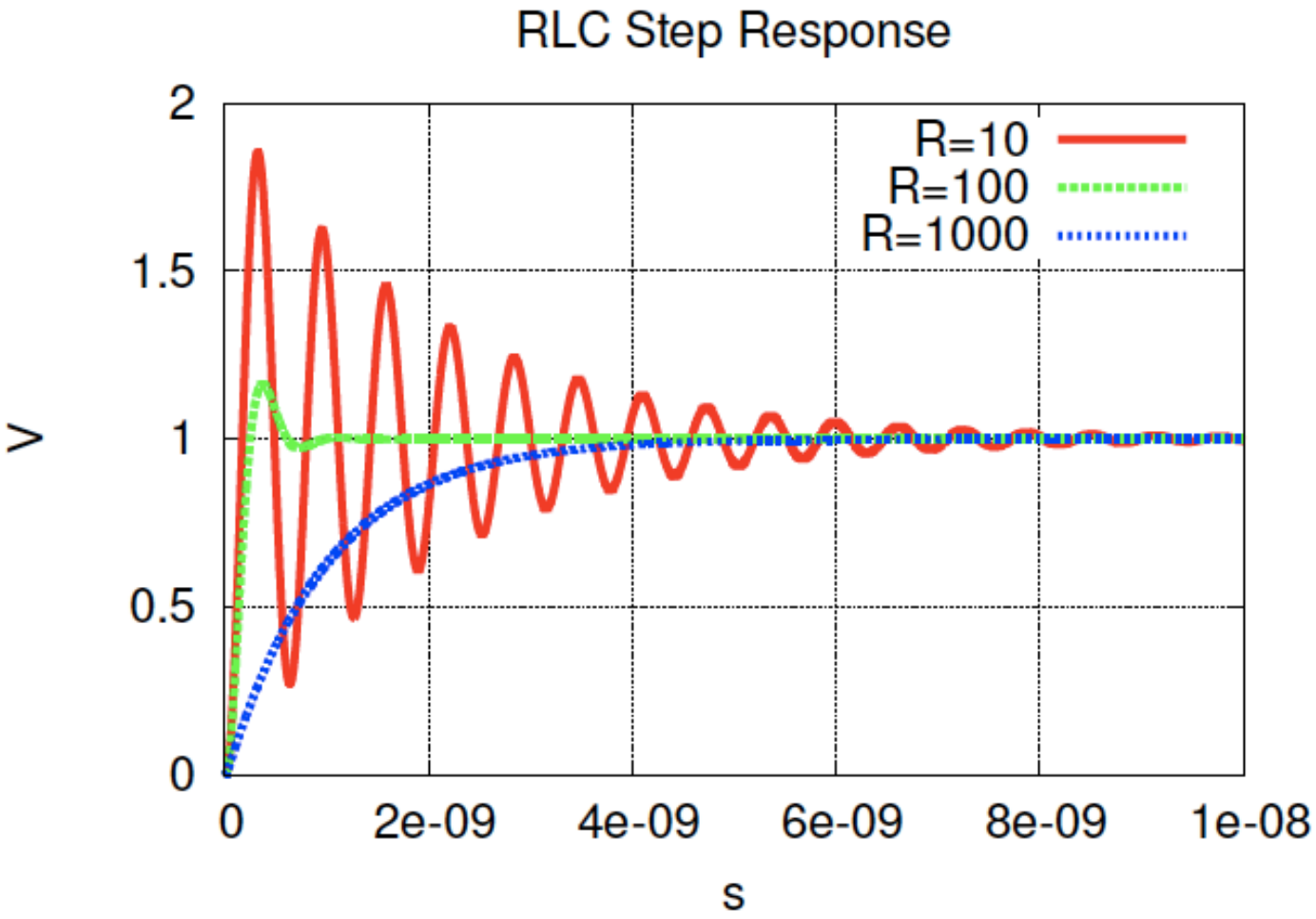


$$\sqrt{\frac{4L}{C}} = 200$$

RLC Response (R=100)



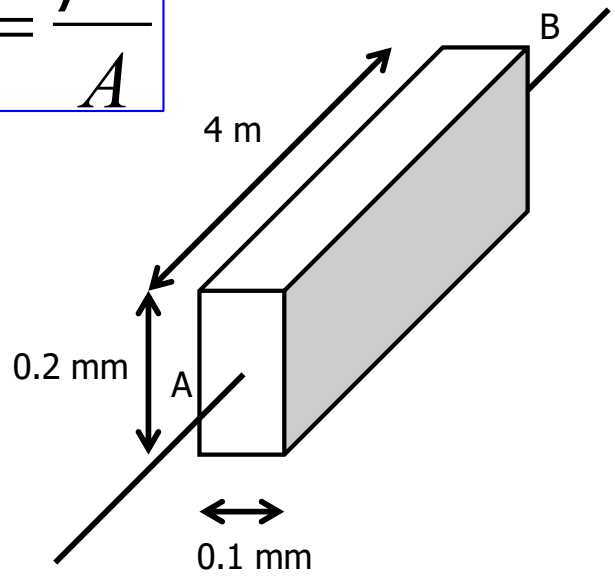
RLC Response



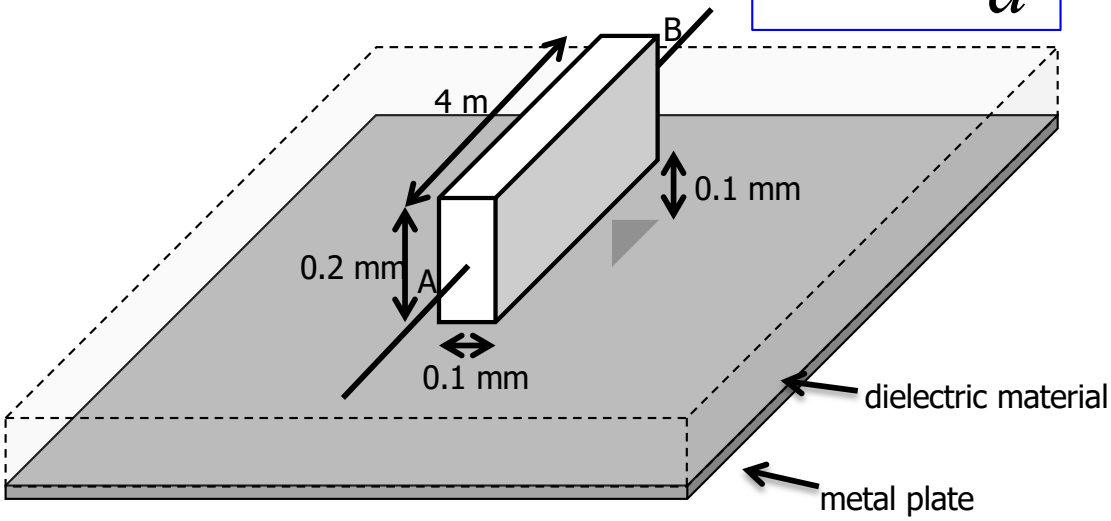
Inductance of Wire

Isolated Wire RC

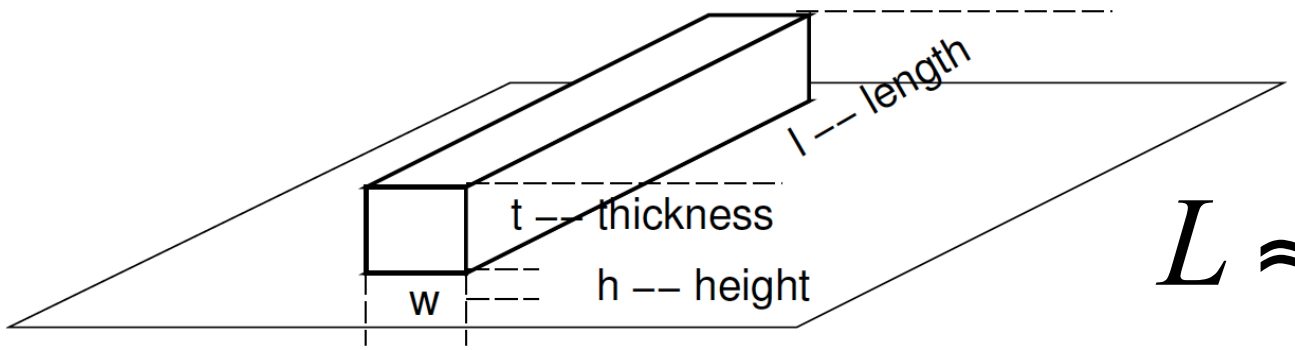
$$R = \frac{\rho L}{A}$$



$$C = \varepsilon_d \frac{A}{d}$$

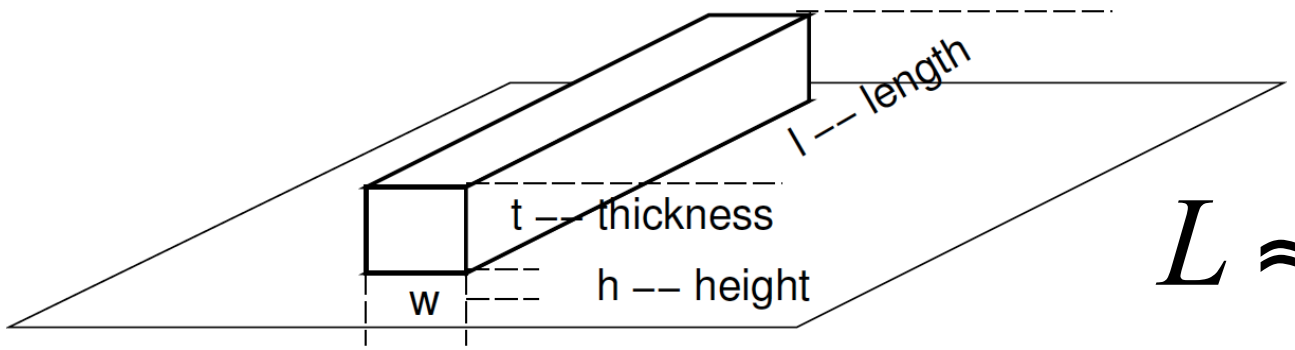


Inductance: Wire over Ground Plane



$$L \approx l\left(\frac{\mu_0 \mu_r h}{w}\right)$$

Inductance: Wire over Ground Plane



$$L \approx l\left(\frac{\mu_0 \mu_r h}{w}\right)$$

$$C = \varepsilon_r \varepsilon_0 \frac{A}{d} = \varepsilon_r \varepsilon_0 \frac{wl}{h} = l\left(\varepsilon_r \varepsilon_0 \frac{w}{h}\right)$$

Inductance: Wire over Ground Plane

$$C' = \varepsilon_r \varepsilon_0 \frac{w}{h} \qquad L' \approx \left(\frac{\mu_0 \mu_r h}{w} \right)$$

$$C'L' = \varepsilon\mu$$

C' and *L'* per unit length

$$L' = \frac{\varepsilon\mu}{C'}$$

On Chip Inductance

- $C_{wire} = 0.16$ pF (for the 1mm)
- $C_{wire} = 0.16$nF/m

- Permeability $\mu_0 \approx \mu_{Si02} = 12.6 \cdot 10^{-7}$H/m
- Permitivity $\varepsilon_{ox} = 3.5 \cdot 10^{-11}$F/m

$$L' = \frac{\varepsilon\mu}{C'}$$

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- C_{wire} = 0.16nF/m

- Permeability $\mu_0 \approx \mu_{Si02} = 12.6 \cdot 10^{-7}$H/m
- Permitivity $\varepsilon_{ox} = 3.5 \cdot 10^{-11}$F/m
- 276 pH (for 1 mm)

$$L' = \frac{\varepsilon\mu}{C'}$$

PCB Trace Inductance (preclass 3)

- Inductance per cm of PCB trace with h=3mil, w=5mil (1mil = .001 inch)
  - $\mu_0 = 1.26 \times 10^{-6}$
  - $\mu_r = 1$

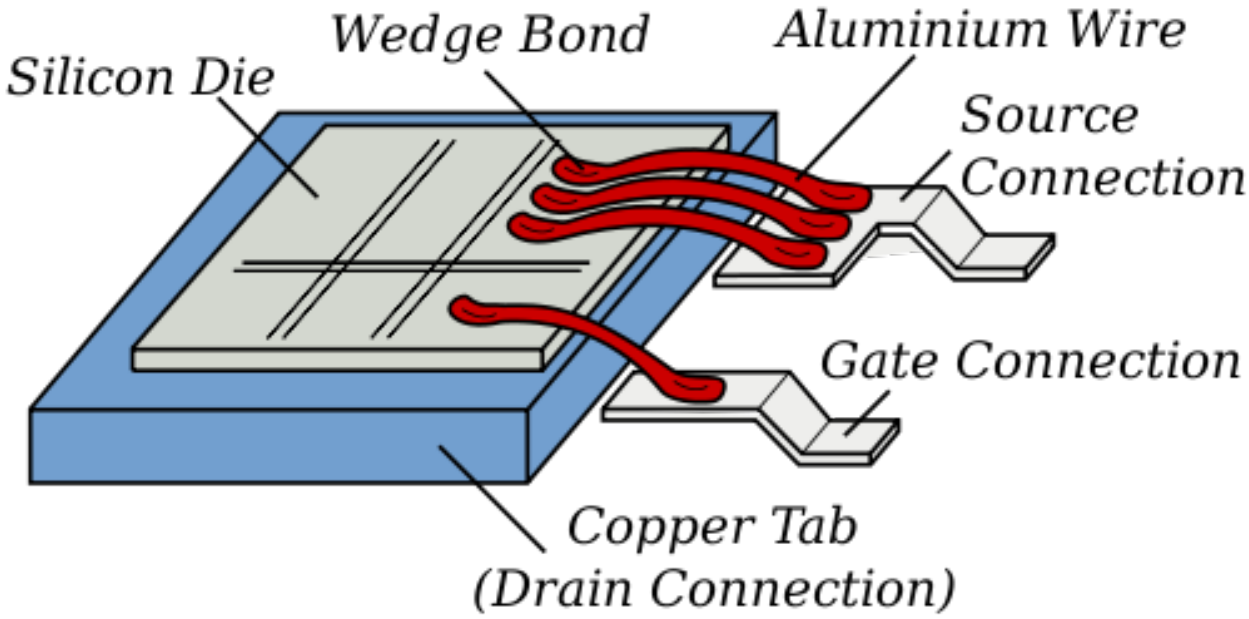
$$L \approx l\left(\frac{\mu_0 \mu_r h}{w}\right)$$

Comparisons

- 5mil trace on PCB
  - 7.56nH/cm
- Breadboard wires (0.6mm diameter)
  - About 7nH/cm
- On chip wire
  - 0.28nH/mm = 2.8nH/cm

Inductors

- Bond pads
- Package leads
- Long wire runs
- Cables

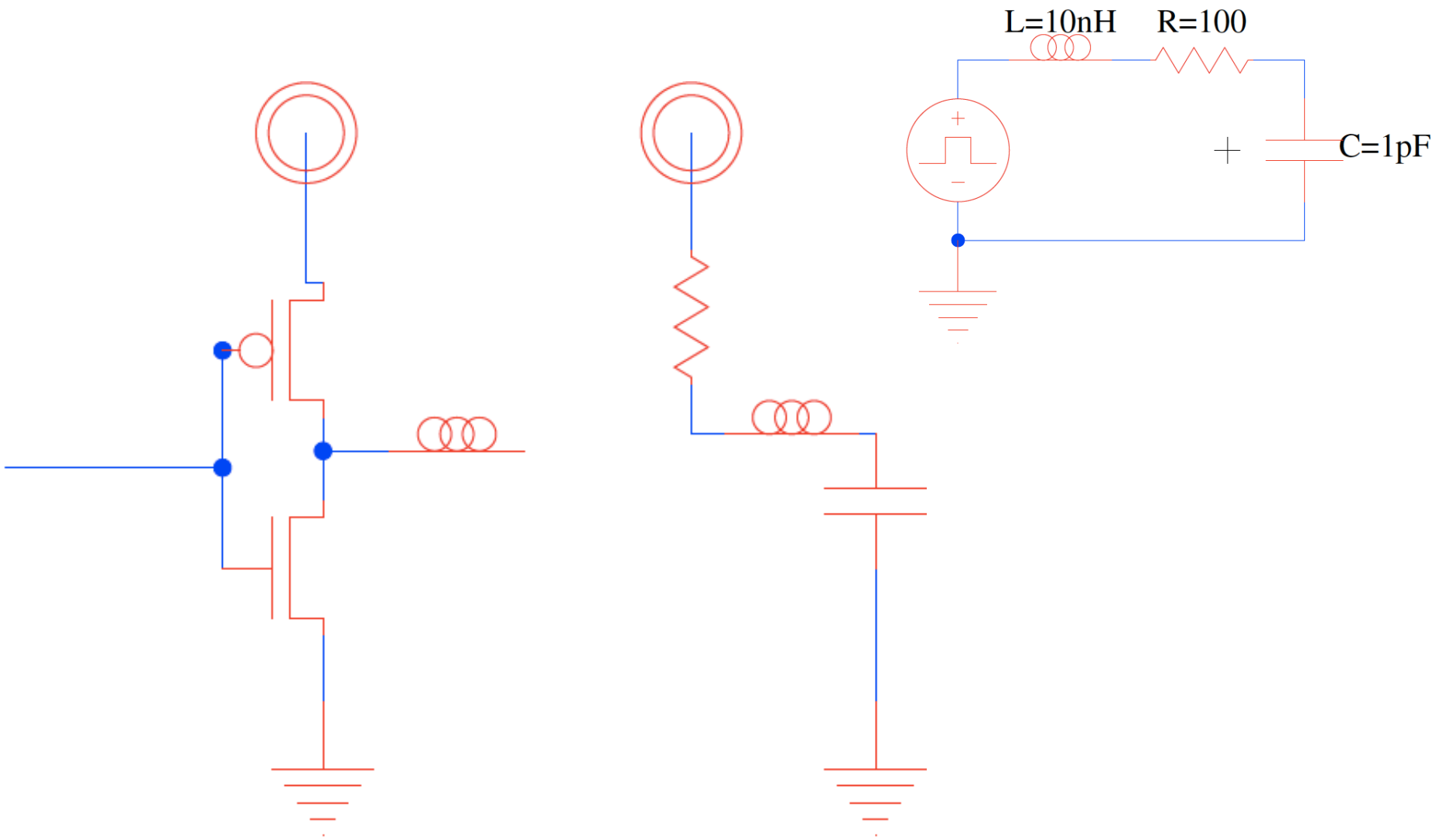


Src: http://en.wikipedia.org/wiki/File:Wirebonding2.svg

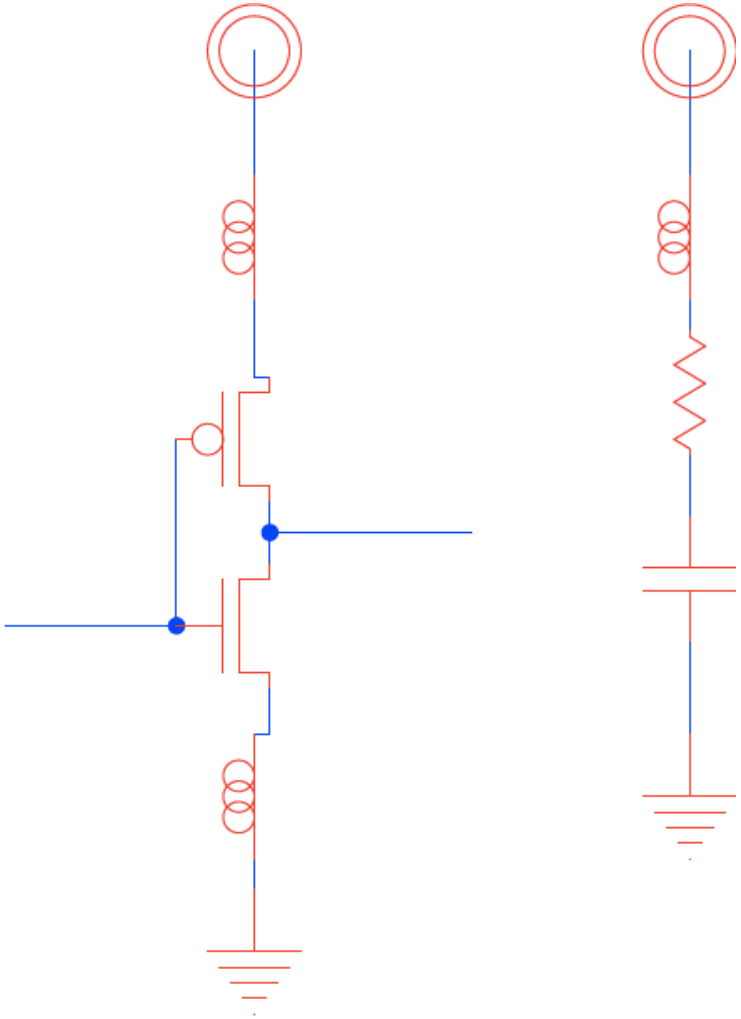
Where Inductance Arises

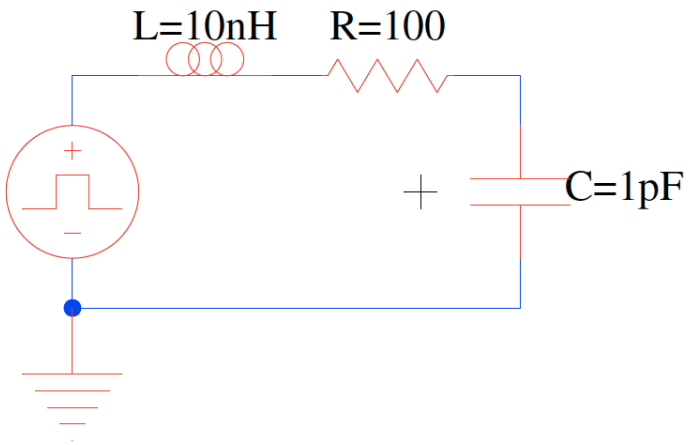
In our digital systems

Signal Path

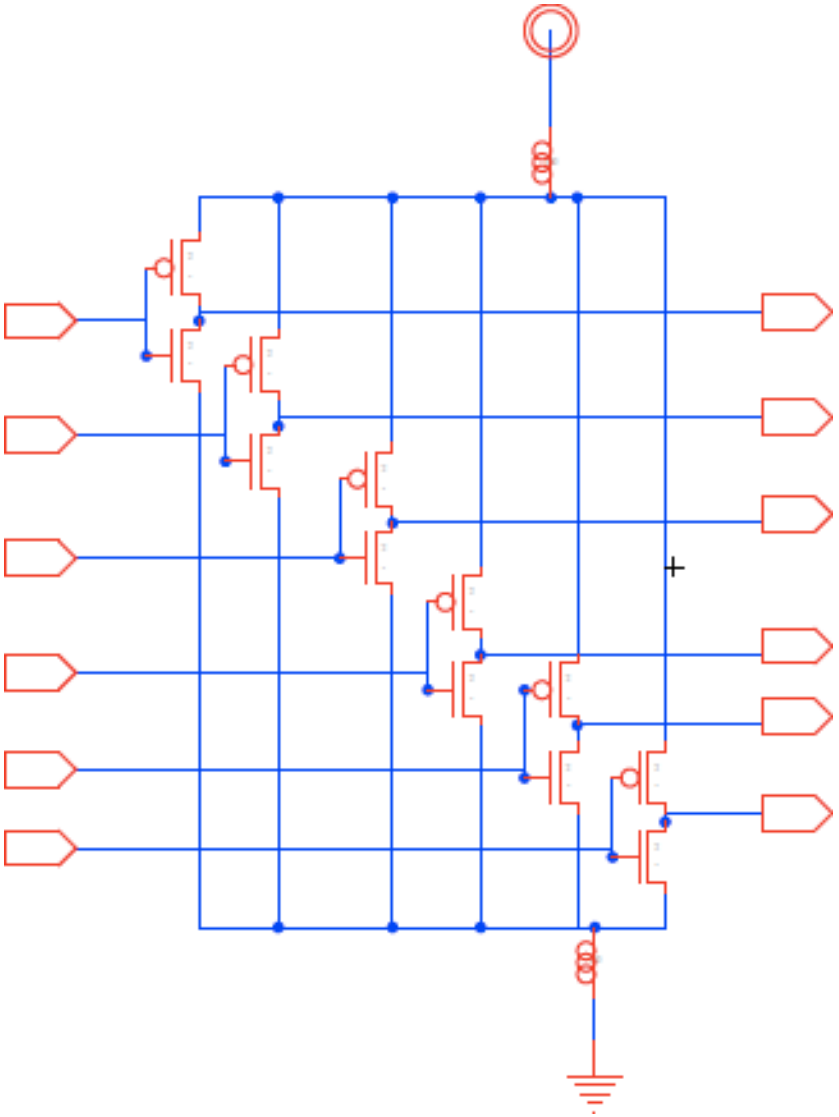


Power Ground





Shared Power/Ground Example: 74x04



Estimate

- R_{eq}, C_{eq} for gates in parallel
  - $R_0 = 25K\,\Omega$
  - $C_0 = 0.01$ fF
    - say $10C_0 = 0.1$fF for typical load
- 250 gates switching at clock

$$V_2 = V_S + Be^{\left(-\frac{R}{2L}\right)t} e^{\left(j\sqrt{\frac{1}{LC}-\left(\frac{R}{2L}\right)^2}\right)t}$$

Decay

Oscillation

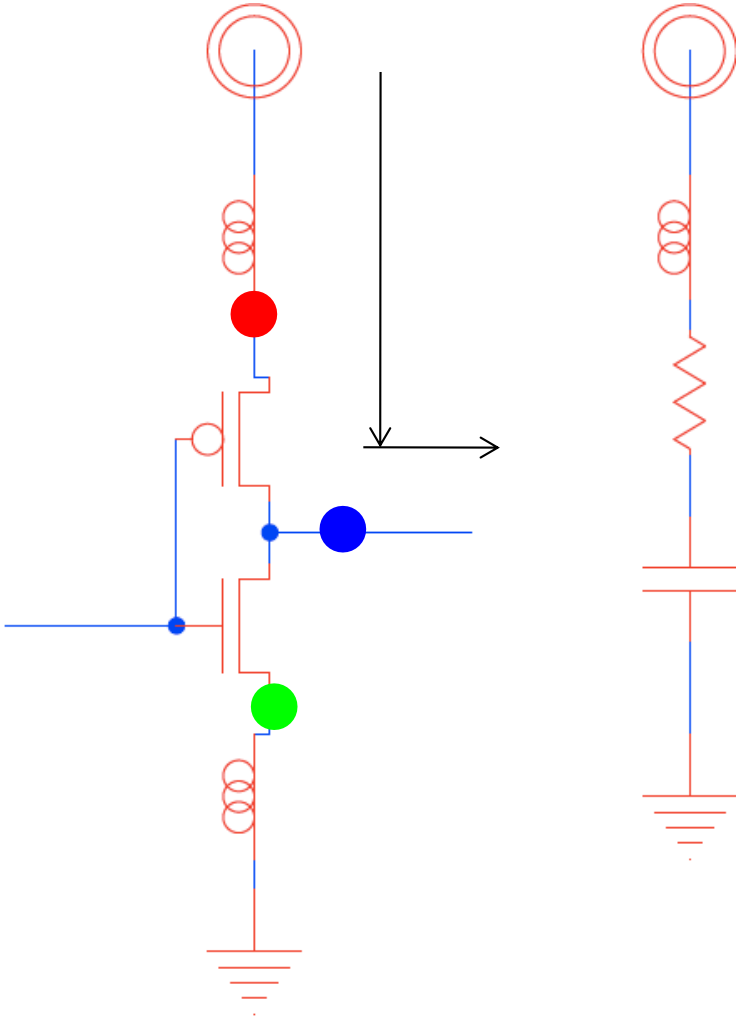
Estimate

- R_{eq}, C_{eq} for gates in parallel
  - $R_0 = 25K\,\Omega$
  - $C_0 = 0.01$ fF
    - say $10C_0 = 0.1$fF for typical load
- 250 gates switching at clock
- $R_{eq} = 100\Omega$ C_{eq}=25fF
- Assume L=1nH
- How long to settle? Oscillation freq?

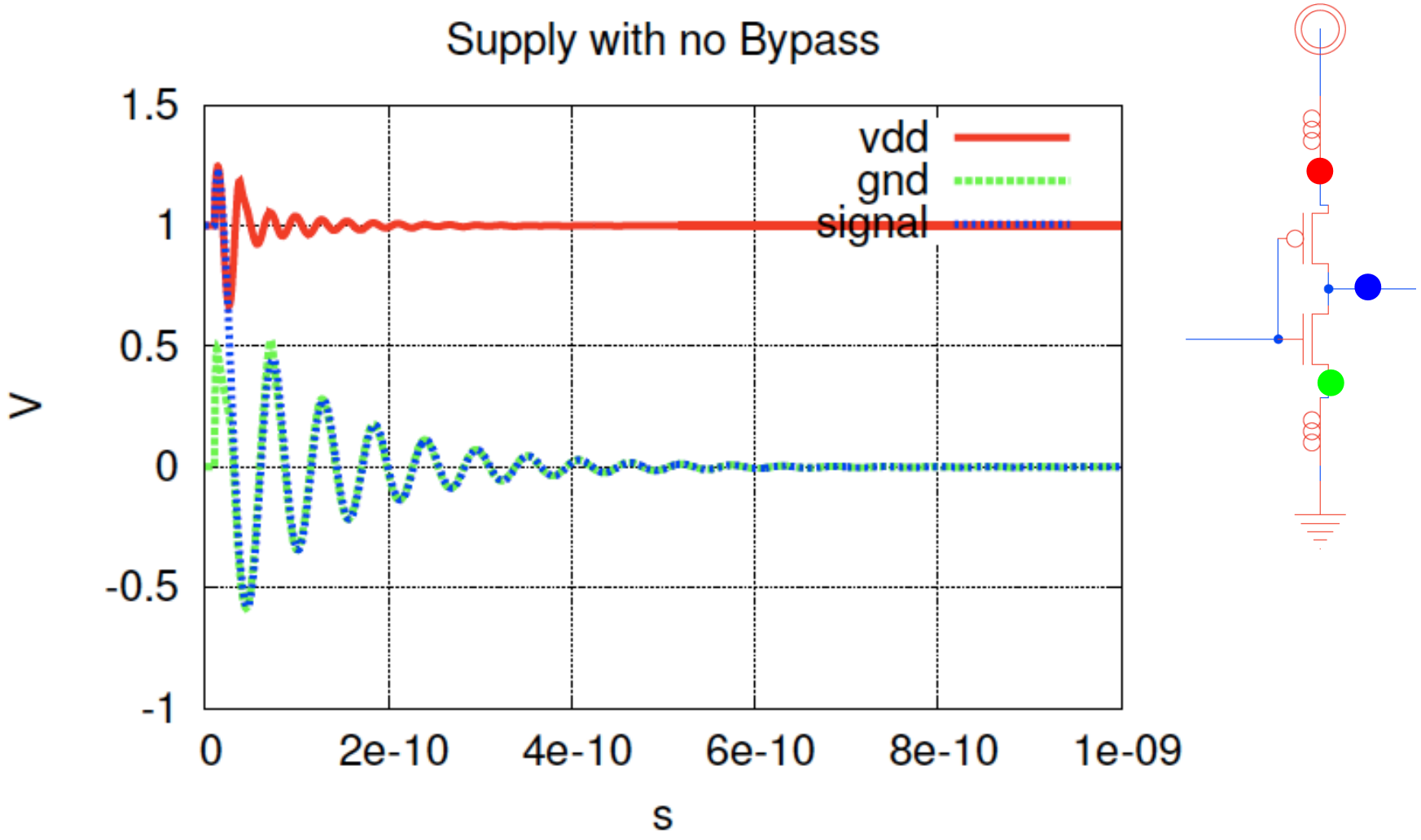
$$V_2 = V_S + Be^{\left(-\frac{R}{2L}\right)t} e^{\left(j\sqrt{\frac{1}{LC}-\left(\frac{R}{2L}\right)^2}\right)t}$$

Decay | Oscillation

Power Ground

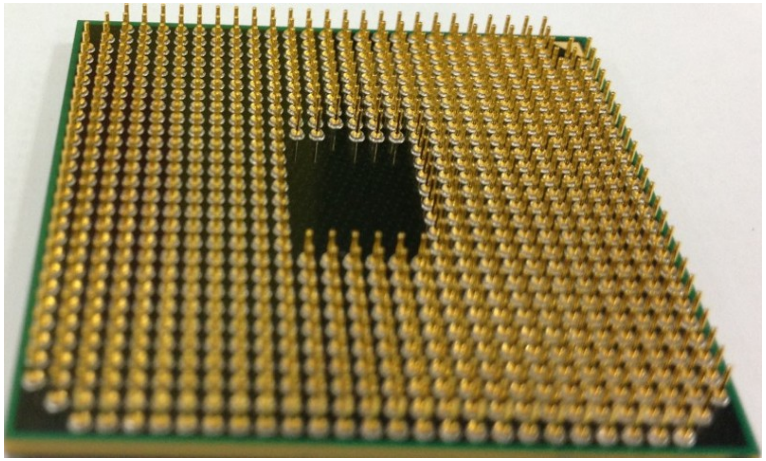


RLC Response



Today's chips: Multiple Power/Ground Pins

- Use many power/ground pins



- Divide switching gates by pins
  - To get effective load on each pin

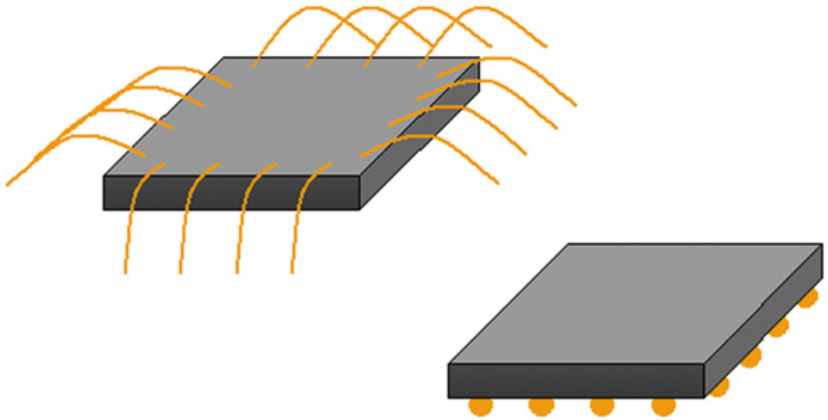
Improve Performance

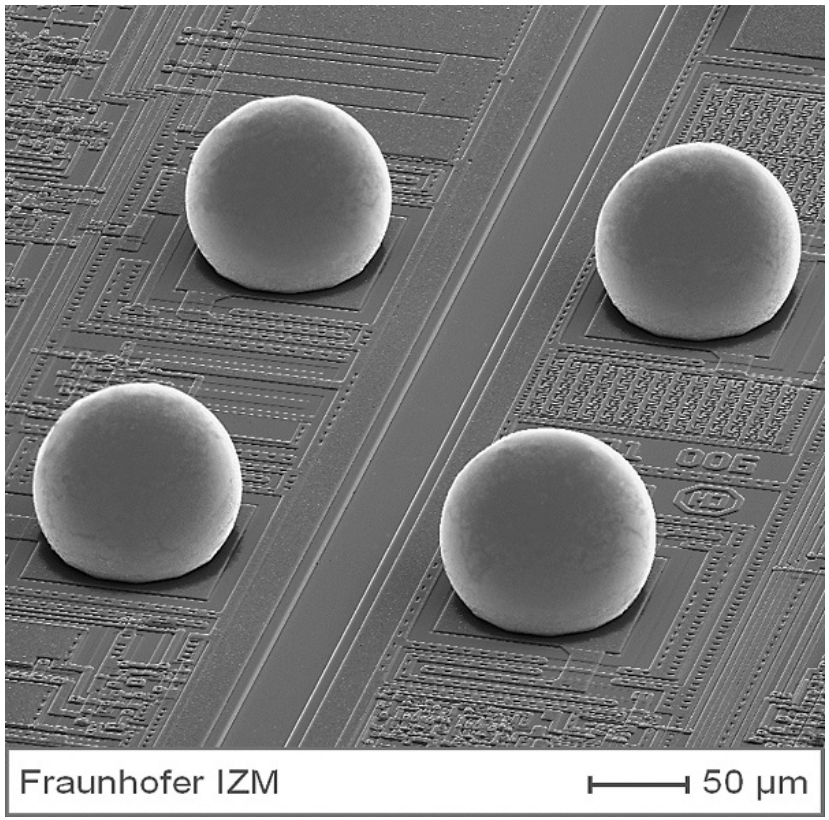
Minimize the L

- Make wires short
- Use power and ground planes
  - Think of power plane as a very wide wire

$$L \approx l\left(\frac{\mu_0 \mu_r h}{w}\right)$$

Flip Chip, Area IO



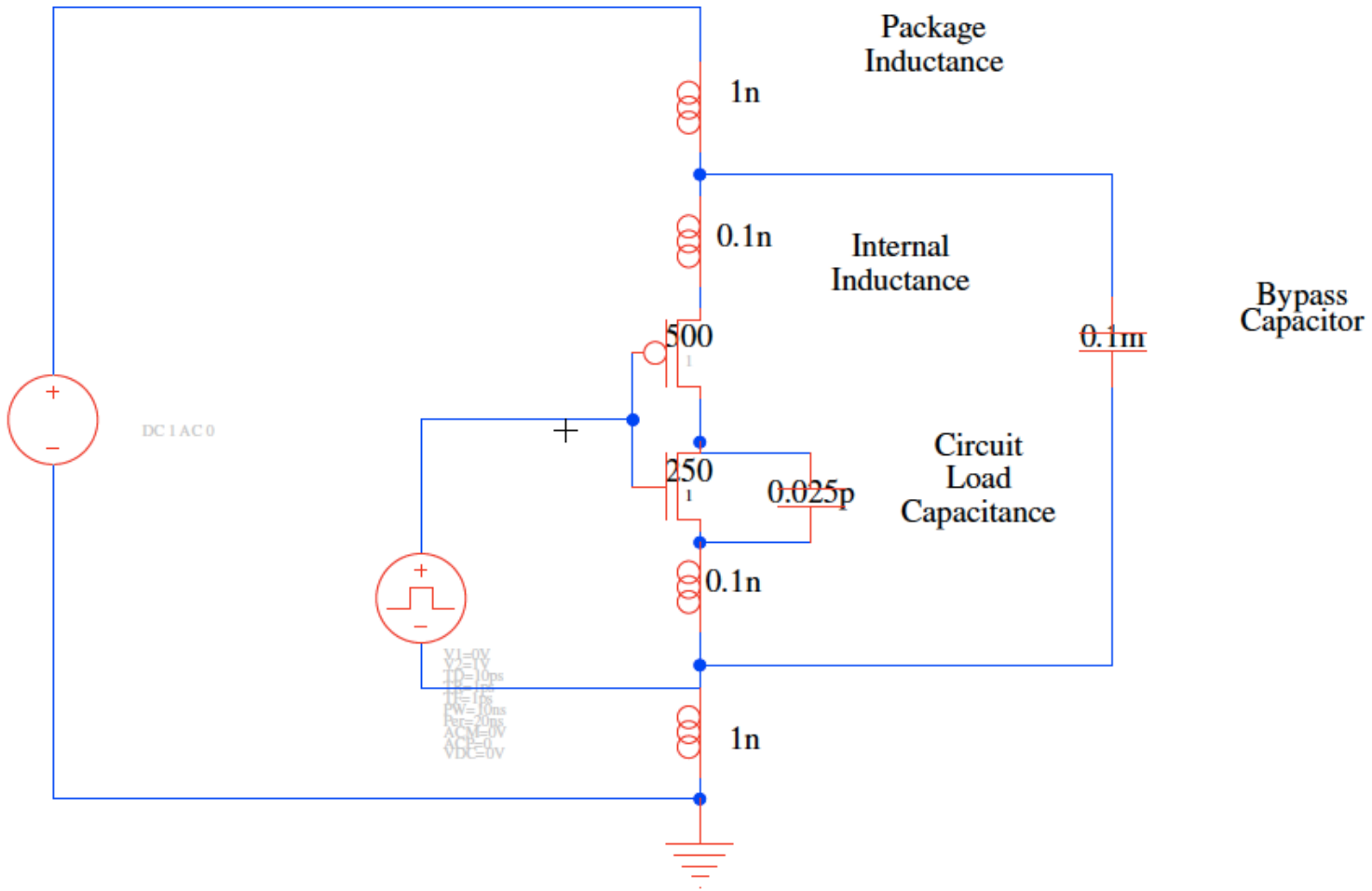


http://www.izm.fraunhofer.de/en/abteilungen/high_density_interconnectwaferlevelpackaging/arbeitsgebiete/arbeitsgebiet1.

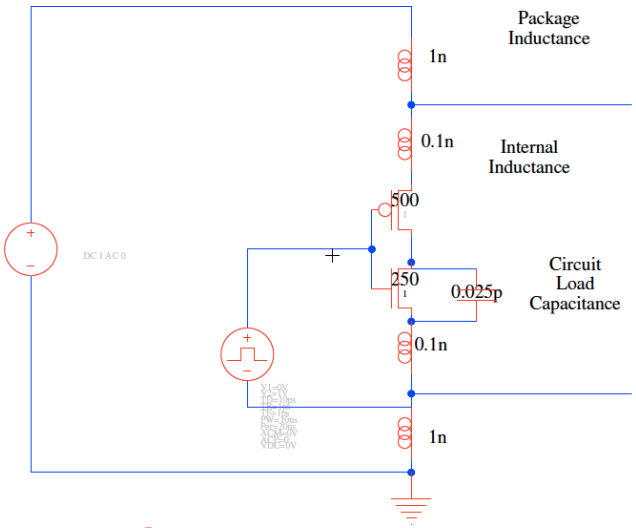
Add Good C's

- Bypass Capacitors – inside the inductances
  - On board
  - On package
  - On chip

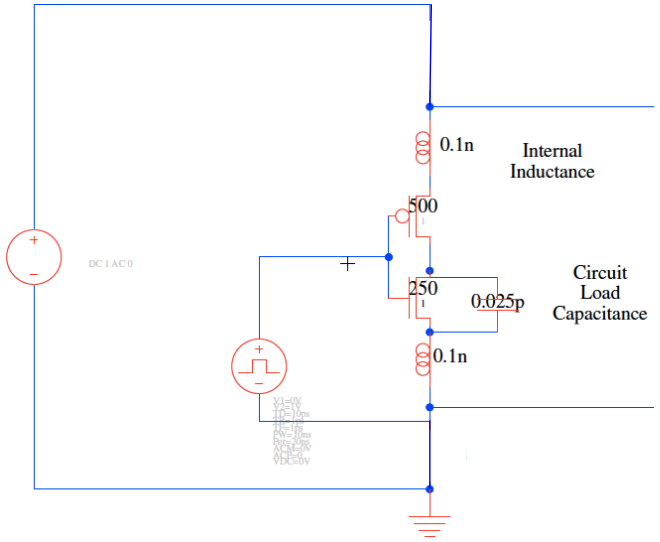
Bypass Capacitor Example



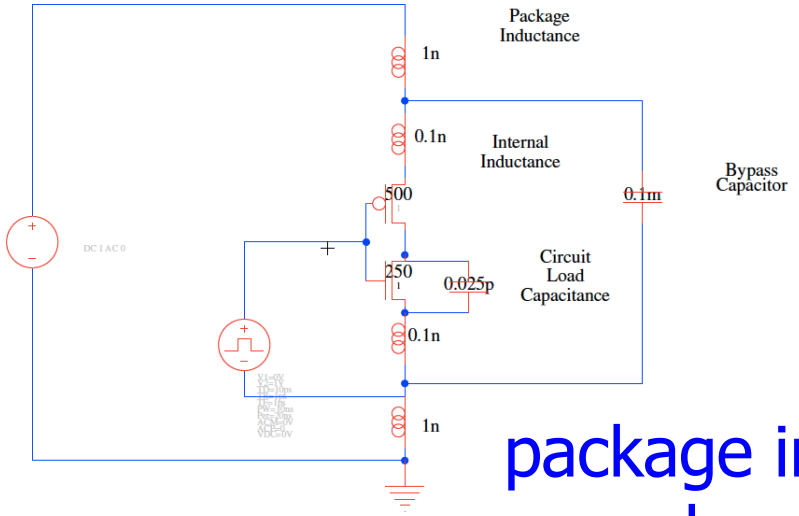
Bypass Capacitor Example



No bypass cap

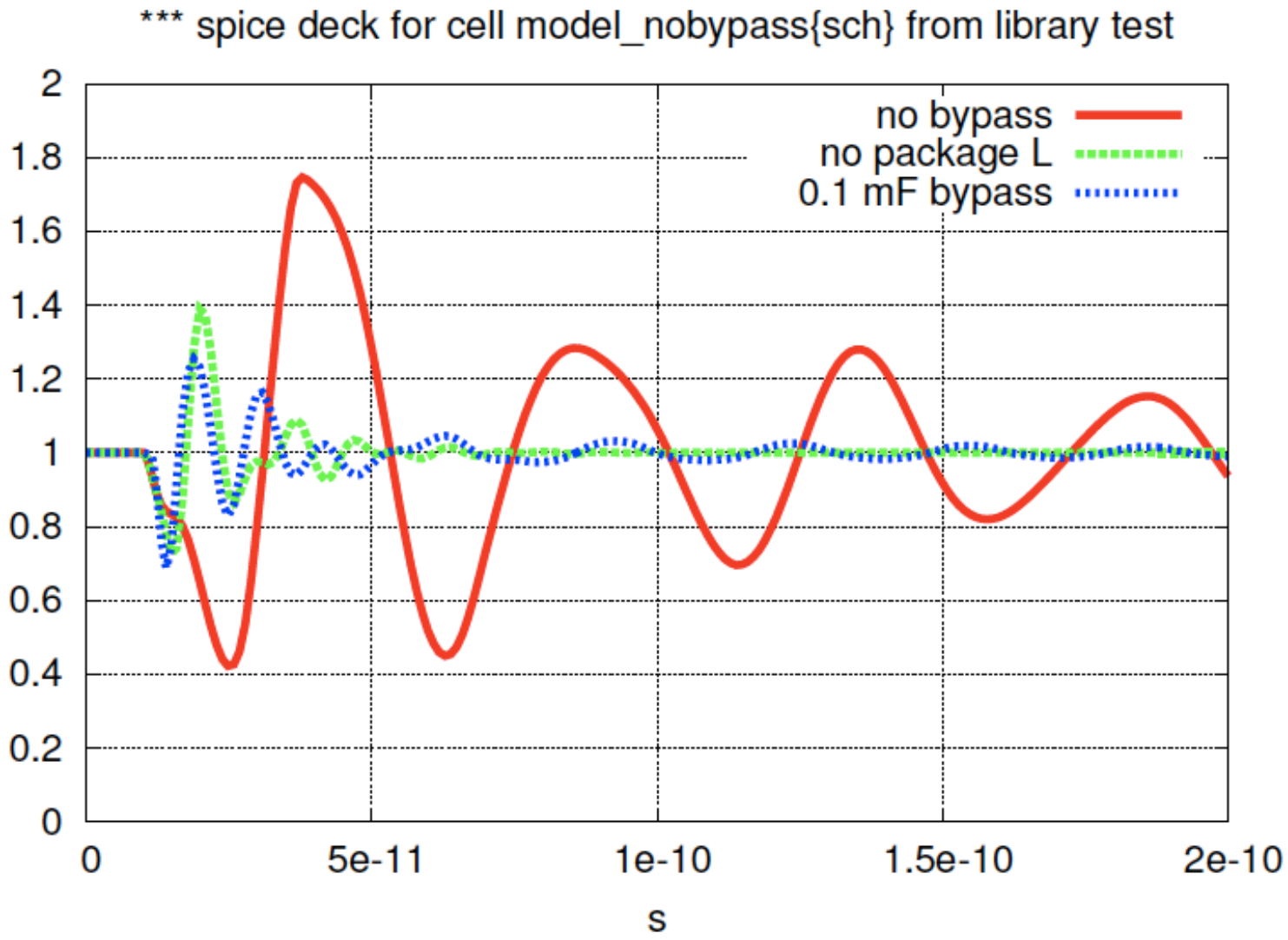


No package inductance

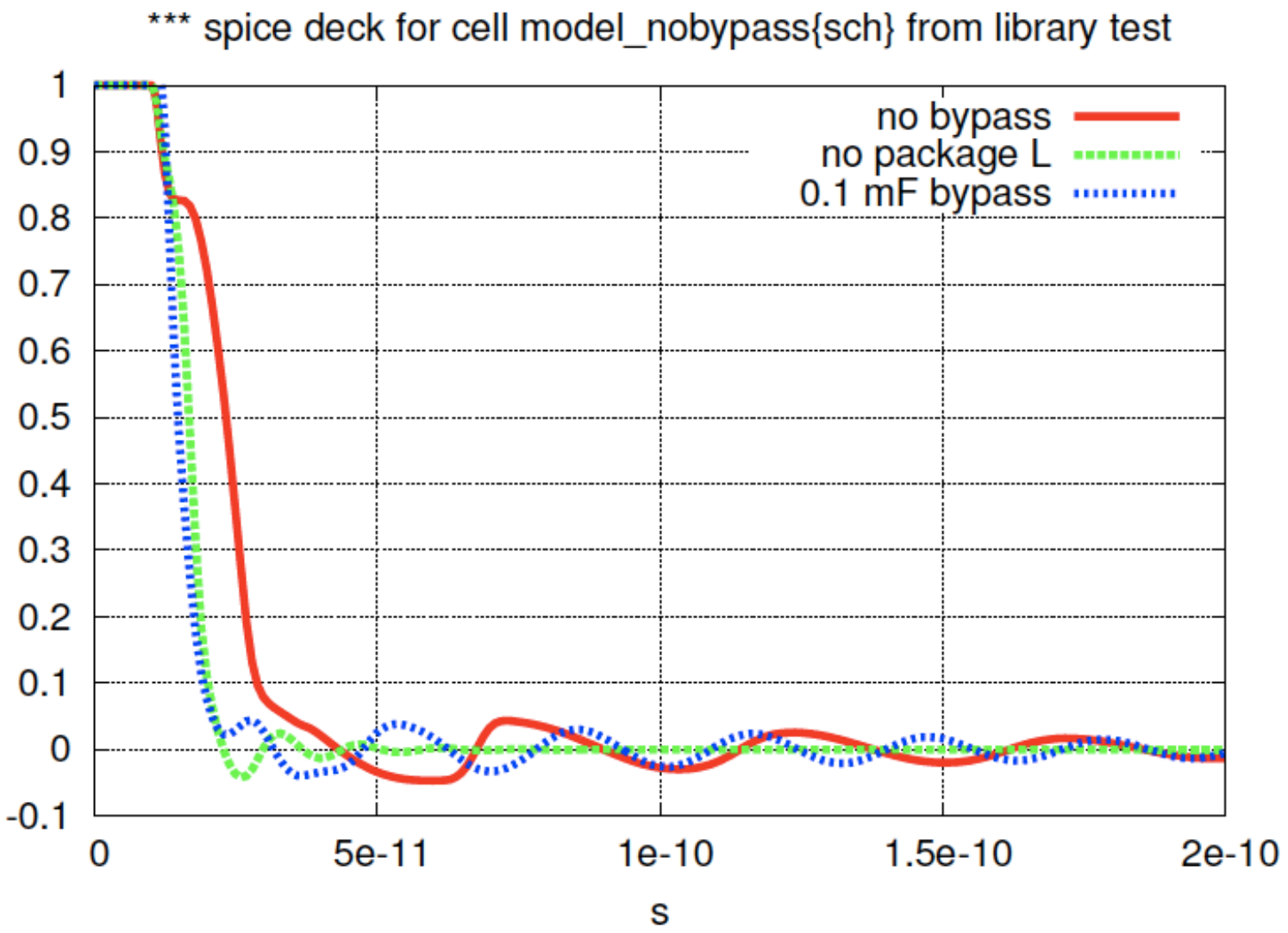


package inductance w/ bypass cap

Bypassed Supplies (@ transistor)



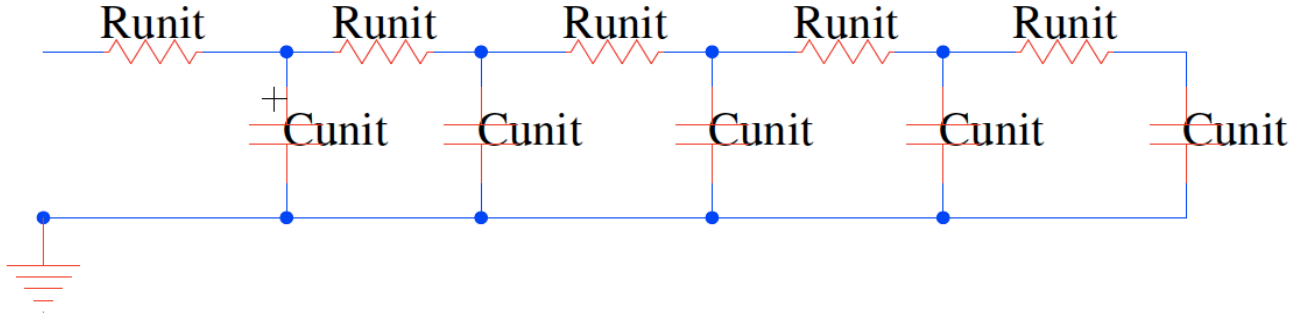
Bypassed Output



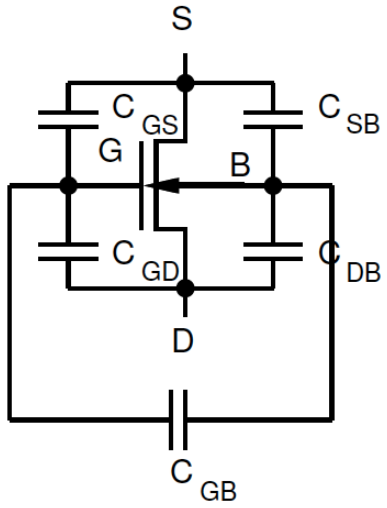
Crosstalk

Capacitance

- There are capacitors everywhere
- We already talked about
  - Wires modeled as a distributed RC network



  - Parasitic capacitances between terminals on transistor



Capacitance Everywhere

- Potentially a capacitor between any two conductors
  - On the chip
  - On the package
  - On the board
- All wires
  - Package pins
  - PCB traces (what you did in lab)
  - Cable wires
  - Bit/word lines

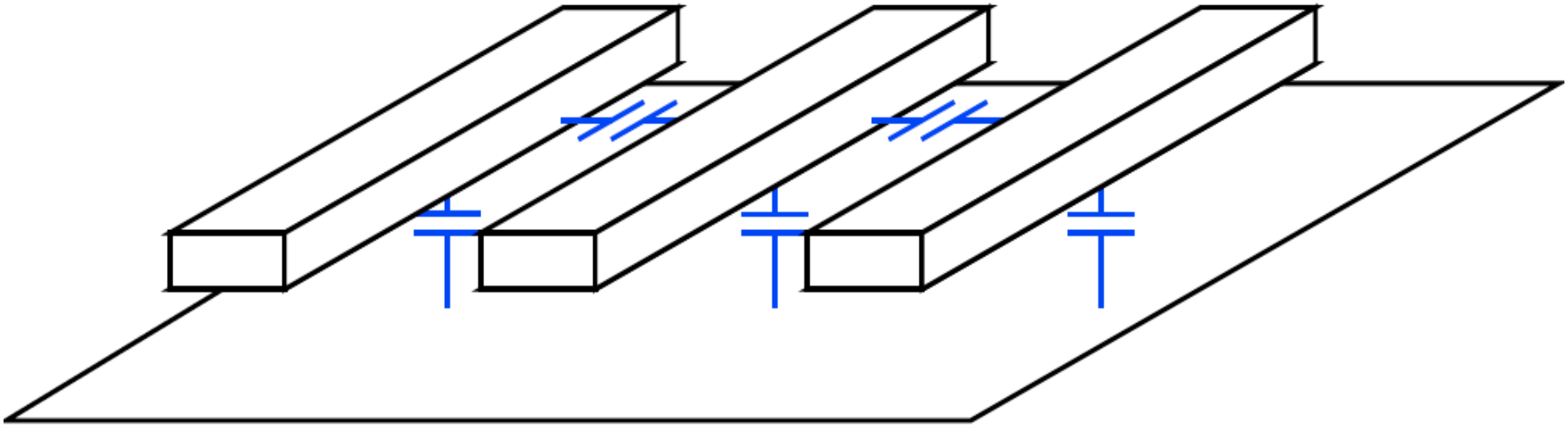
Capacitance…

- …decreases with conductor separation
- …increases with size
- …depends on dielectric

$$C = \varepsilon_r \varepsilon_0 \frac{A}{d}$$

Wire Capacitance

- Changes in voltage on one wire may couple through parasitic capacitance to an adjacent wire



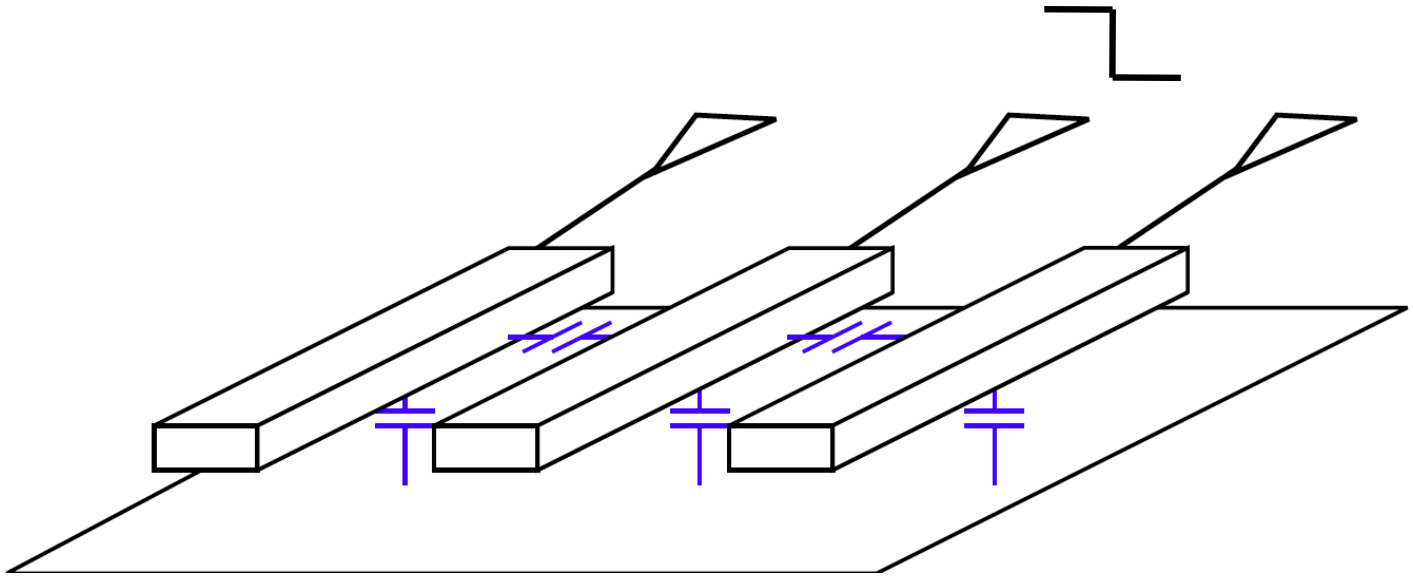
Crosstalk

- A wire has high capacitance to its neighbor.
  - When the neighbor switches from 1-> 0 or 0->1, the wire tends to switch too.
  - Called capacitive *coupling* or *crosstalk*.
- Crosstalk effects
  - Noise on non-switching wires
  - Increased delay on switching wires

Qualitative

Undriven Wire

- What happens to undriven wire?
- Where do we have undriven wires?



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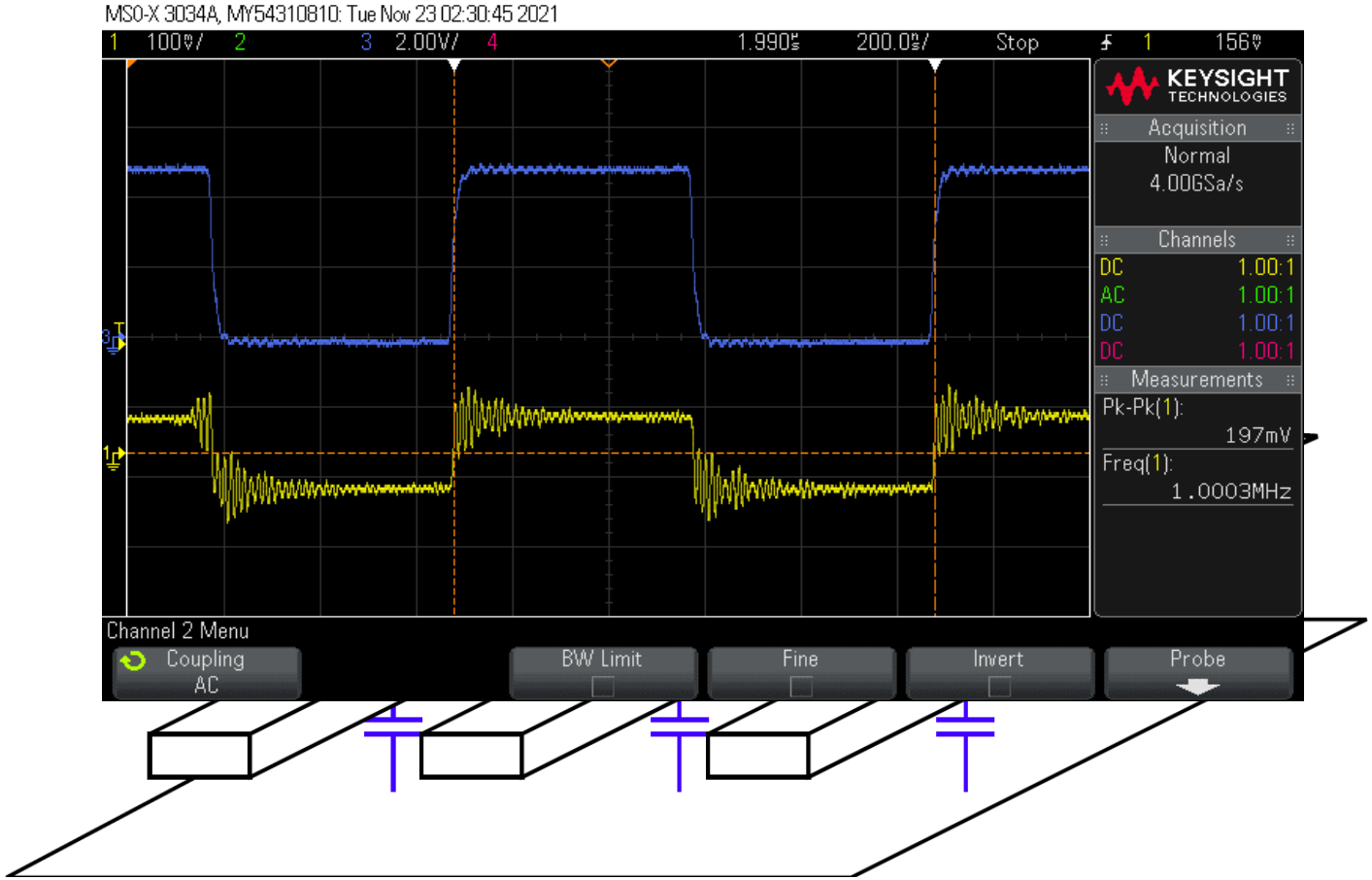
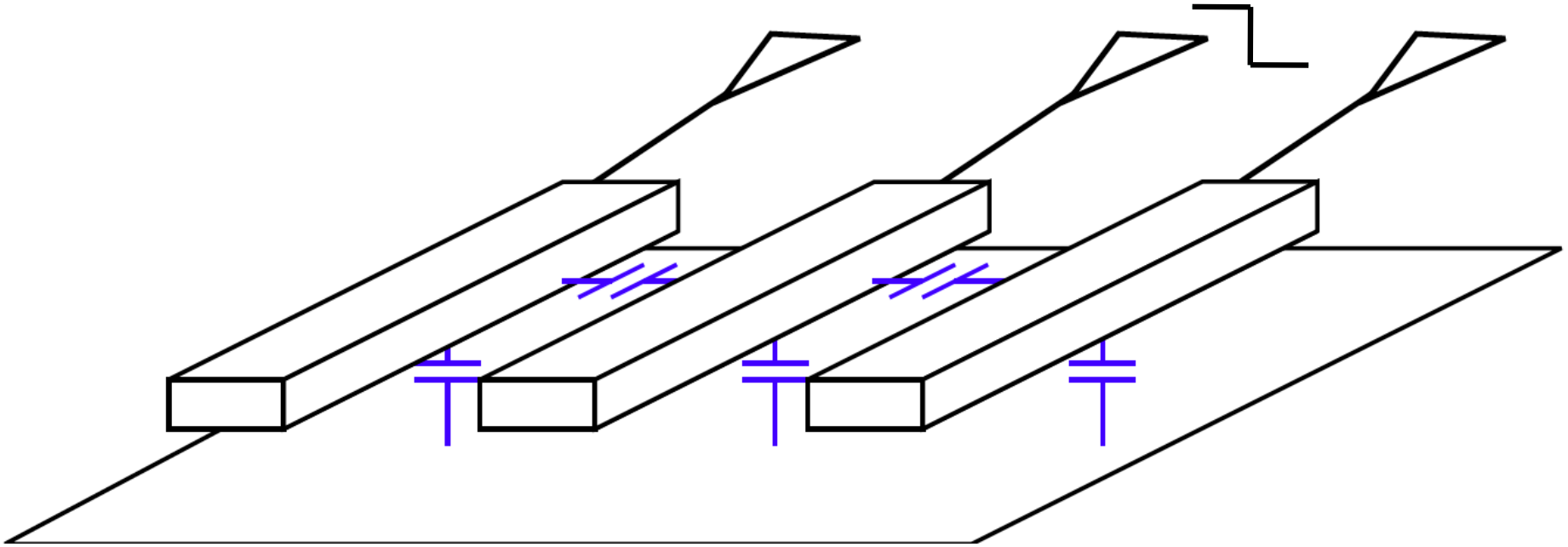


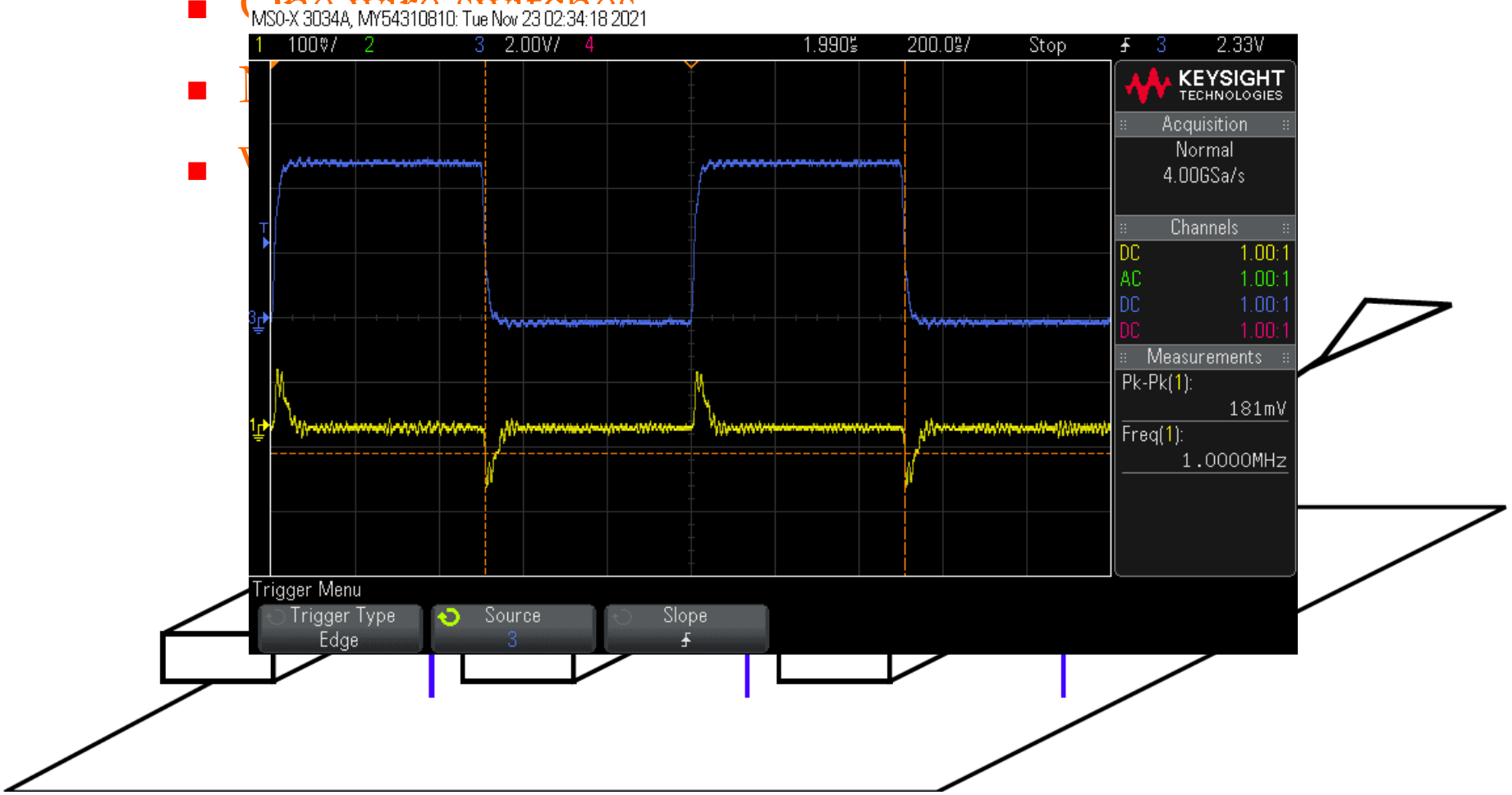
Driven Wire

- What happens to a driven "neighbor" wire?
  - One wire switches
  - Neighbors driven but not switch
  - What happens to neighbors?



Driven Wire

- What happens to a driven "neighbor" wire?
  - One wire switches
  - I
  - V



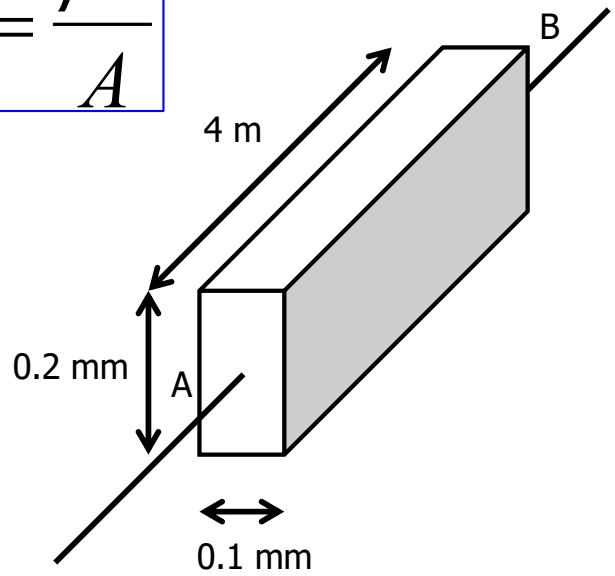
Clocked Logic

- CMOS driven lines
- Clocked logic
  - Willing to wait to settle/evaluate
- Impact is on delay
  - May increase delay of transitions

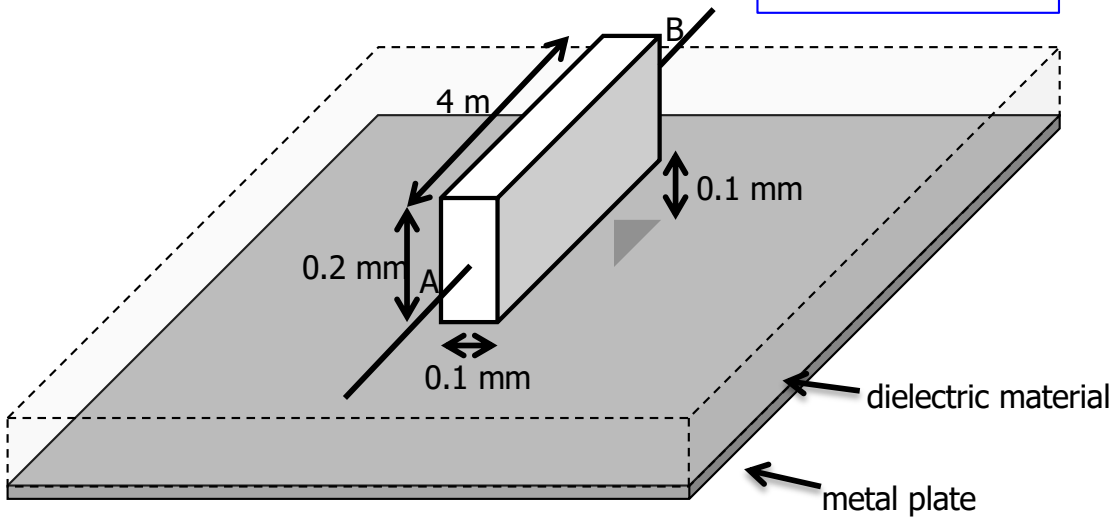
Quantitative

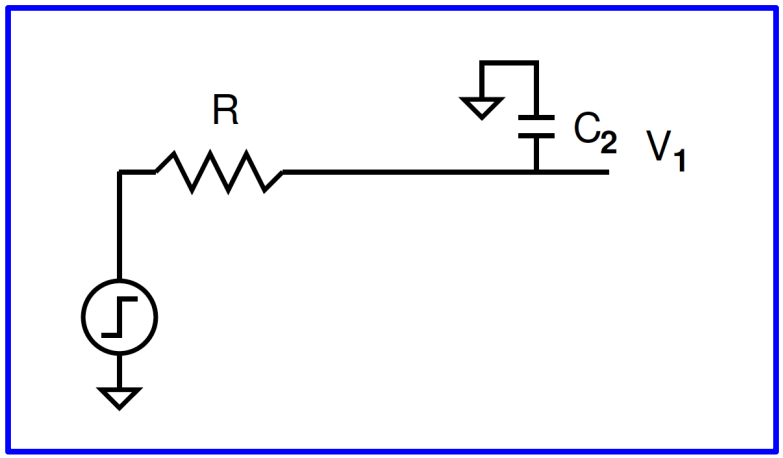
Isolated Wire RC

$$R = \frac{\rho L}{A}$$



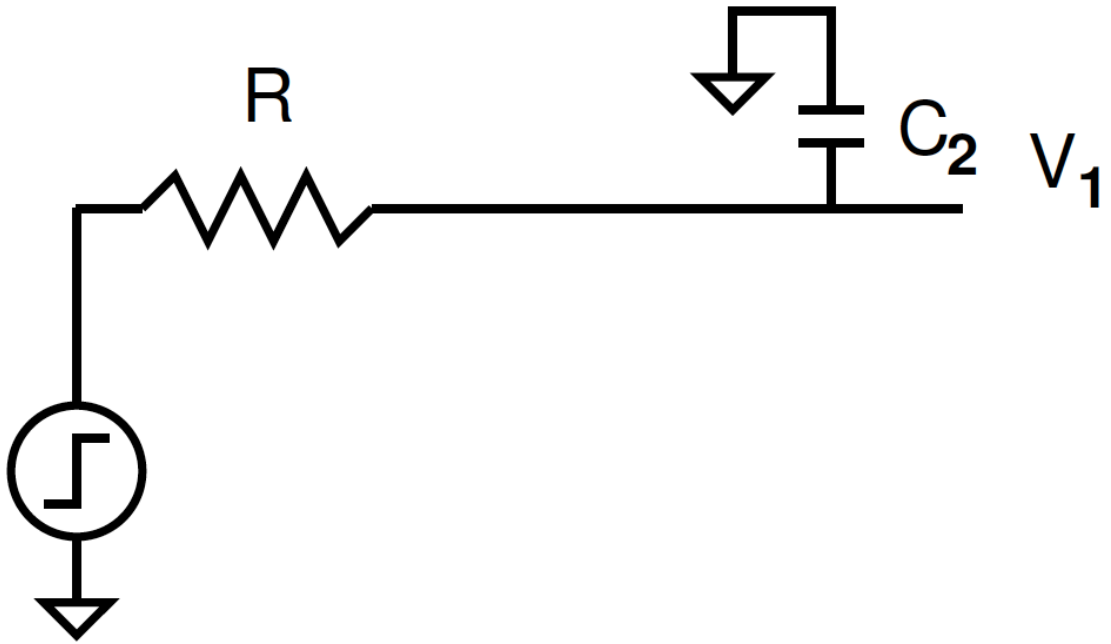
$$C = \varepsilon_d \frac{A}{d}$$





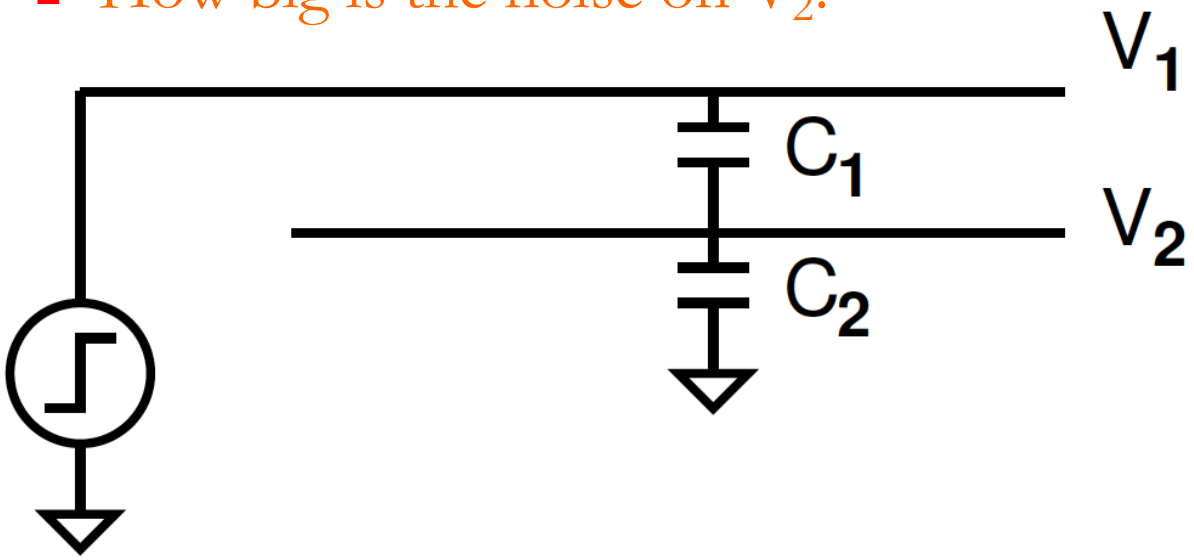
Wire step response (preclass 4)

- Step response for isolated wire?



Undriven Adjacent Wire (preclass 5)

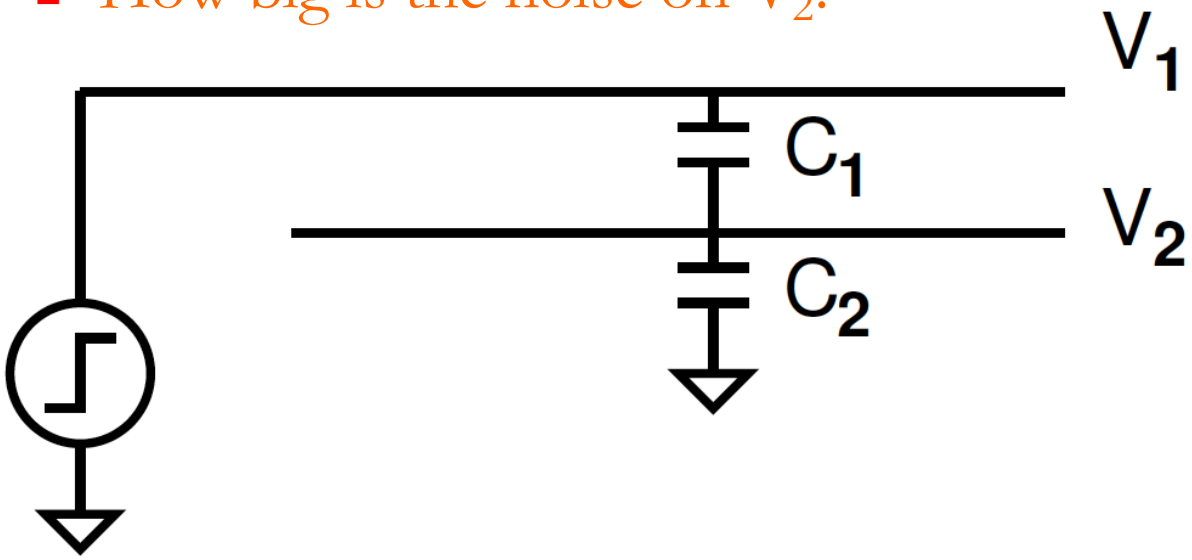
- V_1 transitions from 0 to V
  - How big is the noise on V_2?



Undriven Adjacent Wire

- V_1 transitions from 0 to V
  - How big is the noise on V_2?

$$I(t) = C\frac{dV(t)}{dt}$$



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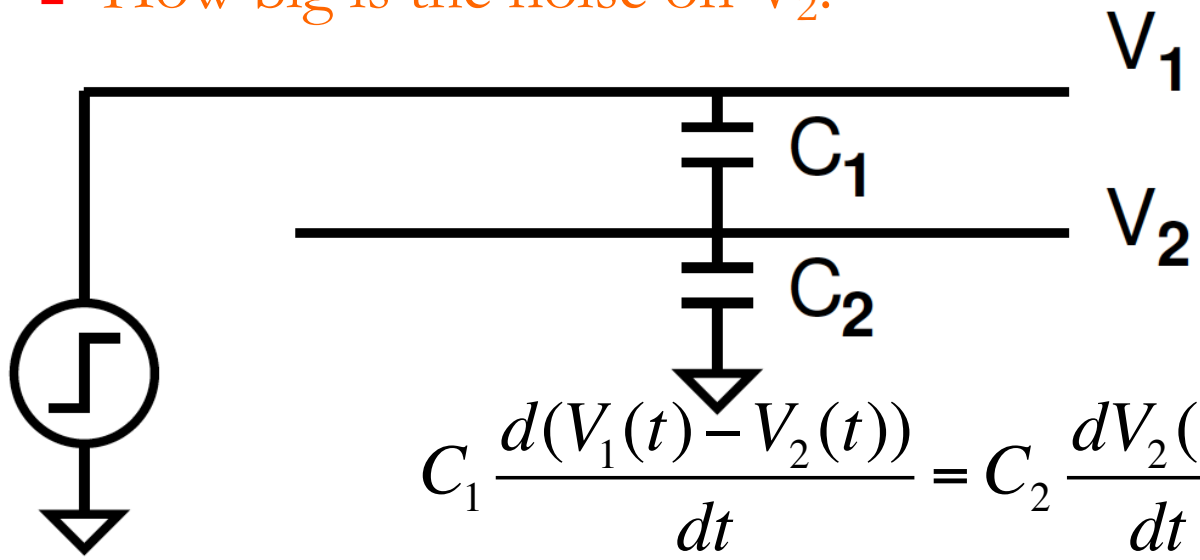

$$C_1\frac{d(V_1(t)-V_2(t))}{dt} = C_2\frac{dV_2(t)}{dt}$$

Undriven Adjacent Wire

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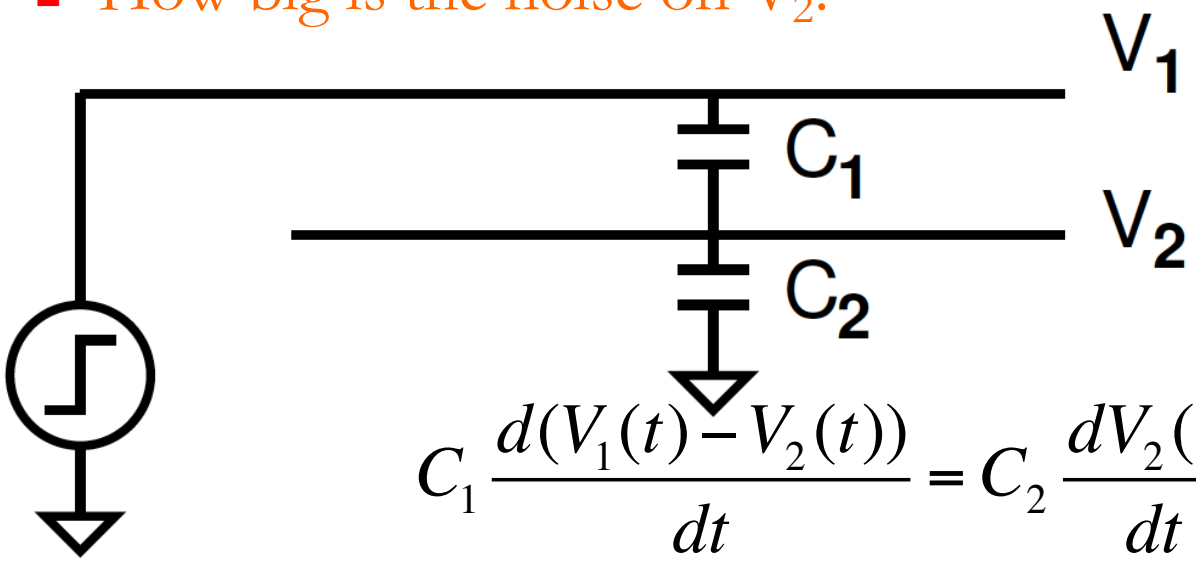
  - How big is the noise on V_2?

$$I(t) = C\frac{dV(t)}{dt}$$



$$C_1\frac{d(V_1(t)-V_2(t))}{dt} = C_2\frac{dV_2(t)}{dt}$$

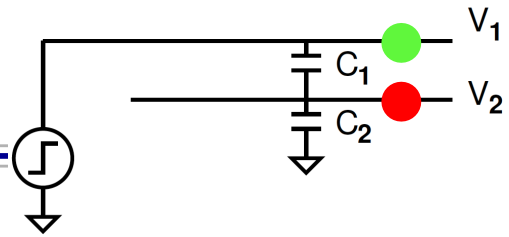
$$C_1\frac{dV_1(t)}{dt} = (C_1+C_2)\frac{dV_2(t)}{dt}$$

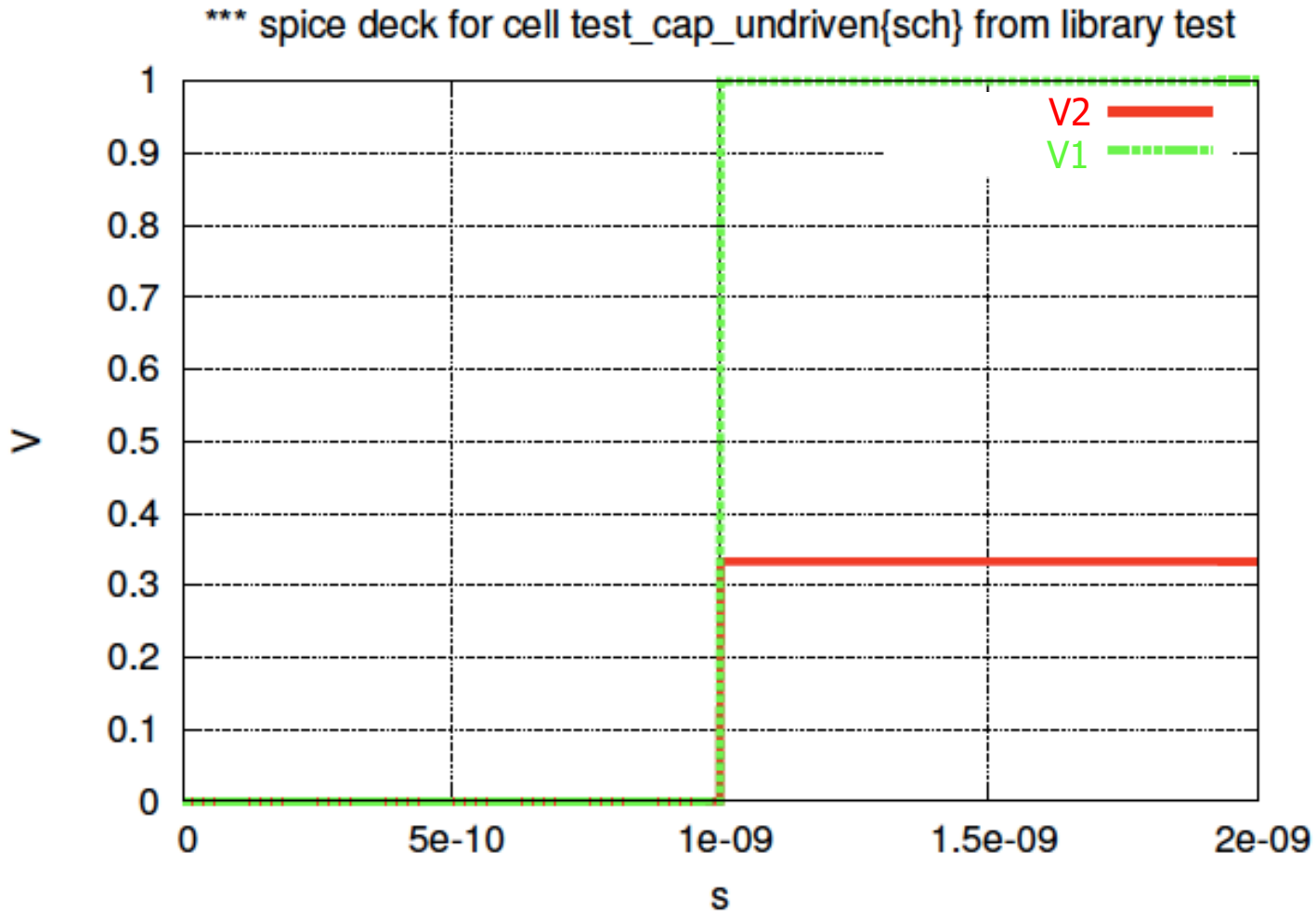
$$C_1V_1(t) = (C_1+C_2)V_2(t)$$

$$V_2(t) = \frac{C_1}{C_1+C_2}V_1(t)$$

$C_1 = 10pF$
$C_2 = 20pF$

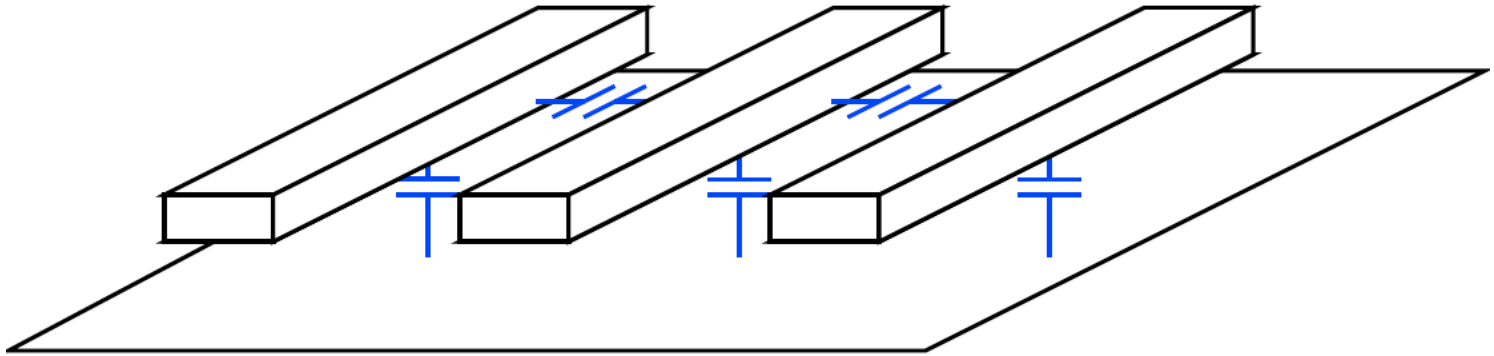
SPICE C_1=10pF, C_2=20pF





Good (?) Capacitance

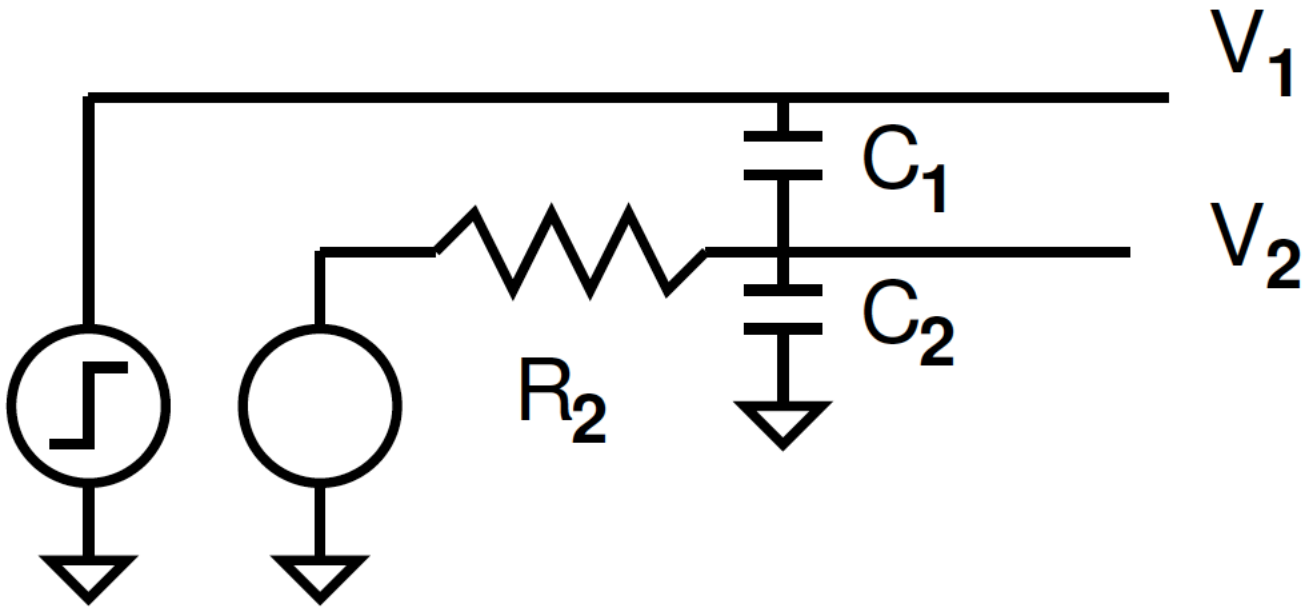
- High capacitance to ground plane (C_2)
  - Limits node swing from adjacent conductors



$$V_2 = \left(\frac{C_1}{C_1 + C_2} \right) V_1$$

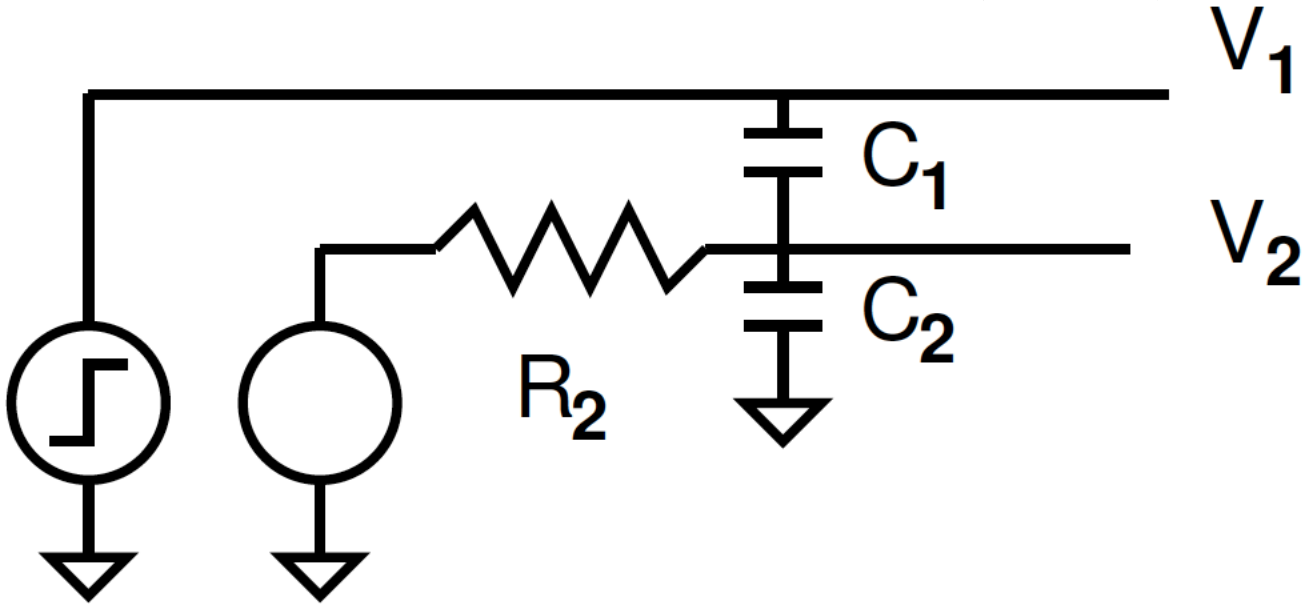
Driven Adjacent Wire (preclass 5)

- What happens when neighbor line is driven?

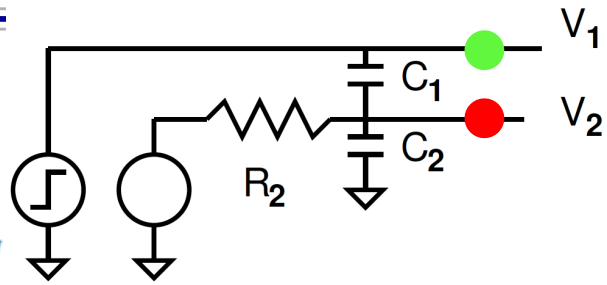


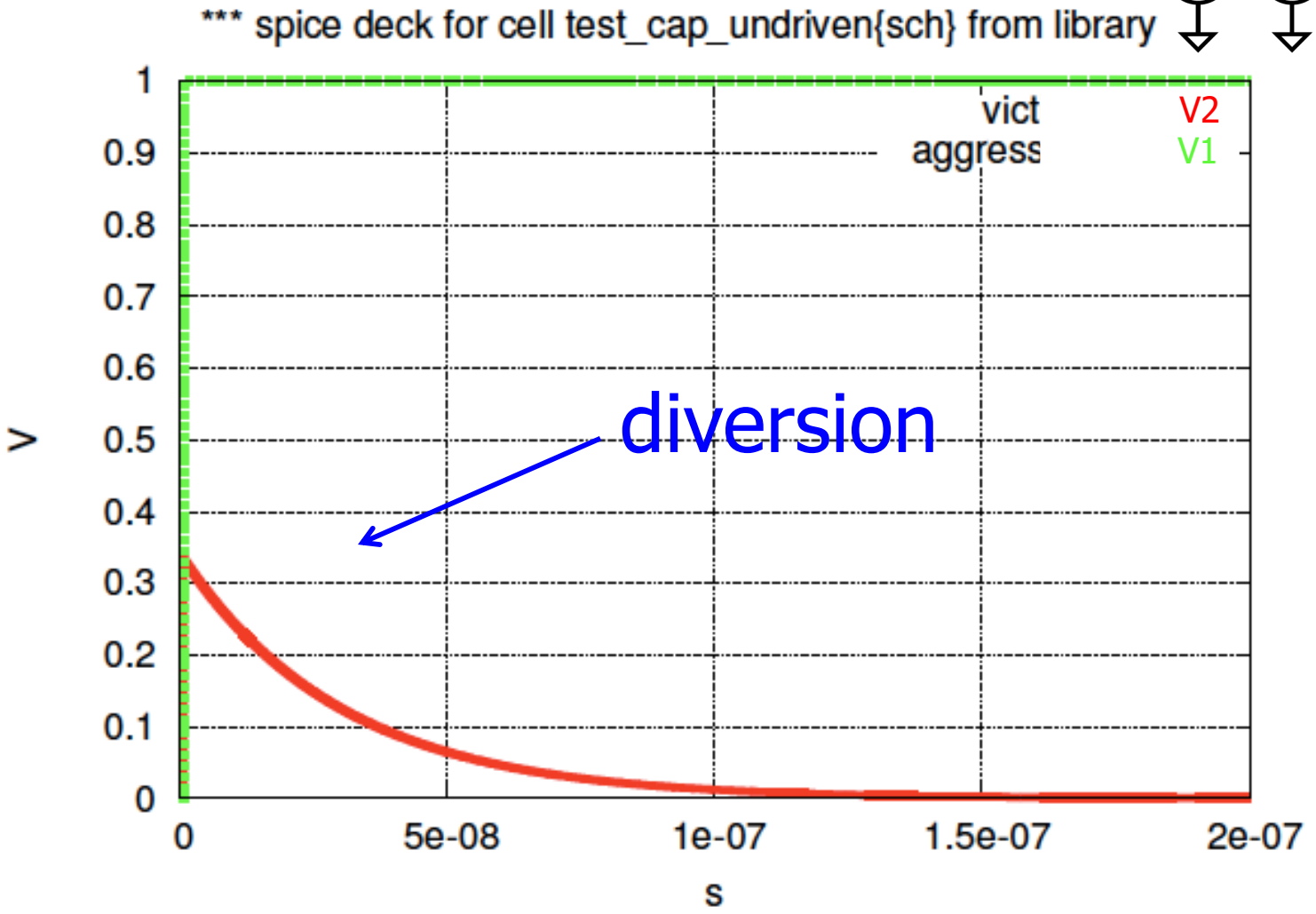
Driven Adjacent Wire

- What happens when neighbor line is driven?
  - Recovers with time constant: $R_2(C_1+C_2)$



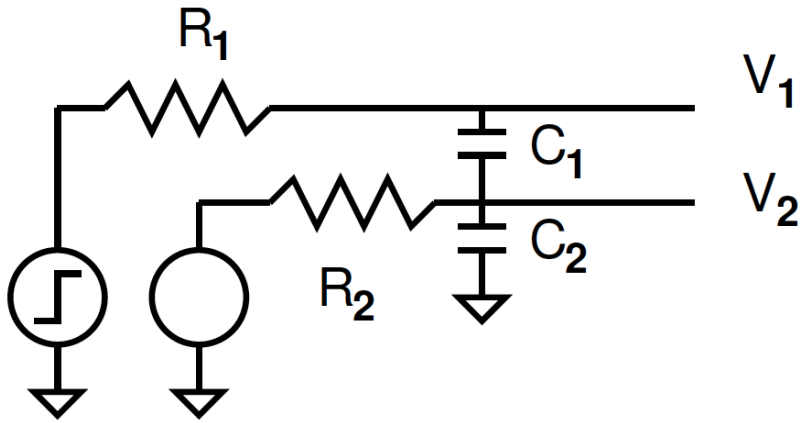
Spice: R_2=1K, C_1=10pF, C_2=20pF





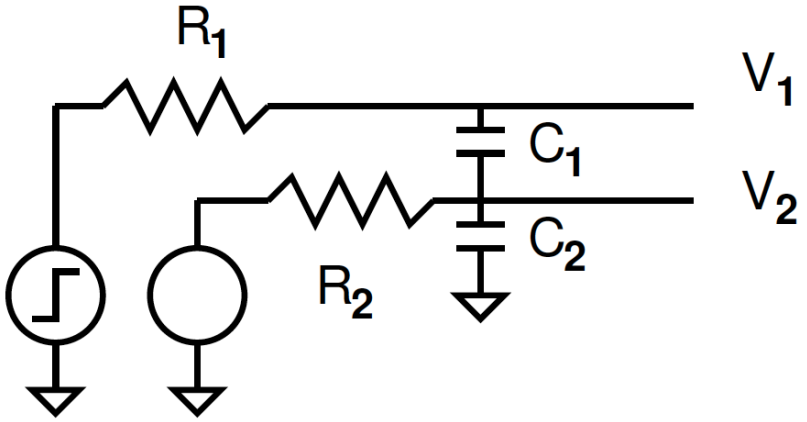
Magnitude of Noise on Driven Line (preclass 6)

- Magnitude of diversion depends on relative time constants
  - $\tau_1 << \tau_2$
  - $\tau_1 >> \tau_2$
  - $\tau_1 \sim = \tau_2$

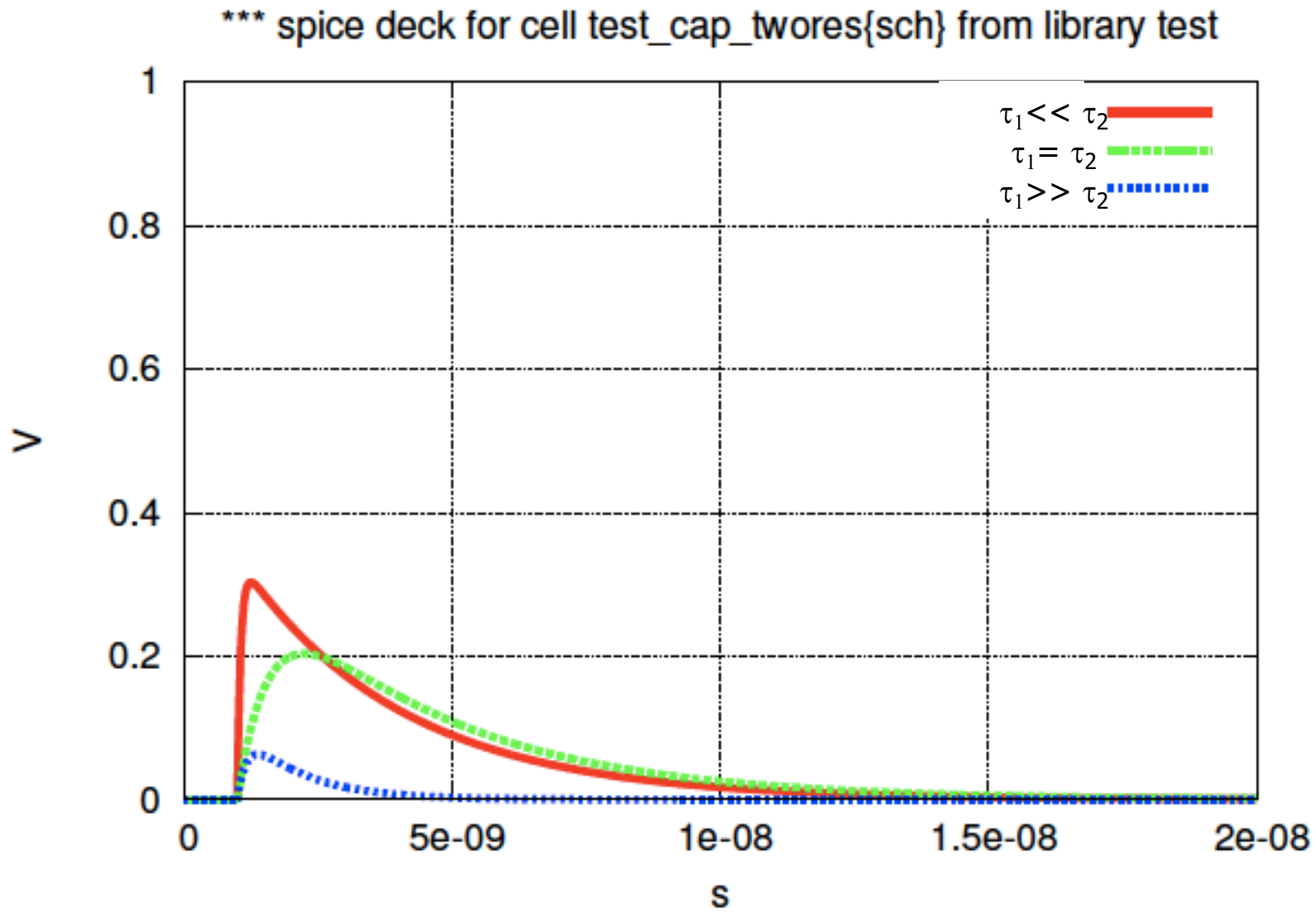


Magnitude of Noise on Driven Line

- Magnitude of diversion depends on relative time constants
  - $\tau_1 << \tau_2$
    - full diversion, then recover
  - $\tau_1 >> \tau_2$
    - Drive capacitor (C_2) faster than line 1 can change
      - little noise
  - $\tau_1 \sim= \tau_2$
    - Somewhere in between

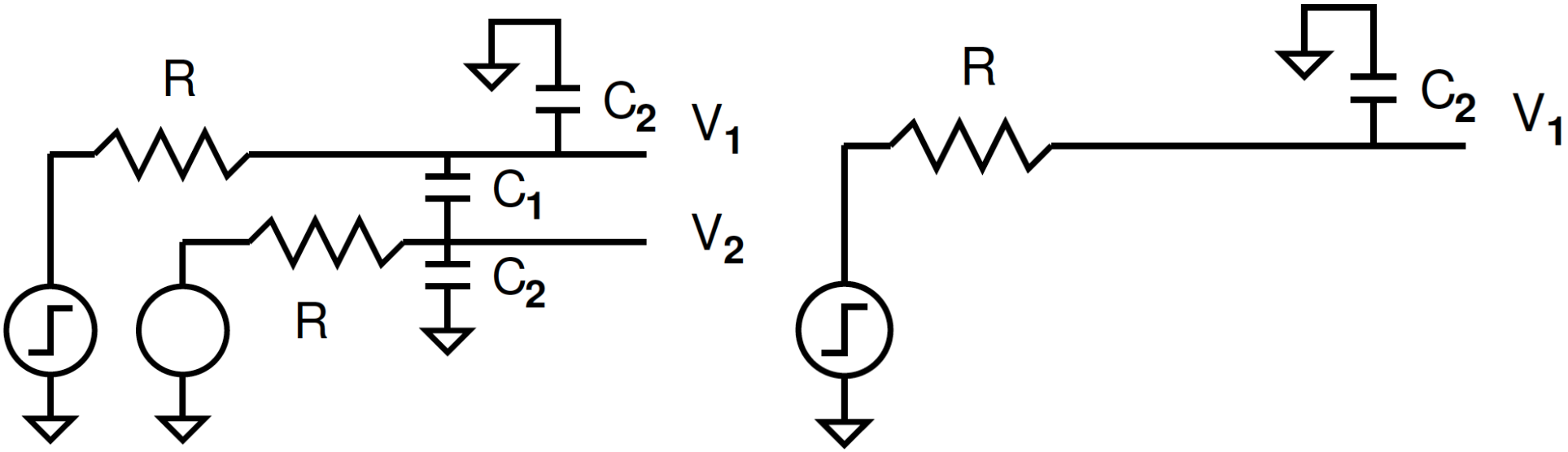


Spice: C_1=1pF, C_2=2pF



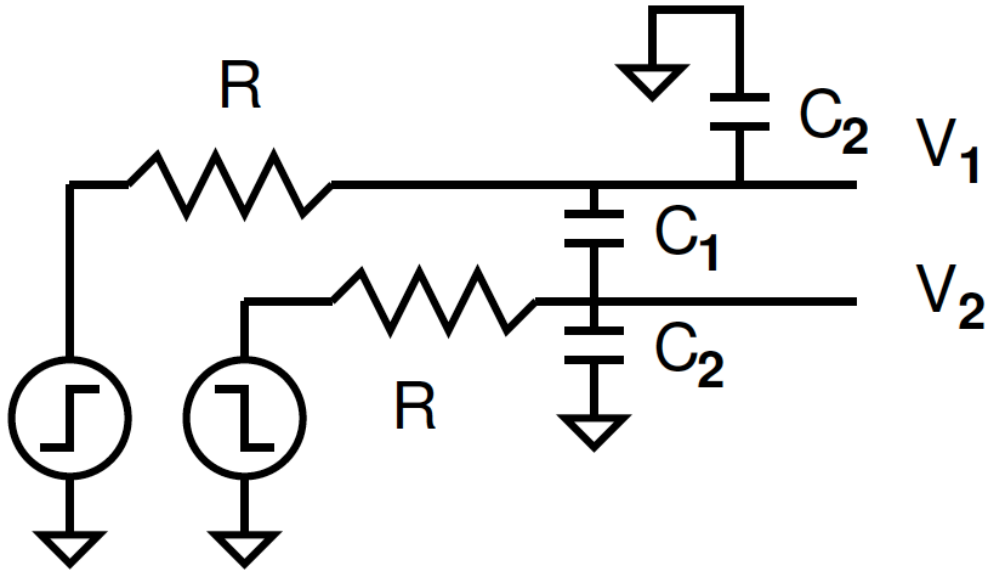
Switching Line with Finite Drive

- What impact does the presence of the neighbour line have on the **switching** line?
  - All previous questions were about noise on non-switching wire
  - Finite drive (R)



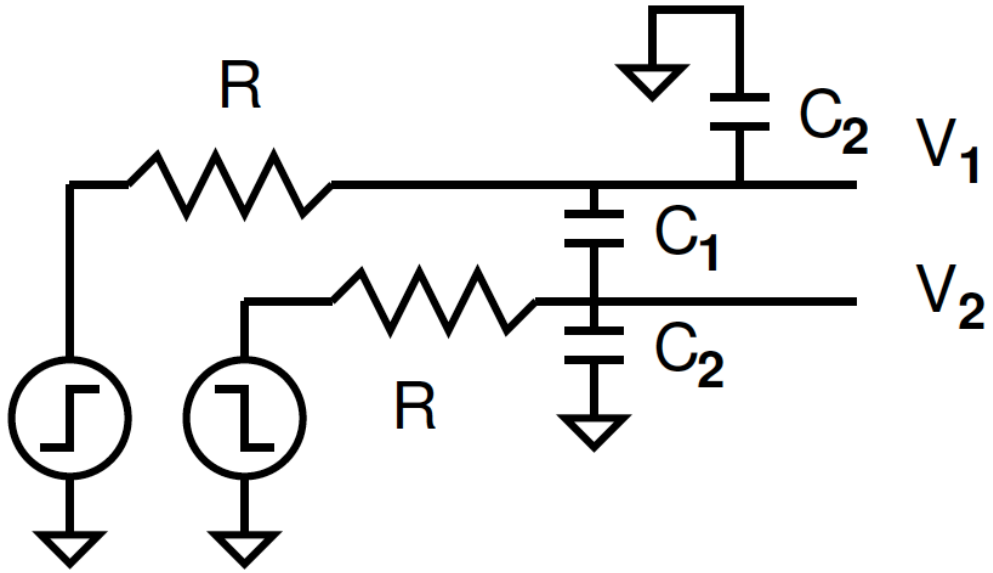
Simultaneous Transition

- What happens if lines transition in opposite directions?



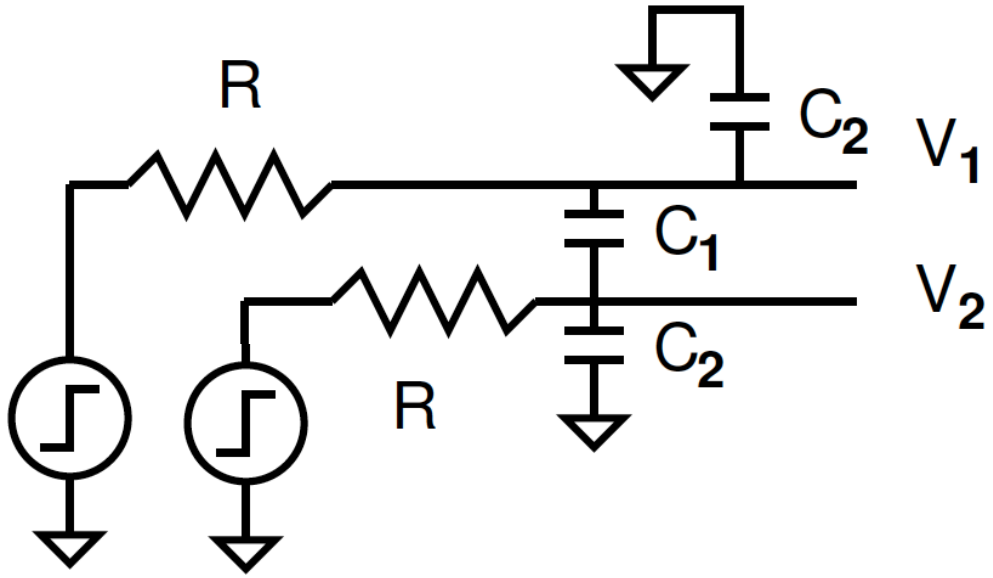
Simultaneous Transition

- What happens if lines transition in opposite directions?
  - Must charge C_1 by 2V
  - Or looks like $2C_1$ between wires



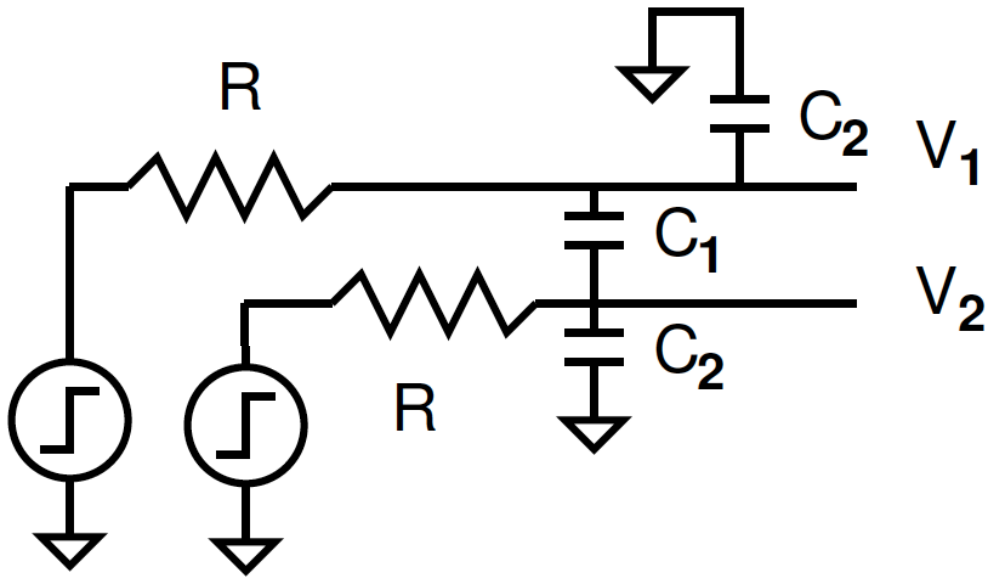
Simultaneous Transition

- What happens if lines transition in same direction?



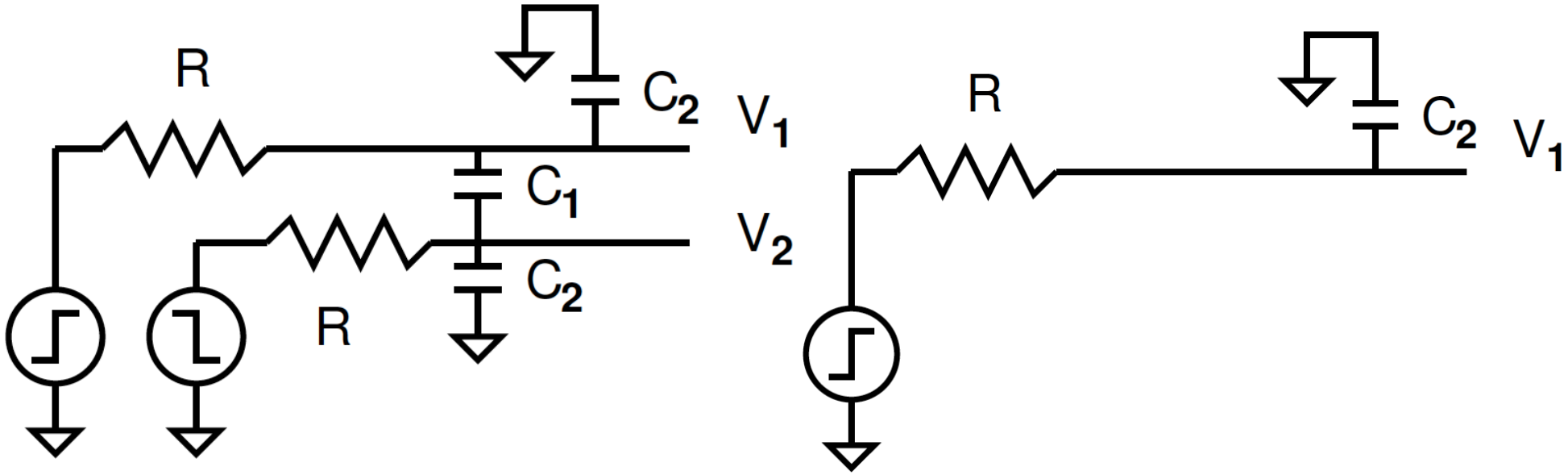
Simultaneous Transition

- What happens if lines transition in same direction?
  - Looks like no coupling capacitor!

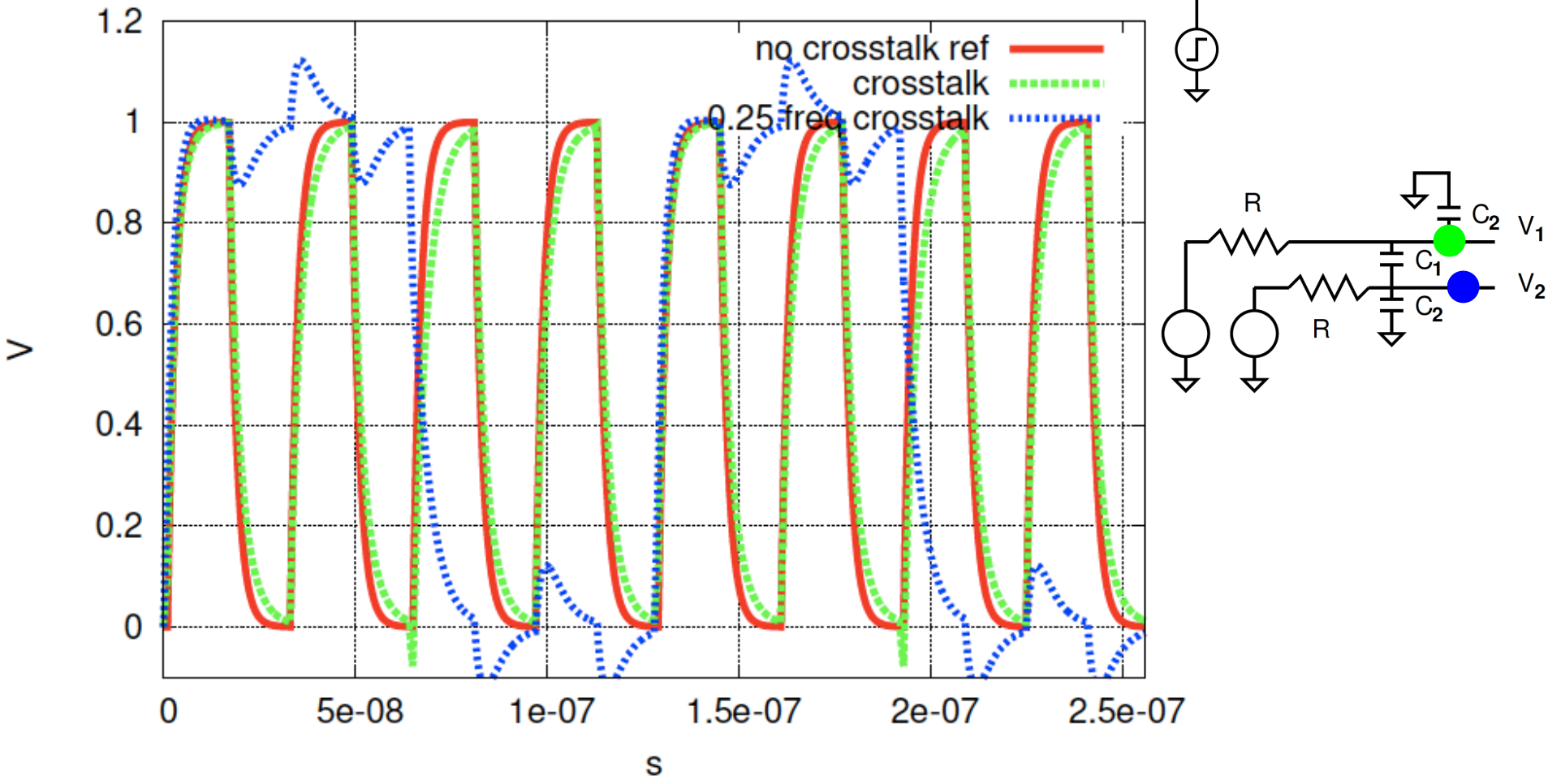


Simulation

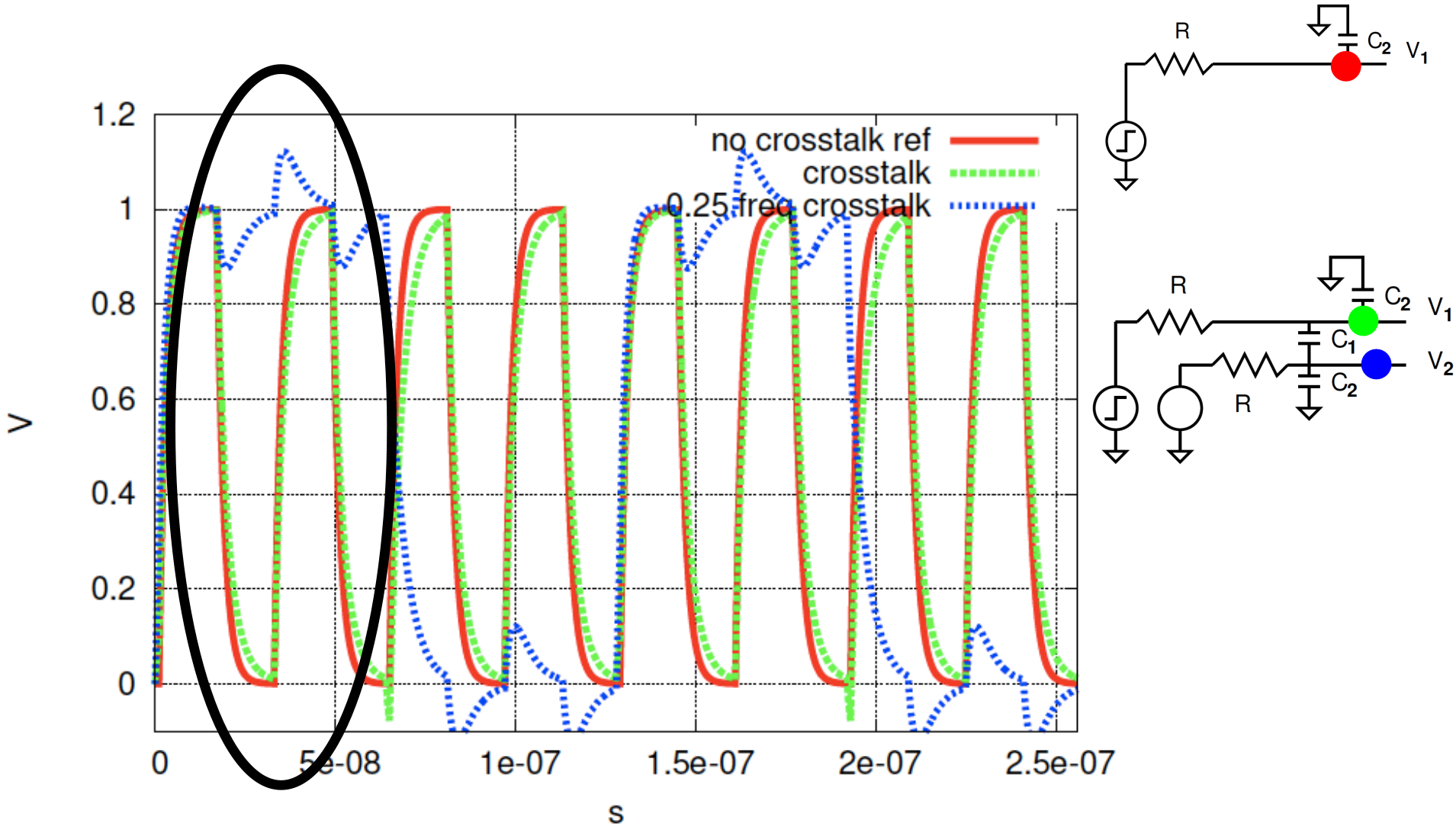
- V_2 switching at ¼ frequency of V_1
- No crosstalk reference case where no V_2



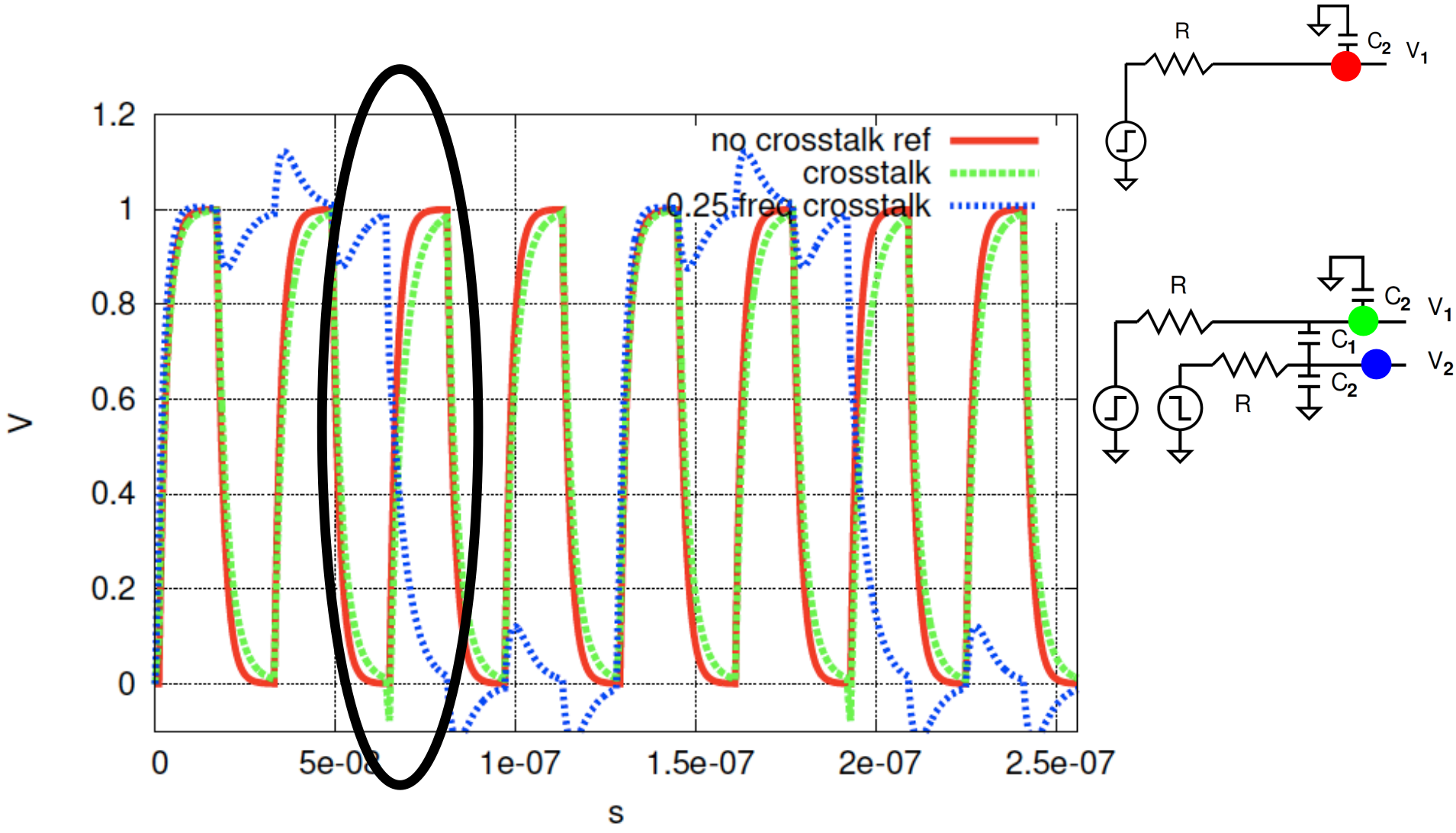
Crosstalk Neighbor Simulations



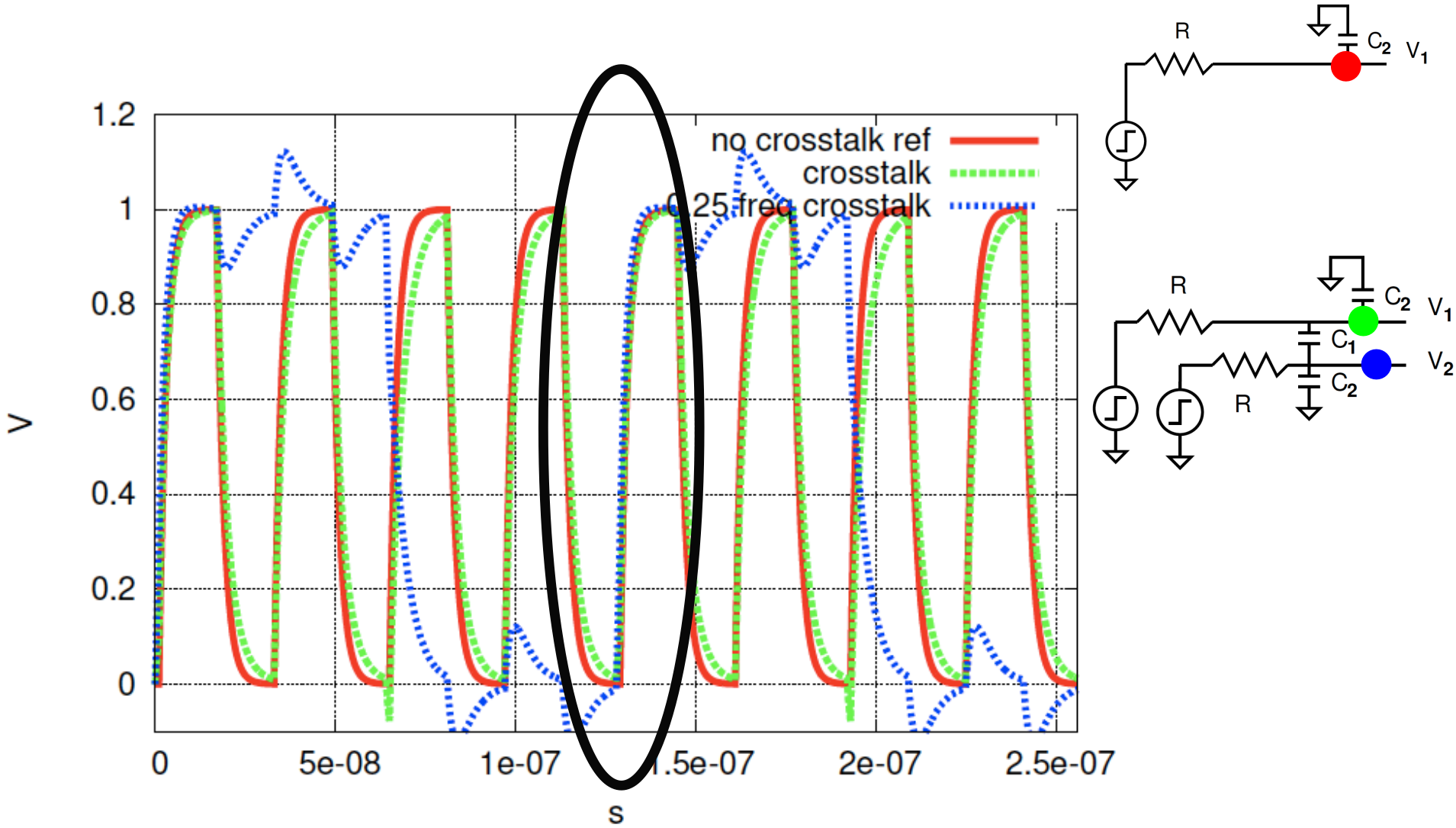
Crosstalk Neighbor Simulations



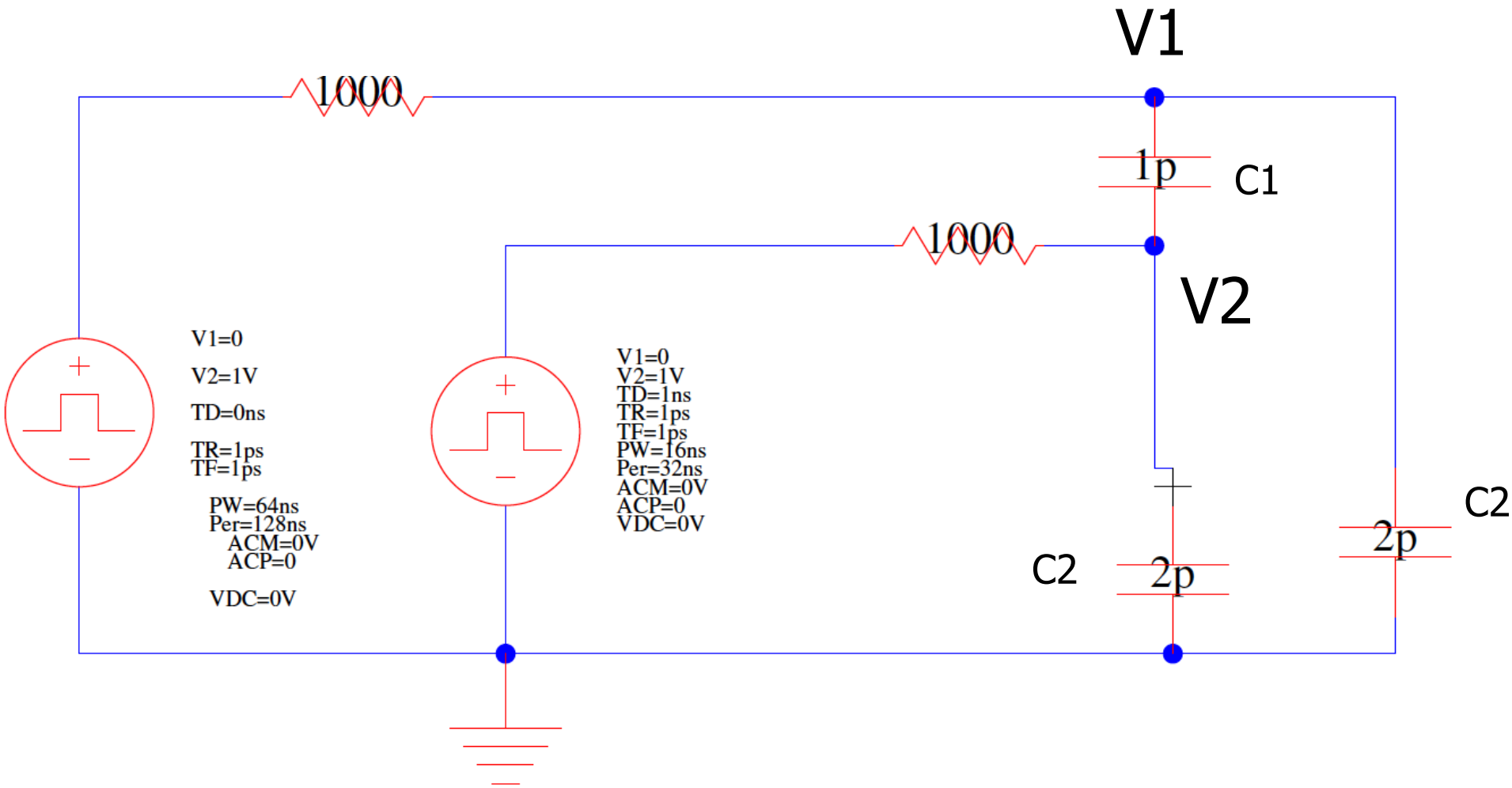
Crosstalk Neighbor Simulations



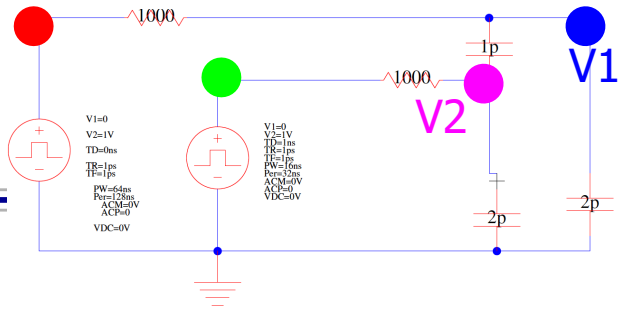
Crosstalk Neighbor Simulations

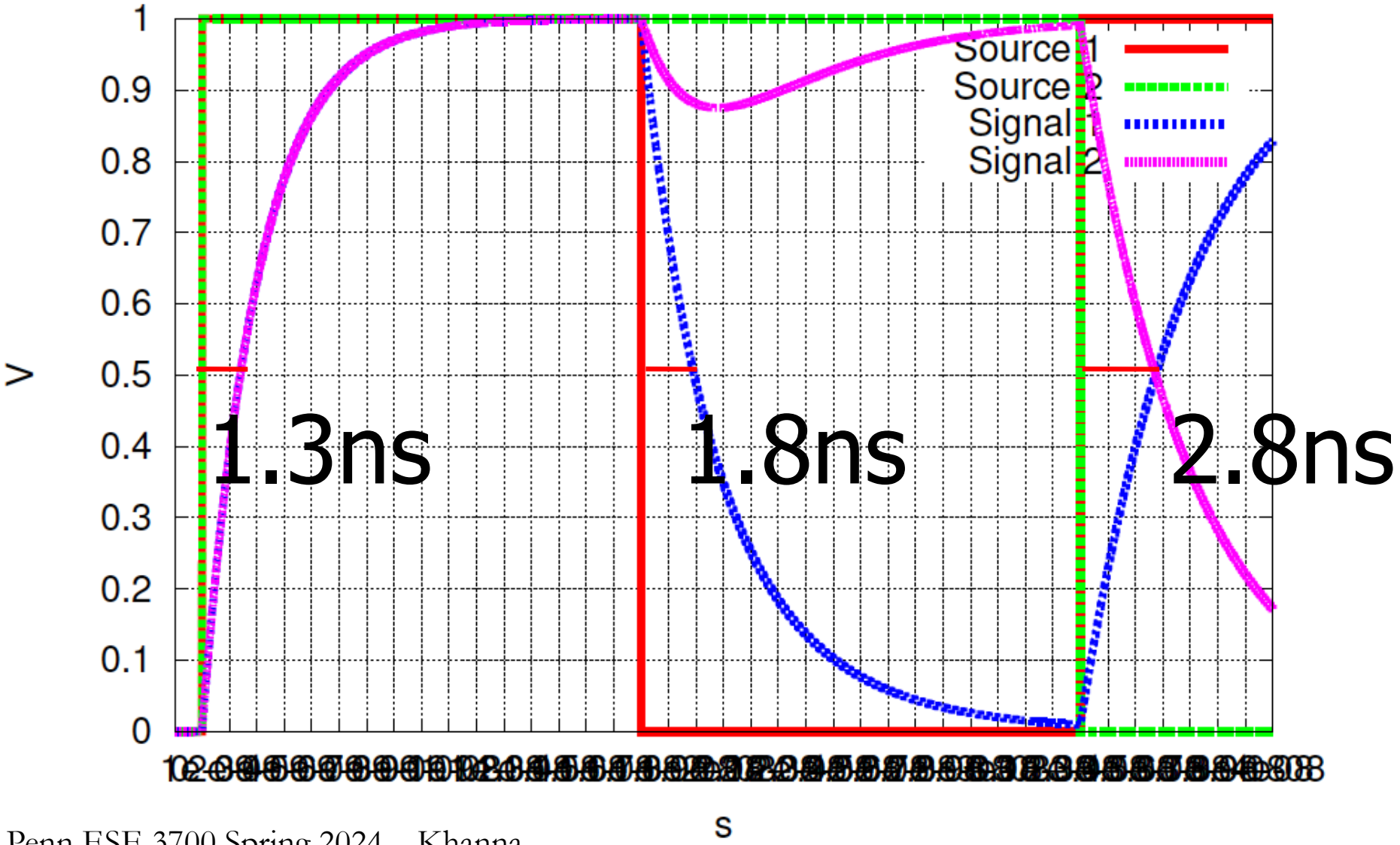


Simulation Setup



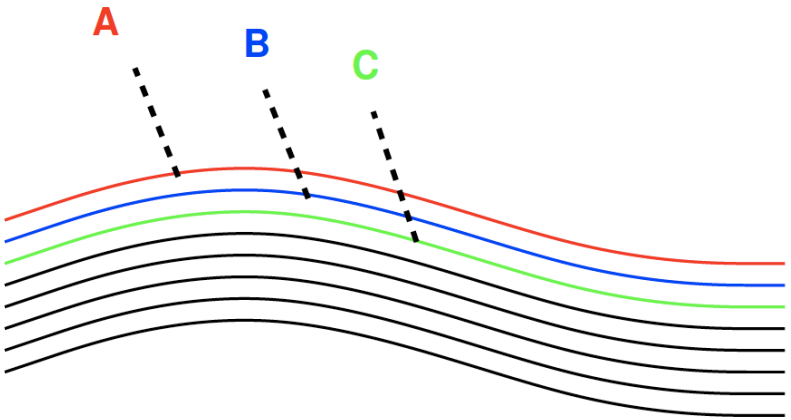
Crosstalk Simulation

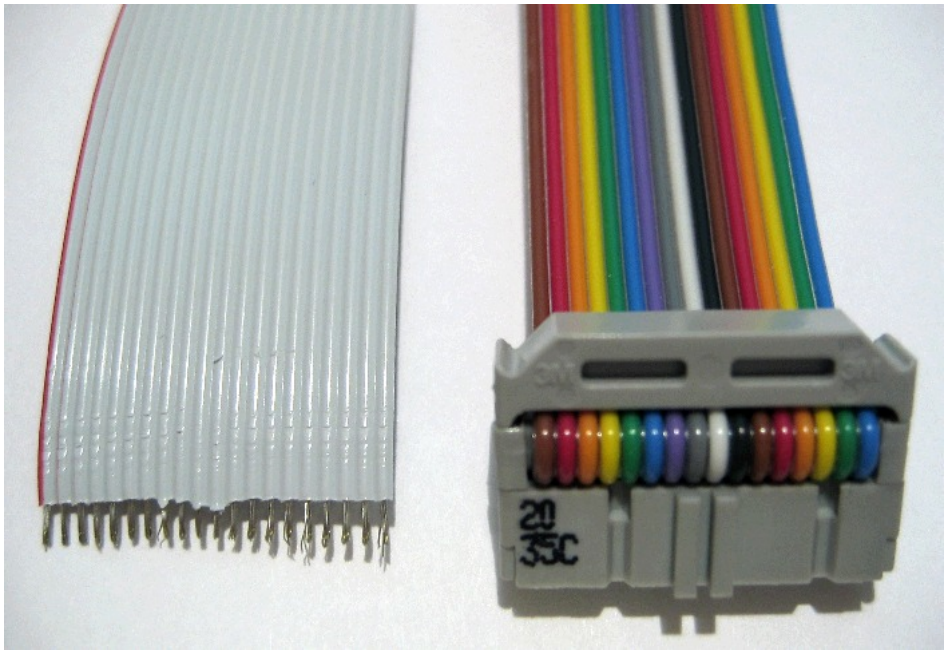




Where Does it Arise?

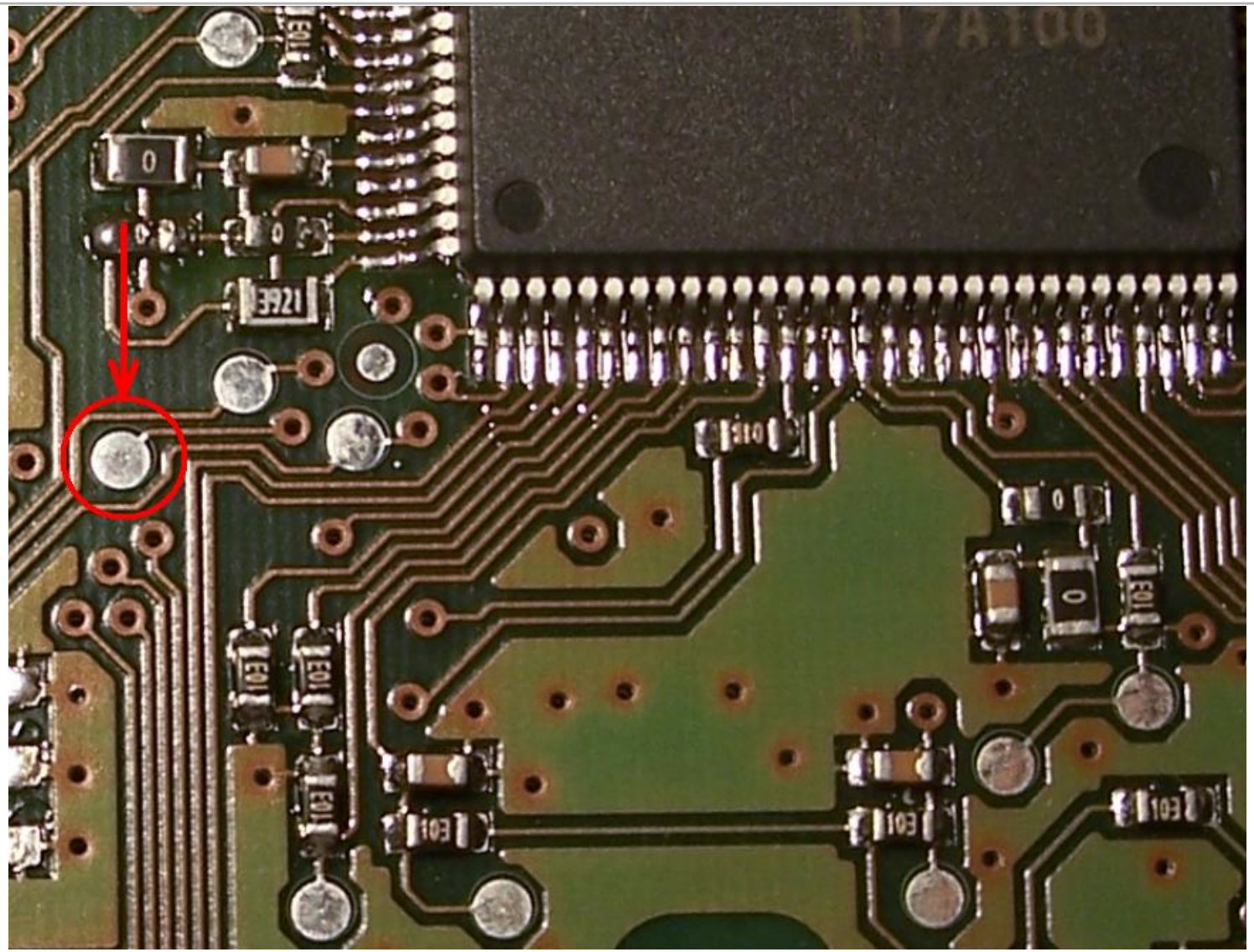
Cables and PCB Wires





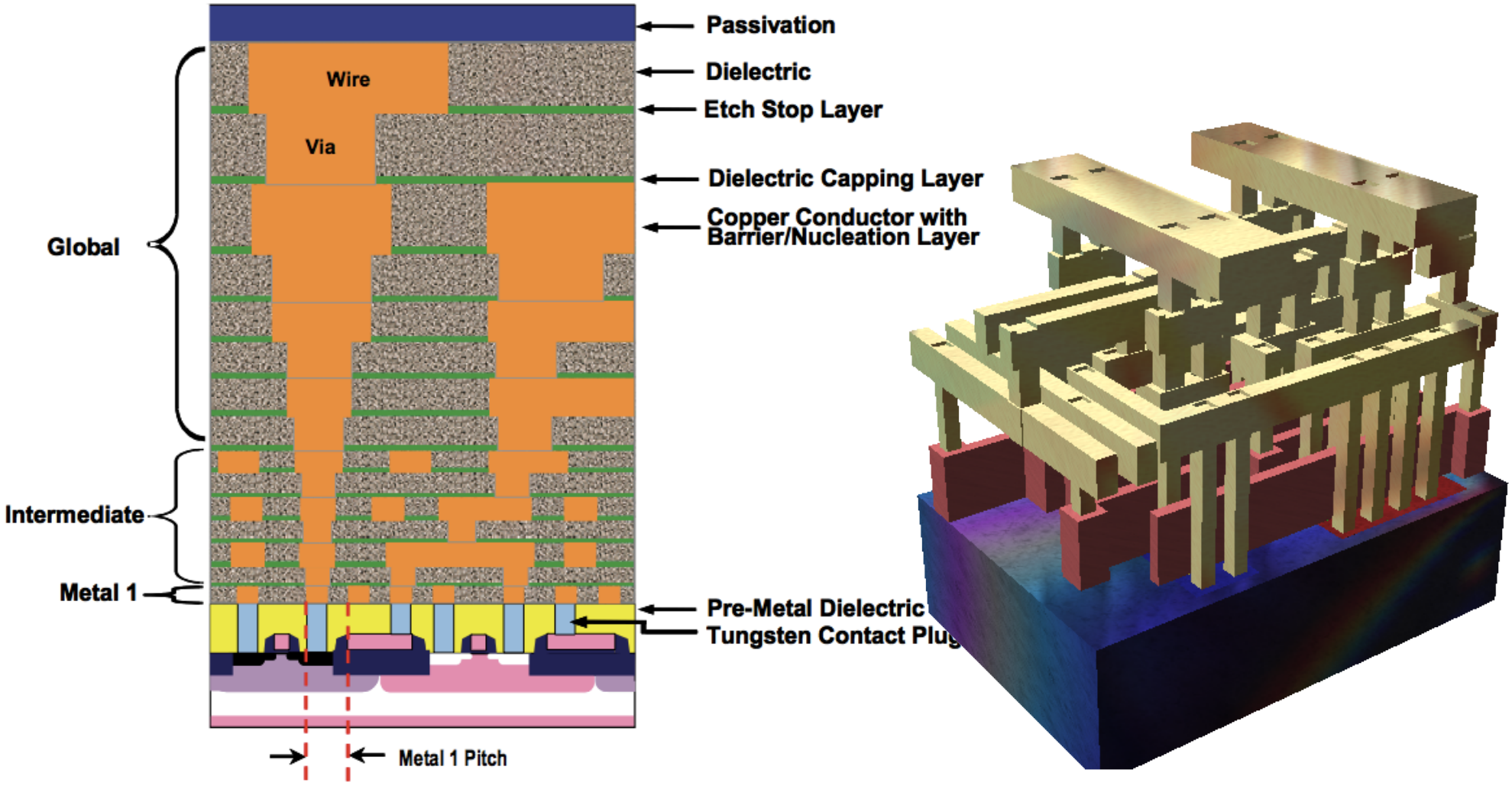
Source; http://en.wikipedia.org/wiki/File:Flachbandkabel.jpg

Printed Circuit Board

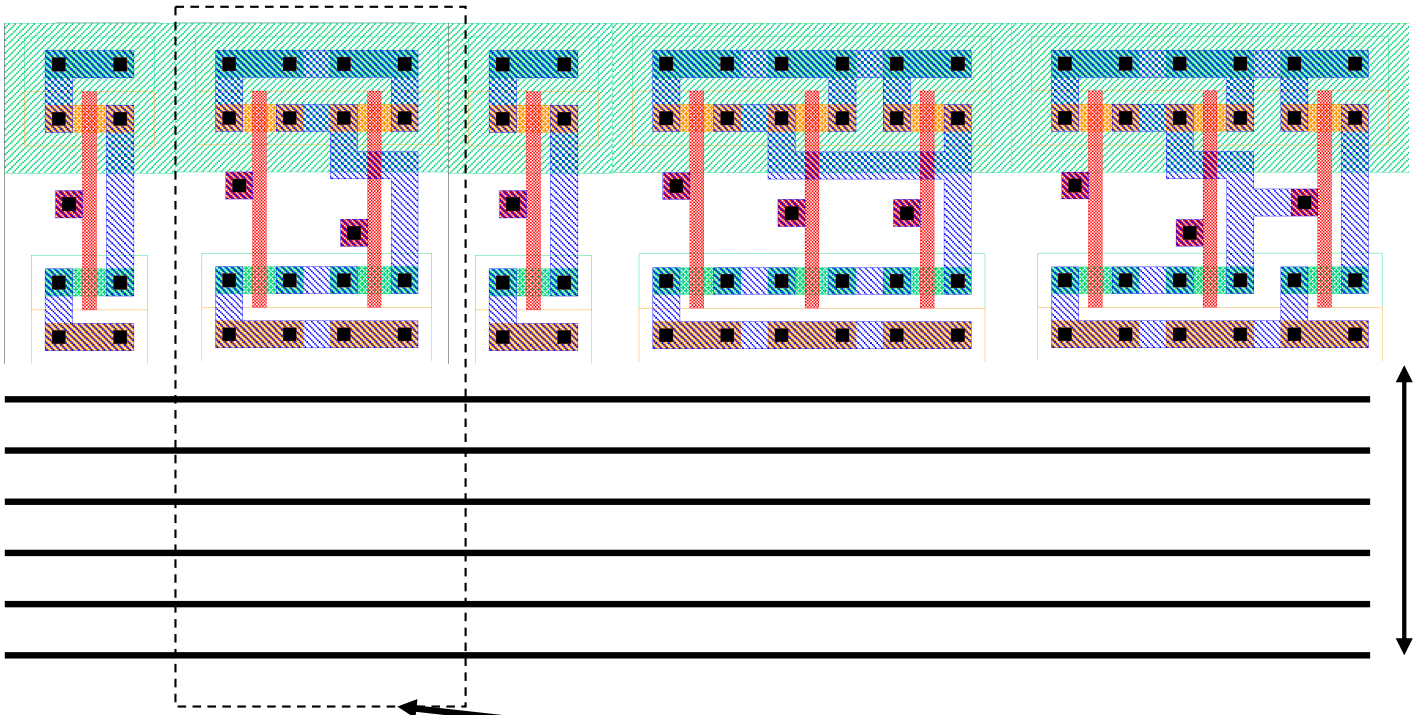


Source: http://en.wikipedia.org/wiki/File:Testpad.JPG

Interconnect Cross Section



Standard Cell Area



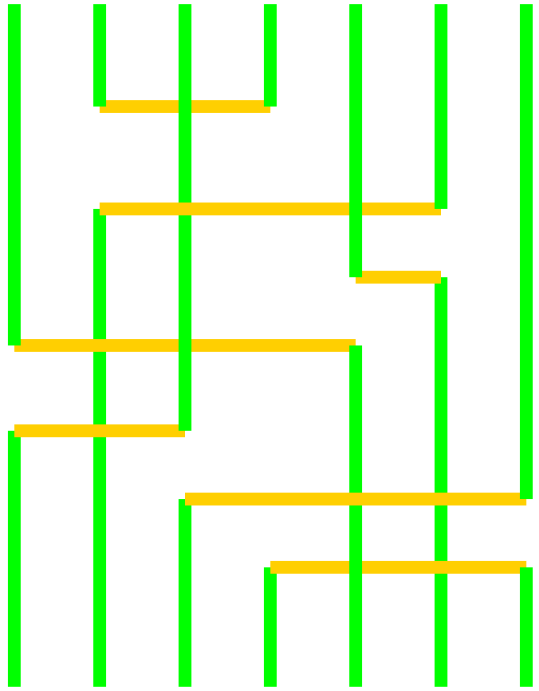
All cells uniform height

Width of channel determined by routing

Cell area

Wires

- Will be capacitively coupled to many adjacent wires of varying degrees



Noise Implications

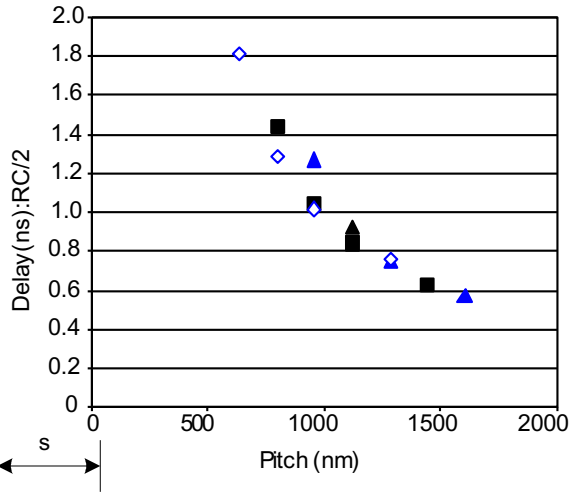
- *So what* if we have noise?
- If the noise is less than the noise margin, nothing happens
- Static CMOS logic will eventually settle to correct output even if disturbed by large noise spikes
  - But glitches cause extra delay
  - Also cause extra power from false transitions
- Dynamic logic never recovers from glitches
  - Can't correct mid-cycle, need precharge nodes
- Memories and other sensitive circuits also can produce the wrong result

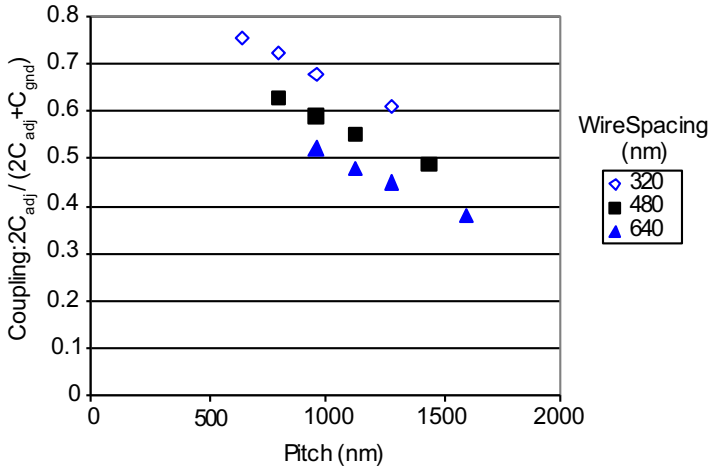
Wire Engineering

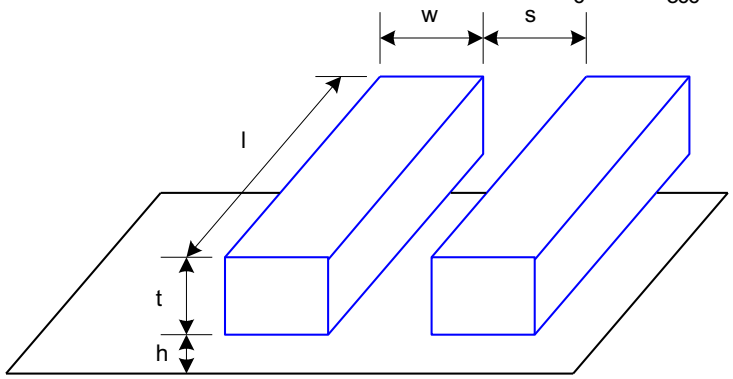
- Goal: achieve delay, area, power goals with acceptable noise
- Degrees of freedom:

Wire Engineering

- Goal: achieve delay, area, power goals with acceptable noise
- Degrees of freedom:
  - Width
  - Spacing
  - Layer

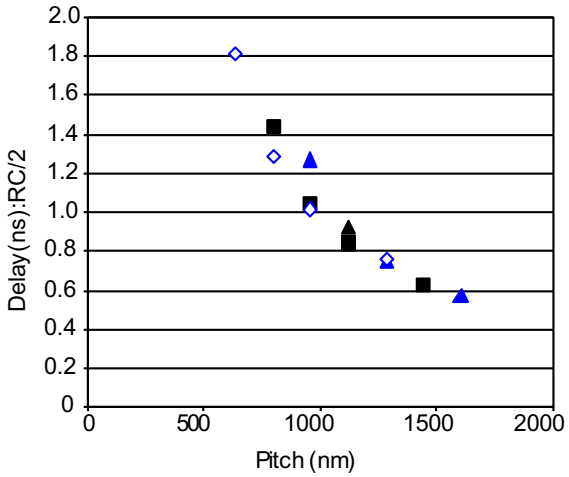


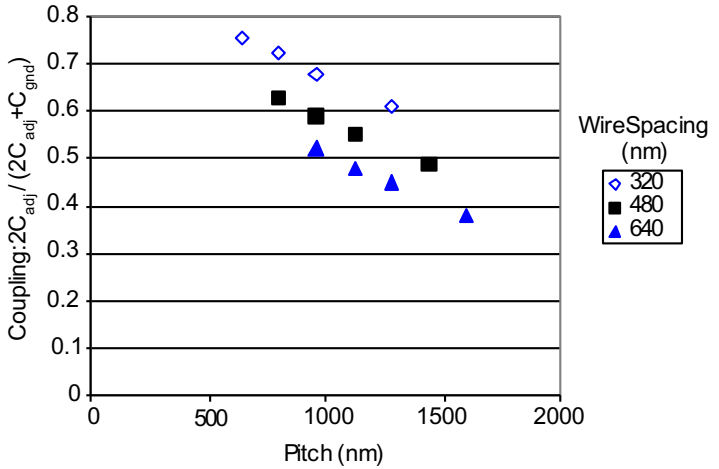


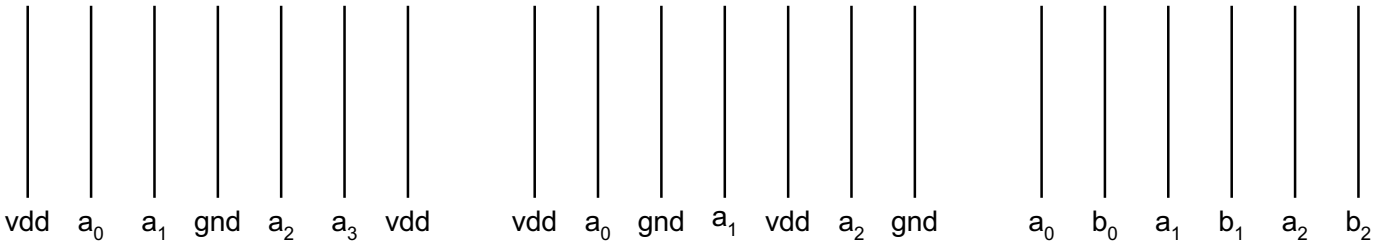


Wire Engineering

- Goal: achieve delay, area, power goals with acceptable noise
- Degrees of freedom:
  - Width
  - Spacing
  - Layer
  - Shielding

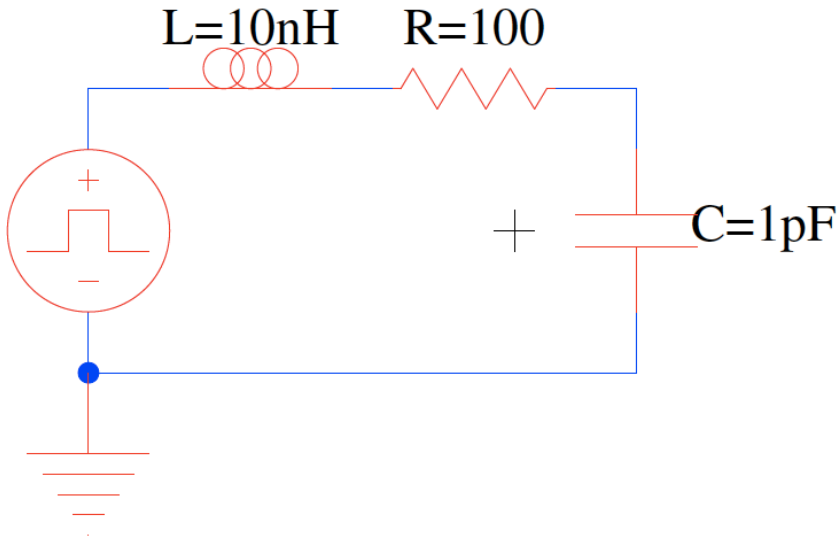






Idea

- Long wires are inductive
  - **Avoid** them
  - Especially on power supplies
- Bypass capacitors help



$$V_2 = V_S + Be^{\left(-\frac{R}{2L}\right)t} e^{\left(j\sqrt{\frac{1}{LC}-\left(\frac{R}{2L}\right)^2}\right)t}$$

Decay

Oscillation

Idea

- Capacitance is everywhere
- Especially between adjacent wires
- Will get "noise" from crosstalk
- Clocked and driven wires
  - Slow down transitions
- Undriven wires voltage changed
- Can cause spurious transitions

Admin

- Project 2
  - Due Wednesday 5/1
    - Feedback by Wednesday