ESE3700: Circuit-Level Modeling, Design and Optimization for Digital Systems

Lec 21: April 29, 2024

Transmission Line

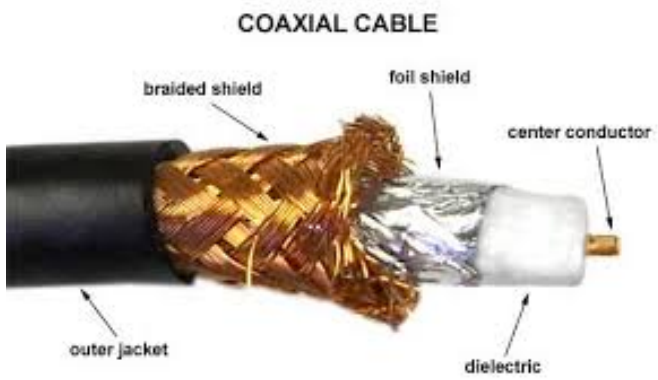
Today

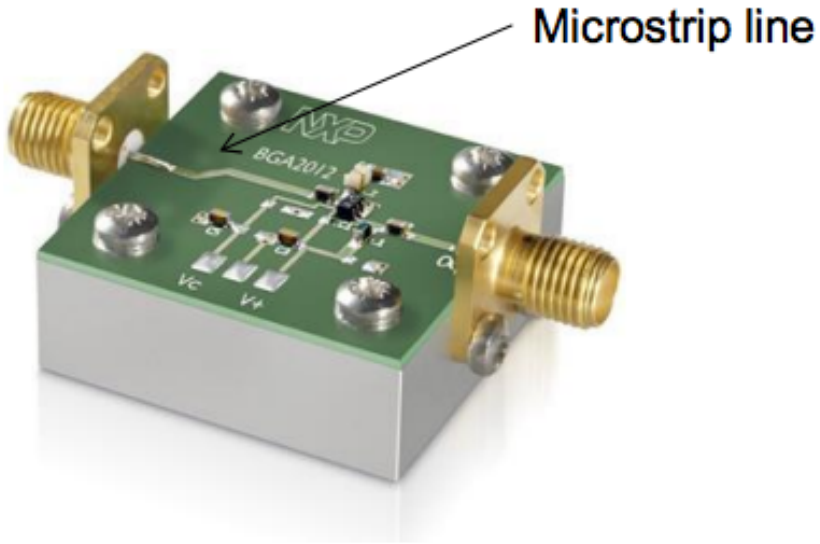
- Saw in action in lab
- Where transmission lines arise?
- General wire formulation
- Lossless Transmission Line
- End of Transmission Line?
- Termination
- Discuss Lossy
- Implications

Where Transmission Lines Arise

Transmission Lines

- Cable: coaxial
- PCB
  - Strip line
  - Microstrip line
- Twisted Pair (Cat5)





Transmission Lines

- How did the traces behave in lab?
- How does this differ from
  - Ideal equipotential?
  - RC-wire on chip?

Transmission Lines

- This is what long wires/cables look like
  - Aren't an ideal equipotential
  - Signals take time to propagate
  - Maintain shape of input signal
    - Within limits
  - Shape and topology of wiring effects how signals propagate

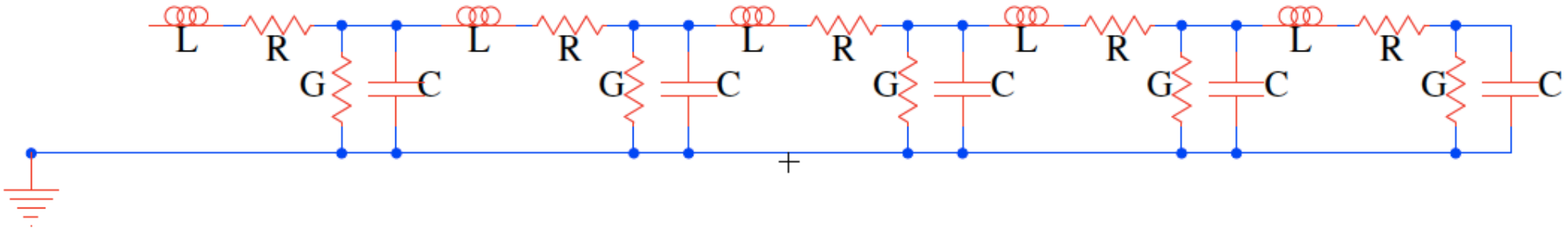
Transmission Lines

- Need theory/model to support design
  - Reason about behavior
  - Understand what can cause noise
  - Engineer high performance/speed communication

Wire Formulation

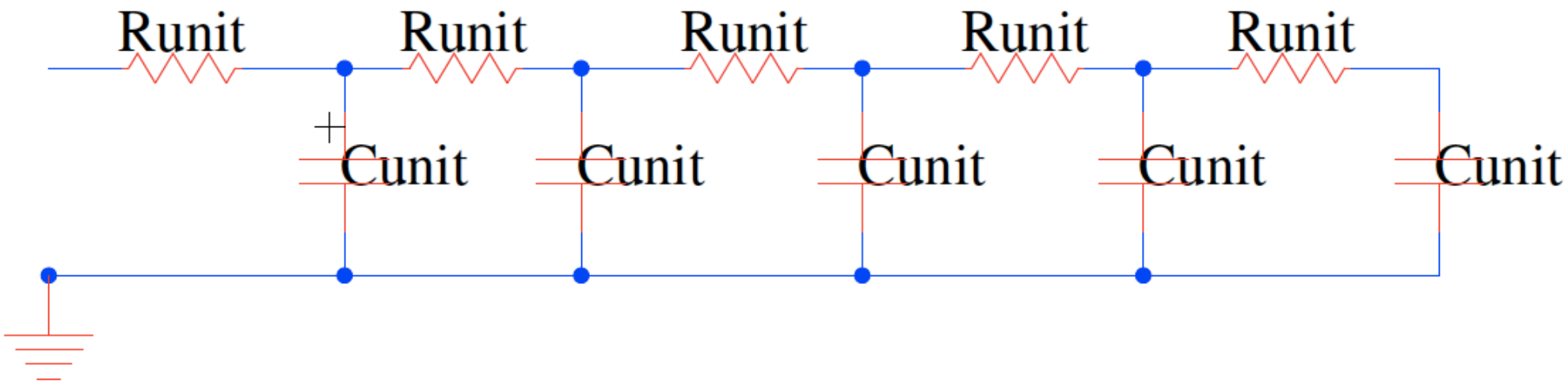
Wires

- In general, our "wires" have distributed R, L, C components



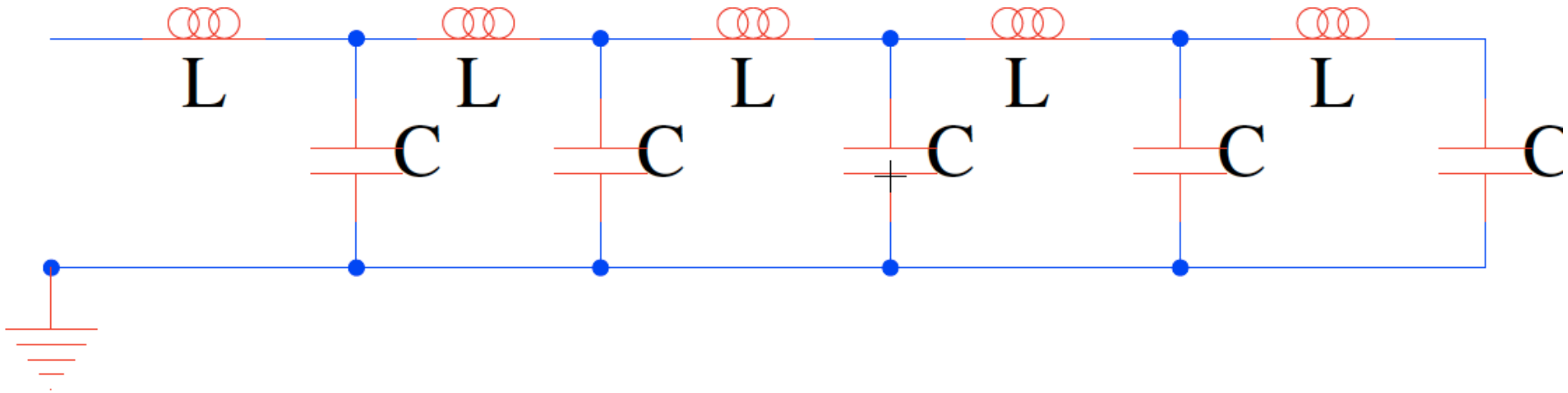
RC Wire (Preclass 1)

- When R dominates L
  - We have the distributed RC Wires
  - Typical of on-chip wires in ICs
  - What is RC response to step?



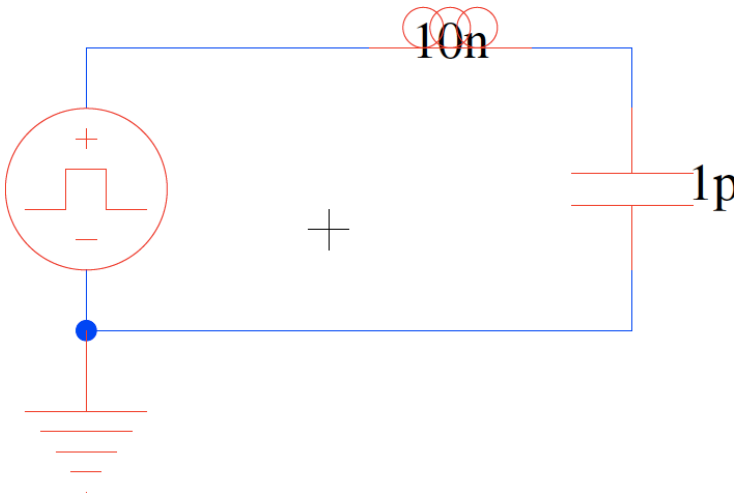
Transmission Line

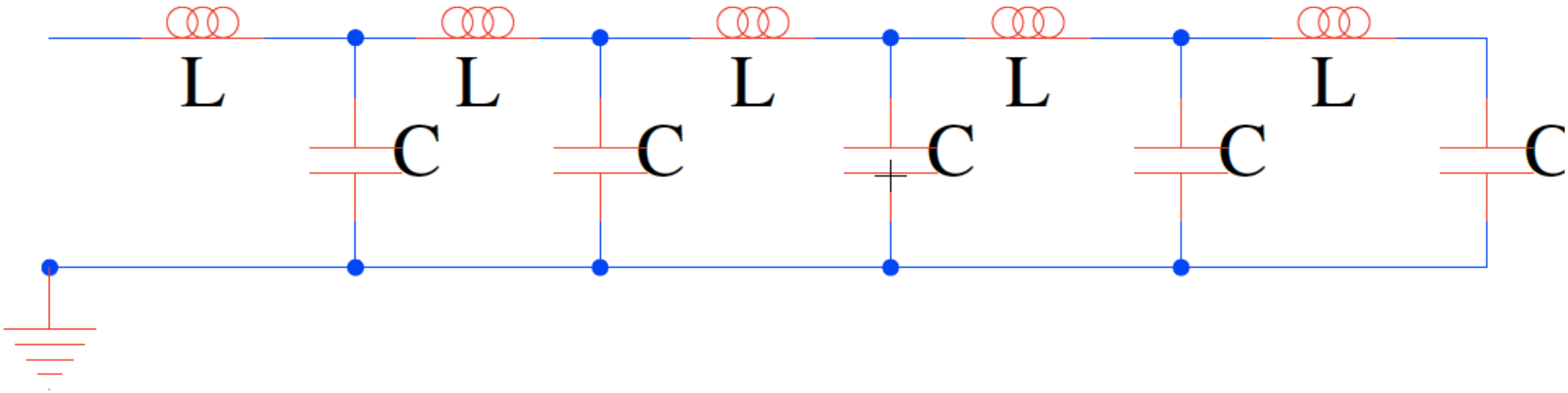
- When resistance is negligible
  - Have LC wire = Lossless Transmission Line
    - No energy dissipation (loss) through R's
  - More typical of printed circuit board (PCB) wires and bond wires



Build Intuition from LC (Preclass 2)

- What did one LC do?
- What will chain do?





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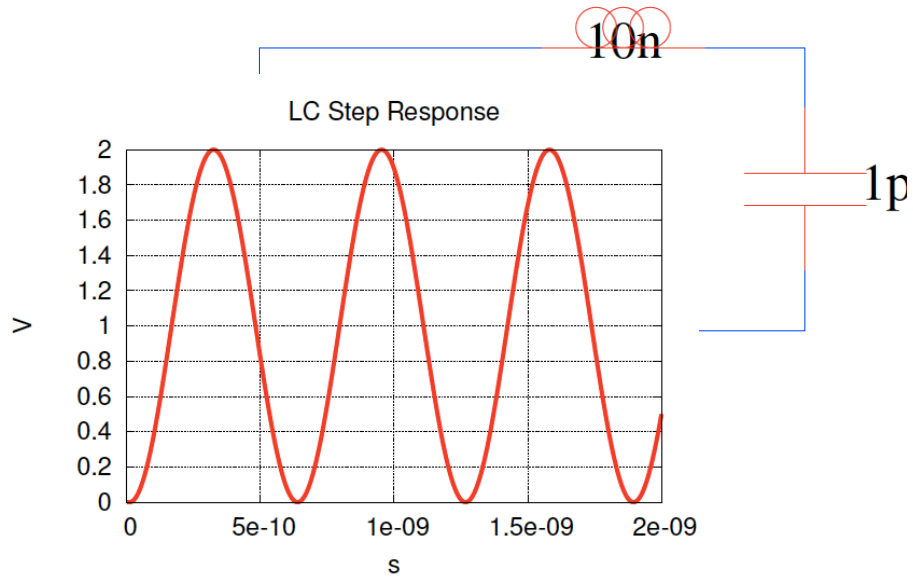
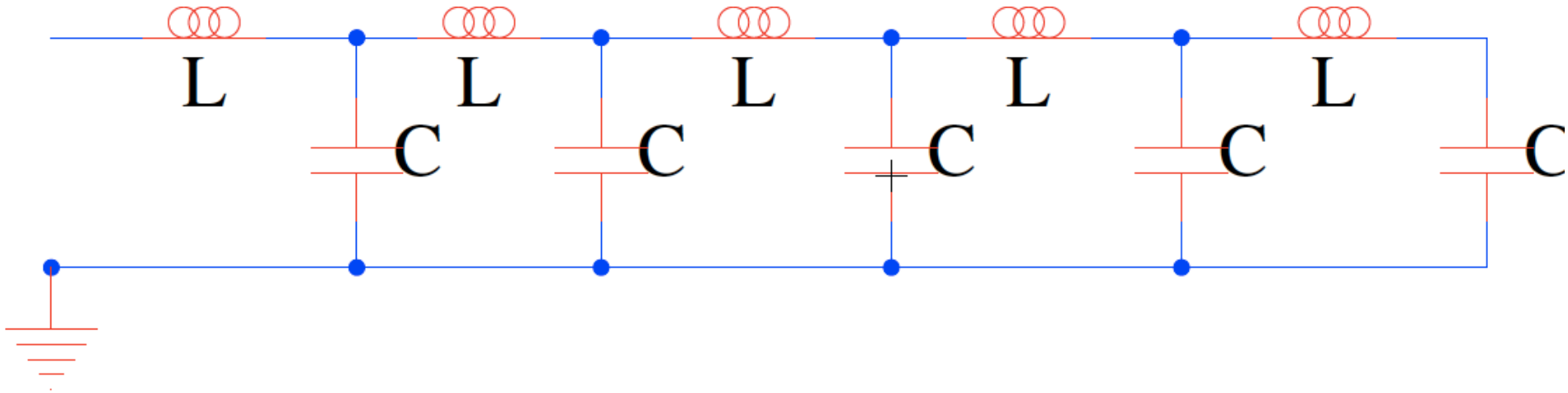
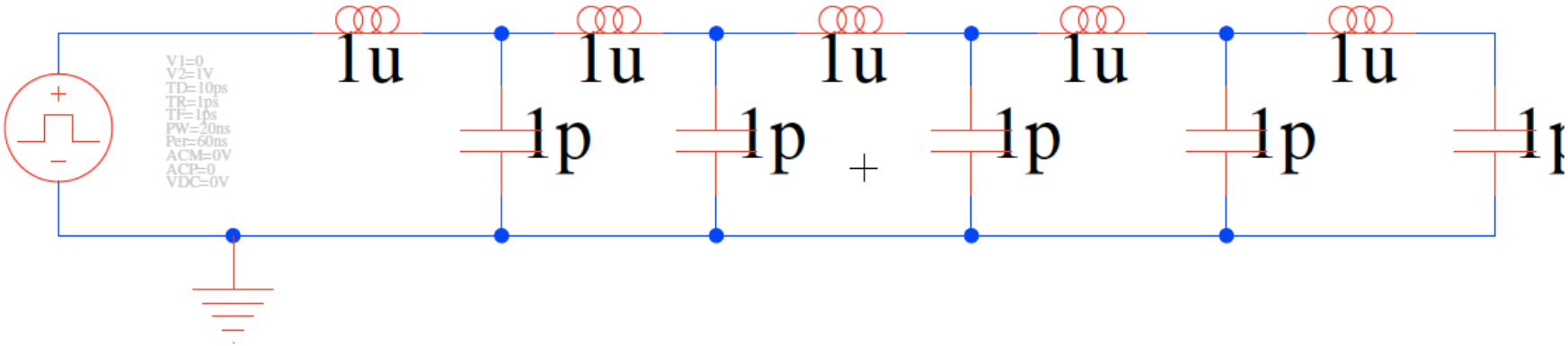




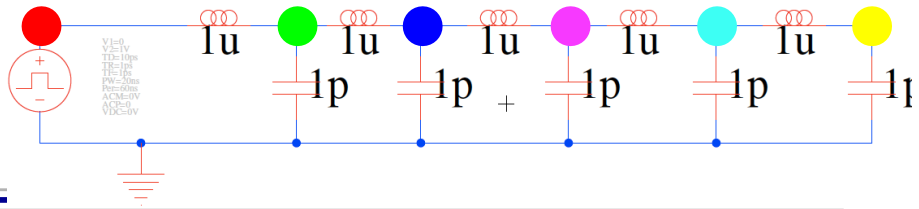
Intuitive: Lossless

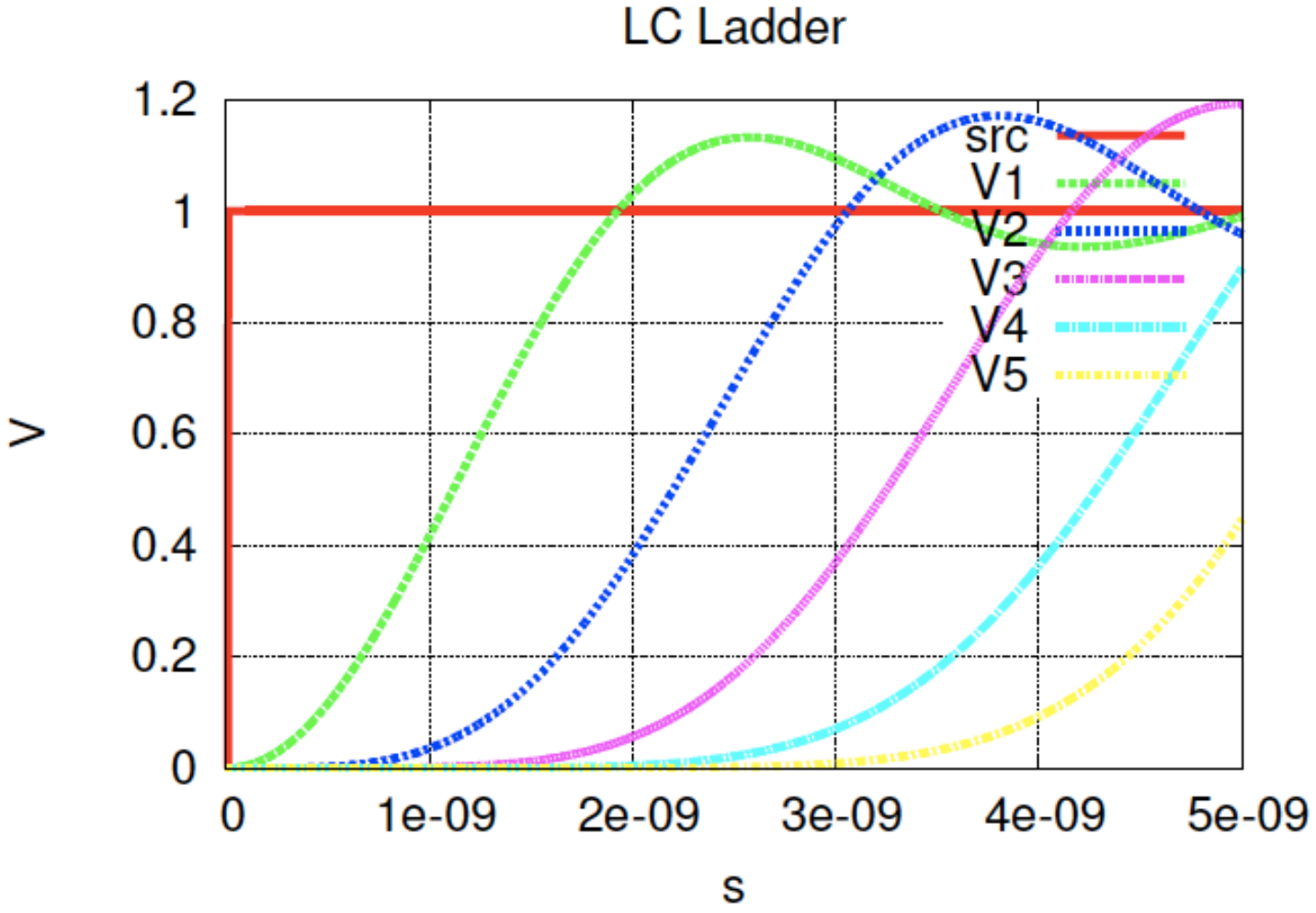
- Pulses travel as waves without distortion
  - (up to a characteristic frequency)

SPICE Simulation

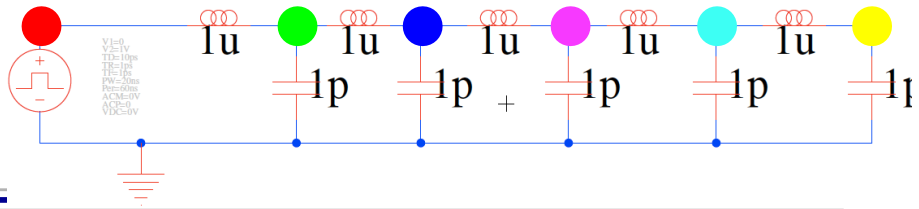


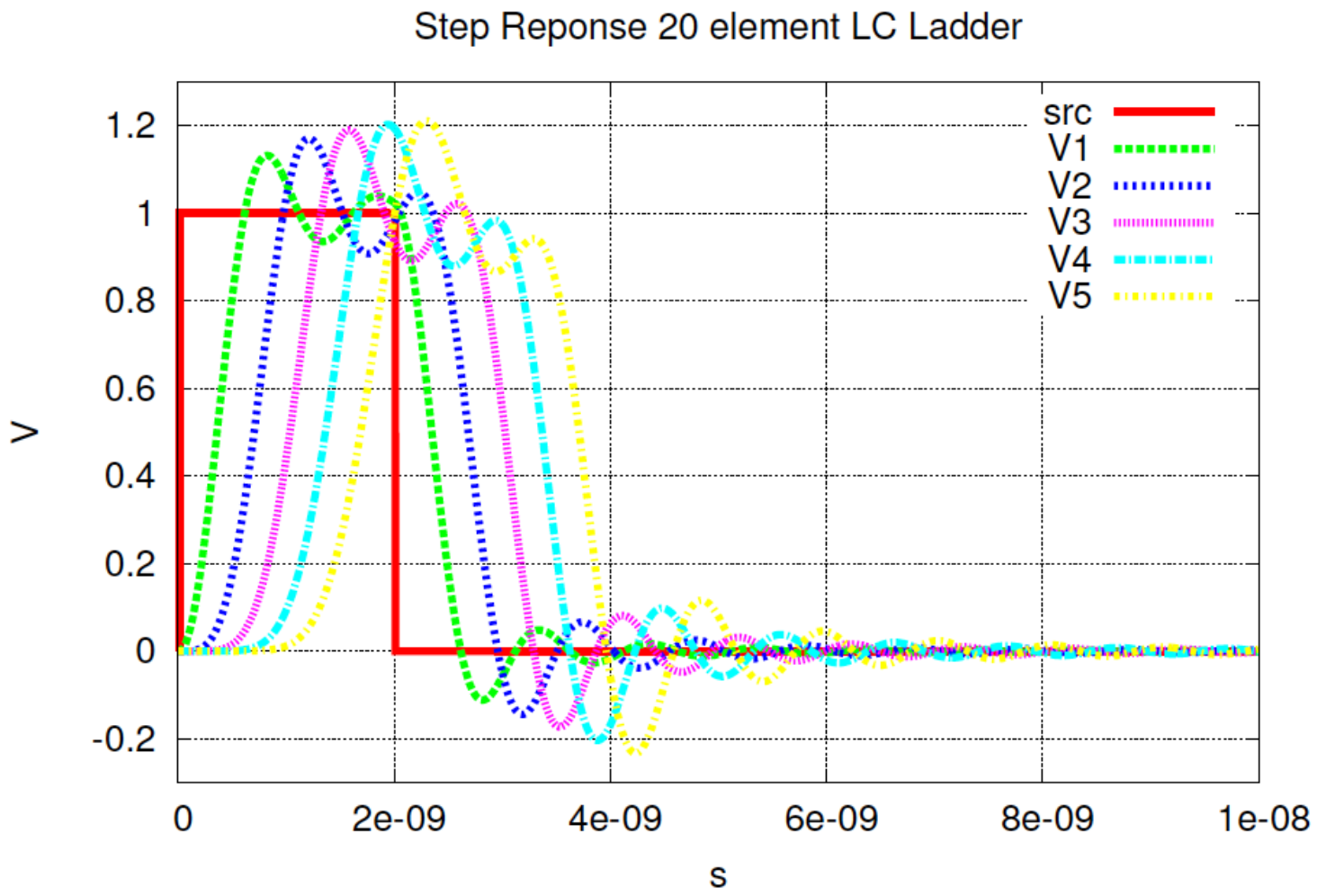
Step Response SPICE



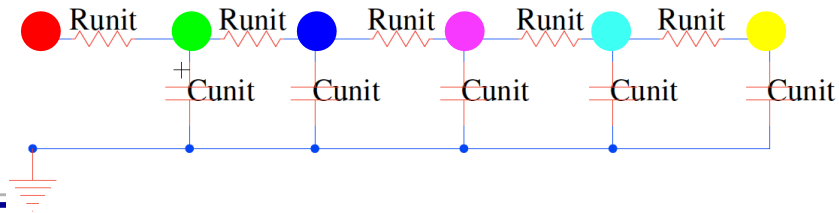


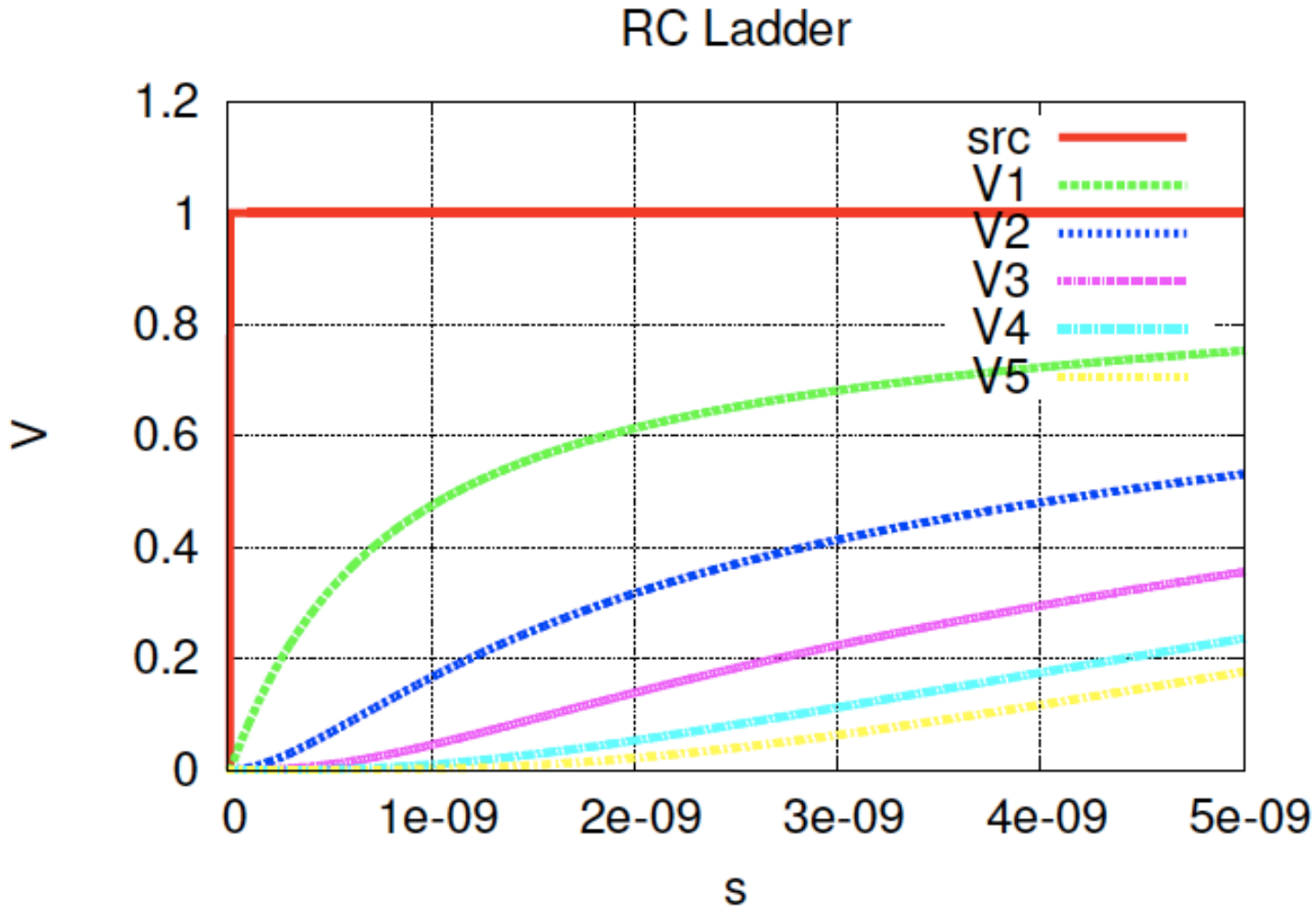
Pulse Response SPICE



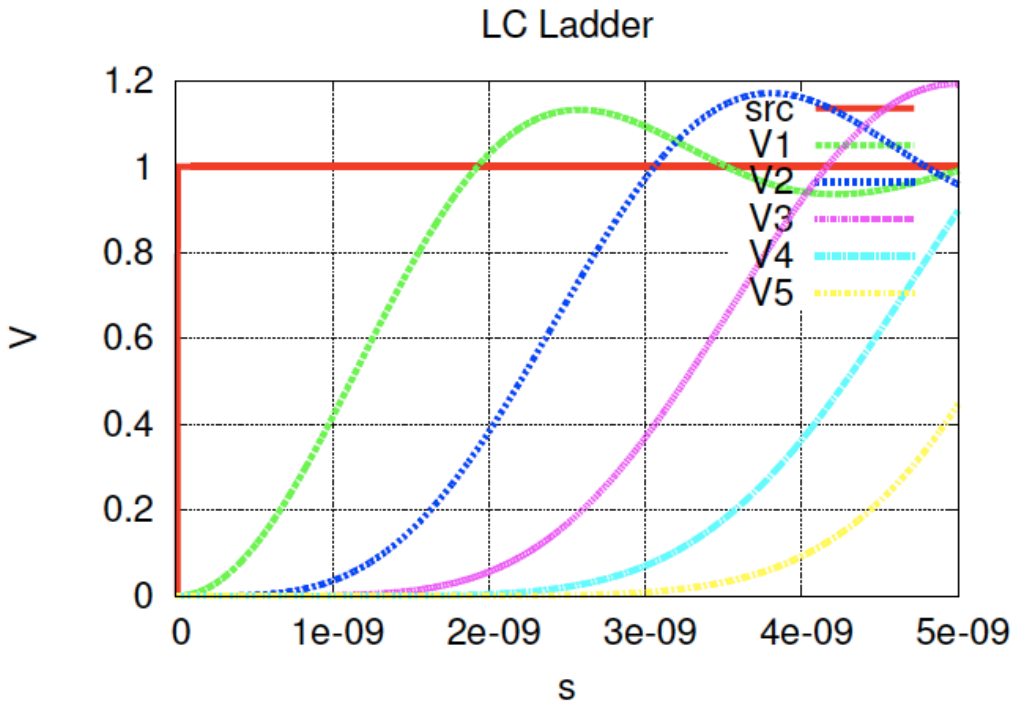


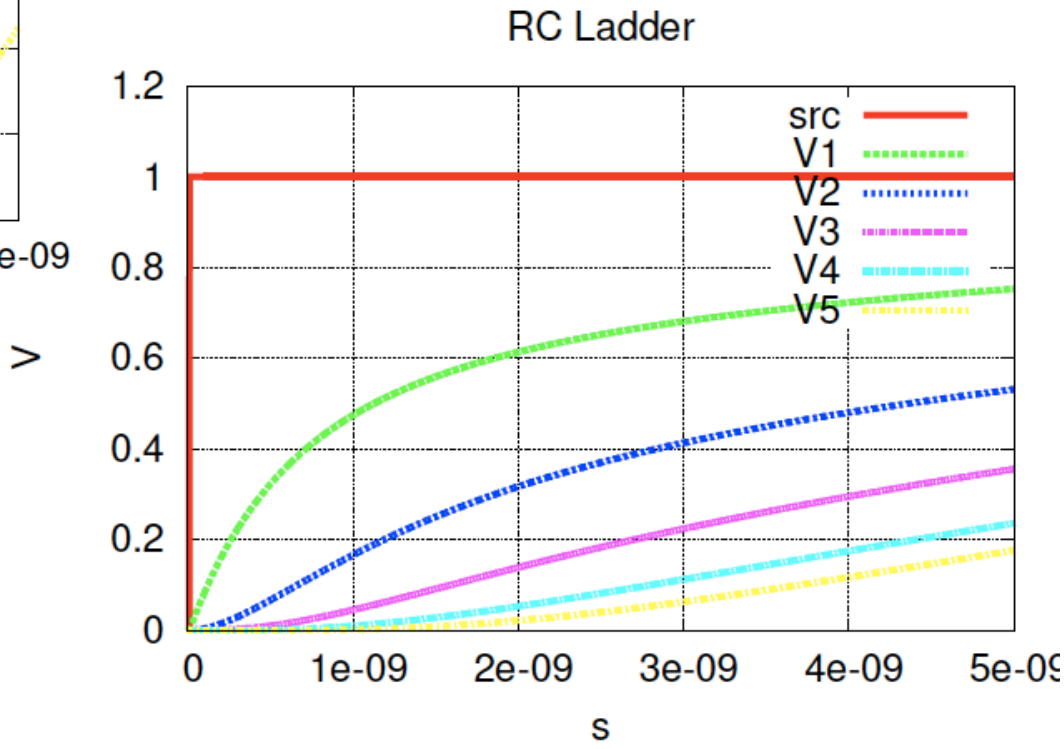
Contrast RC Wire





Contrast


LC Ladder
1.2
1
0.8
0.6
0.4
0.2
0
V
0
1e-09
2e-09
3e-09
4e-09
5e-09
s
src
V1
V2
V3
V4
V5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s
src
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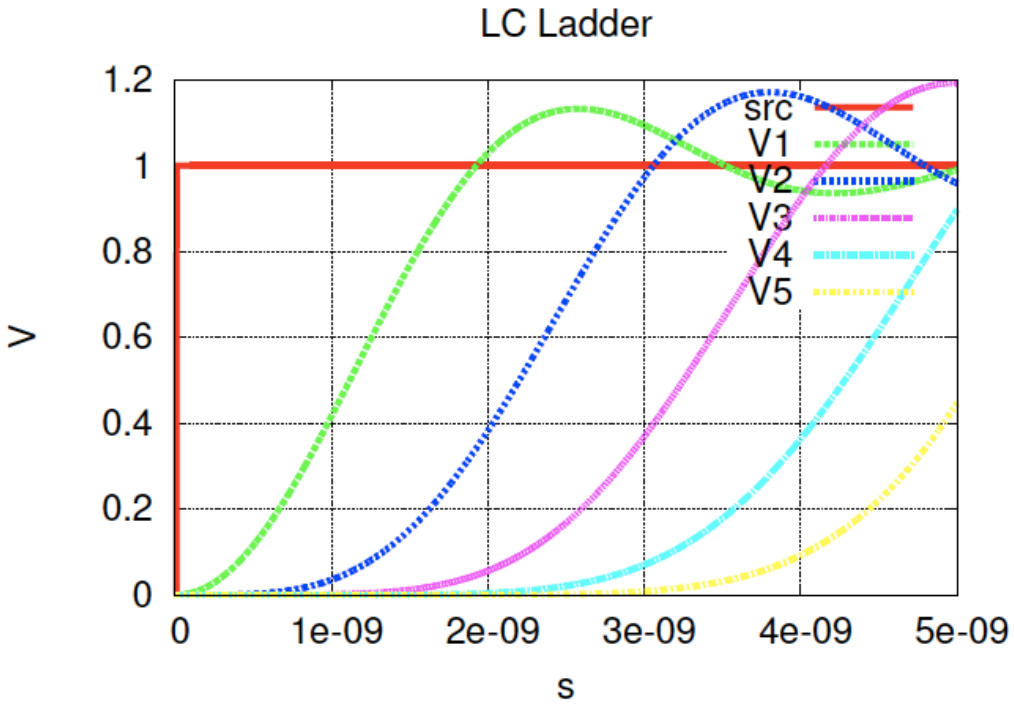
V5

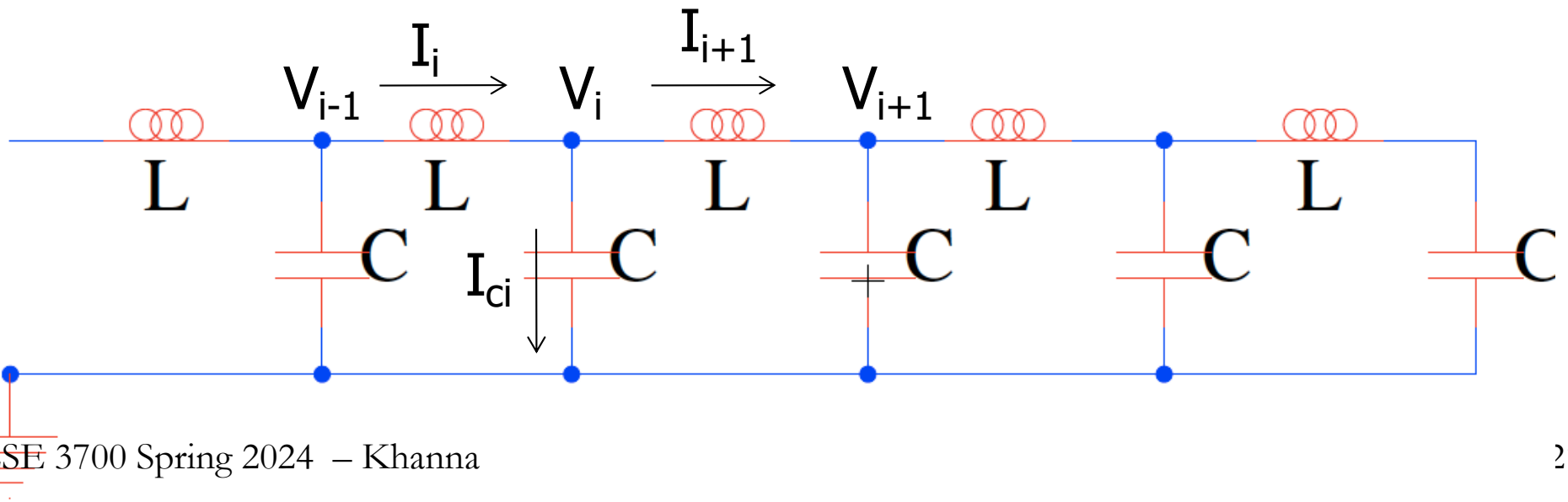
Model

- Now voltage is a function of time **and** position
  - Position along wire – distance from source
- Want to get V(x,t)
  - And I(x,t)



Setup Relations

- i is a node, x is the distance from source, Δx is distance between nodes
- Position along wire: $x = i \times \Delta x$
- So $V_i(t) = V(x = i\Delta x, t)$



Implication

- Wave equation:

$$\frac{\partial^2 V}{\partial x^2} = LC\frac{\partial^2 V}{\partial t^2}$$

- Solution:

$$V(x,t) = A + Be^{x-wt}$$

- What is w?

Implication

- Wave equation:

$$\frac{\partial^2 V}{\partial x^2} = LC\frac{\partial^2 V}{\partial t^2}$$

- Solution:

$$V(x,t) = A + Be^{x-wt}$$

- What is w?

$$Be^{x-wt} = LCw^2 Be^{x-wt}$$

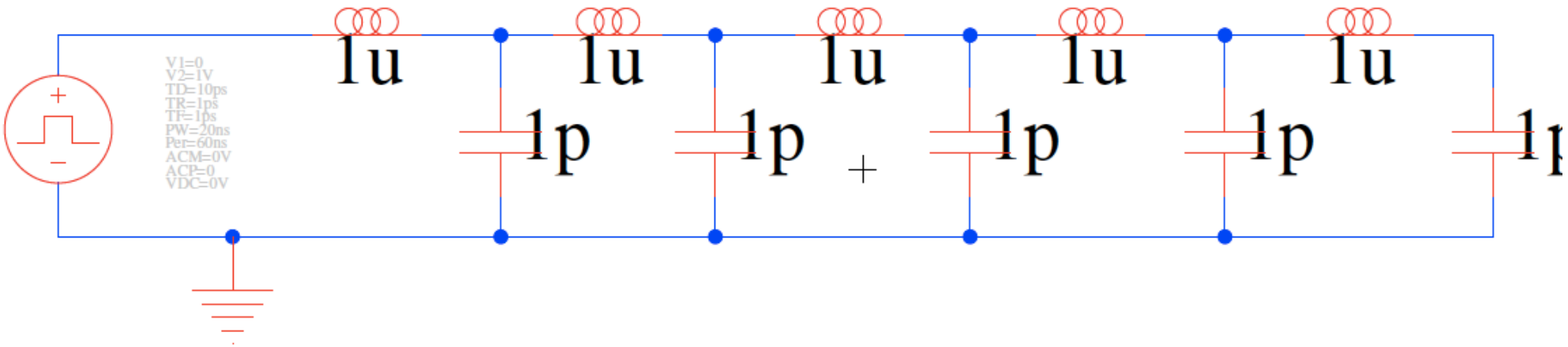
$$w = \sqrt{\frac{1}{LC}}$$

w is the rate of propagation

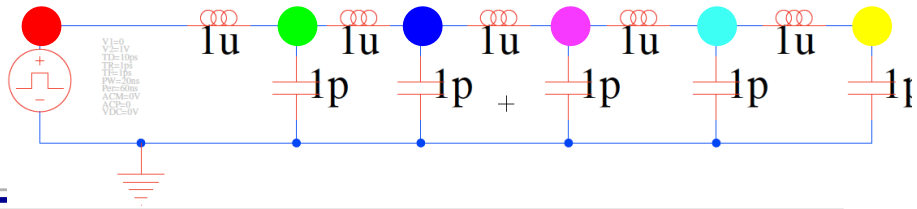
Propagation Rate in Example

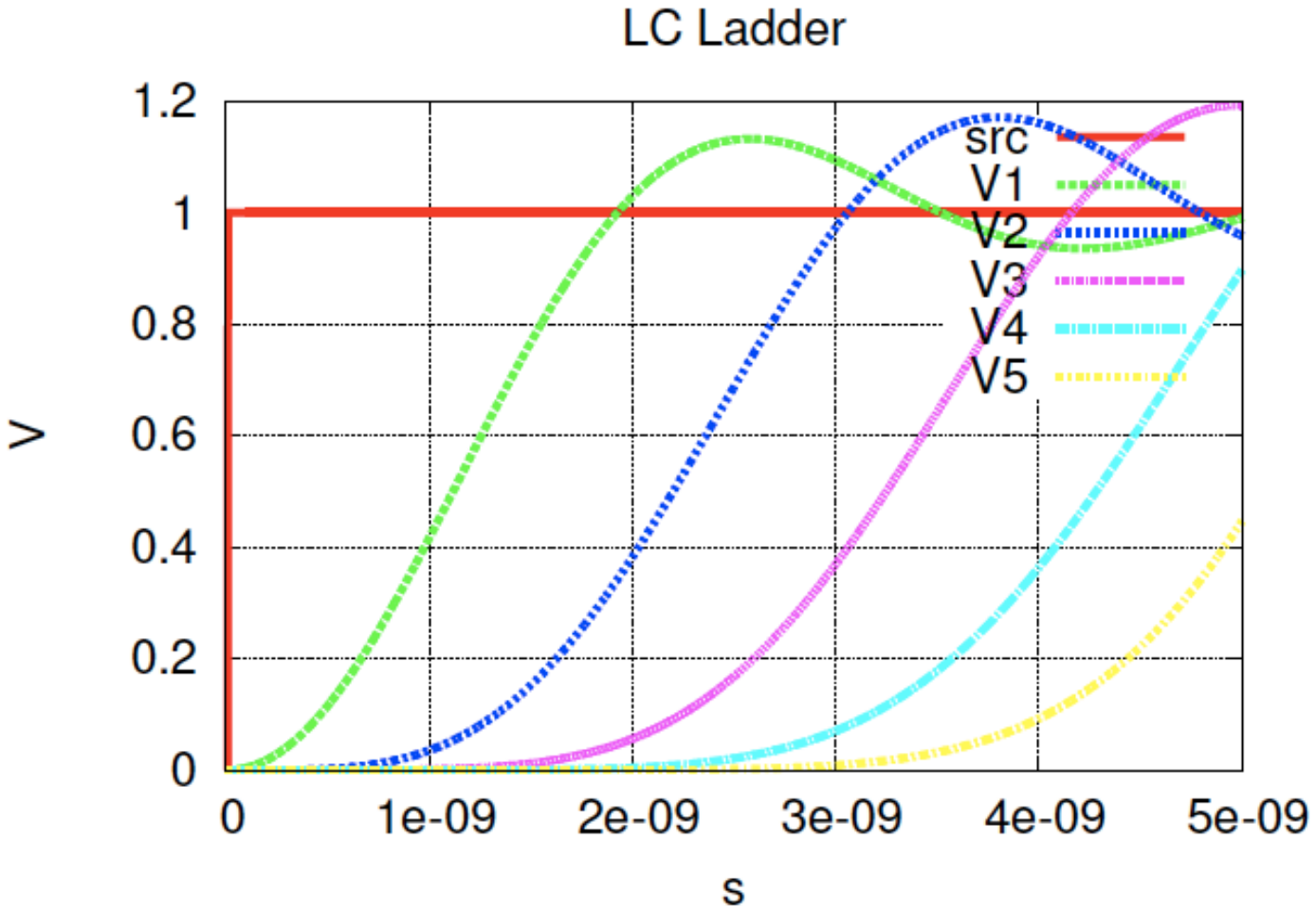
- L=1uH
- C=1pF
- What is w?

$$w = \frac{1}{\sqrt{LC}}$$



Signal Propagation





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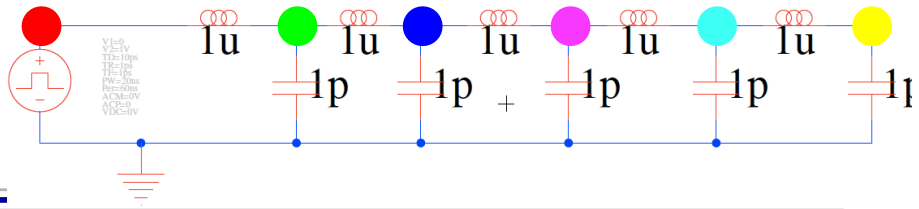
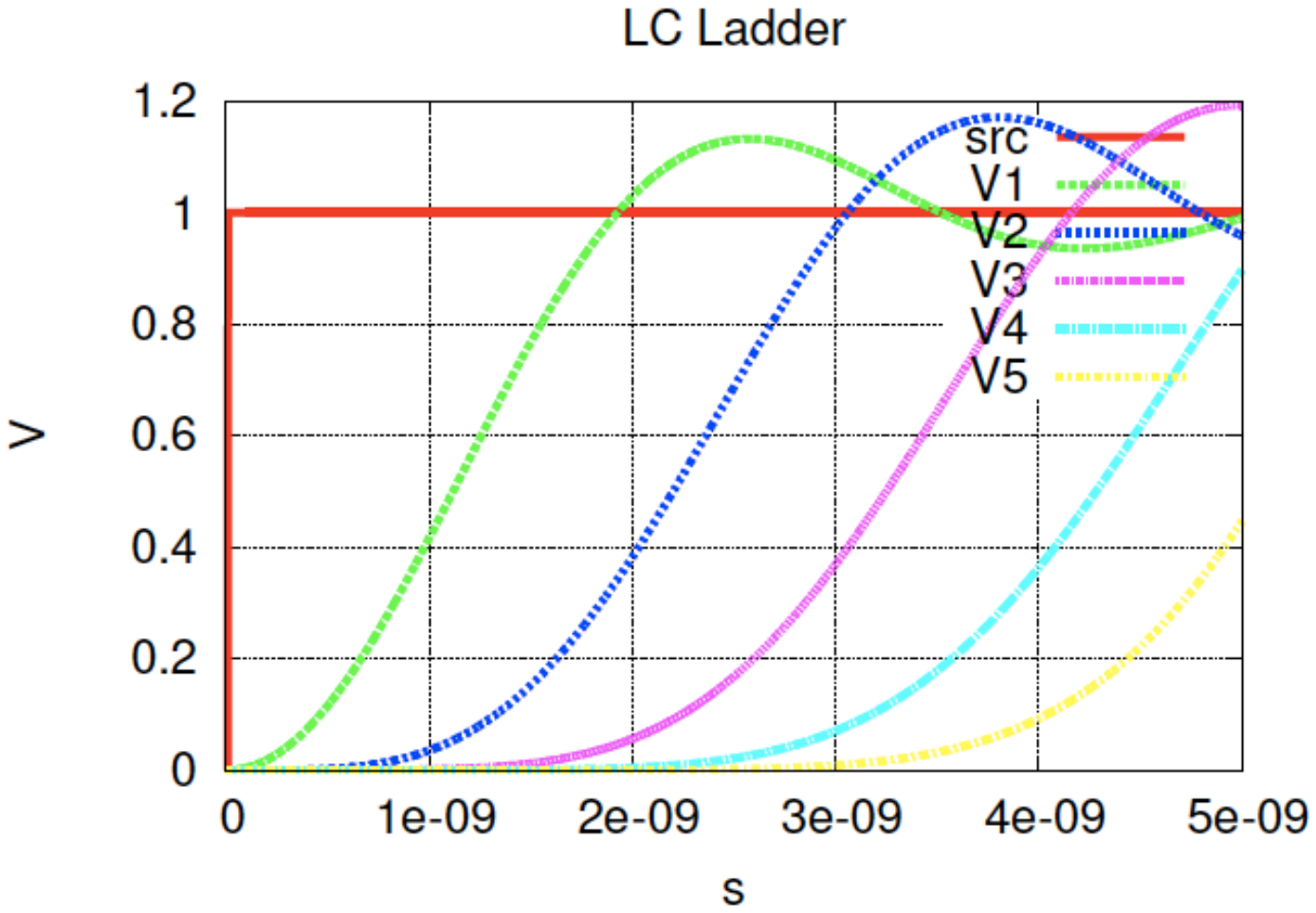
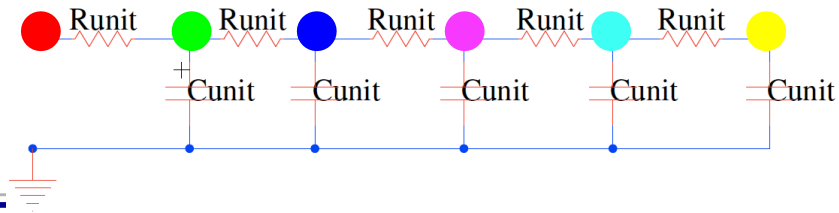


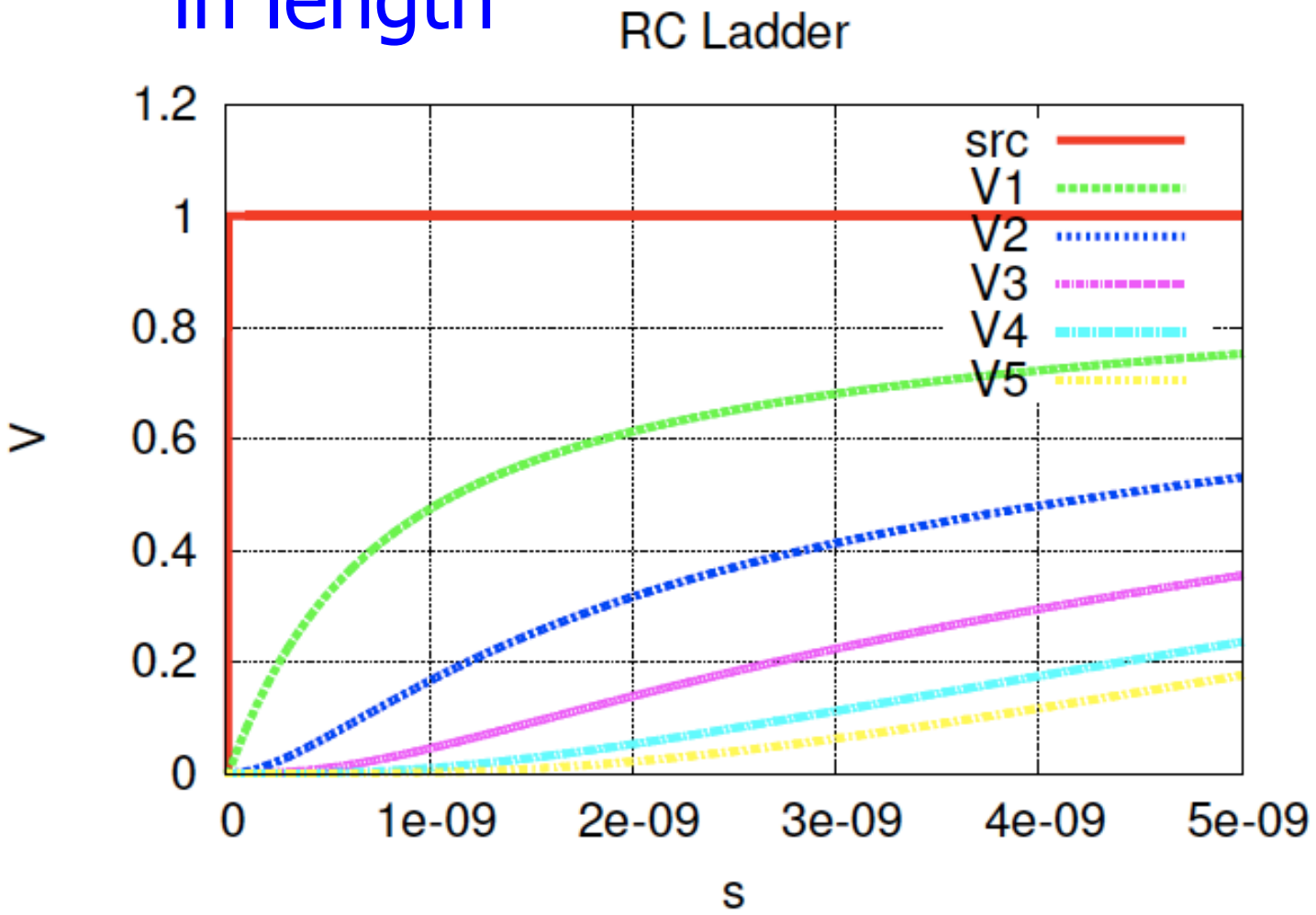
Delay linear in length



Contrast RC Wire



RC wire delay quadratic in length

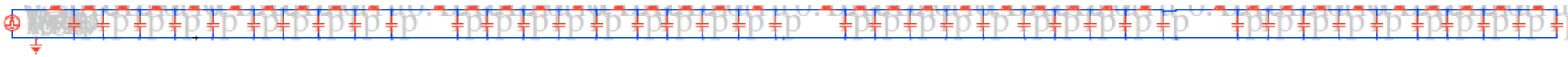


Longer LC (open)

- 40 Stages
- L=100nH
- C=1pF

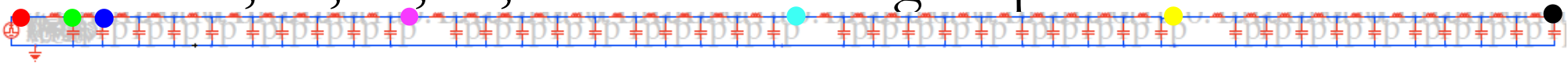
$$w = \frac{1}{\sqrt{LC}}$$

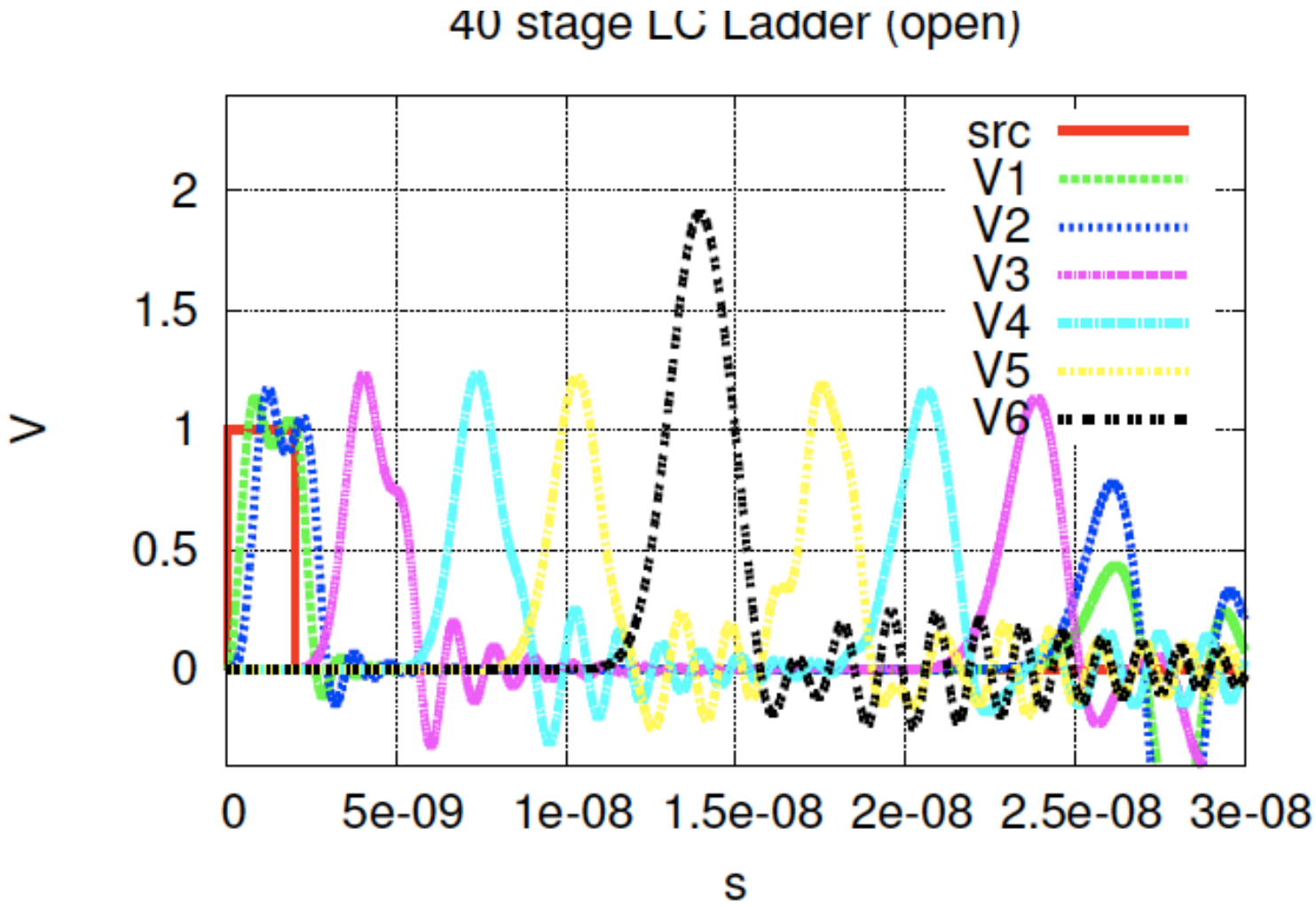
Stage delay? How long to propagate?



Reflection Teaser: Pulse Travel RC

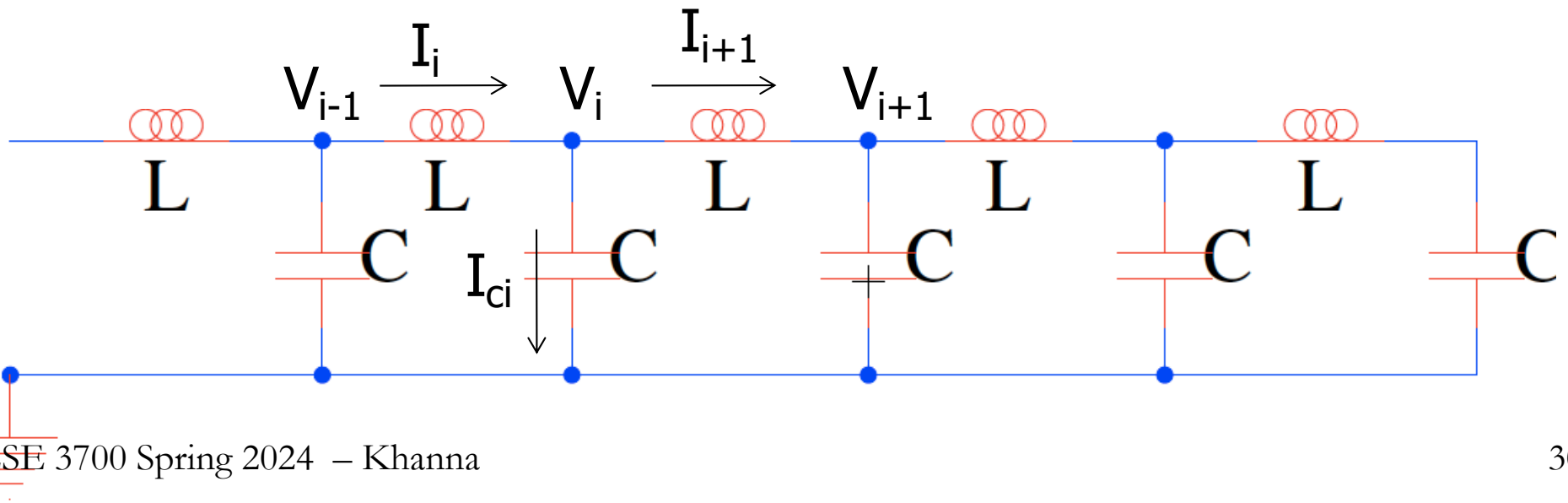
- V1,V3,V4,V5,V6 about 10 stages apart





Wire "Resistance" (preclass 4)

- What is the resistance at V_i ?
  - Q needed to charge C to V_i?
  - I_i given velocity w?
  - $R = V_i/I_i$?

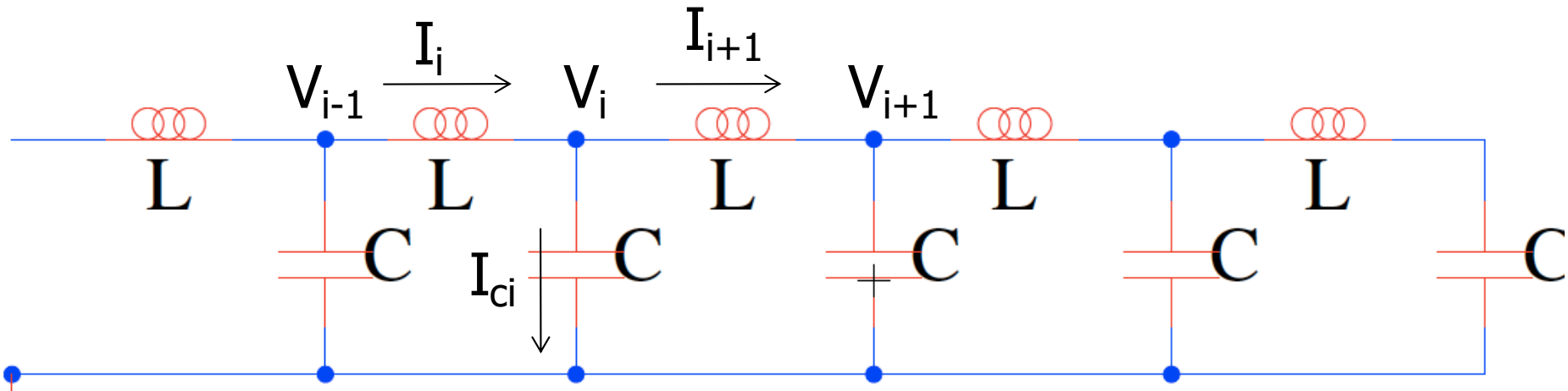


Wire "Resistance"

- $Q=CV_i$
- $I_i = dQ/dt$
- Moving at rate w
- $I_i=wCV_i$
- $R=V_i/I_i=1/(wC)$

$$w = \frac{1}{\sqrt{LC}}$$

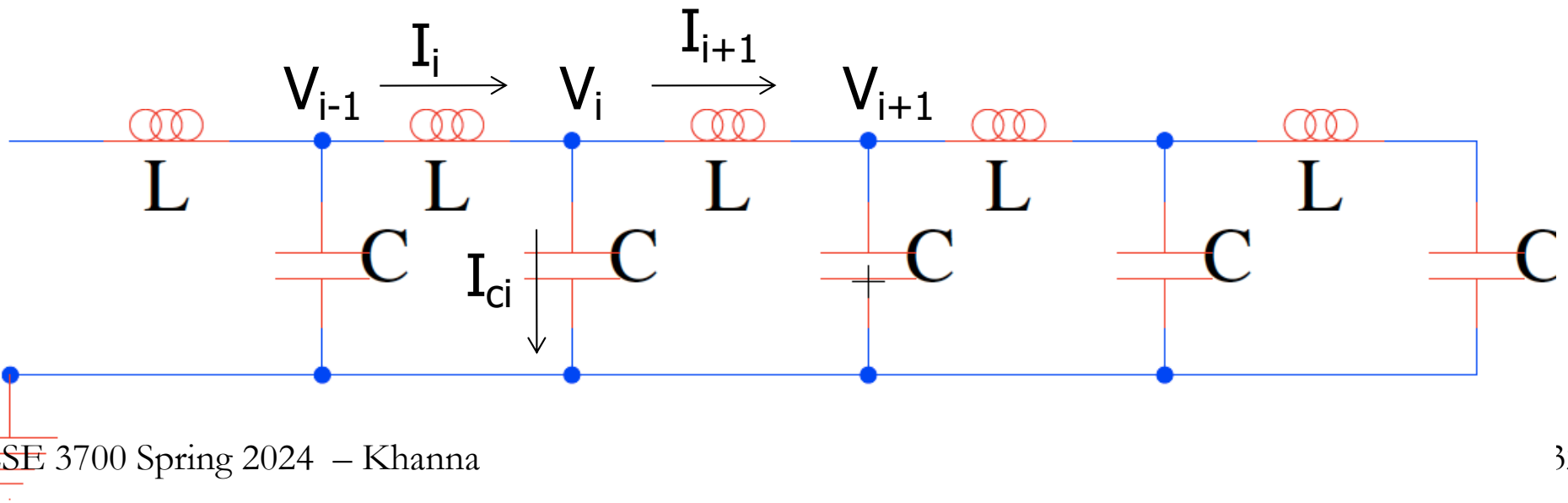
$$R = \frac{\sqrt{LC}}{C}$$



Characteristic Impedance

- $Z_0 = R$

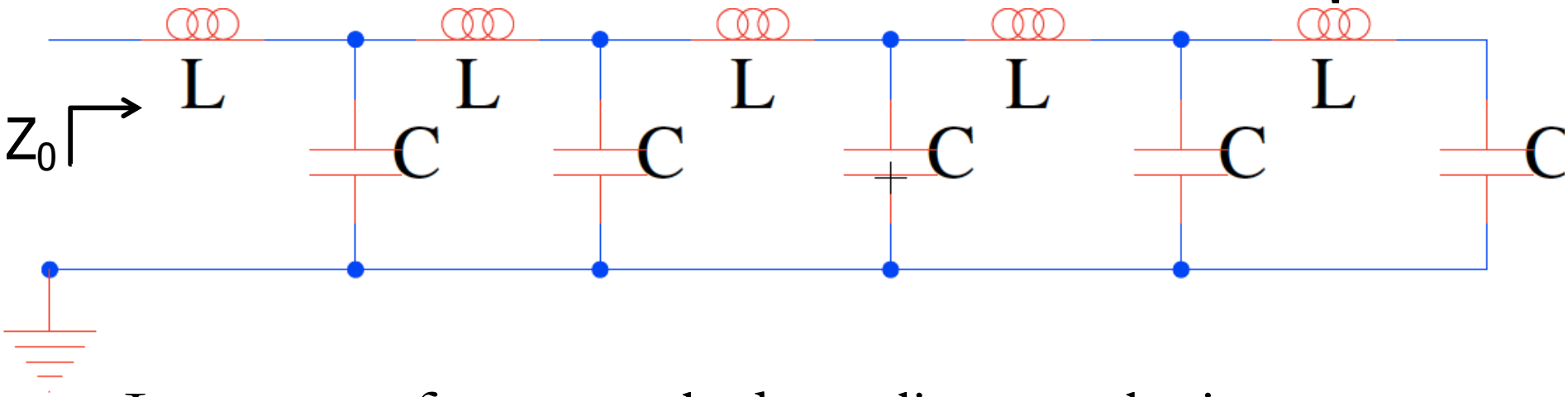
$$R = \frac{\sqrt{LC}}{C} = \sqrt{\frac{L}{C}} = Z_0$$



Infinite Lossless Transmission Line

- Transmission line looks like resistive load

$$Z_0 = \sqrt{\frac{L}{C}}$$



- Input waveform travels down line at velocity
  - Without distortion

$$w = \frac{1}{\sqrt{LC}}$$

Transmission Line Agenda

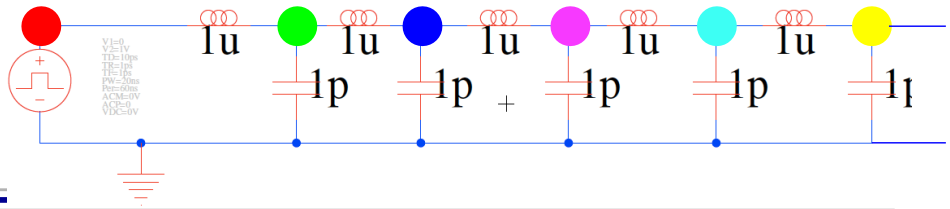
- ~~See in action in lab~~
- ~~Where transmission lines arise?~~
- ~~General wire formulation~~
- ~~Lossless Transmission Line~~
- ~~Impedance~~
- End of Transmission Line?
  - Open, short, matched
- Termination
- Discuss Lossy
- Implications

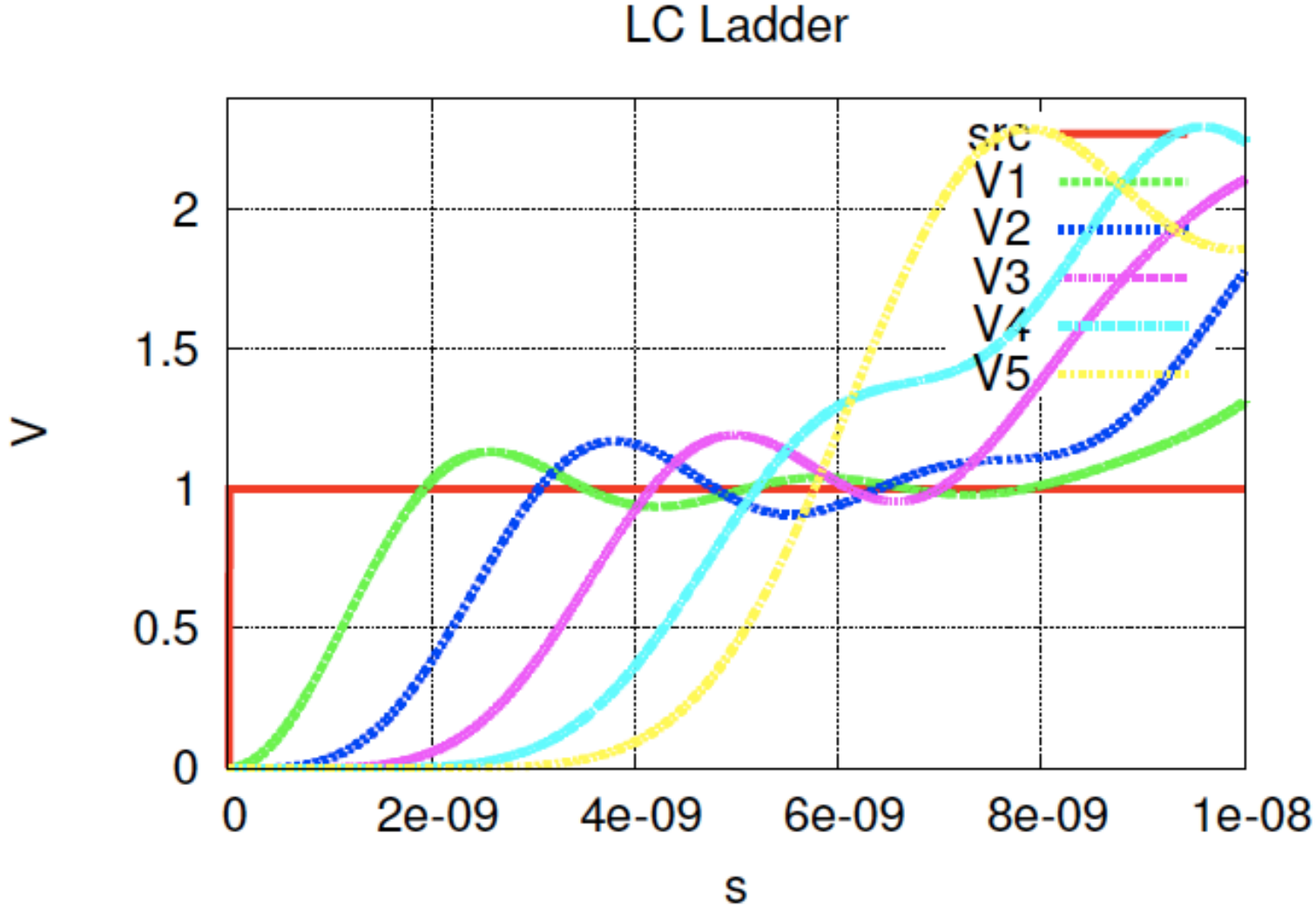
End of Line

- What happens at the end of the transmission line?
  - Short Circuit
  - Terminate with $R=Z_0$
  - Open Circuit

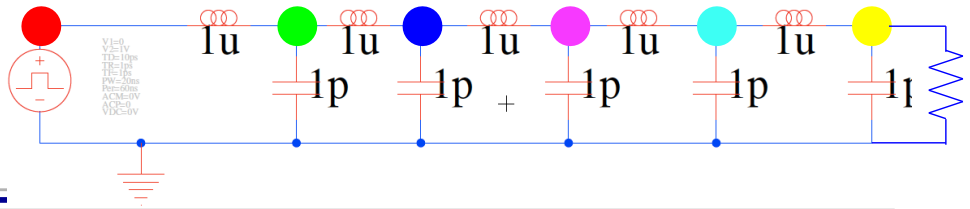
- What did the reflections look like in each case in lab?

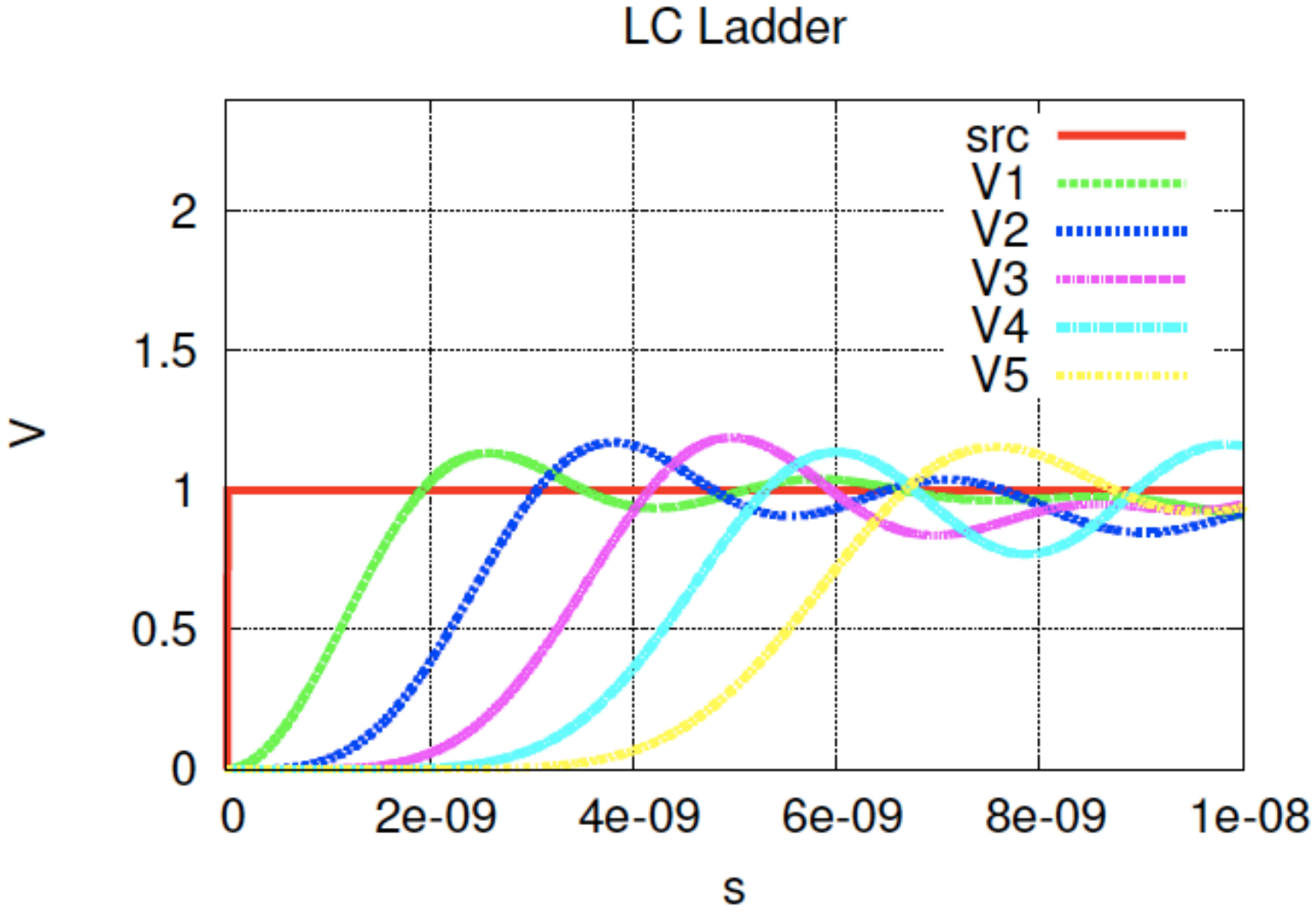
Open


1u
1u
1u
1u
1u
1p
1p
1p
1p
1p

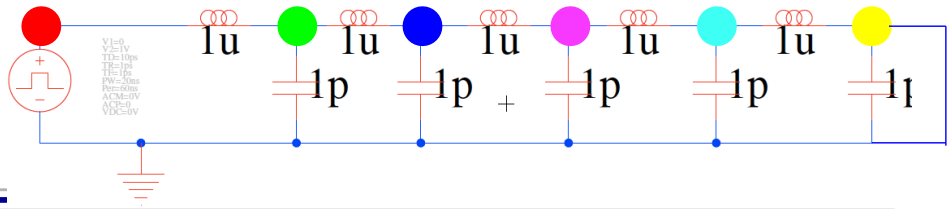

LC Ladder
src
V1
V2
V3
V4
V5
2
1.5
1
0.5
0
V
0
2e-09
4e-09
6e-09
8e-09
1e-08
s

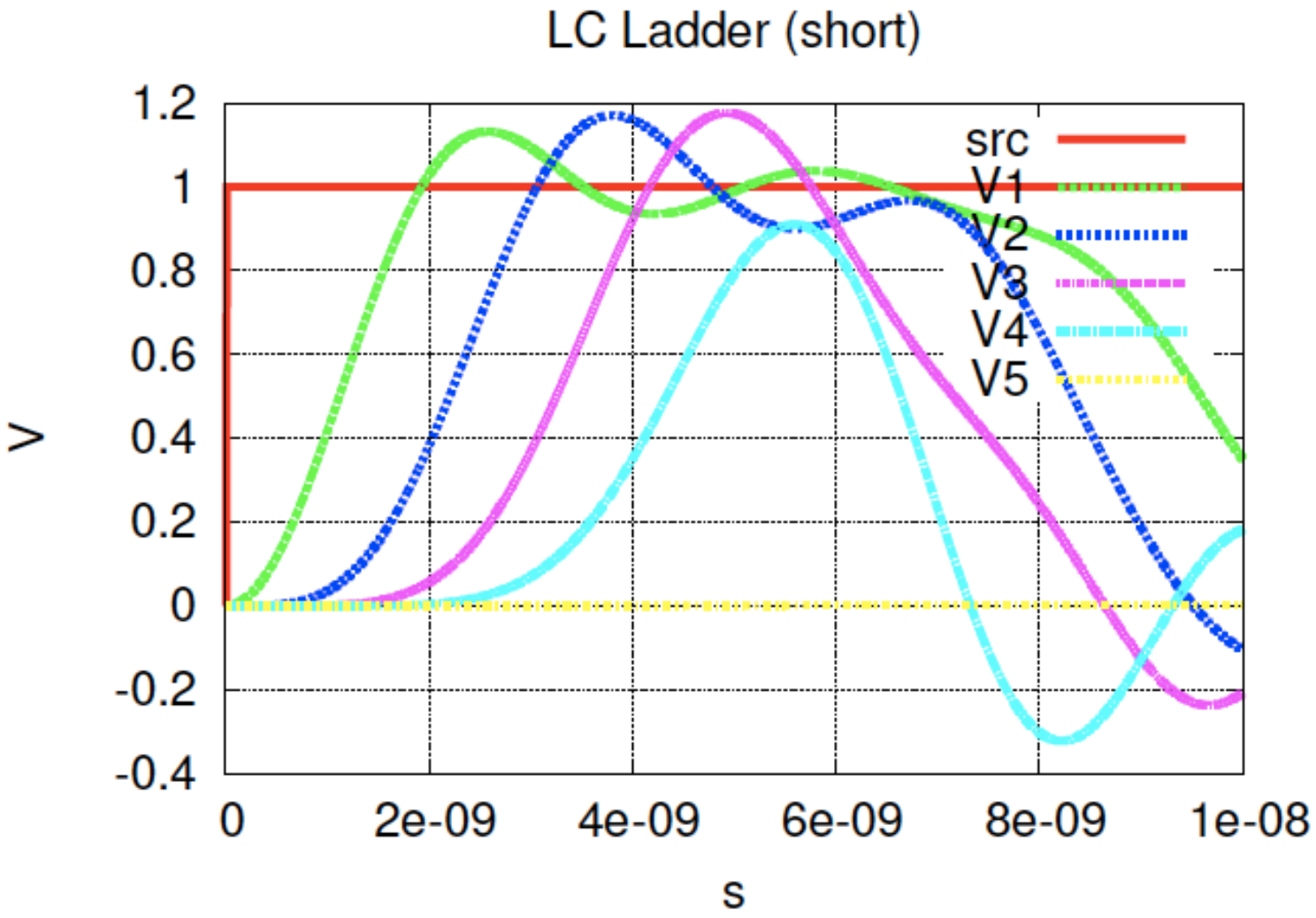
Terminate R=Z_0





Short


1u
1u
1u
1u
1u
1p
1p
1p
1p
1p

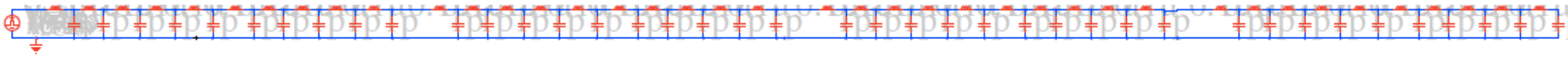

LC Ladder (short)
1.2
1
0.8
0.6
0.4
0.2
0
-0.2
-0.4
V
0
2e-09
4e-09
6e-09
8e-09
1e-08
s
src
V1
V2
V3
V4
V5

Longer LC (open)

- 40 Stages
- L=100nH
- C=1pF

$$w = \frac{1}{\sqrt{LC}}$$

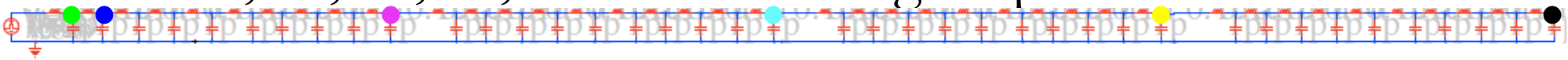
Stage delay? How long to propogate?

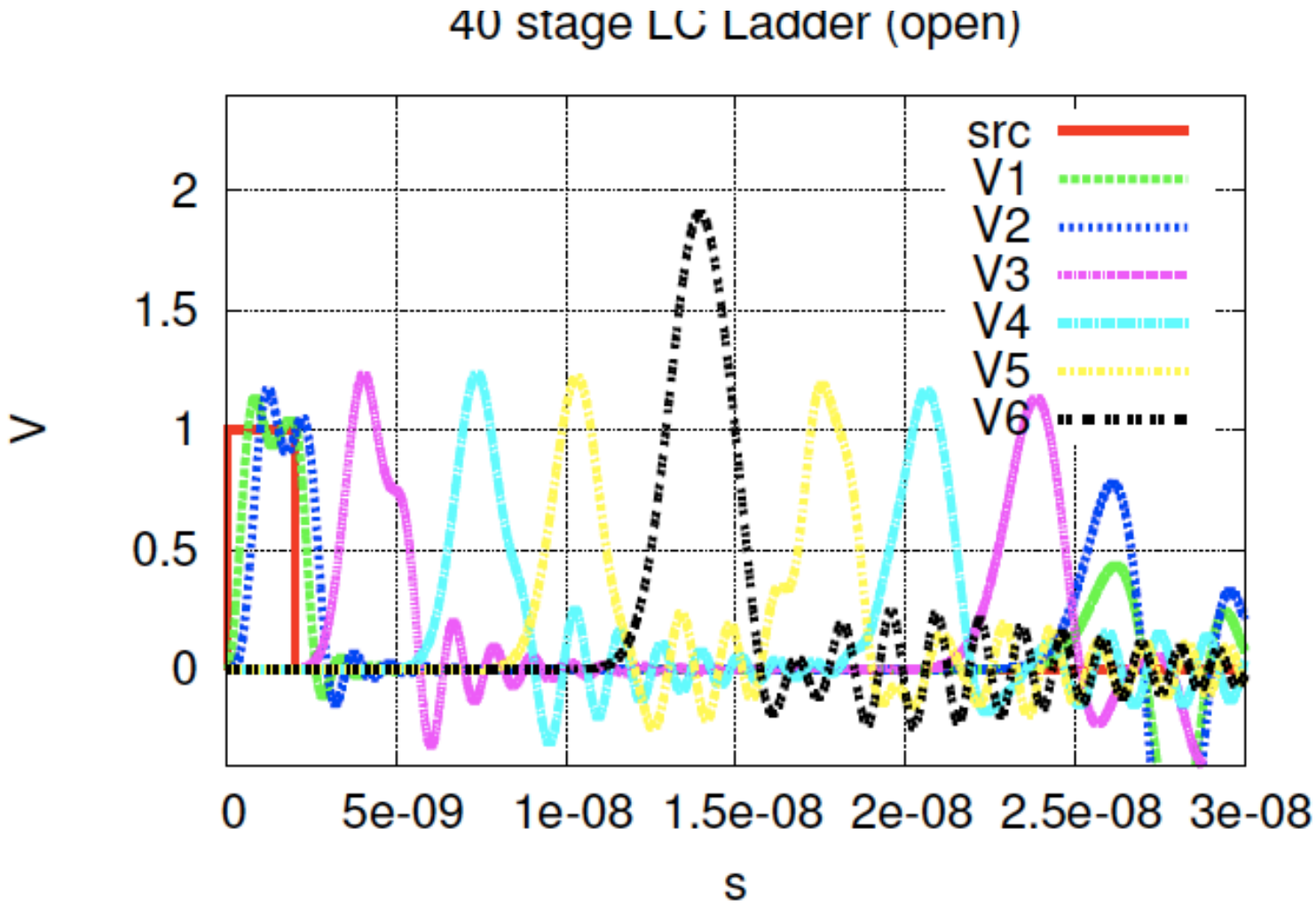


- Drive with 2ns Pulse
- No termination (open circuit)
  - What reflection do we expect?

Pulse Travel RC

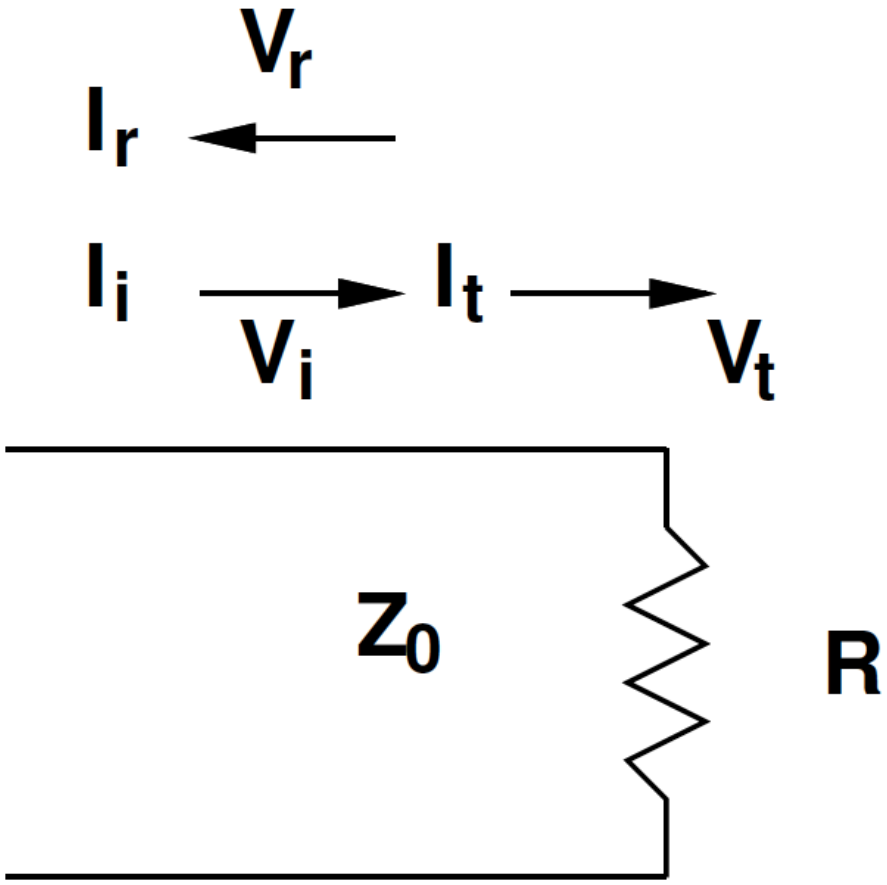
- V1,V3,V4,V5,V6 about 10 stages apart

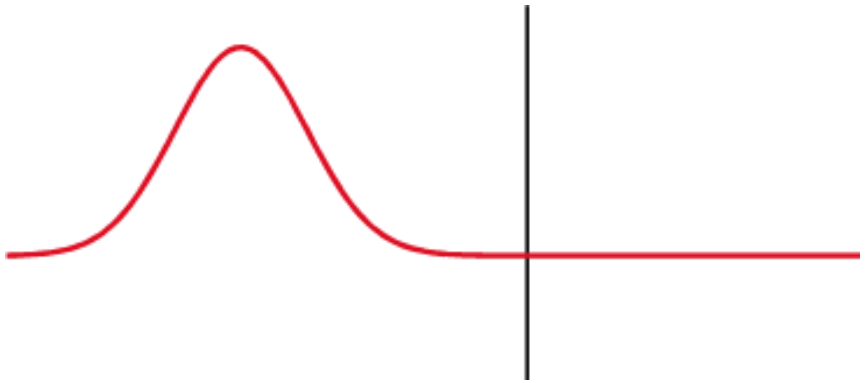




Analyze End of Line

- *I*ncident Wave, *R*eflected Wave, *T*ransverse Wave

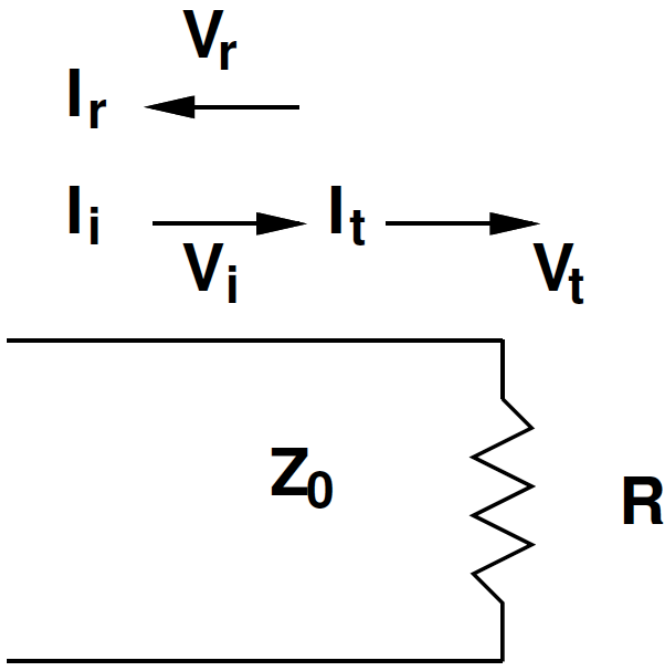




Source: https://en.wikipedia.org/wiki/Reflection_coefficient

Analyze End of Line

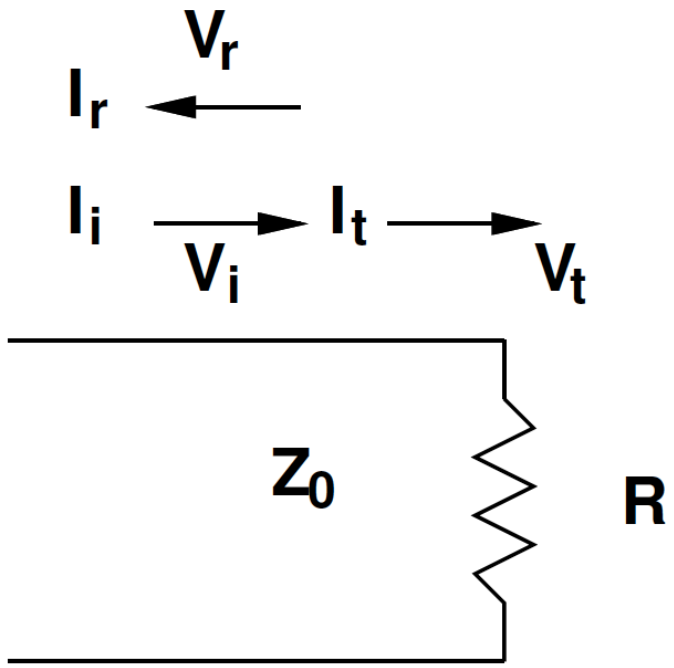
- Incident wave $V_i = I_i \times Z_0$
- @ T-δ V_i is voltage on line
- V_t is what goes forward
  - Voltage seen by end of line at T
- V_r is the reflected voltage that starts moving back towards source at T+δ



Reflection

Reflection coefficient

$$V_i\left(\frac{R - Z_0}{R + Z_0}\right) = V_r$$



Analyze End of Line

- $V_i+V_r=V_t$

$$V_i\left(\frac{R-Z_0}{R+Z_0}\right)=V_r$$

$$V_i\left(\frac{R-Z_0}{R+Z_0}\right)=V_t-V_i$$

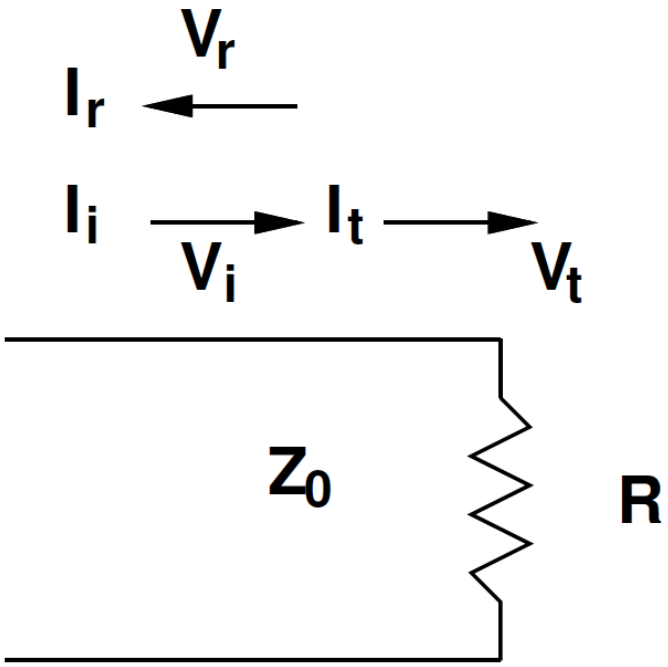
$$V_i\left(\frac{R-Z_0}{R+Z_0}+1\right)=V_t$$

$$V_i\left(\frac{2R}{R+Z_0}\right)=V_t$$

Transmission coefficient

Reflection

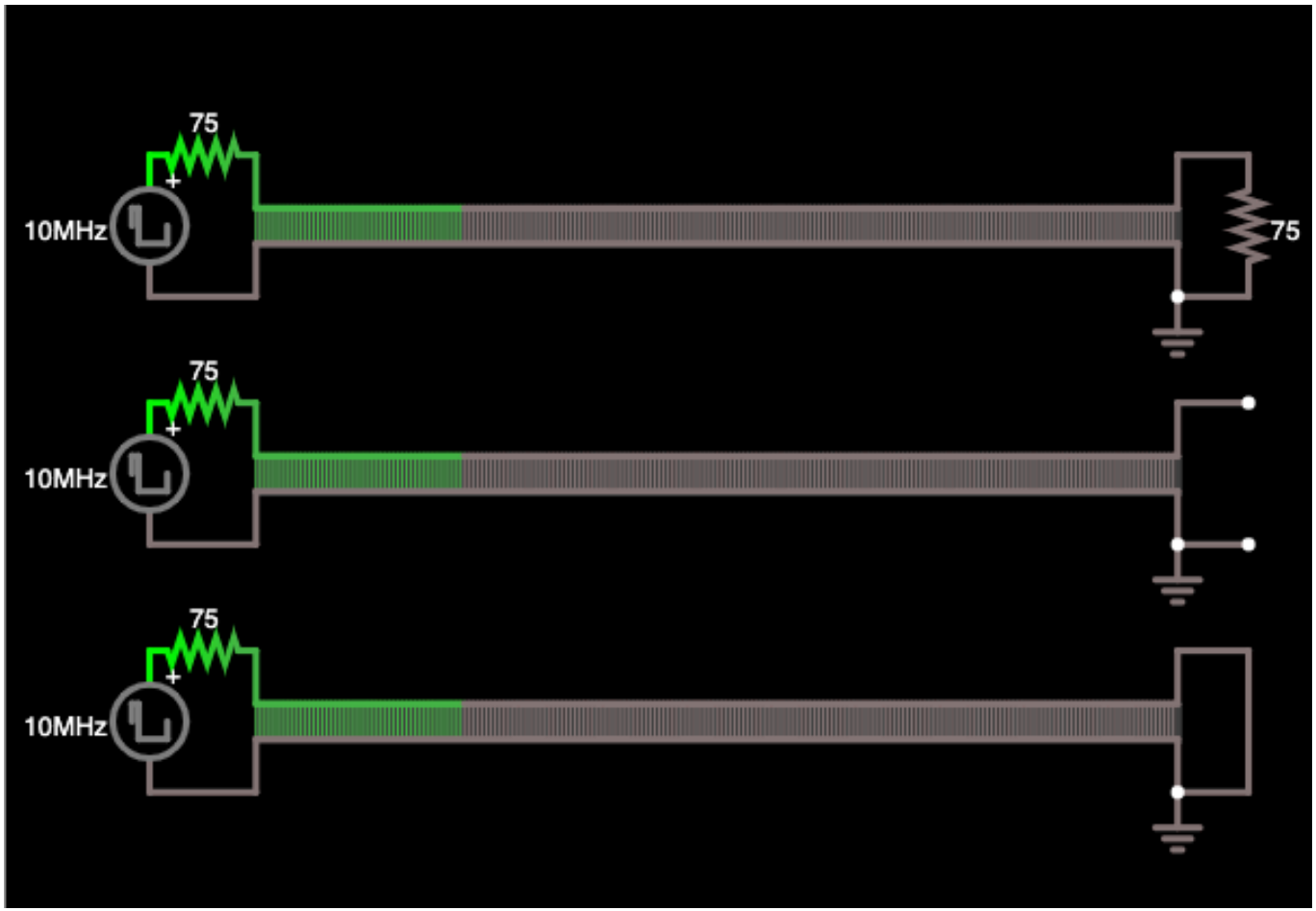
- Sanity check with previous
  - Short
  - Matched
  - Open



$$V_i\left(\frac{R-Z_0}{R+Z_0}\right)=V_r$$

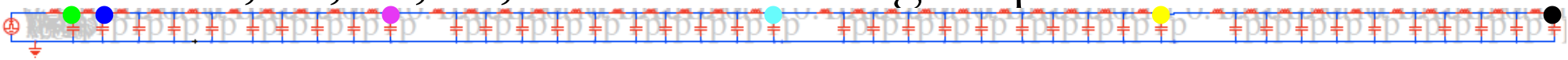
Visualization

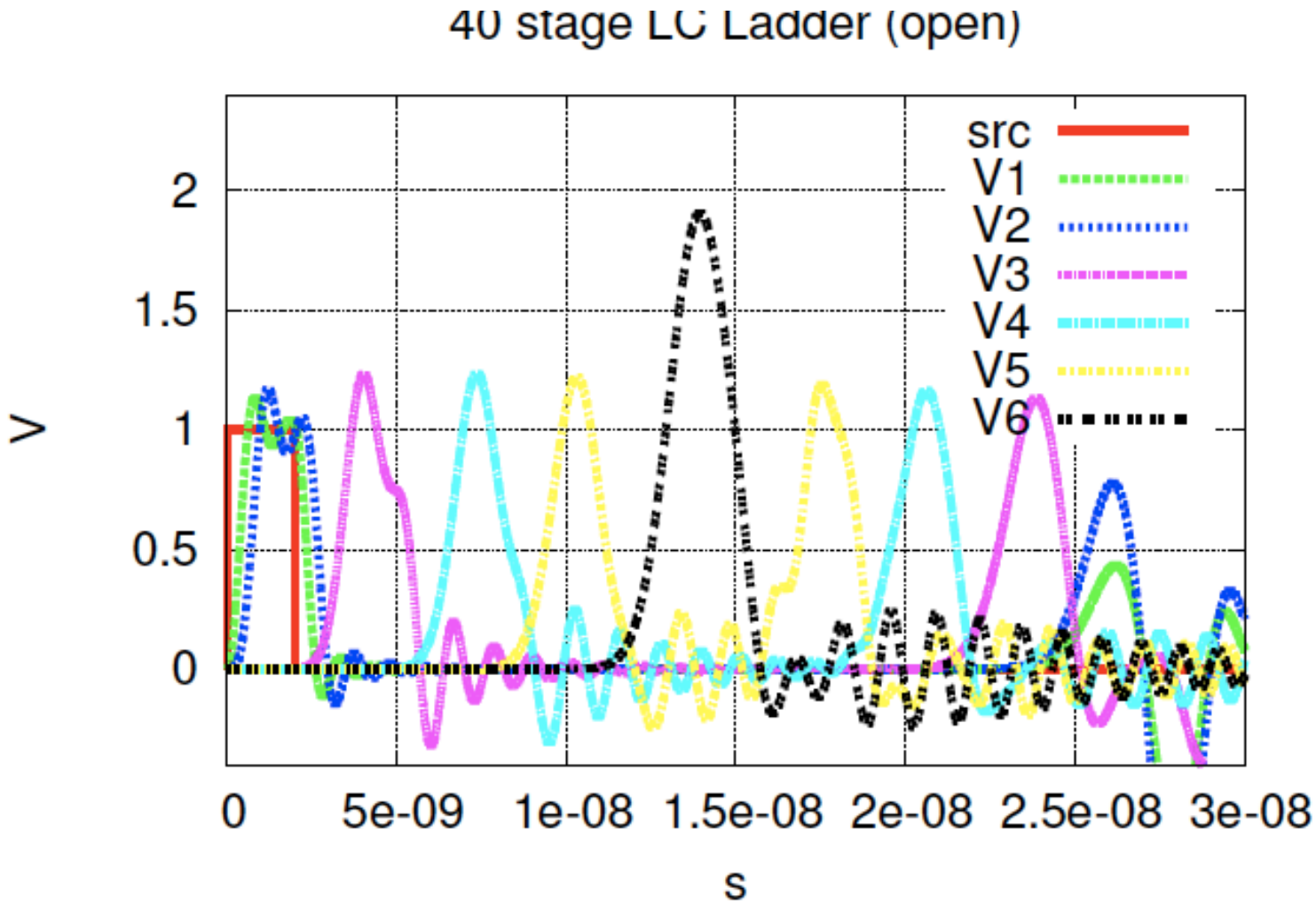
- https://tinyurl.com/y2jortrq

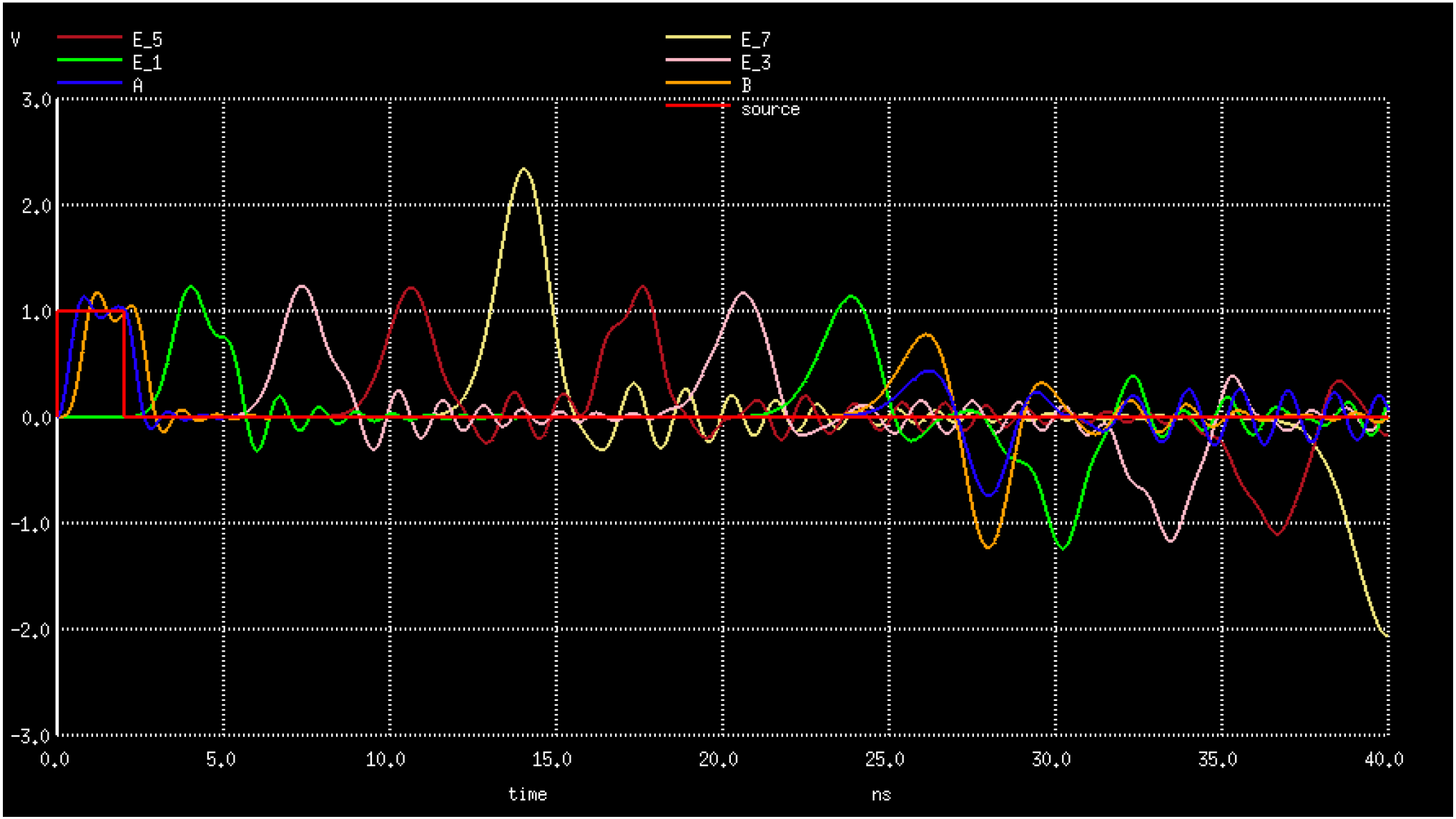


Pulse Travel RC

- V1,V3,V4,V5,V6 about 10 stages apart






V
E_5
E_1
A
E_7
E_3
B
source
3.0
2.0
1.0
0.0
-1.0
-2.0
-3.0
0.0
5.0
10.0
15.0
20.0
25.0
30.0
35.0
40.0
time
ns

Back to Source

Back at Source? (Preclass 5)

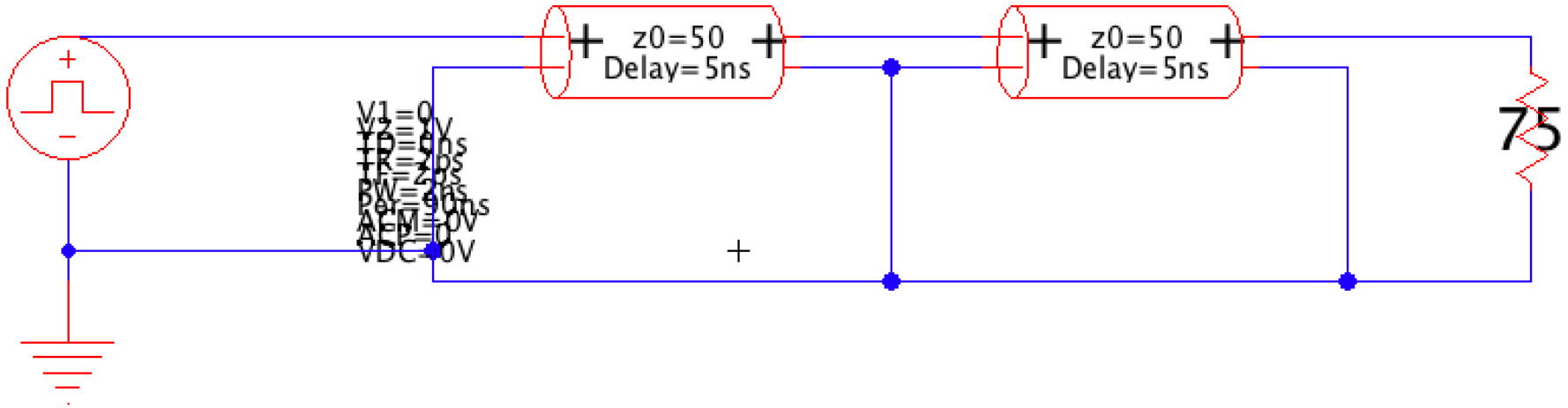
- What happens at source?
  - Depends on how it's terminated
  - Looks like a sink end now

$R \neq Z_0$

- What happens?
  - 75 Ω termination on 50 Ω line

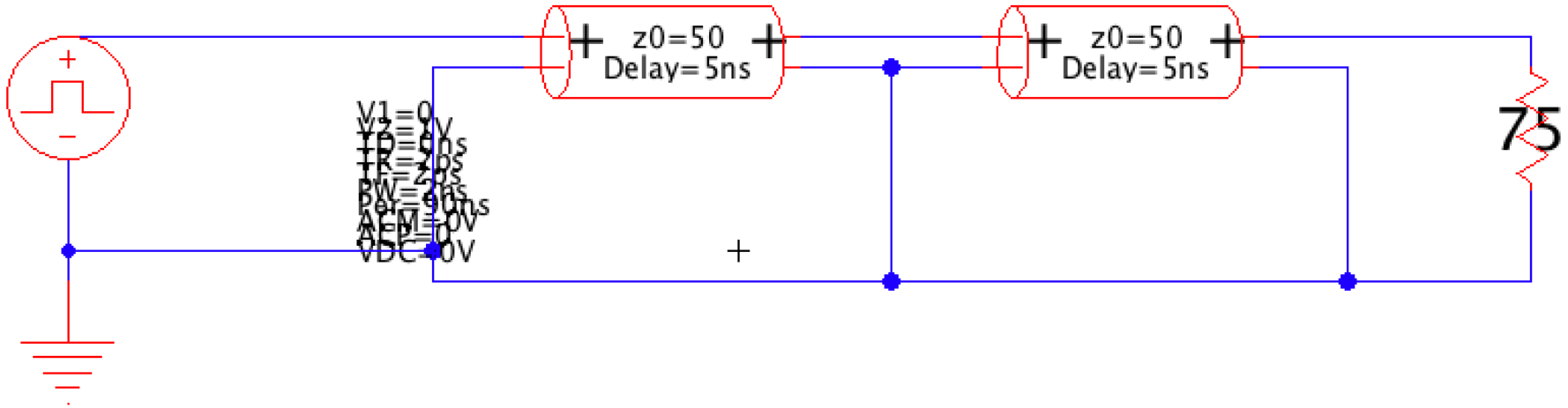
Transmission Line Symbol

- Specify delay of full Tline and characteristic impedance
- Need reference

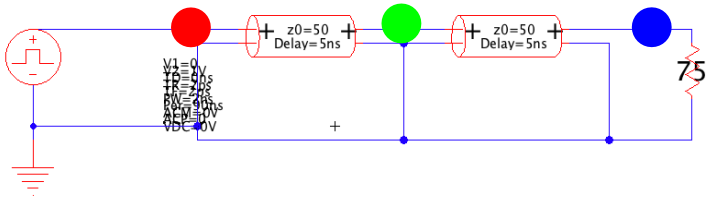


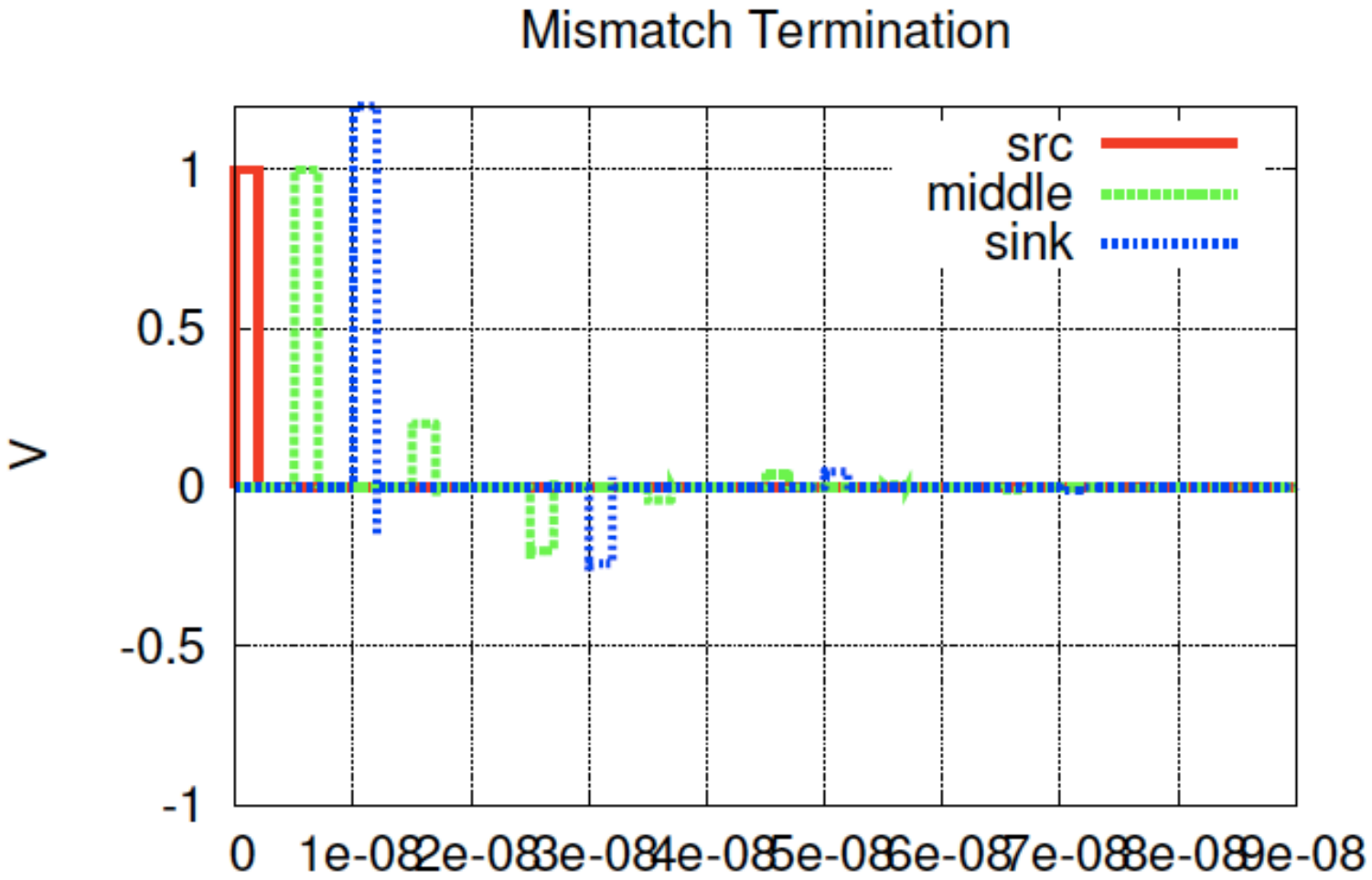
Simulation (Preclass 6)

- For these, with direct drive from voltage source
  - Source looks like short circuit (not typical of CMOS)
    - Source cannot be changed



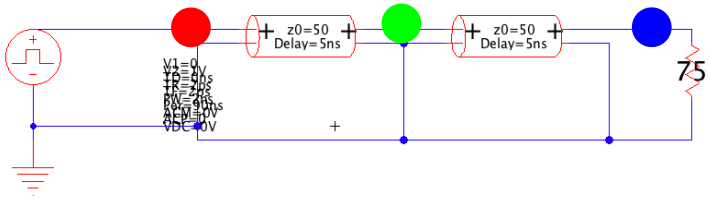
50Ω line, 75Ω termination

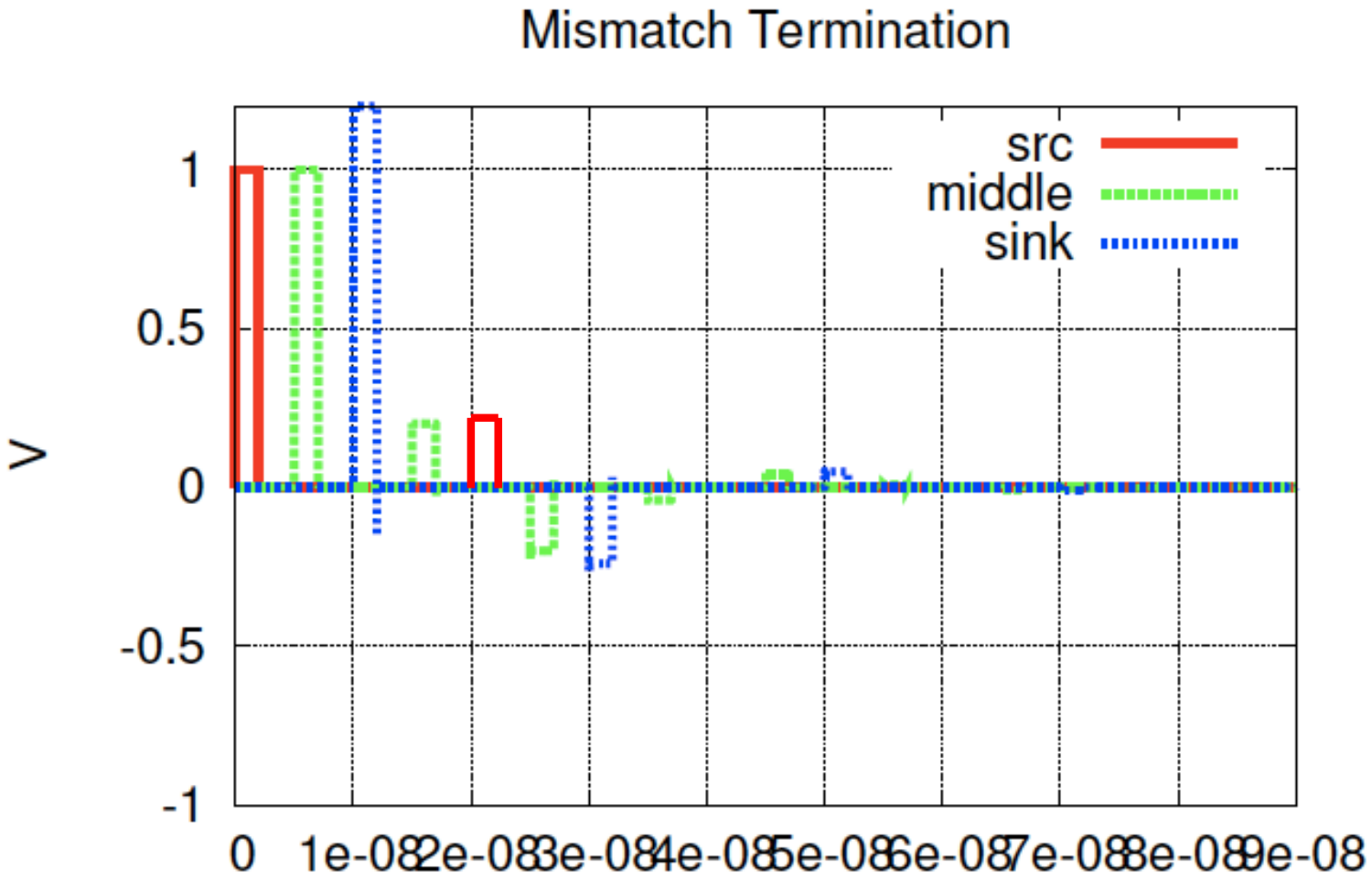




$$V_r = V_i\left(\frac{R - Z_0}{R + Z_0}\right) \overset{S}{=} V_i\left(\frac{75 - 50}{75 + 50}\right) = 0.2V_i$$

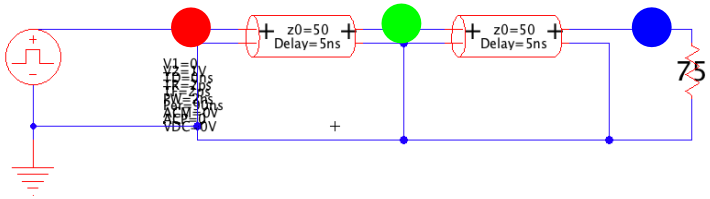
50Ω line, 75Ω termination

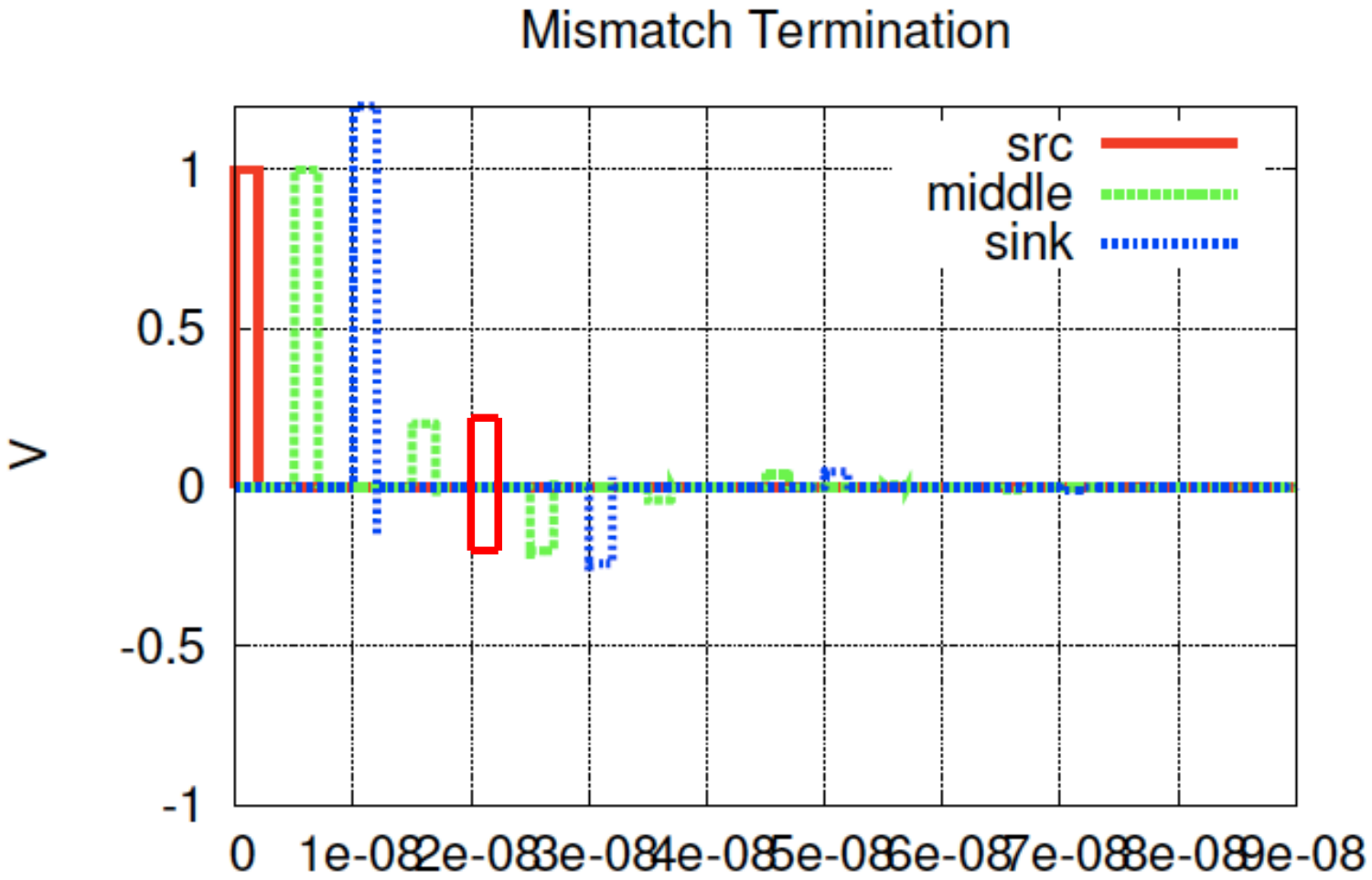




$$V_r = V_i\left(\frac{R - Z_0}{R + Z_0}\right) \overset{S}{=} V_i\left(\frac{75 - 50}{75 + 50}\right) = 0.2V_i$$

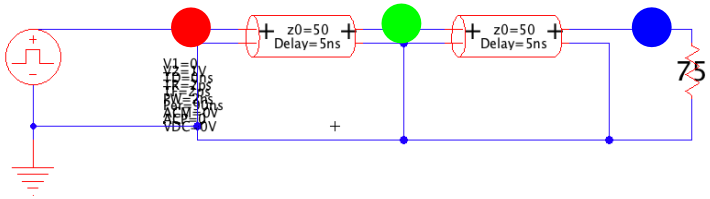
50Ω line, 75Ω termination

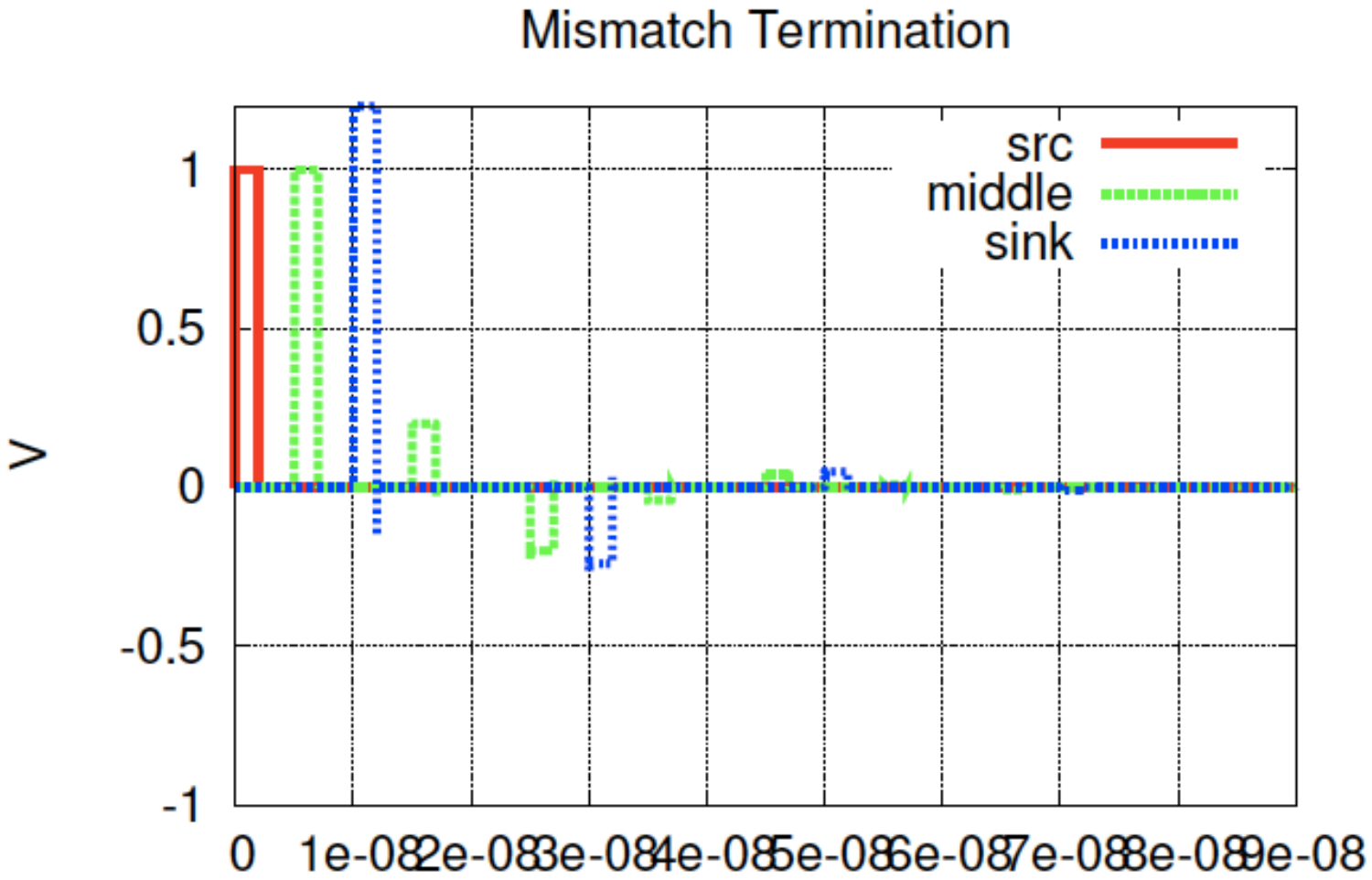




$$V_r = V_i\left(\frac{R - Z_0}{R + Z_0}\right) \overset{S}{=} V_i\left(\frac{75 - 50}{75 + 50}\right) = 0.2V_i$$

50Ω line, 75Ω termination

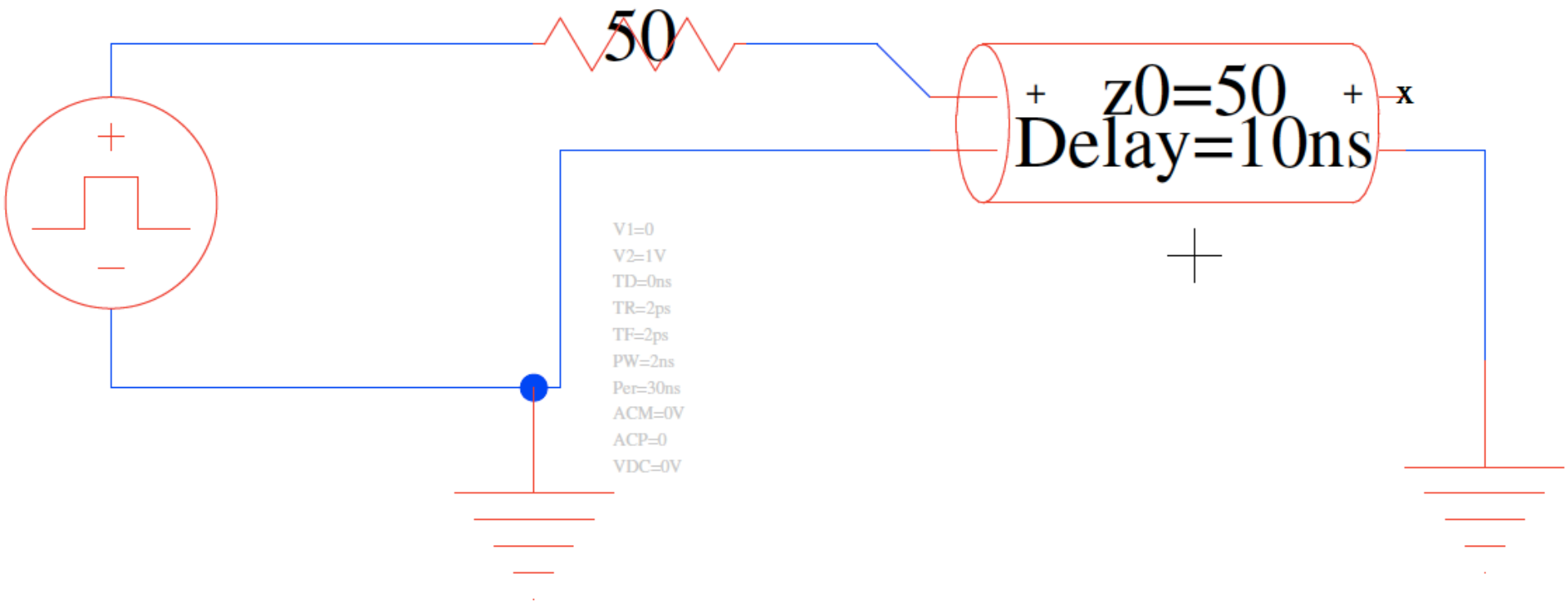




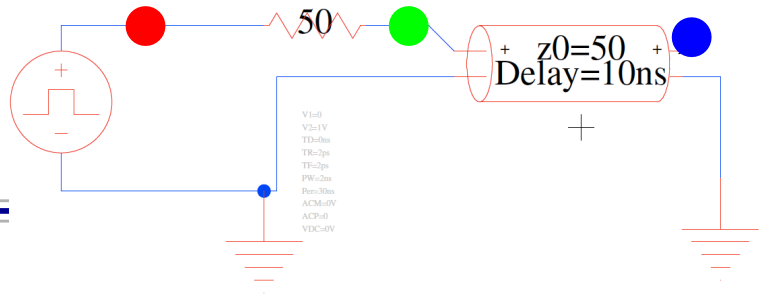
$$V_r = V_i\left(\frac{R - Z_0}{R + Z_0}\right) \overset{S}{=} V_i\left(\frac{75 - 50}{75 + 50}\right) = 0.2V_i$$

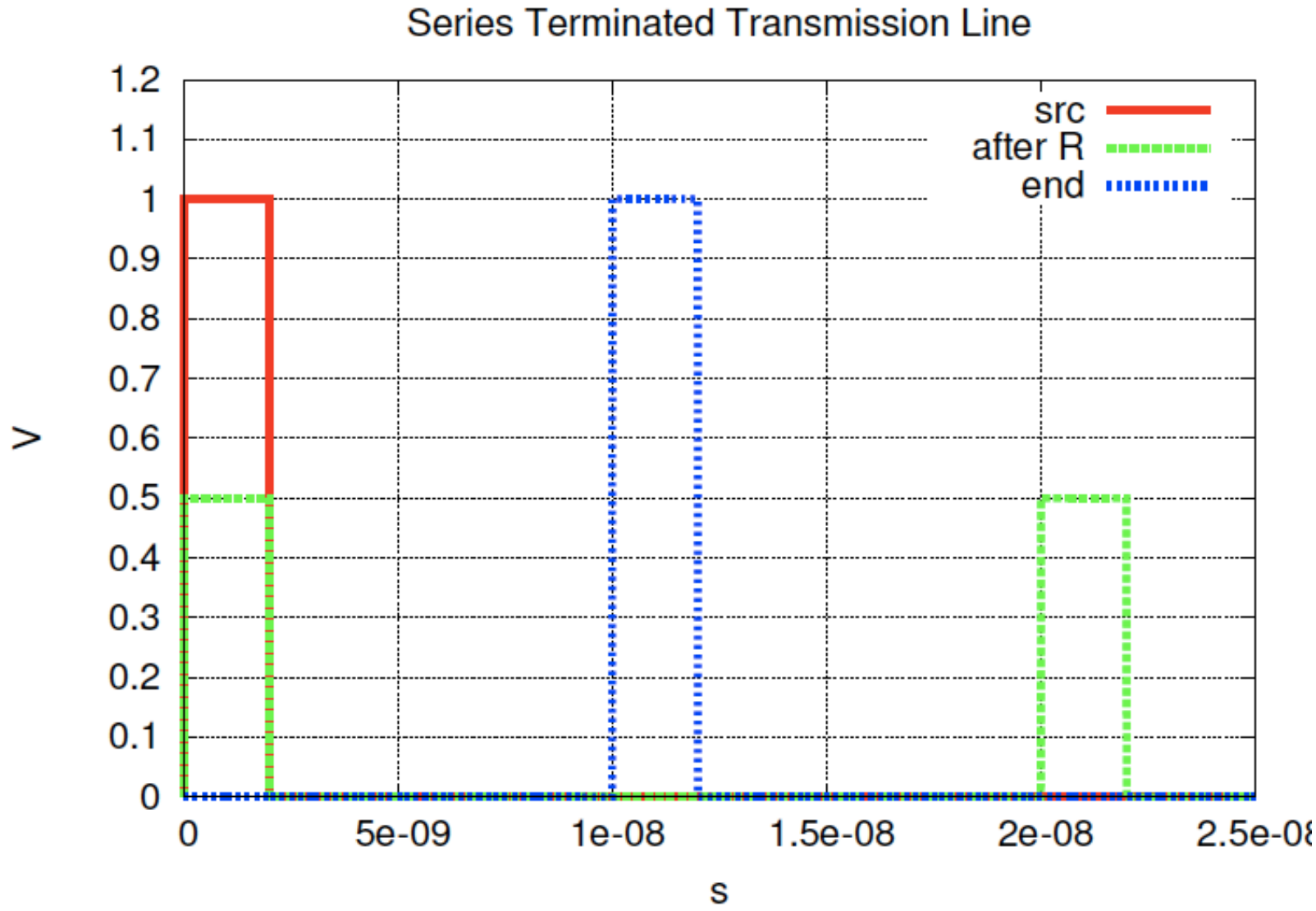
Source Series Termination

- What happens here?



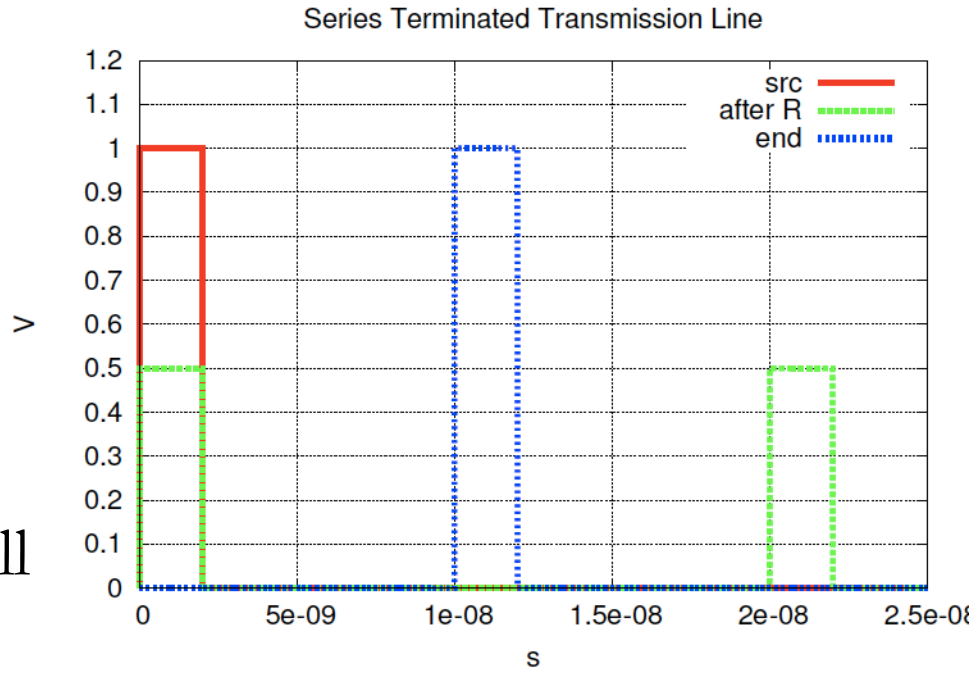
Simulation

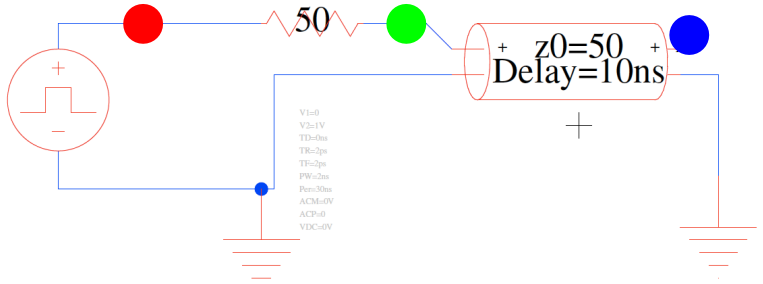

50
z0=50
Delay=10ns


Series Terminated Transmission Line
src
after R
end
1.2
1.1
1
0.9
0.8
0.7
0.6
0.5
0.4
0.3
0.2
0.1
0
V
0
5e-09
1e-08
1.5e-08
2e-08
2.5e-08
s

Series Termination

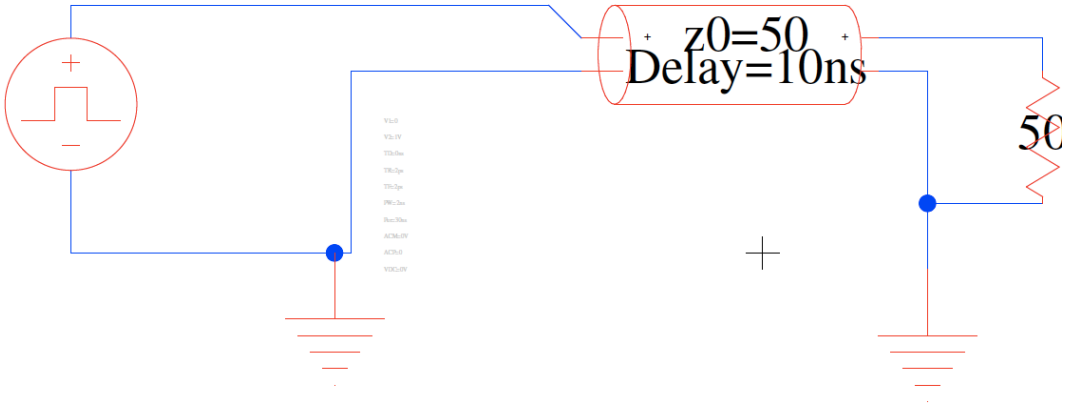
- $R_{series} = Z_0$
- Initial voltage divider
  - Half voltage pulse propogates down Tline
- End of line open circuit
  - Sees single transition to full voltage (full reflection)
- Reflection returns to source and sees termination $R_{series} = Z_0$
- No further reflections



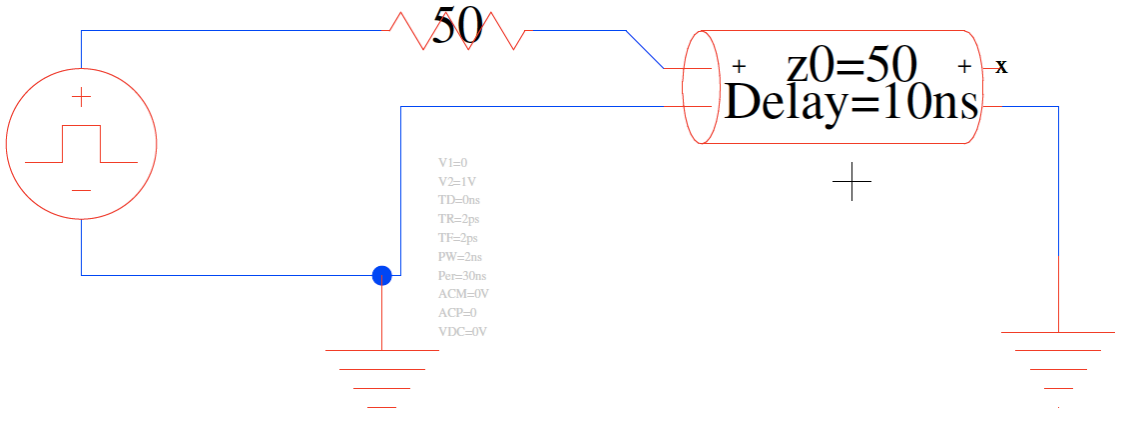


Termination Cases

- Termination in parallel at Sink

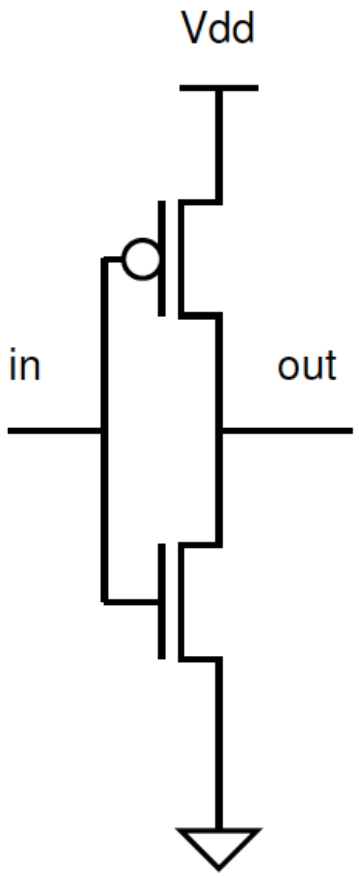


- Termination in series at Source



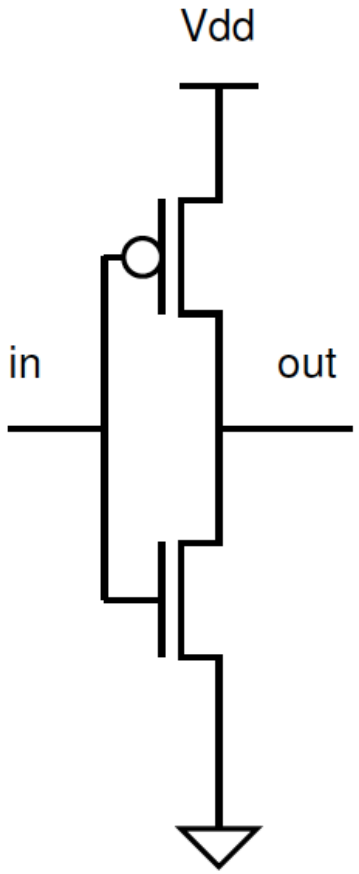
CMOS Driver / Receiver

- Driver: What does a CMOS driver look like at the source?
  - $I_{d,sat}$=1200μA/μm @ 45nm, V_{dd}=1V
- Receiver: What does a CMOS inverter look like at the sink?



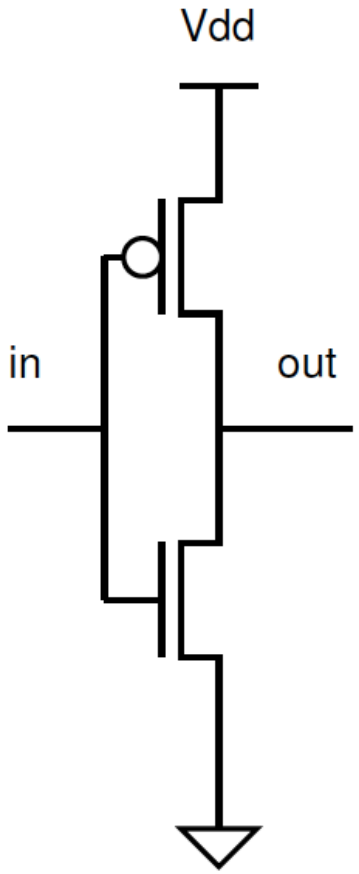
CMOS Driver

- Driver: What does a CMOS driver look like at the source?
  - $I_{d,sat}$=1200μA/μm @ 45nm, V_{dd}=1V
  - Min size:
    - I_{drive}=1200μA/μm*45nm=54μA
    - $R_{out}=V_{dd}/I_{drive}$=18kΩ



CMOS Driver

- Driver: What does a CMOS driver look like at the source?
  - $I_{d,sat}$=1200μA/μm @ 45nm, V_{dd}=1V
  - Min size:
    - I_{drive}=1200μA/μm*45nm=54μA
    - $R_{out}=V_{dd}/I_{drive}$=18kΩ
  - W=370
    - I_{drive}=1200μA/μm*45nm*370=20mA
    - $R_{out}=V_{dd}/I_{drive}$=50Ω



Idea

- Signal propagates as wave down transmission line
  - Delay linear in wire length
  - Speed
  - Impedance
- Behavior at end of line depends on termination
- Both src and sink are "ends" with reflections

$$w = \frac{1}{\sqrt{LC}} = \frac{c_0}{\sqrt{\varepsilon_r \mu_r}}$$

$$Z_0 = \sqrt{\frac{L}{C}}$$

$$V_r = V_i \left(\frac{R - Z_0}{R + Z_0} \right)$$

Transmission Line Agenda

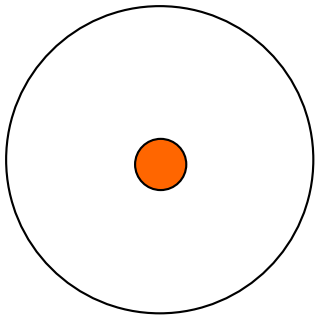
- ~~See in action in lab~~
- ~~Where transmission lines arise?~~
- ~~General wire formulation~~
- ~~Lossless Transmission Line~~
- ~~Impedance~~
- ~~End of Transmission Line?~~
  - ~~Open, short, matched~~
- Physical Geometry
- Discuss Lossy
- Implications/Effects

Transmission Lines Specifics

Characteristics arise form their geometry

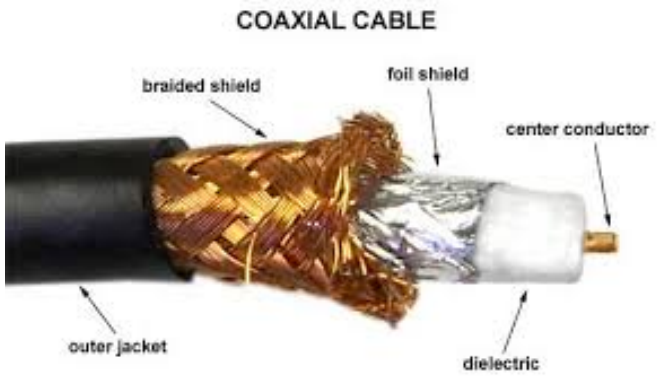
Coaxial Cable

- Inner core conductor: radius r
- Insulator: out to radius R
- Outer core shield (ground)



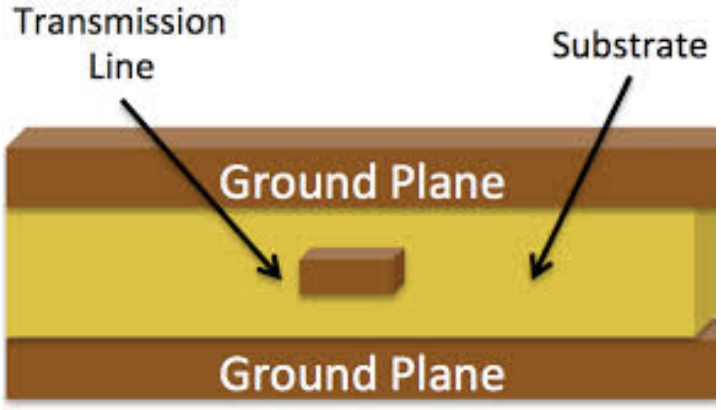
$$L = \left(\frac{\mu}{2\pi}\right)\ln\left(\frac{R}{r}\right) \qquad Z_0 = \left(\frac{1}{2\pi}\right)\left(\sqrt{\frac{\mu}{\varepsilon}}\right)\ln\left(\frac{R}{r}\right)$$

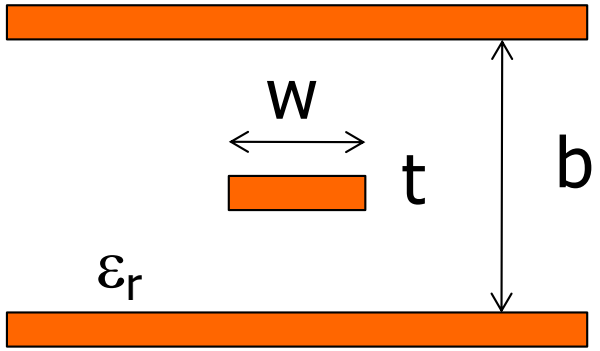
- RG-58 Z_0= 50Ω – networking
- RG-59 Z_0= 75Ω – video
- HDMI Z_0= 100Ω – video



Printed Circuit Board

- Stripline
  - Trace between ground planes

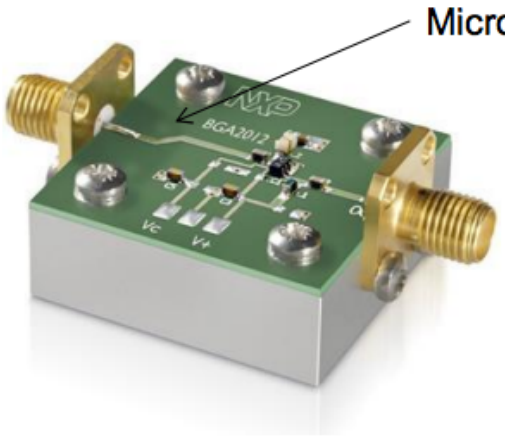


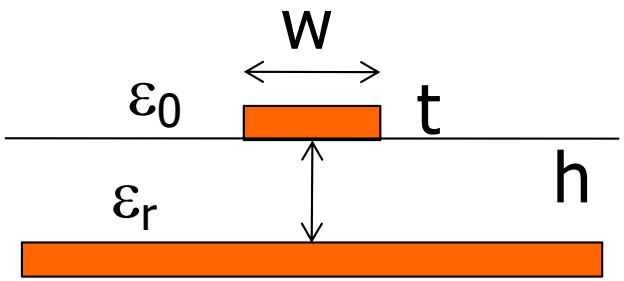


$$Z_0 = \left(\frac{1}{4}\right)\left(\sqrt{\frac{\mu}{\varepsilon}}\right)\ln\left(\frac{1+W/b}{t/b+W/b}\right)$$

Printed Circuit Board

- Microstrip line
  - Trace over single supply plane





$$Z_0 = \left(\frac{1}{2\pi}\right)\left(\sqrt{\frac{\mu}{(0.475\varepsilon_r + 0.67)\varepsilon_0}}\right)\ln\left(\frac{4h}{0.536W + 0.67t}\right)$$

Twisted Pair

- Category 5 ethernet cable
  - $Z_0=100\Omega$
  - $w=0.64c_0$

Implications

Example (Preclass 7)

- 25 meter category-5e cable (Z_0=100Ω, w=0.64c)
  - c = $3x10^8$ m/s
- Supporting 1Gb/s ethernet
  - 4 pairs at 250Mb/s
- a) Time to send data from one end to the other?
- b) Time between bits at 250Mb/s?
- c) Bits on each pair in the cable?

Pipeline Bits

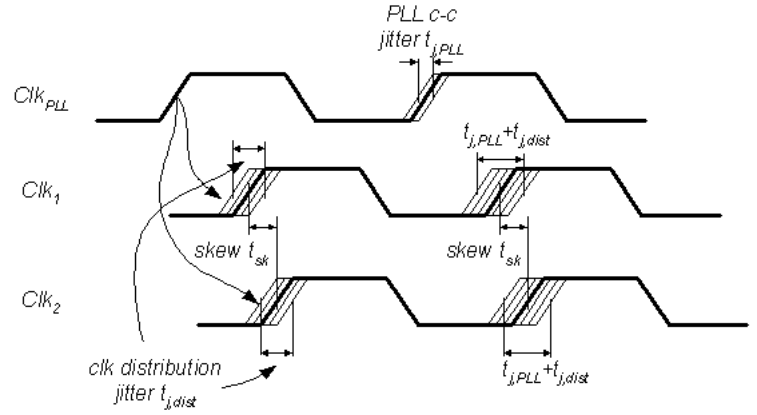
- For properly terminated transmission line
  - Do not need to wait for bits to arrive at sink
  - Can stick new bits onto wire

Limits to Bit Pipelining (Preclass 8)

- What limits? (why only 250Mb/s)

Limits to Bit Pipelining (Preclass 3)

- What limits? (why only 250Mb/s)
  - Rise time/signal distortion
  - Clocking
    - Skew
    - Jitter
  - For bus
    - Wire length differences between lines

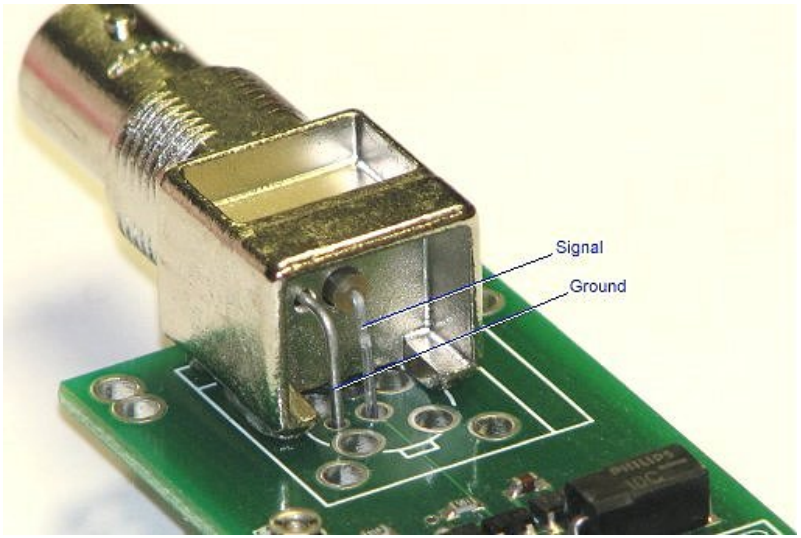


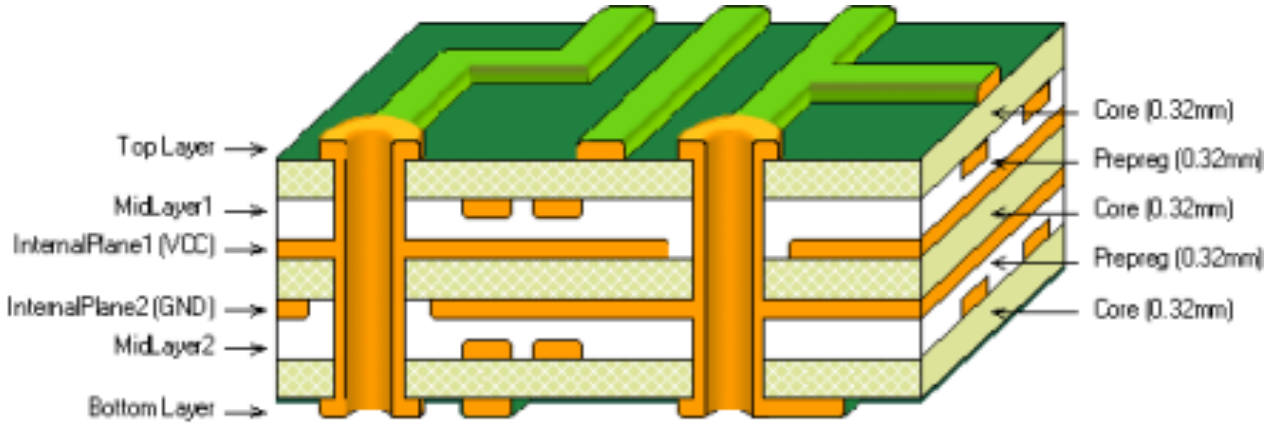
Termination / Mismatch

- Wires do look like these transmission lines
- We are terminating them in some way when we connect to chip (gate)
  - Need to be deliberate about how terminate, if we care about high performance

Where is Mismatch?

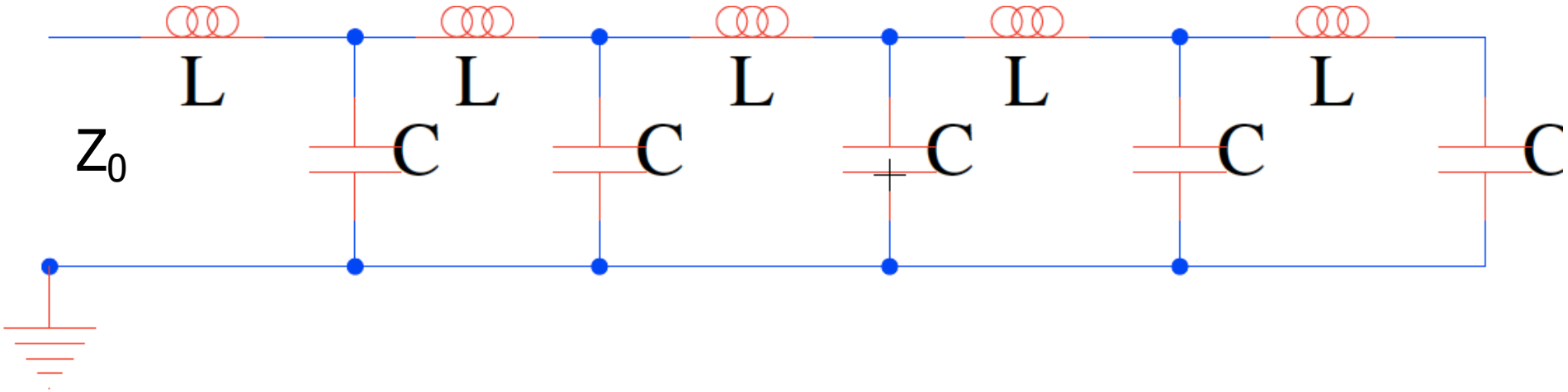
- Vias
- Wire corners
- Branches
- Connectors
- Board-to-cable
- Cable-to-cable





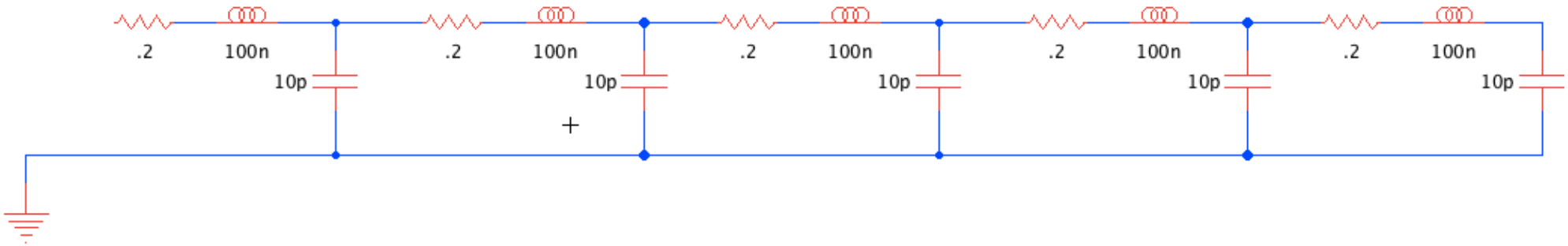
Lossless Transmission Line

- What prevents us from having a 500km cat-5 cable?



Lossy Transmission Line (Preclass 9)

- How do addition of R's change?
  - Concretely, discretely think about R=0.2Ω every meter on Z_0=100Ω
    - what does each R do? Voltage impact?



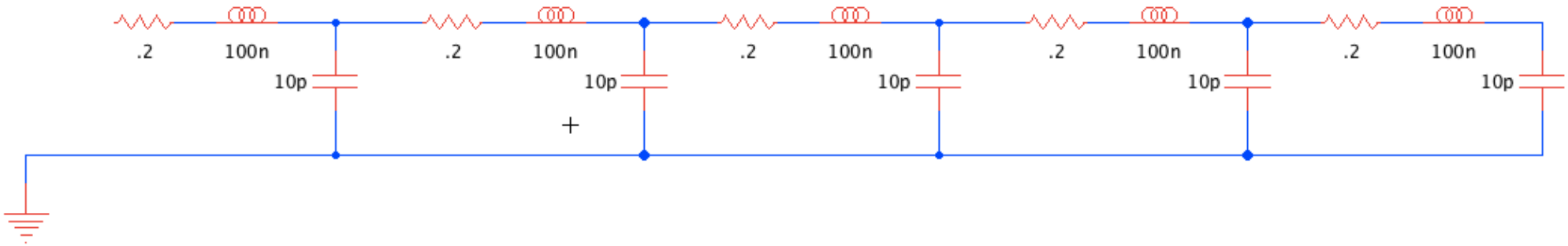
Lossy Transmission Line

- Each R is a mismatched termination

$$V_t = V_i\left(\frac{2(R+Z_0)}{(R+Z_0)+Z_0}\right)$$

- Each R is a voltage divider

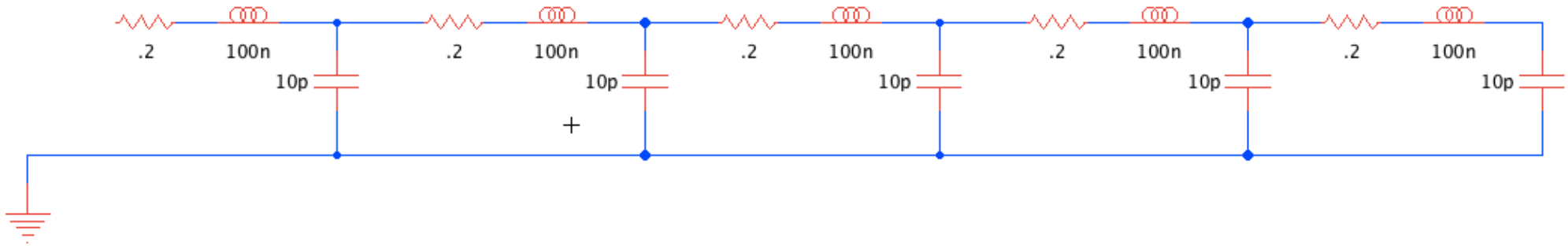
$$V_{i+1} = V_t\left(\frac{Z_0}{R+Z_0}\right)$$



Lossy Transmission Line

$$V_{i+1} = V_i \left(\frac{2(R + Z_0)}{(R + Z_0) + Z_0} \right) \left(\frac{Z_0}{R + Z_0} \right)$$

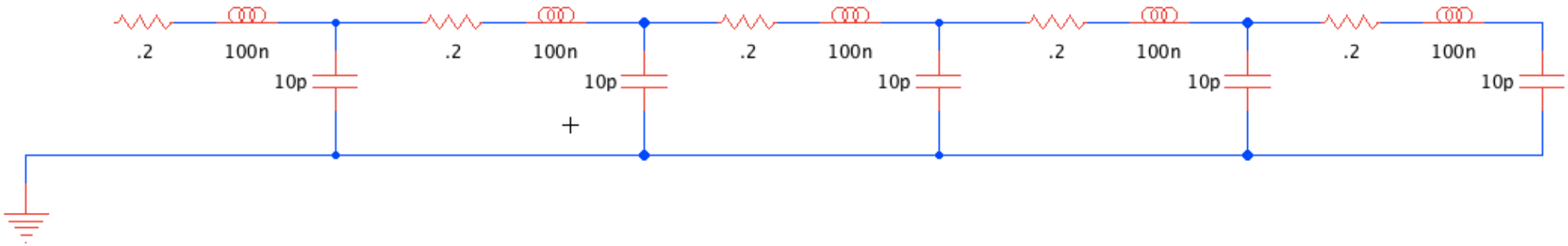
$$V_{snk} = V_{src} \left(\left(\frac{2(R + Z_0)}{(R + Z_0) + Z_0} \right) \left(\frac{Z_0}{R + Z_0} \right) \right)^N$$



Lossy Transmission Line (Preclass 9)

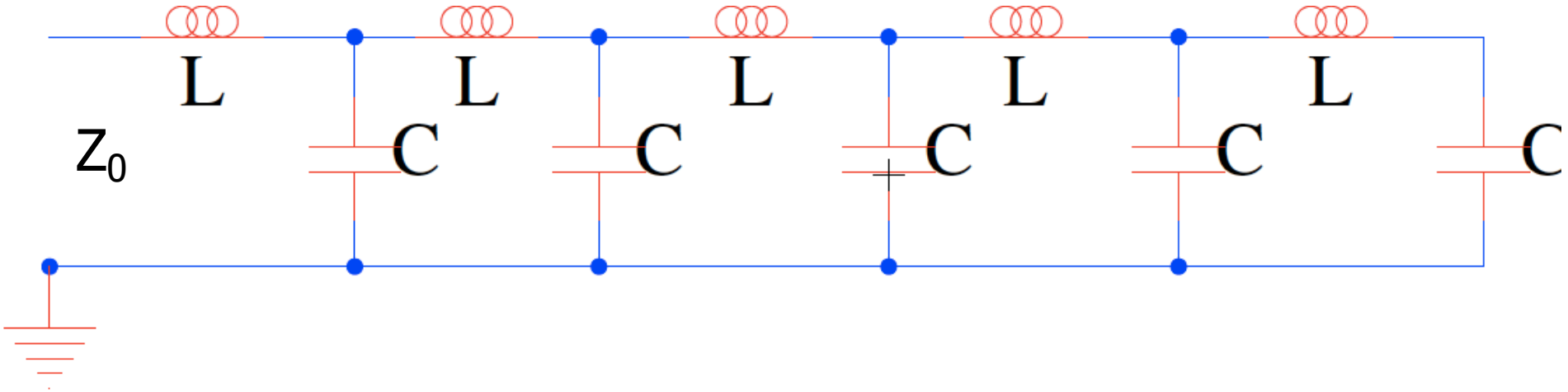
- How long before drop voltage by half?
  R=0.2Ω every meter on Z_0=100Ω

$$V_{snk} = V_{src}\left(\left(\frac{2(R+Z_0)}{(R+Z_0)+Z_0}\right)\left(\frac{Z_0}{R+Z_0}\right)\right)^N$$



Lossless Transmission Line

- What prevents us from having a 500km cat-5 cable?
  - Not actually lossless!

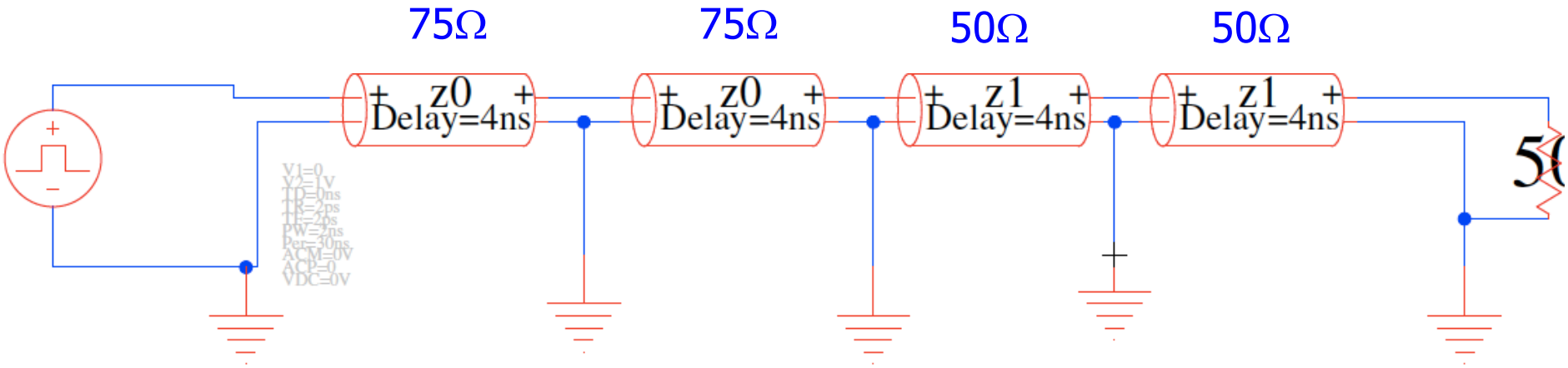


More Examples…

Time Permitting

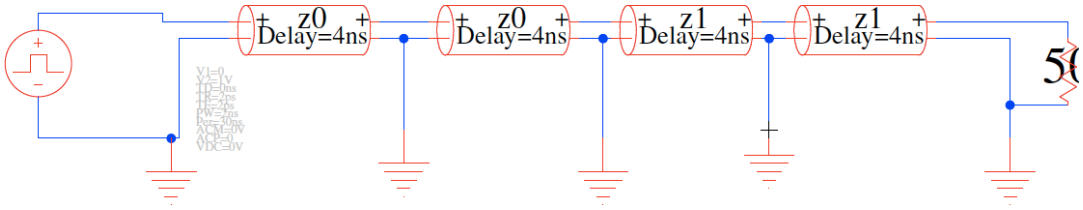
Impedance Change (Preclass 10)

- What happens if there is an impedance change in the wire? Z_0=75Ω, Z_1=50Ω
  - What reflections and transmission do we get?



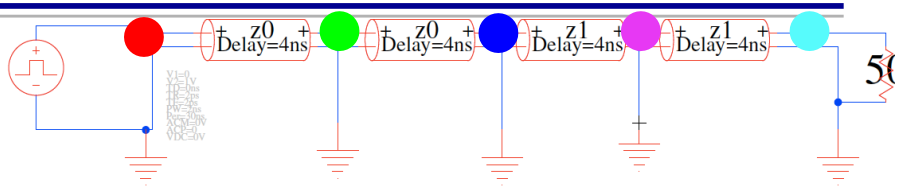
Z_0=75, Z_1=50 (Preclass 10)

- At junction:
  - Reflects
    - $V_r=(50-75)/(50+75)V_i=-0.2V_i$
  - Transmits
    - $V_t=(100/(50+75))V_i=0.8V_i$



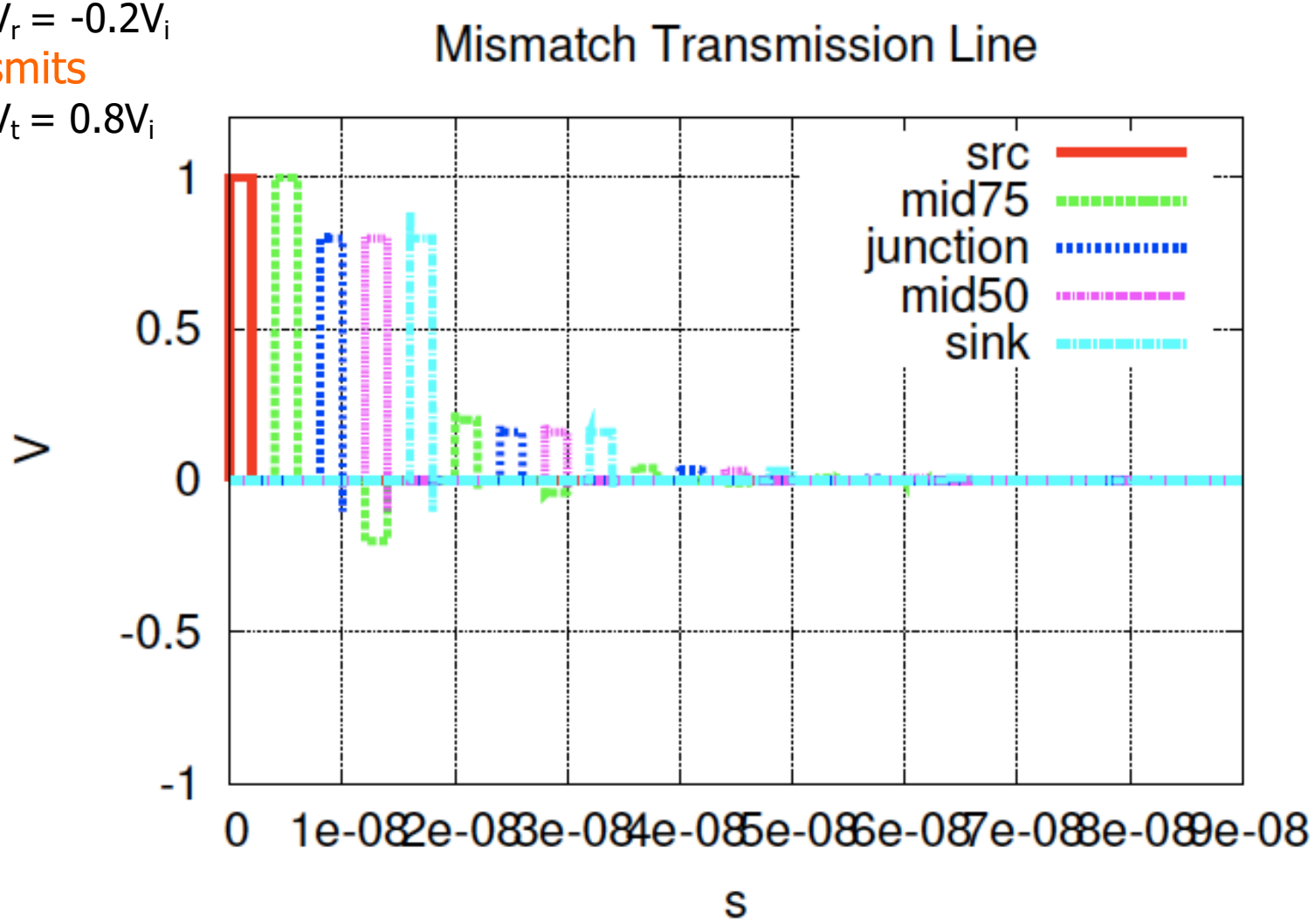
$$V_i\left(\frac{R-Z_0}{R+Z_0}\right)=V_r \qquad V_i\left(\frac{2R}{R+Z_0}\right)=V_t$$

Impedance Change Z_0=75, Z_1=50 (Preclass 10)

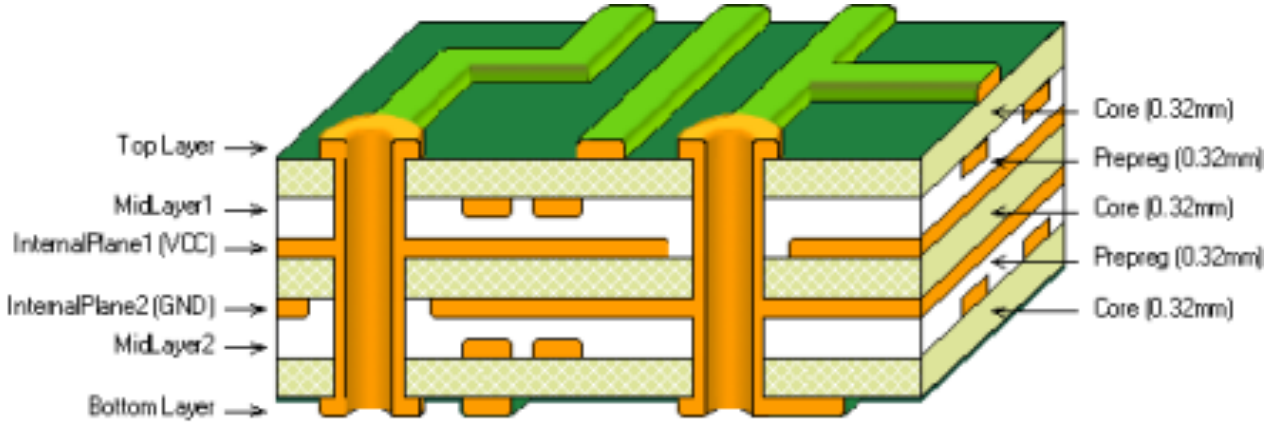


At junction:

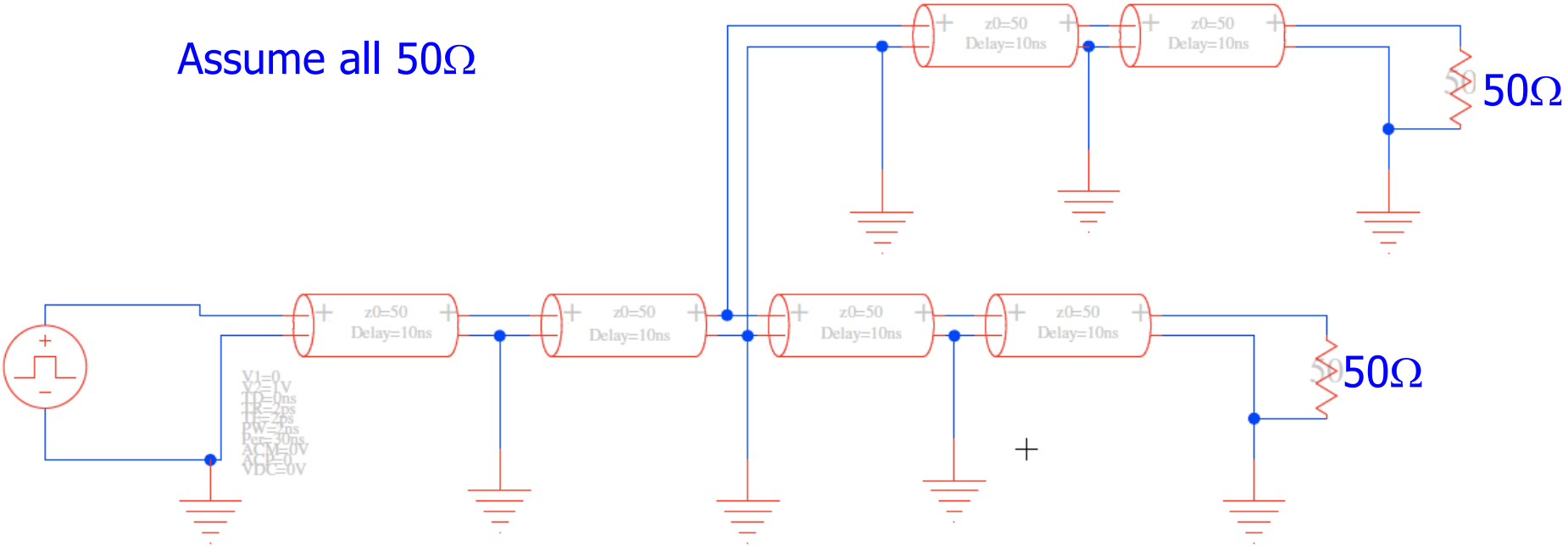
- Reflects
  - $V_r = -0.2V_i$
- Transmits
  - $V_t = 0.8V_i$



What happens at branch?

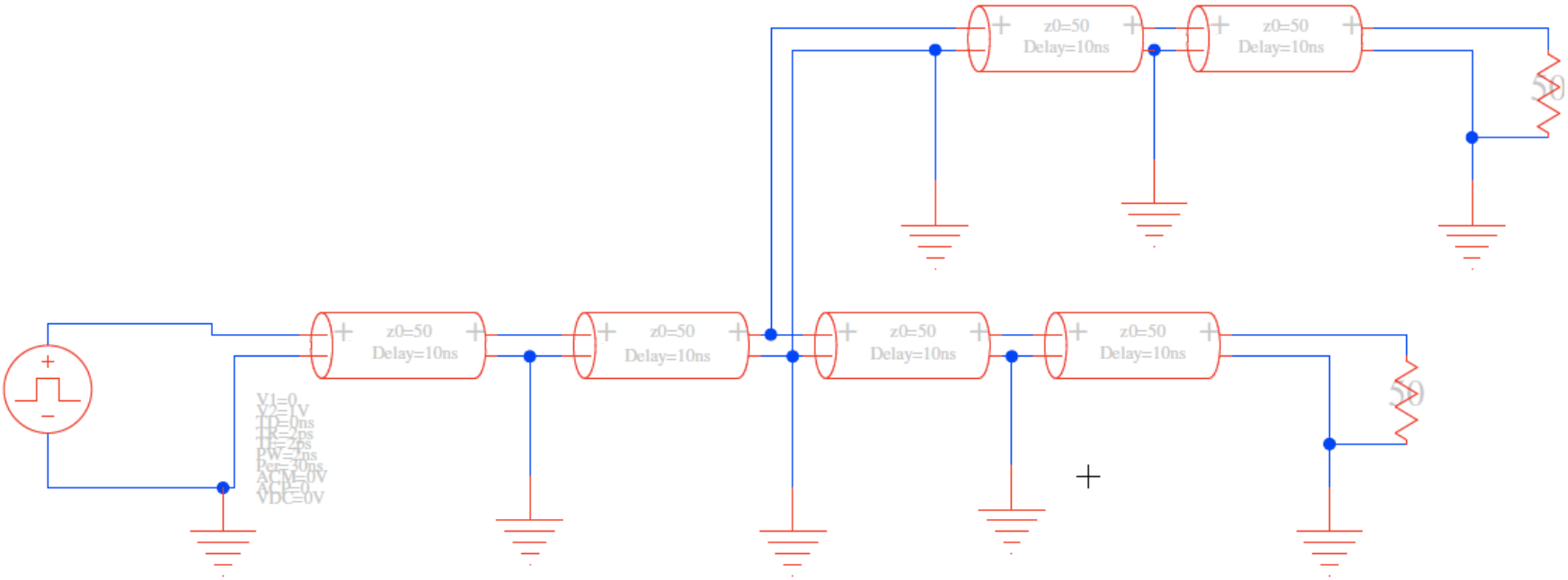


Assume all 50Ω

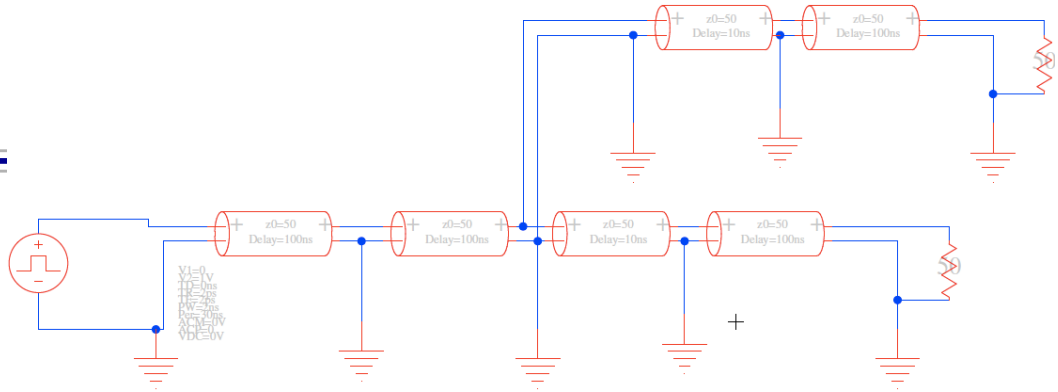


Branch (preclass 11)

- Transmission line sees two Z_0 in parallel
  - Looks like $Z_0/2$



$Z_0=50, Z_1=25$

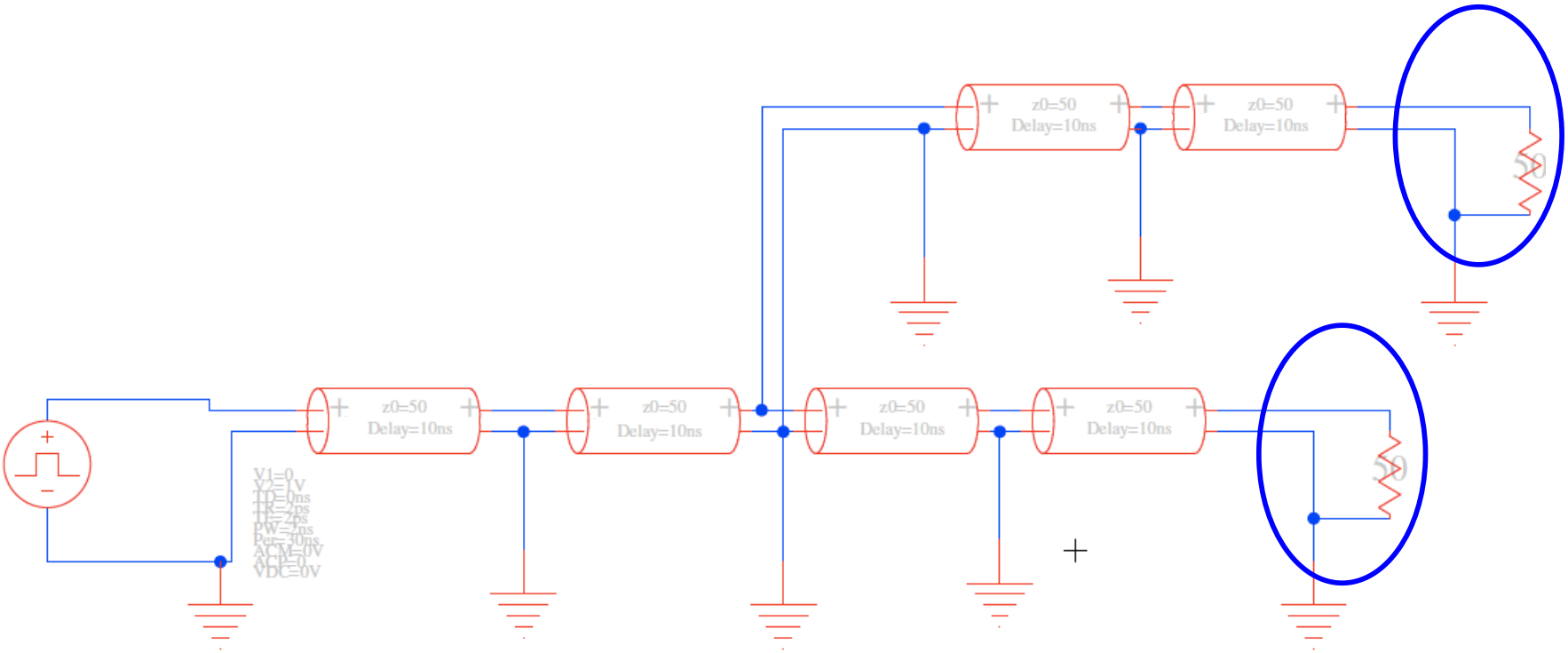


- At junction:
  - Reflects
    - $V_r=(25-50)/(25+50)V_i=-0.33V_i$
  - Transmits
    - $V_t=(50/(25+50))V_i=0.67V_i$

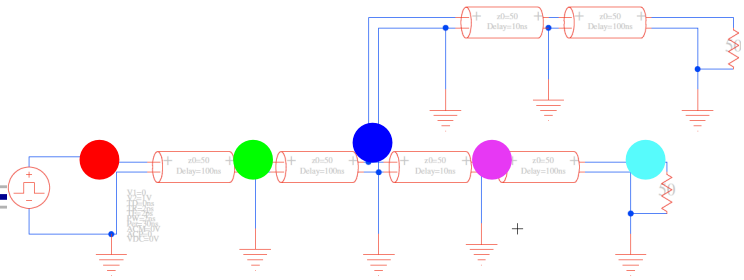
$$V_i\left(\frac{R-Z_0}{R+Z_0}\right)=V_r \qquad V_i\left(\frac{2R}{R+Z_0}\right)=V_t$$

End of Branch

- What happens at end?
- If ends in matched, parallel termination
  - No further reflections



Branch Simulation



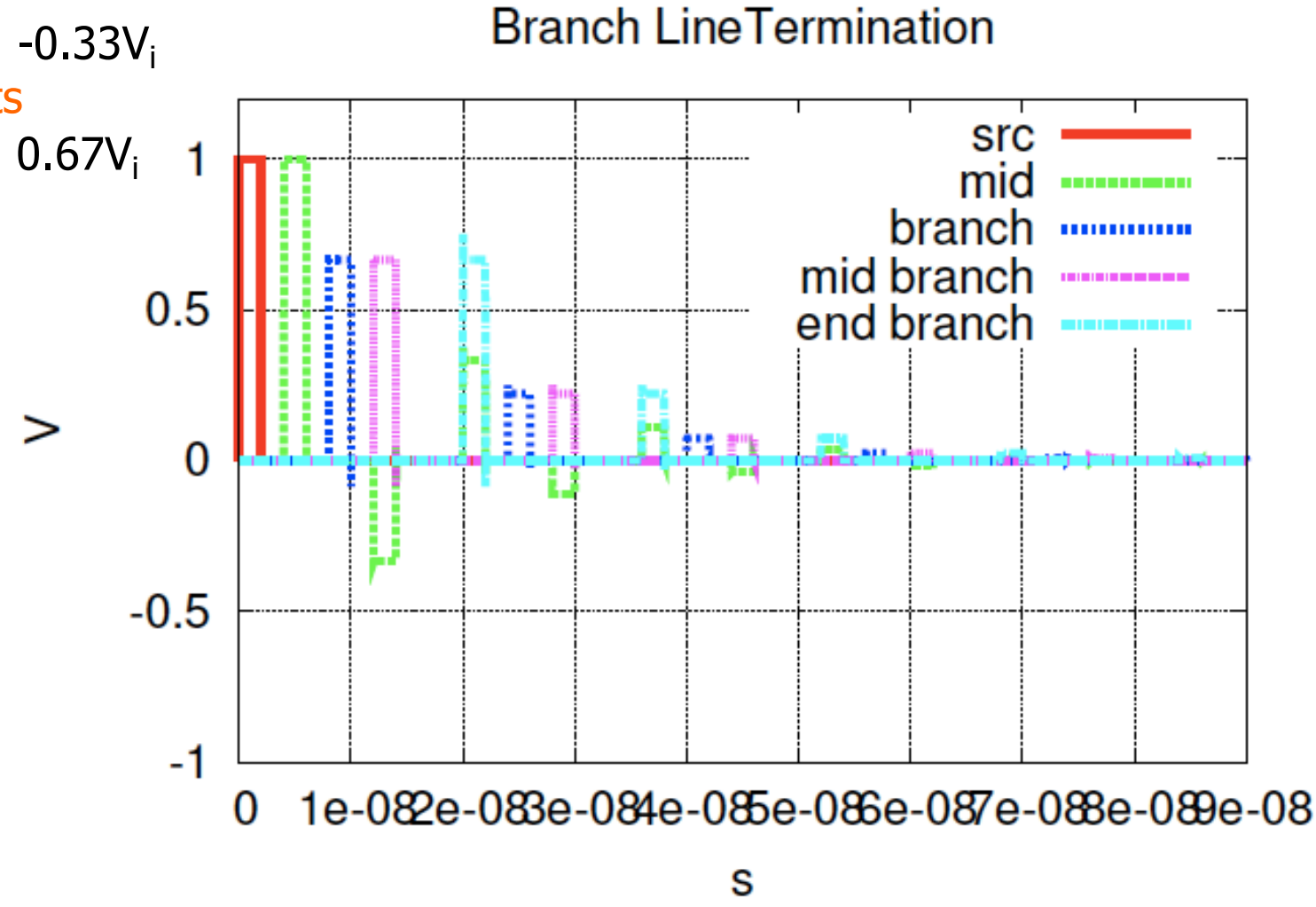
At junction:

Reflects

$V_r = -0.33V_i$

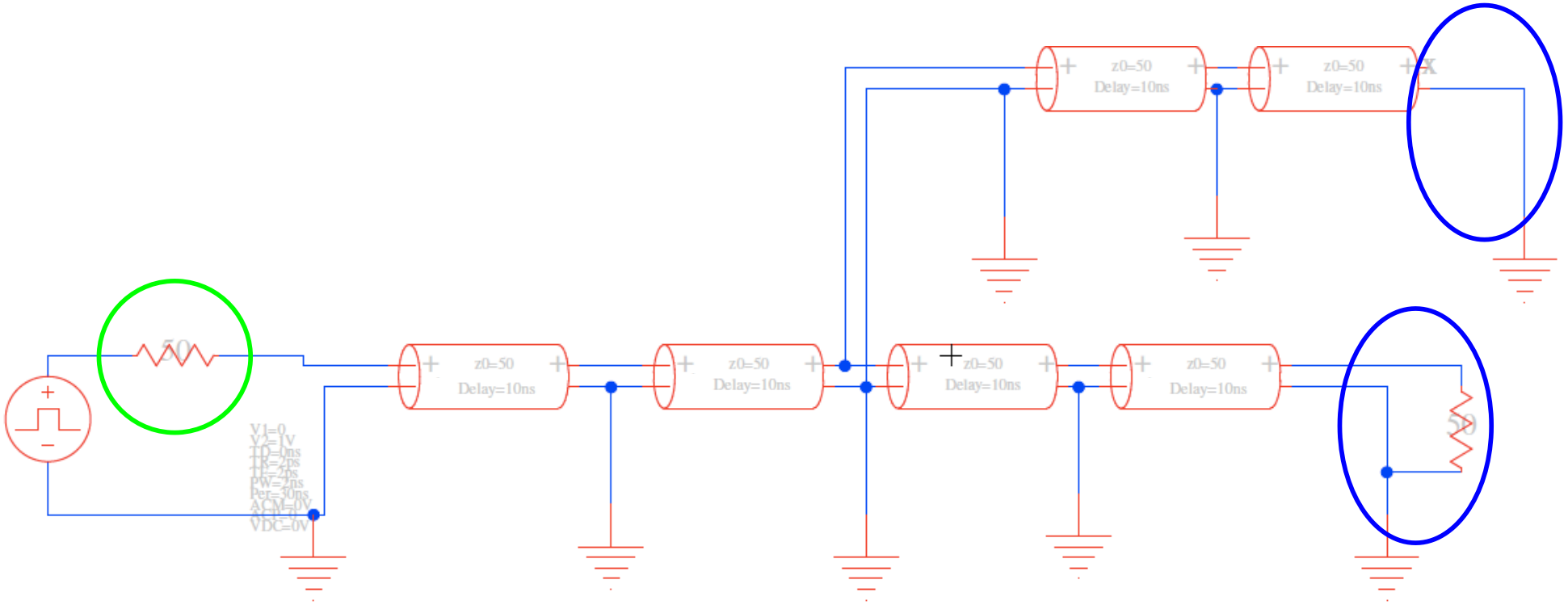
Transmits

$V_t = 0.67V_i$



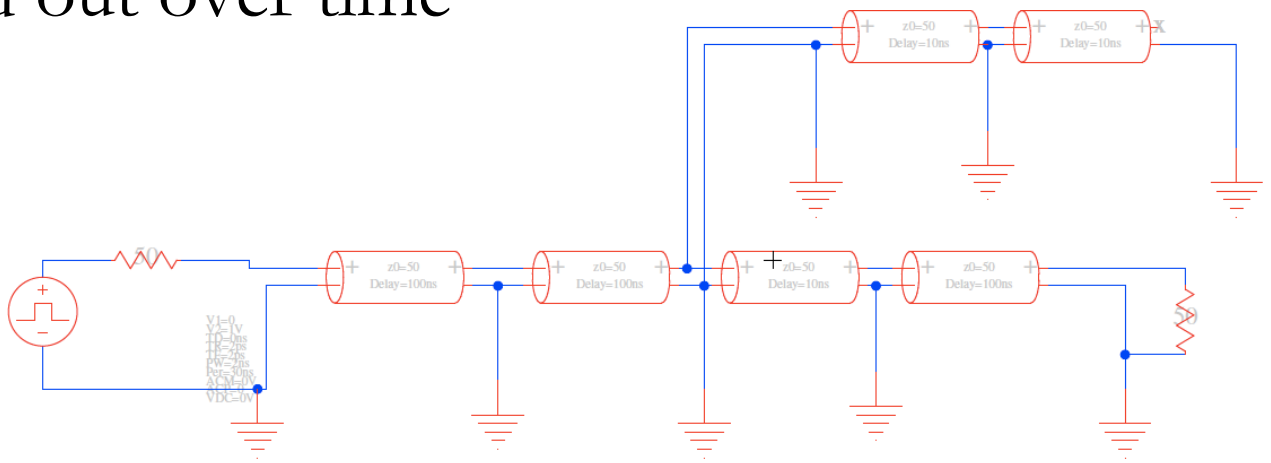
Branch with Open Circuit?

- What happens if branch open circuit?
- And source termination?

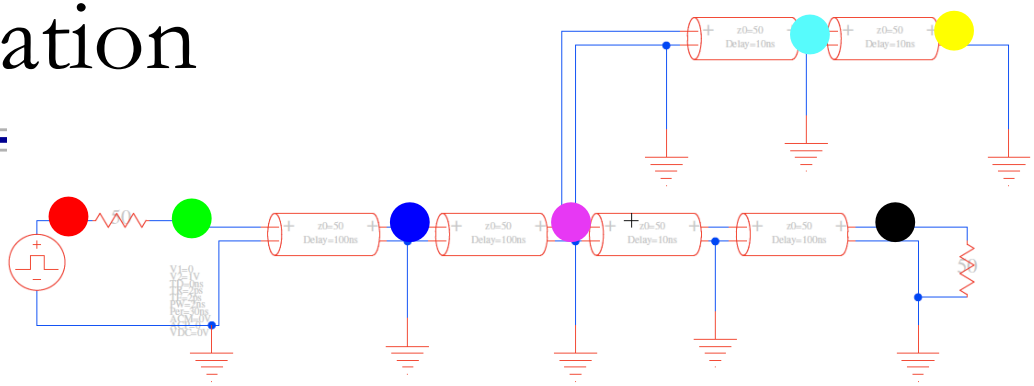


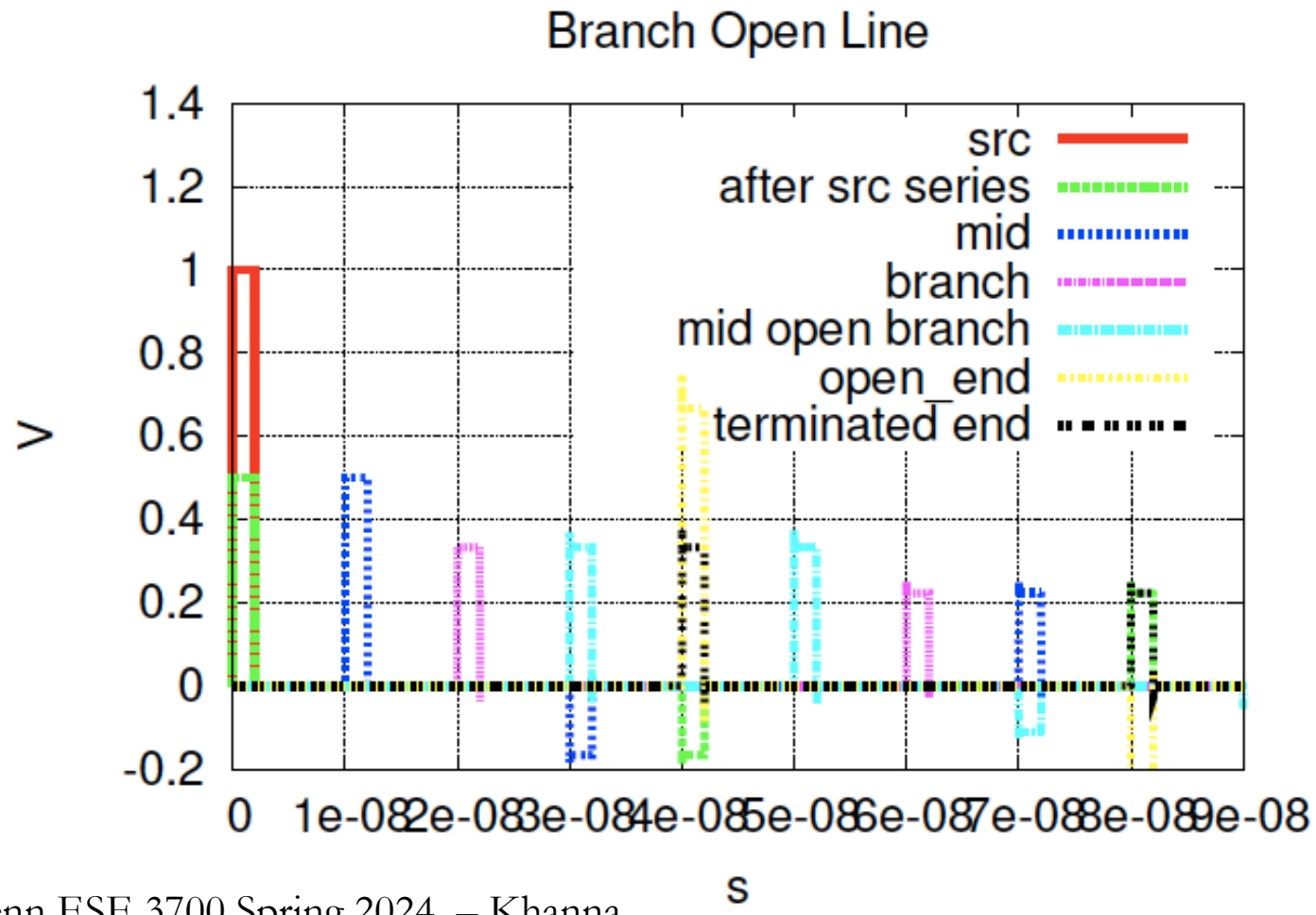
Branch with Open Circuit

- Reflects at end of open-circuit stub
- Reflection returns to branch
  - …and encounters branch again
  - Send transmission pulse to both
    - Source and other branch
- Sink sees original pulse as multiple smaller pulses spread out over time

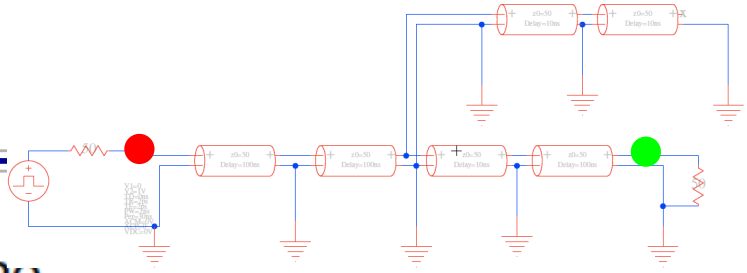


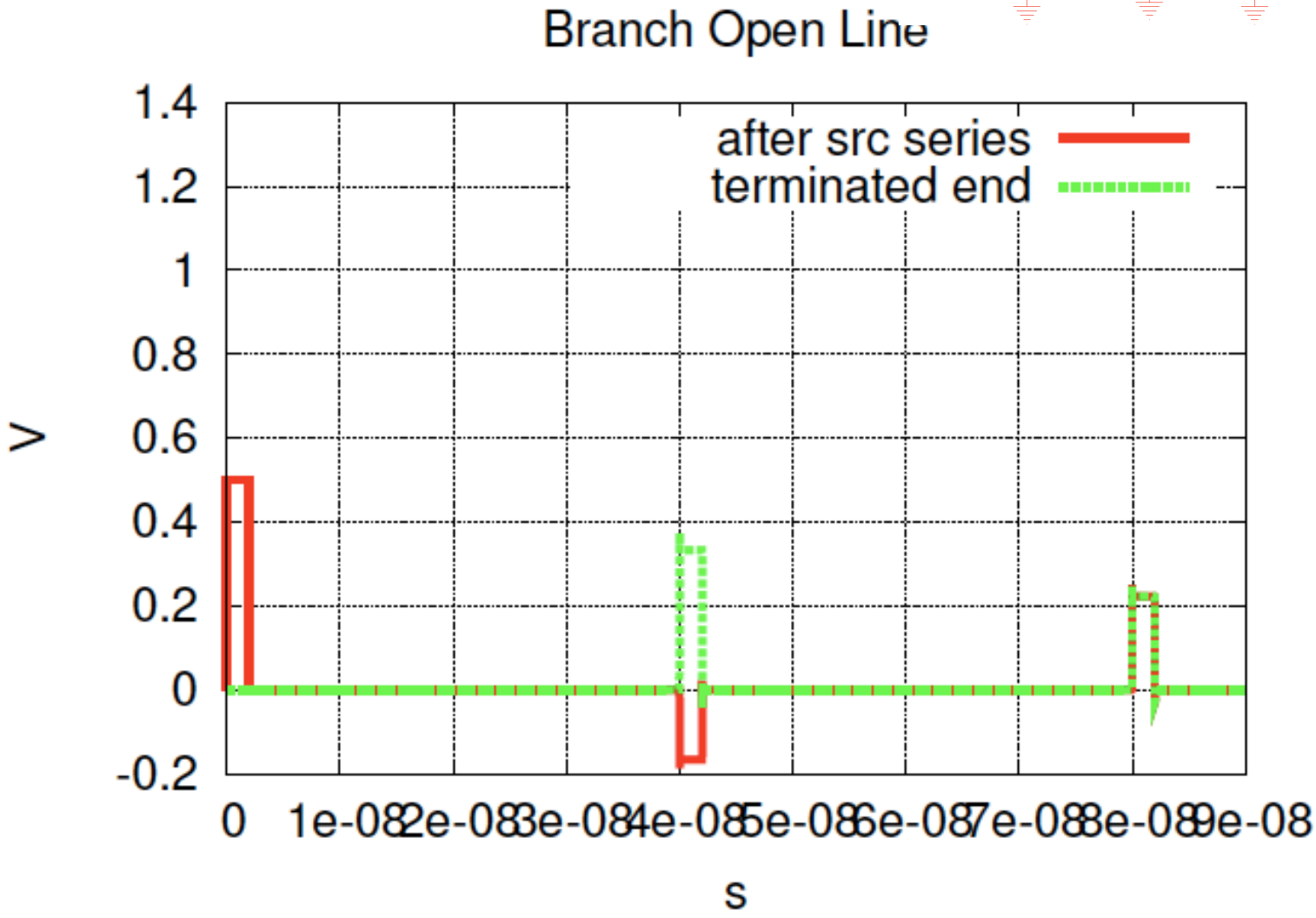
Open Branch Simulation





Open Branch Simulation





Transmission Line Noise

- Frequency limits
- Imperfect termination
- Mismatched segments/junctions/vias/connectors
- Loss due to resistance in line
  - Limits length

Idea

- Transmission lines
  - high-speed
  - high throughput
  - long-distance signaling
- Termination
- Signal quality losses

$$w = \frac{1}{\sqrt{LC}} = \frac{c_0}{\sqrt{\varepsilon_r \mu_r}}$$

$$Z_0 = \sqrt{\frac{L}{C}}$$

$$V_r = V_i \left(\frac{R - Z_0}{R + Z_0} \right)$$

Admin

- Wednesday 5/1 Project 2 Due
  - Can turn it in up to Friday 5/3 midnight with no penalty
    - No submissions accepted after 5/3
- Final (T 5/7)
  - 3-5pm in Towne 311
  - Cumulative: Lec 1 – 19
    - Big Idea slides from each lecture
  - Finals 2010—2021 online
    - Coverage was different
  - Wednesday lecture review/course summary
  - TA review session F 5/3 3-5pm, Towne 307