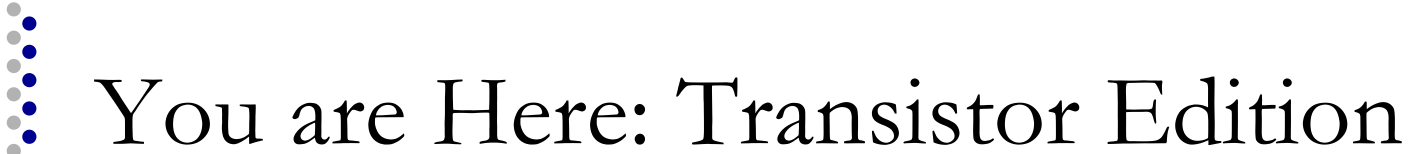
ESE3700: Circuit-Level Modeling, Design and Optimization for Digital Systems

Lec 5: February 7, 2024

MOS Model and Transistor Operating Regions, Part I



You are Here: Transistor Edition

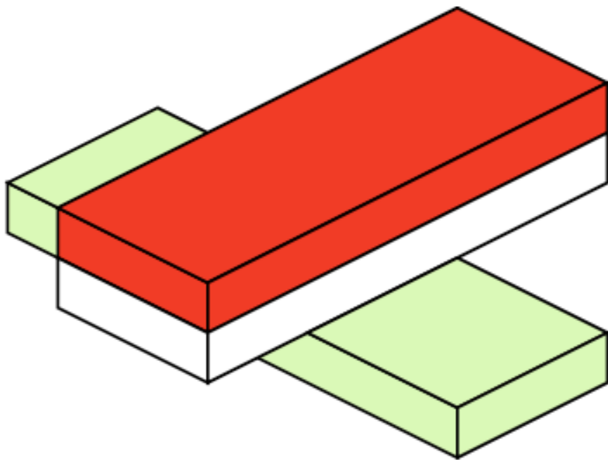
- Previously: simple models (0th and 1st order)
  - Comfortable with basic functions and circuits
- This lecture and the next one
  - Detailed semiconductor discussion
  - MOSFET phenomenology
- Rest of term
  - Implications of the MOS device

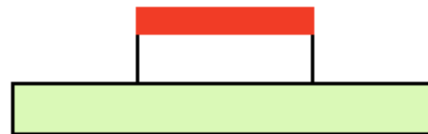
Today

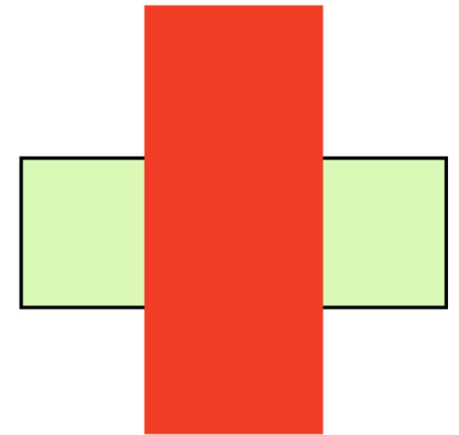
- MOS Structure
- Basic Fabrication
- Threshold
- Operating Regions
  - Resistive
  - Saturation
  - Subthreshold
  - Velocity Saturation (next lecture)

MOS

- Metal Oxide Semiconductor

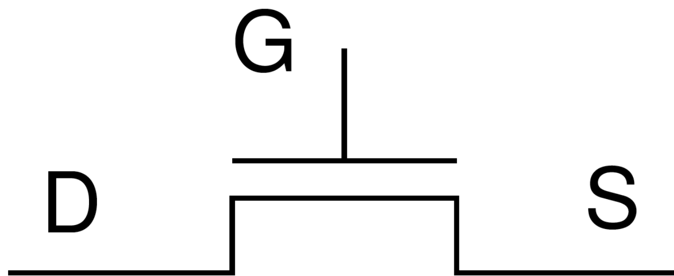


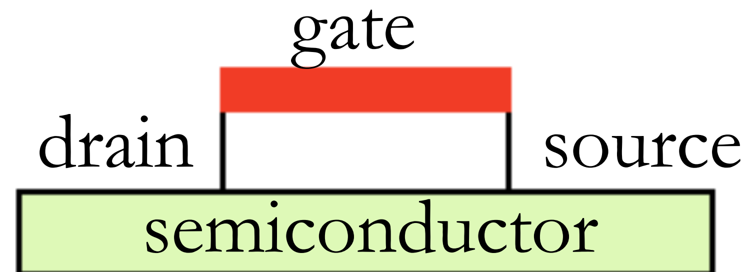




MOS

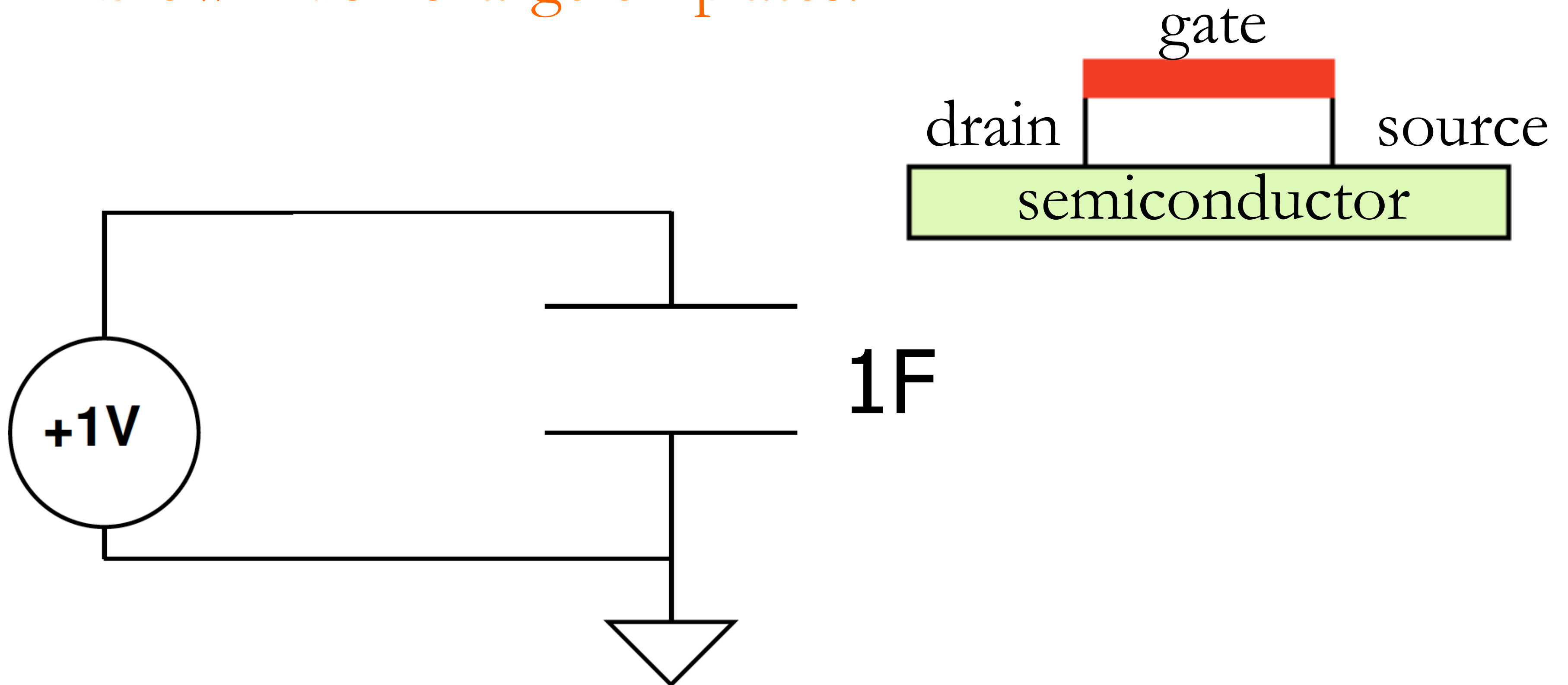
- **M**etal – gate
- **O**xide – insulator separating gate from semiconductor
  - Ideally: no conduction from gate to semiconductor
- **S**emiconductor – between source and drain
- See why gate input is capacitive?





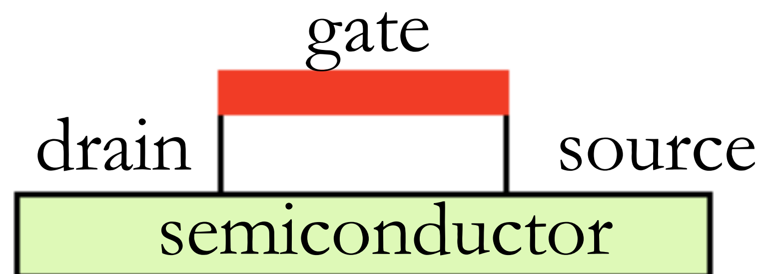
(MOS) Capacitor (preclass 1)

- Charge distribution and field?
- How much charge on plates?

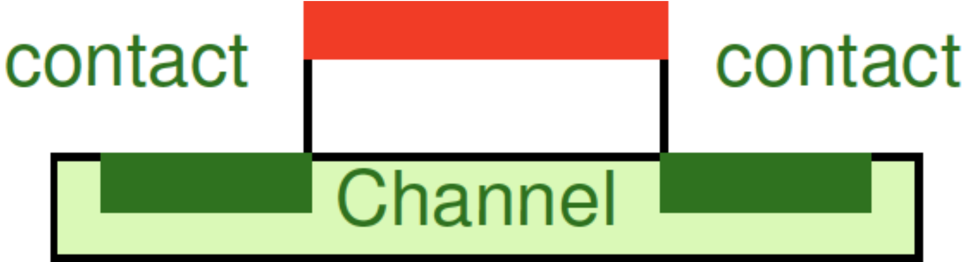


Idea

- Semiconductor – can behave as metal or insulator
- Voltage on gate induces an electrical field
- Induced field attracts (repels) charge in semiconductor to form a channel
  - Semiconductor can be switched between conducting and not conducting
  - Hence "Field-Effect" Transistor



Source/Drain Contacts



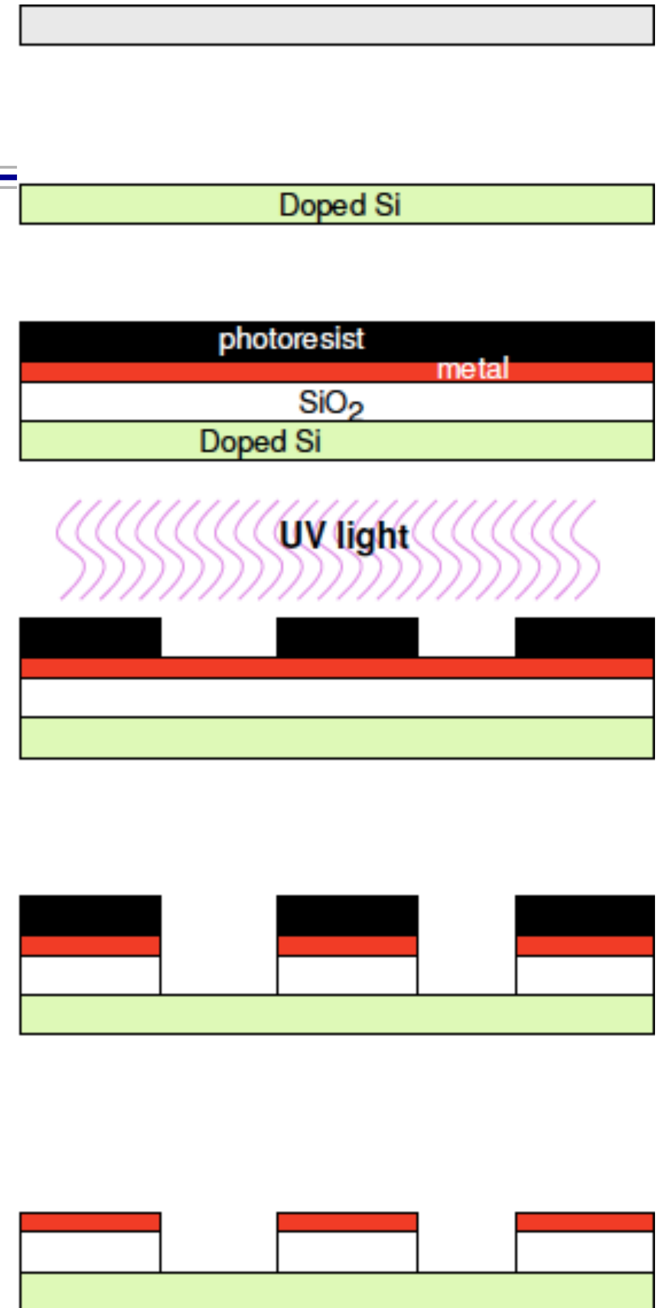
- Contacts: Conductors → metallic
  - Connect to metal wires that connect transistors

Fabrication

- Start with Silicon wafer
- Dope silicon
- Grow Oxide (SiO_2)
- Deposit Metal
- Photoresist mask and etch to define where features go

https://youtu.be/35jWSQXku74?t=119

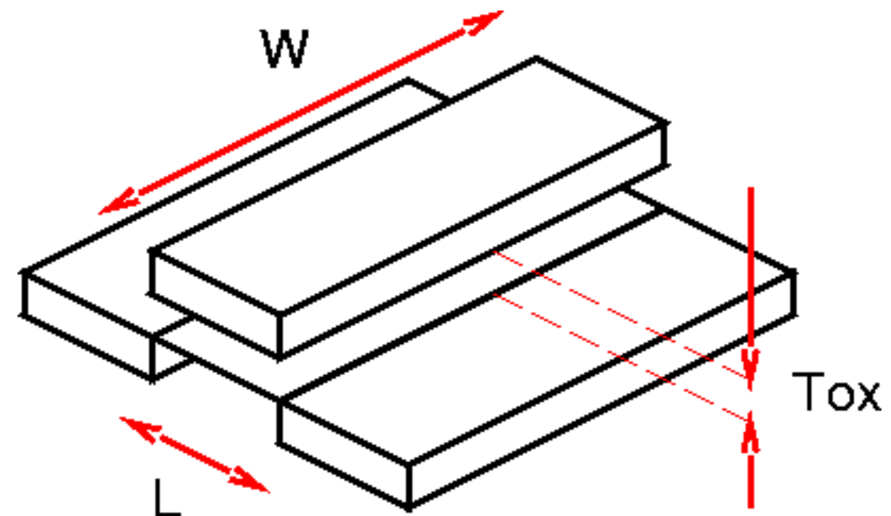
Time Code: 2:00-4:30



Dimensions

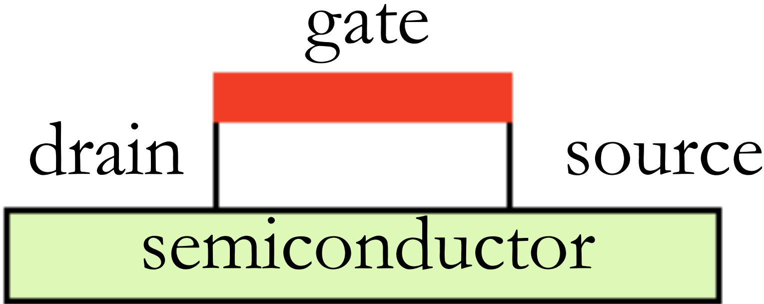
- Channel Length (L)
- Channel Width (W)
- Oxide Thickness (T_{ox})

- Process named by minimum length
  - 22nm → L=22nm

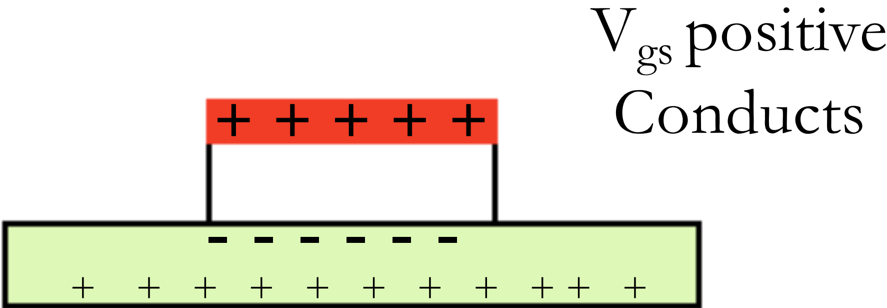


MOS Transistor Operation

So far– MOS model

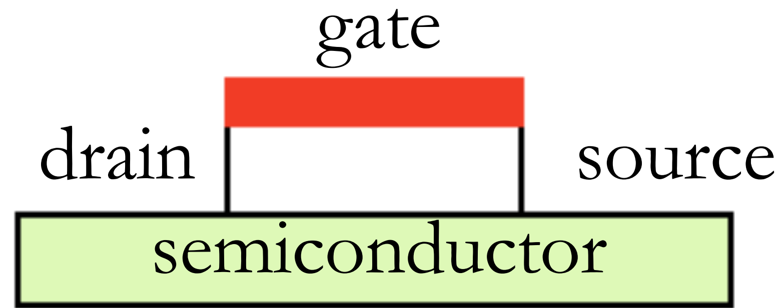


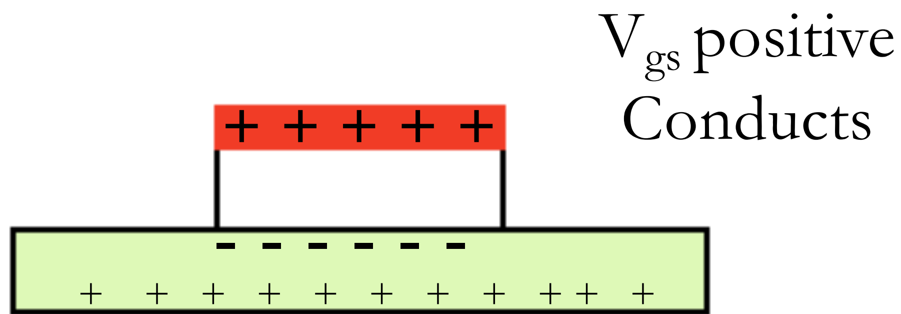
V_{gs} positive
Conducts



NMOS

So far– MOS model





V_{gs} positive
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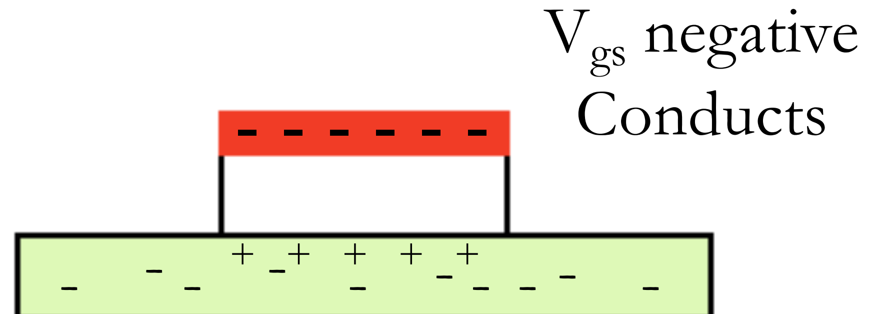


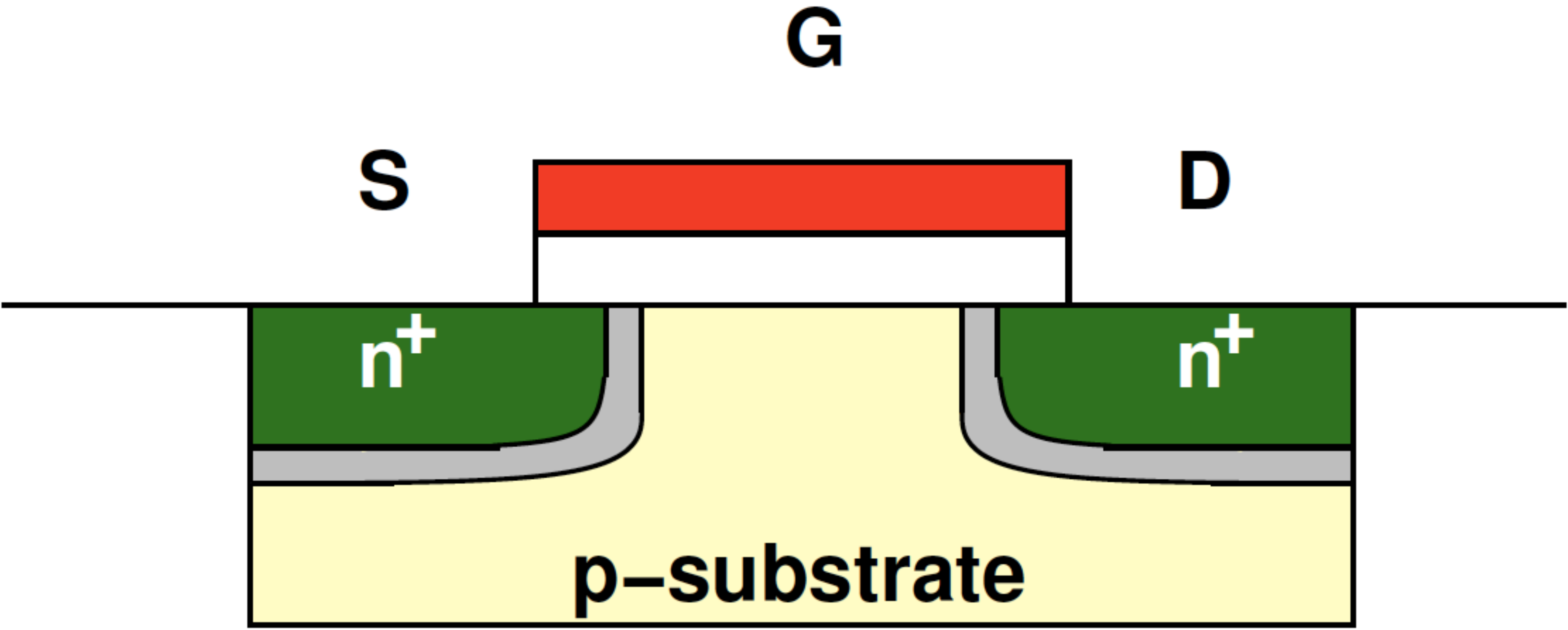
V_{gs} negative
Conducts

NMOS

PMOS

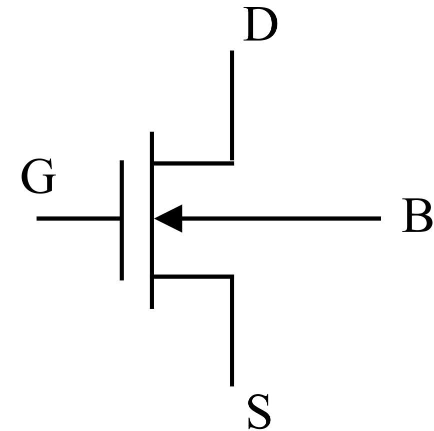
Refinement

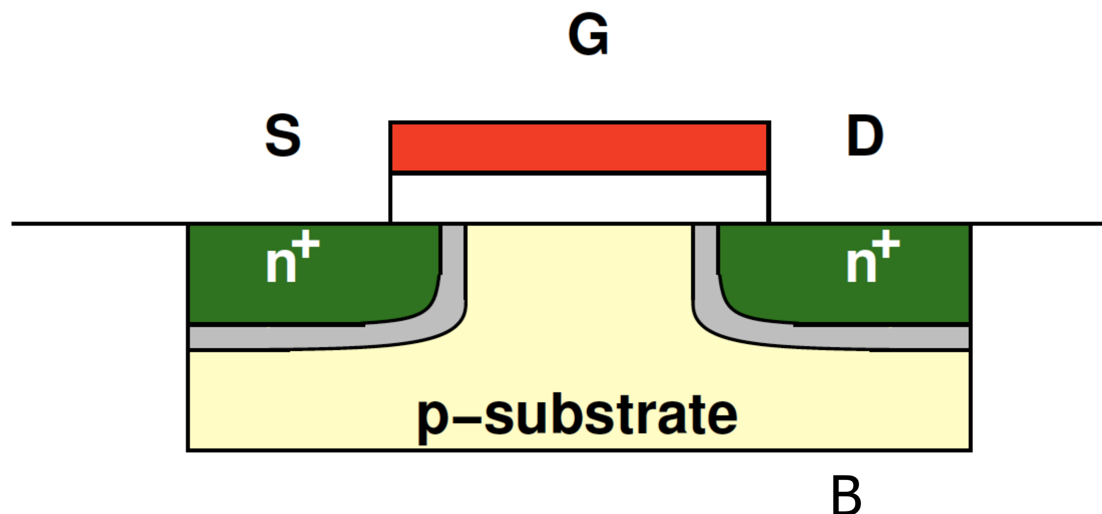
- Depletion region around D/S→ excess carriers depleted



Bulk/Body Contact

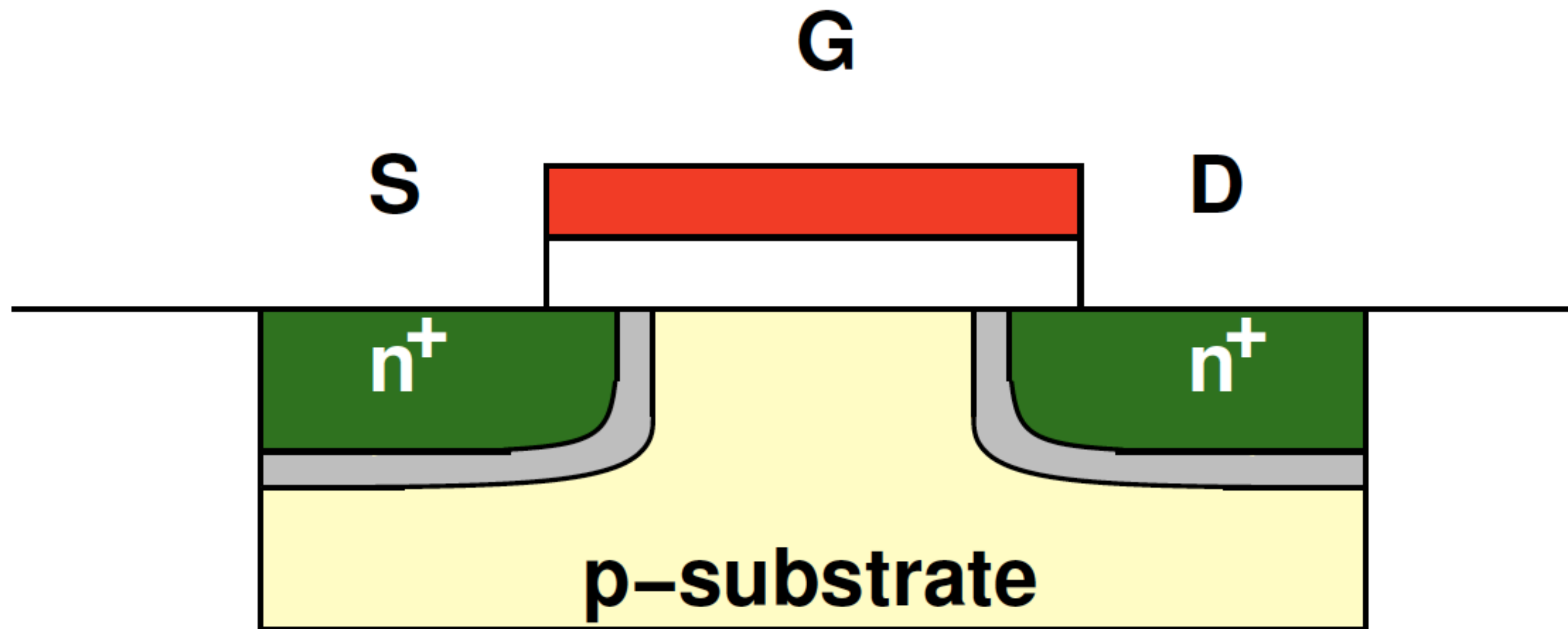
- MOS actually has four contacts
- Also effects fields
- Ideally substrate and source connected
  - Settle for substrate being <= source
  - Gnd for nmos (V_{dd} for pmos)





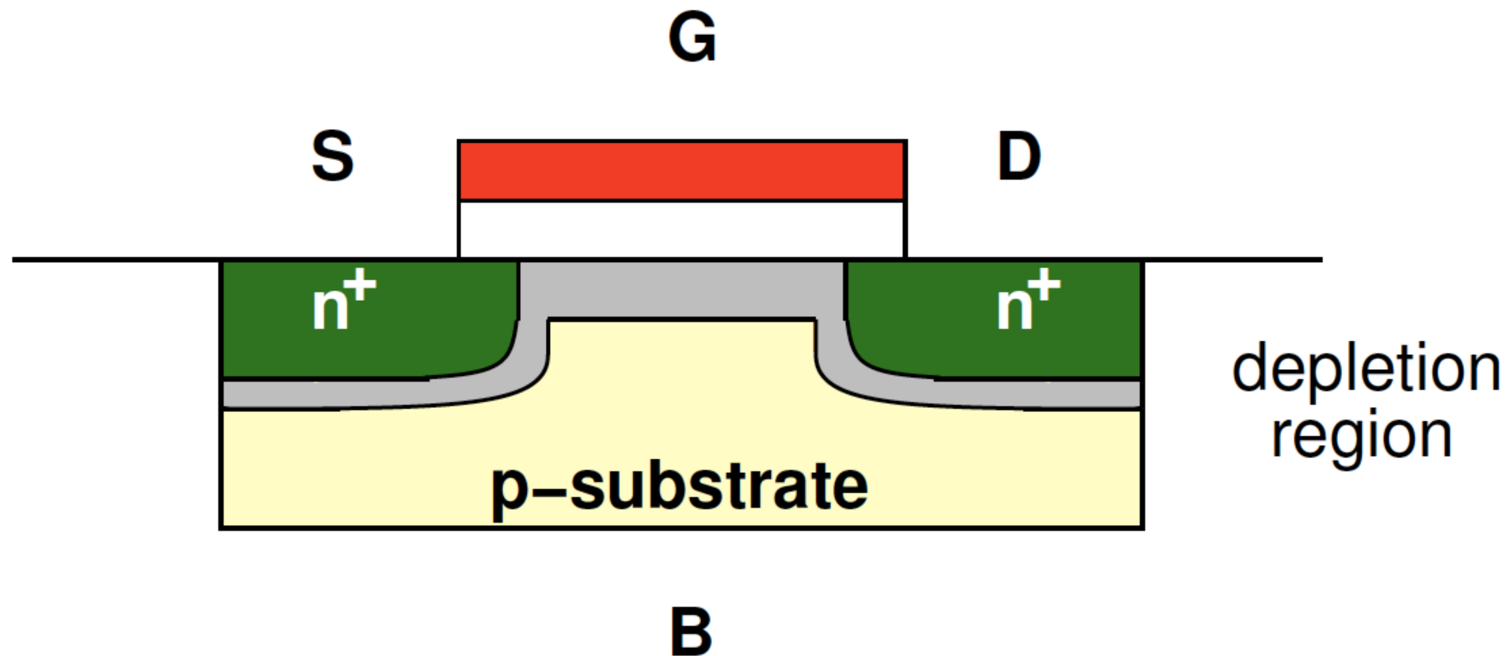
No Field

- $V_{GS}=0$, $V_{DS}=0$

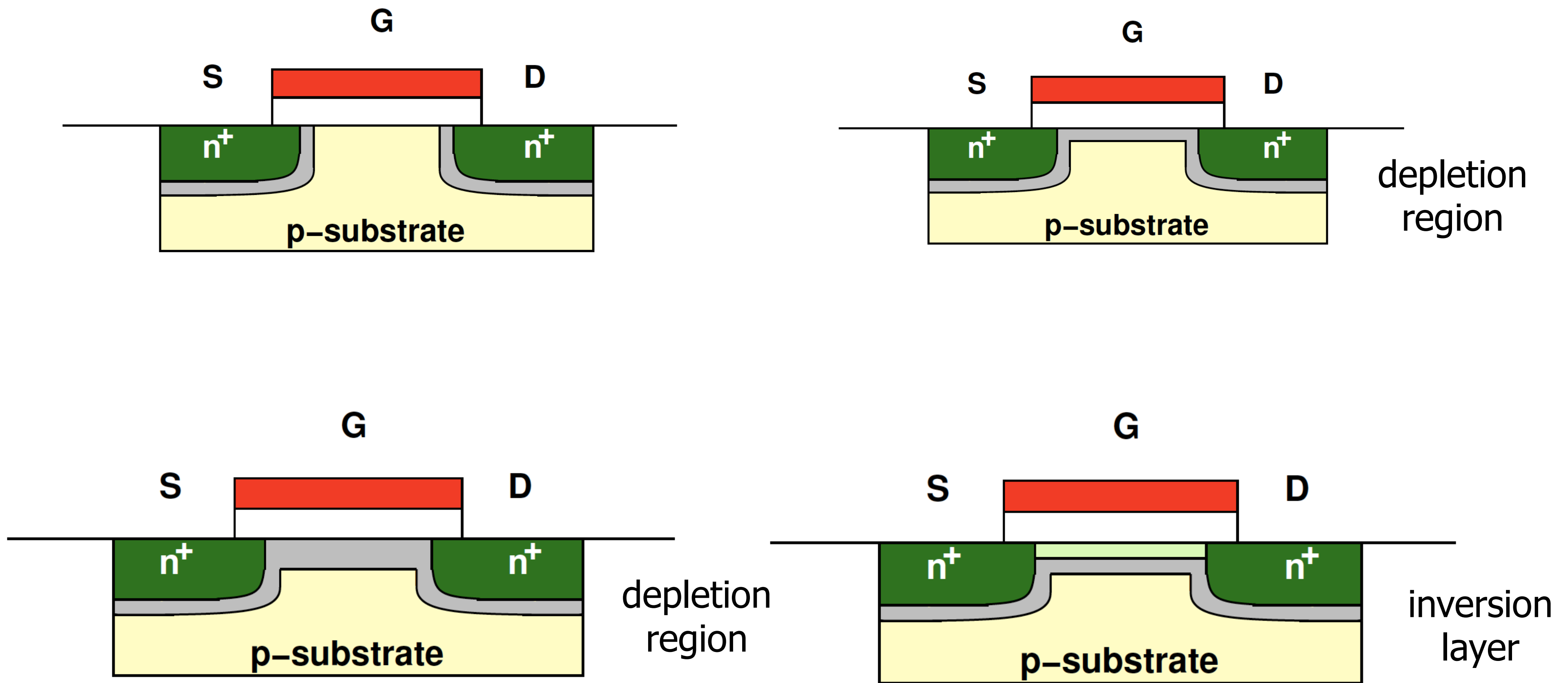


Apply $V_{GS}>0$

- Deplete excess positive charge under oxide
- Left with negative charge
  - Repel holes

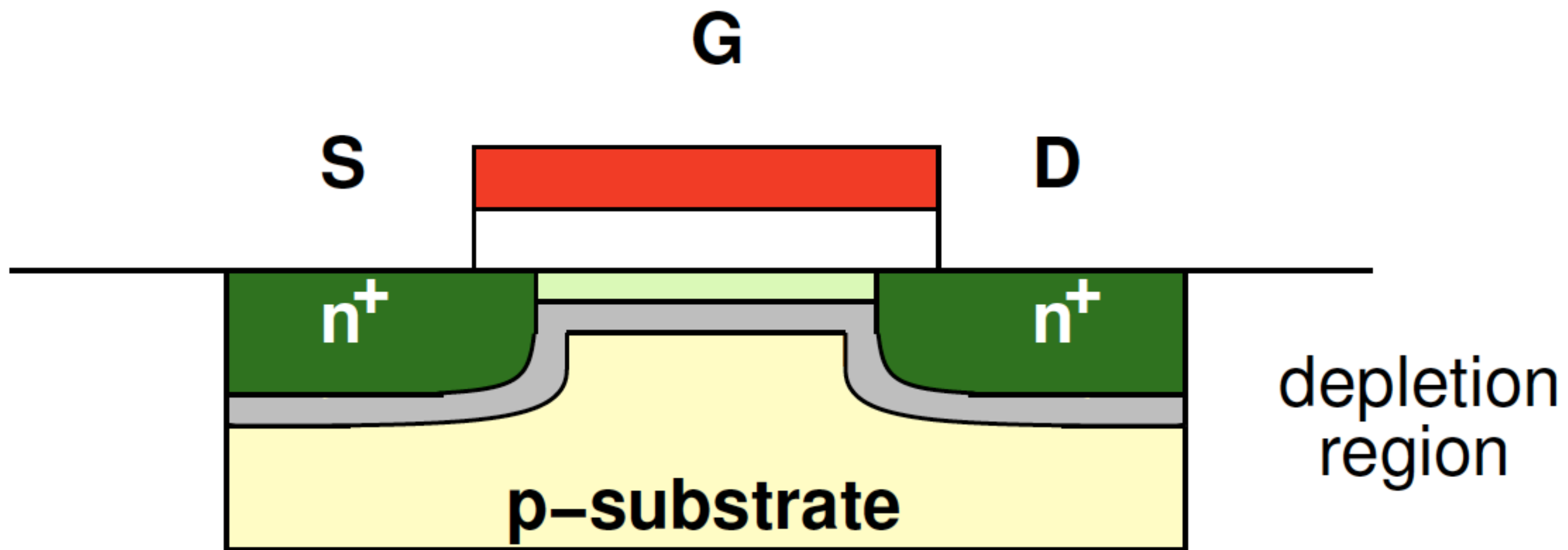


Channel Evolution -- Increasing Vgs



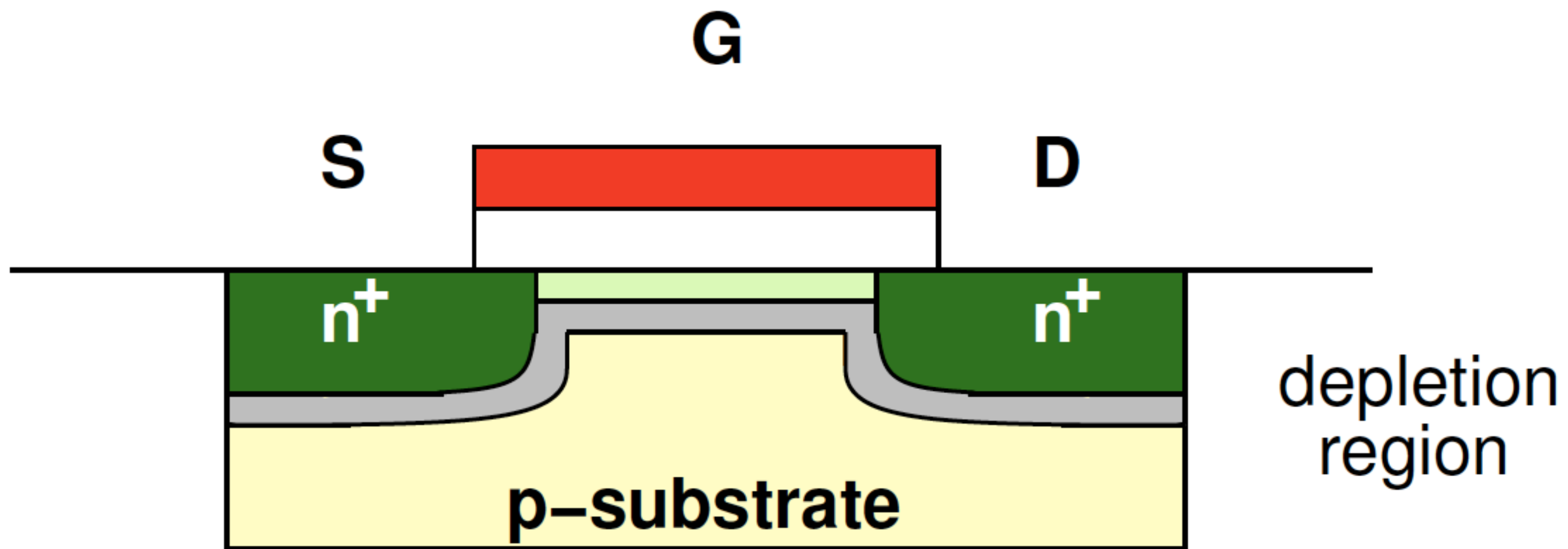
Inversion

- Surface builds electrons
  - Inverts to n-type
  - Draws electrons from n^+ source terminal



Threshold

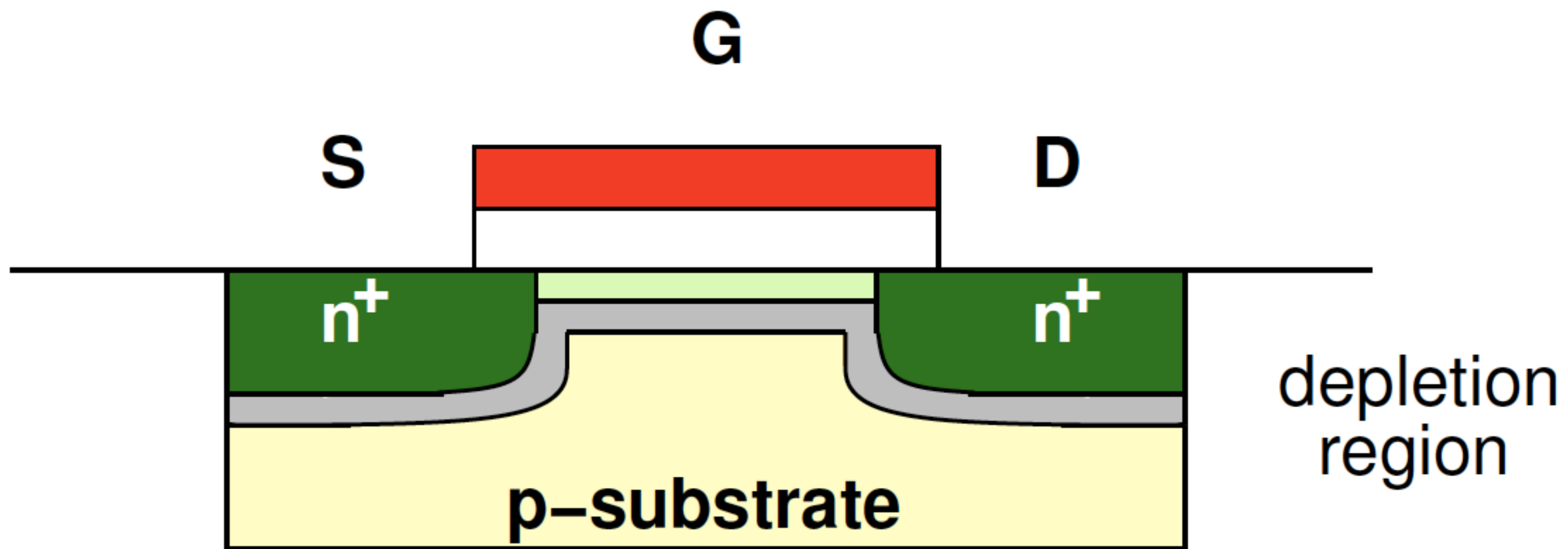
- Voltage where strong inversion occurs → threshold voltage
  - $V_{th} \sim= 2\phi_F$



Threshold

- Voltage where strong inversion occurs → threshold voltage
  - $V_{th} \sim= 2\phi_F$
  - Engineer by controlling doping (N_A)

$$\phi_F = \frac{kT}{q}\ln\left(\frac{N_A}{n_i}\right)$$



MOSFET – IV Characteristics

I_{DS}

Drain current [arbitrary unit]

50
40
30
20
10
0

0 2 4 6 8 10

Gate to source voltage [V]

V_{th}

V_{GS}

MOSFET – IV Characteristics

$V_{DS} < V_{GS} - V_{TH}$

linear region

$V_{GS}-V_{th}$=7 V

6 V

saturation region

5 V

$V_{DS} \geq V_{GS} - V_{TH}$

3 V

2 V

1 V

50 40 30 20 10 0

0 2 4 6 8 10

Drain current [arbitrary unit]

Drain to source voltage [V]

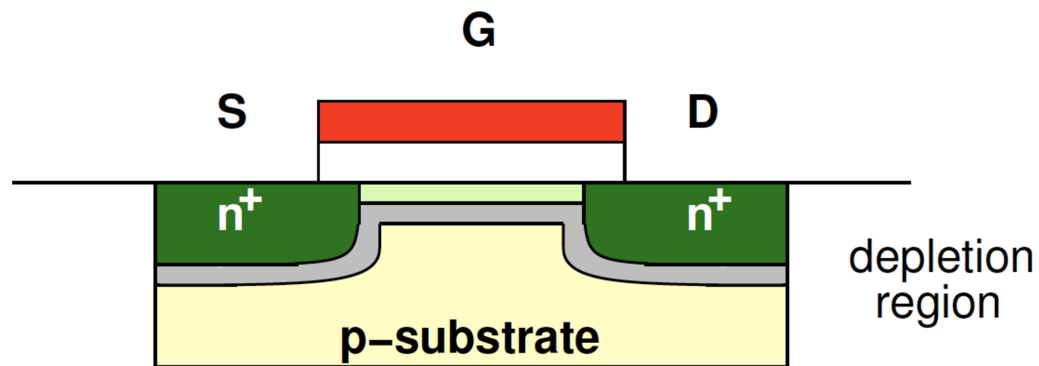
I_{DS}

V_{DS}

$V_{GS} - V_{th}$

Linear Region

- $V_{GS} > V_{th}$ and V_{DS} small



$$C_{OX} = \frac{\varepsilon_{OX}}{t_{OX}}$$

$$I_{DS} = \mu_n C_{OX}\left(\frac{W}{L}\right)\left[\left(V_{GS} - V_{th}\right)V_{DS} - \frac{V_{DS}^2}{2}\right]$$

Linear Region

- $V_{GS}>V_{th}$ and V_{DS} small
- V_{GS} fixed → looks like resistor
  - Current linear in V_{DS}

$$I_{DS}=\mu_n C_{OX}\left(\frac{W}{L}\right)\left[\left(V_{GS}-V_{th}\right)V_{DS}-\frac{V_{DS}^2}{2}\right]$$

Linear Region

- $V_{GS} > V_{th}$ and V_{DS} small
- V_{GS} fixed → looks like resistor
  - Current linear in V_{DS}

$$I_{DS} = \mu_n C_{OX}\left(\frac{W}{L}\right)\left[\left(V_{GS} - V_{th}\right)V_{DS} - \frac{V_{DS}^2}{2}\right]$$

~0

$$I_{DS} \approx \mu_n C_{OX}\left(\frac{W}{L}\right)\left(V_{GS} - V_{th}\right)V_{DS}$$

$$I_{DS} \propto V_{DS}$$

MOSFET – IV Characteristics

$V_{DS} < V_{GS} - V_{TH}$

linear region

$V_{GS} - V_{th} = 7$ V

6 V

saturation region

5 V

$V_{DS} \geq V_{GS} - V_{TH}$

3 V

2 V

1 V

Drain current [arbitrary unit]

0 10 20 30 40 50

0 2 4 6 8 10

Drain to source voltage [V]

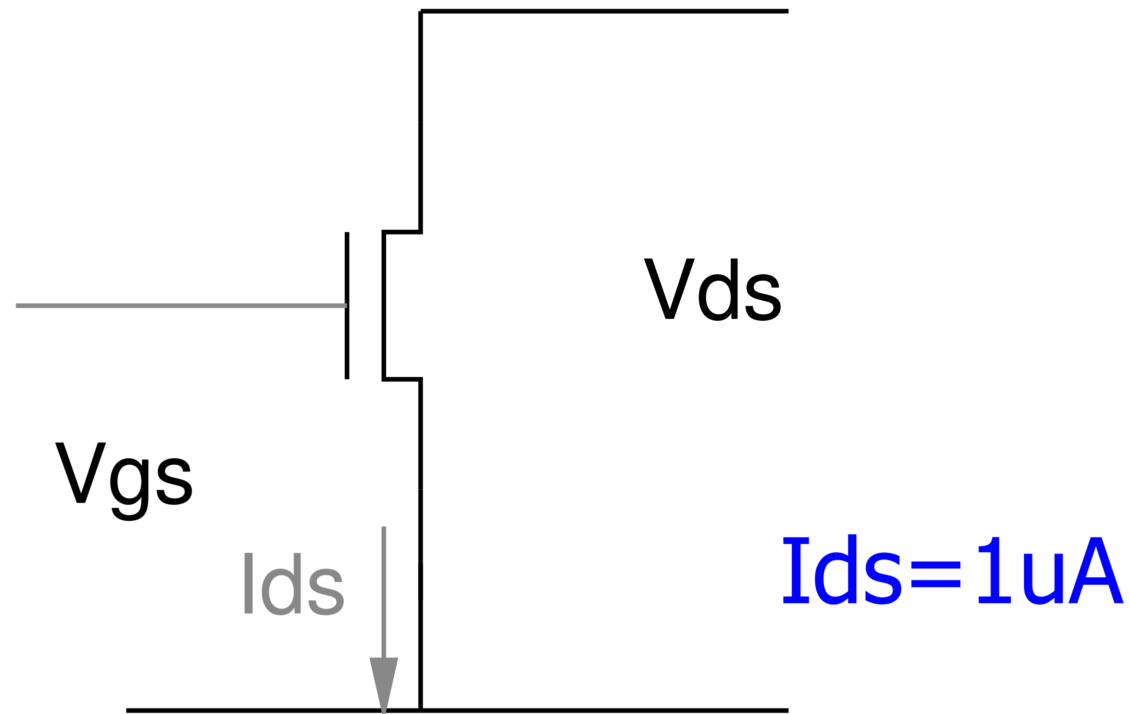
I_D

V_{DS}

$V_{GS} - V_{th}$

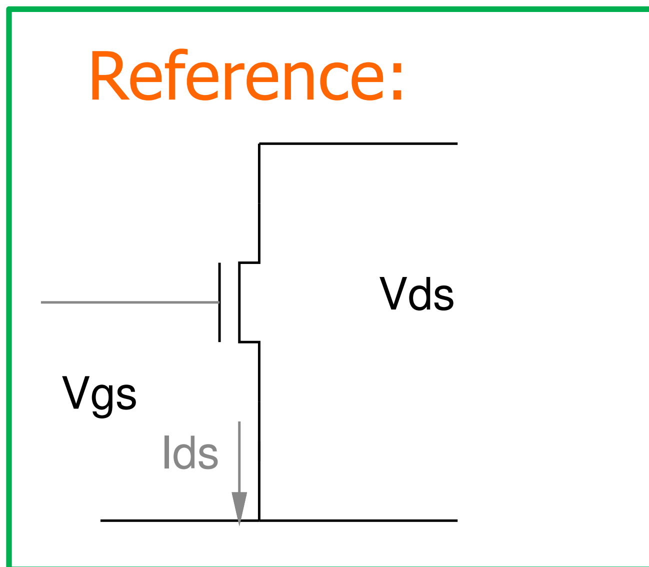
Preclass 2

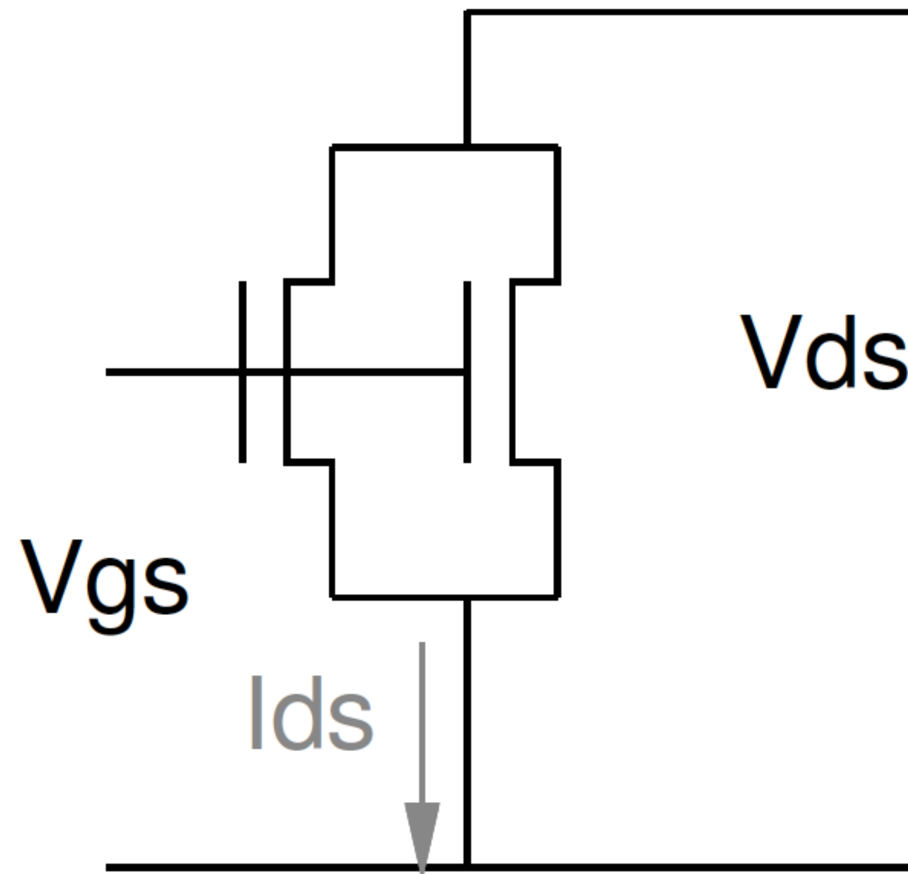
- Reference: I_{ds} for single transistor with Vgs and Vds bias



Preclass 2

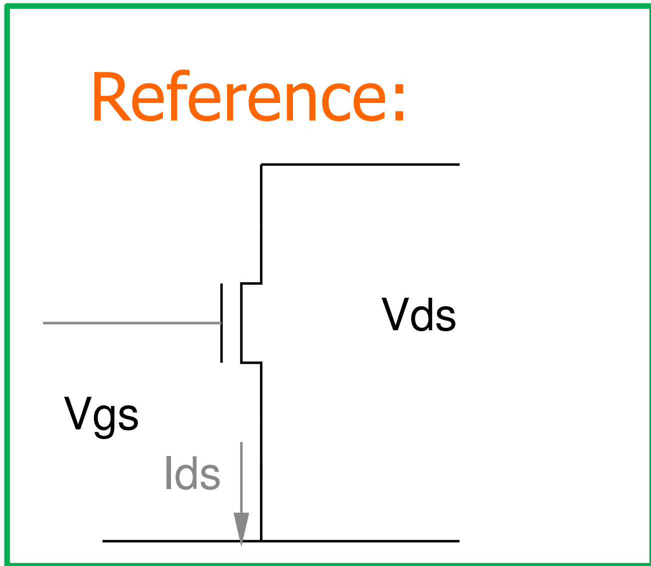
- I_{ds} for identical transistors in parallel?

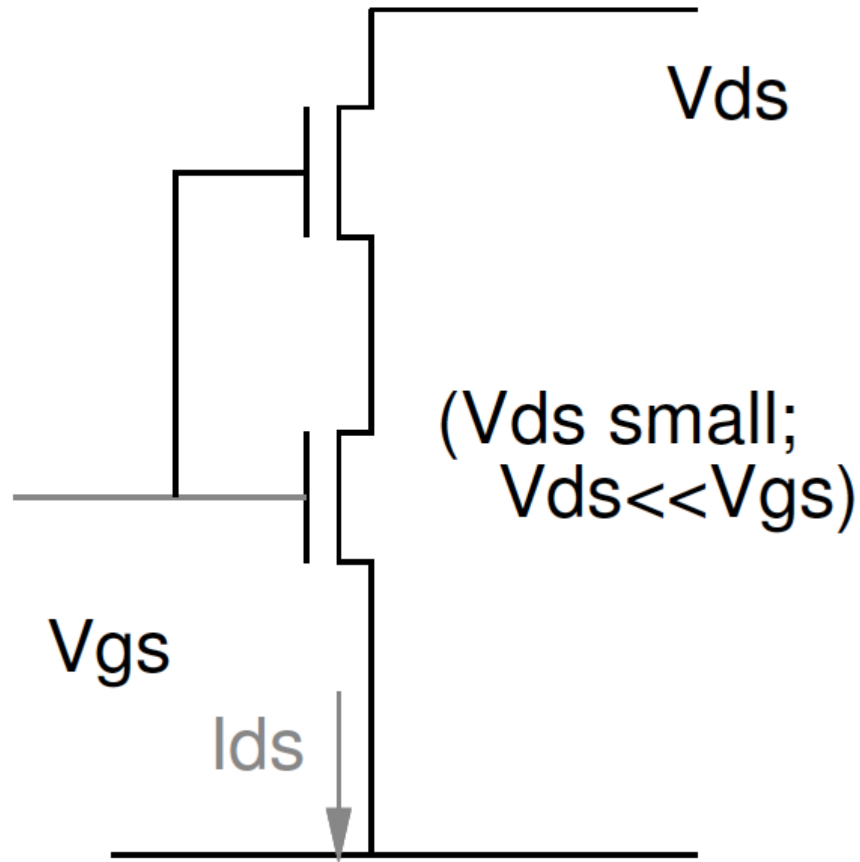




Preclass 2

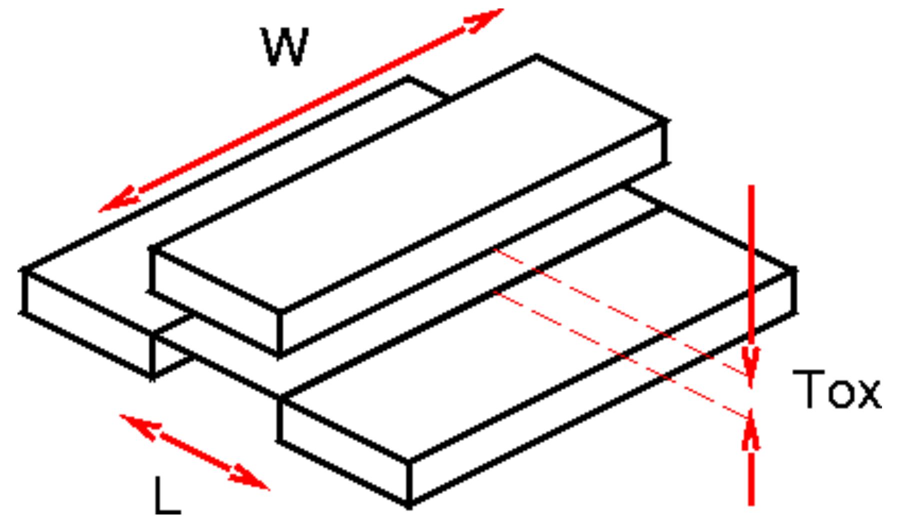
- I_{ds} for identical transistors in series?
  - (Vds small)

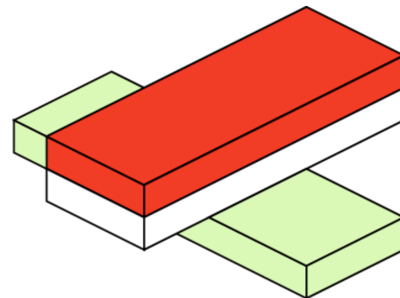




Dimensions

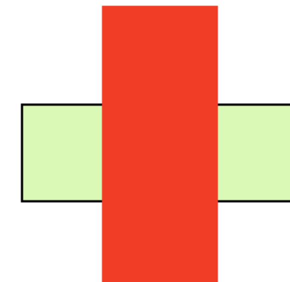
- Channel Length (L)
- Channel Width (W)
- Oxide Thickness (T_{ox})





Oblique

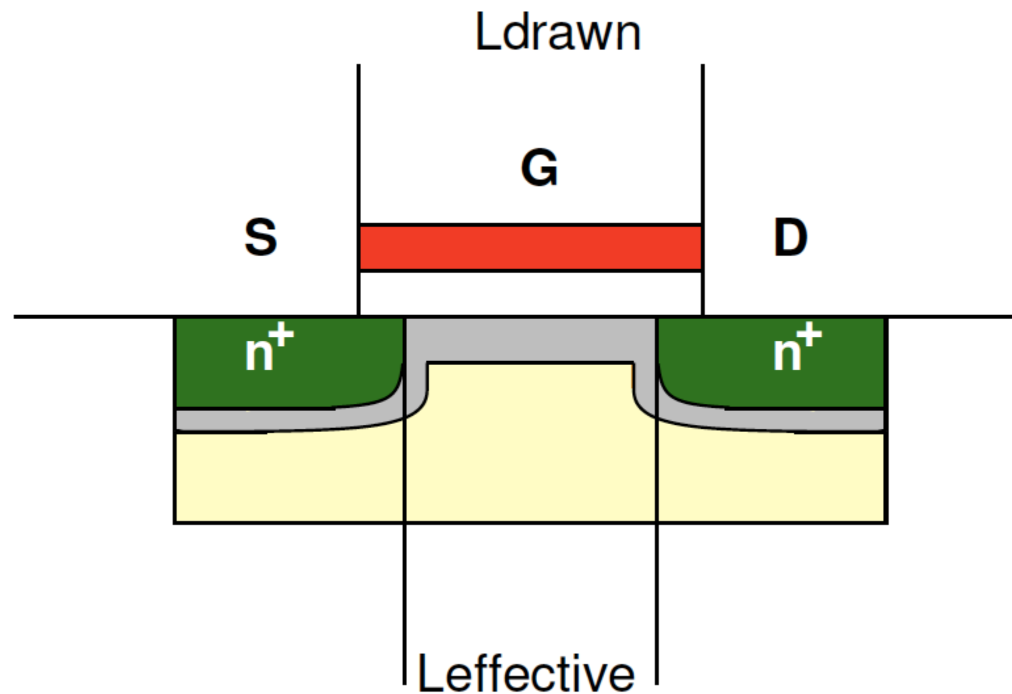
Side



Top

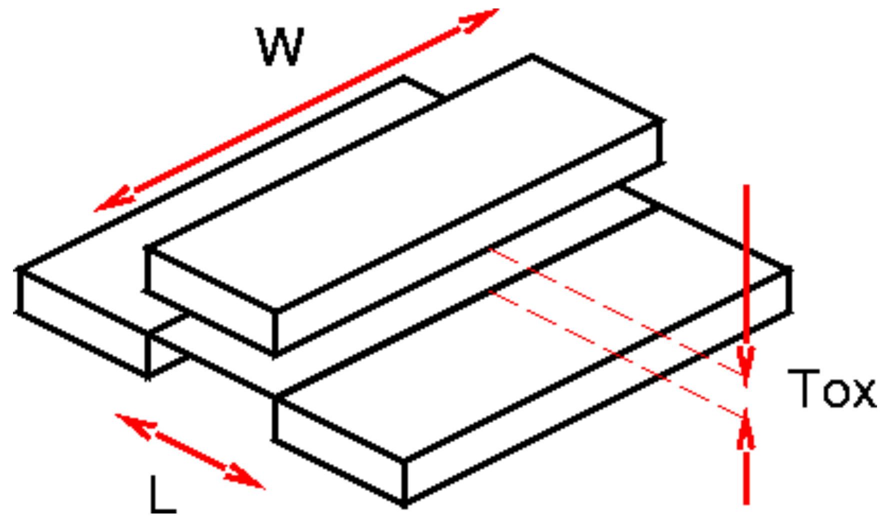
L_{drawn} vs. $L_{effective}$

- Doping not perfectly straight
- Spreads under gate
- Effective L smaller than draw gate width



Transistor Strength (W/L)

$$C_{OX} = \frac{\varepsilon_{OX}}{t_{OX}}$$



$$I_{DS} = \mu_n C_{OX}\left(\frac{W}{L}\right)\left[\left(V_{GS} - V_{th}\right)V_{DS} - \frac{V_{DS}^2}{2}\right]$$

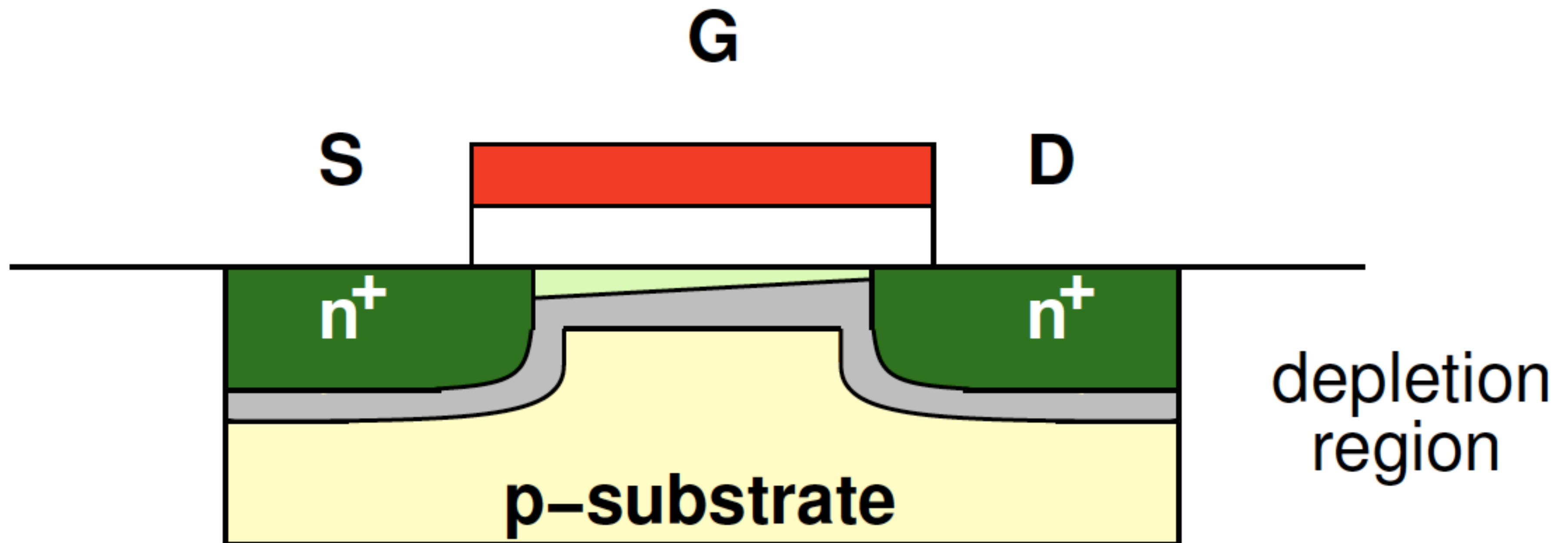
- Shape dependence match Resistance intuition
  - Wider = parallel resistors → decrease R
  - Longer = series resistors → increase R

$$R = \frac{\rho L}{A}$$

$$I_{DS} = \mu_n C_{OX}\left(\frac{W}{L}\right)\left[\left(V_{GS} - V_{th}\right)V_{DS} - \frac{V_{DS}^2}{2}\right]$$

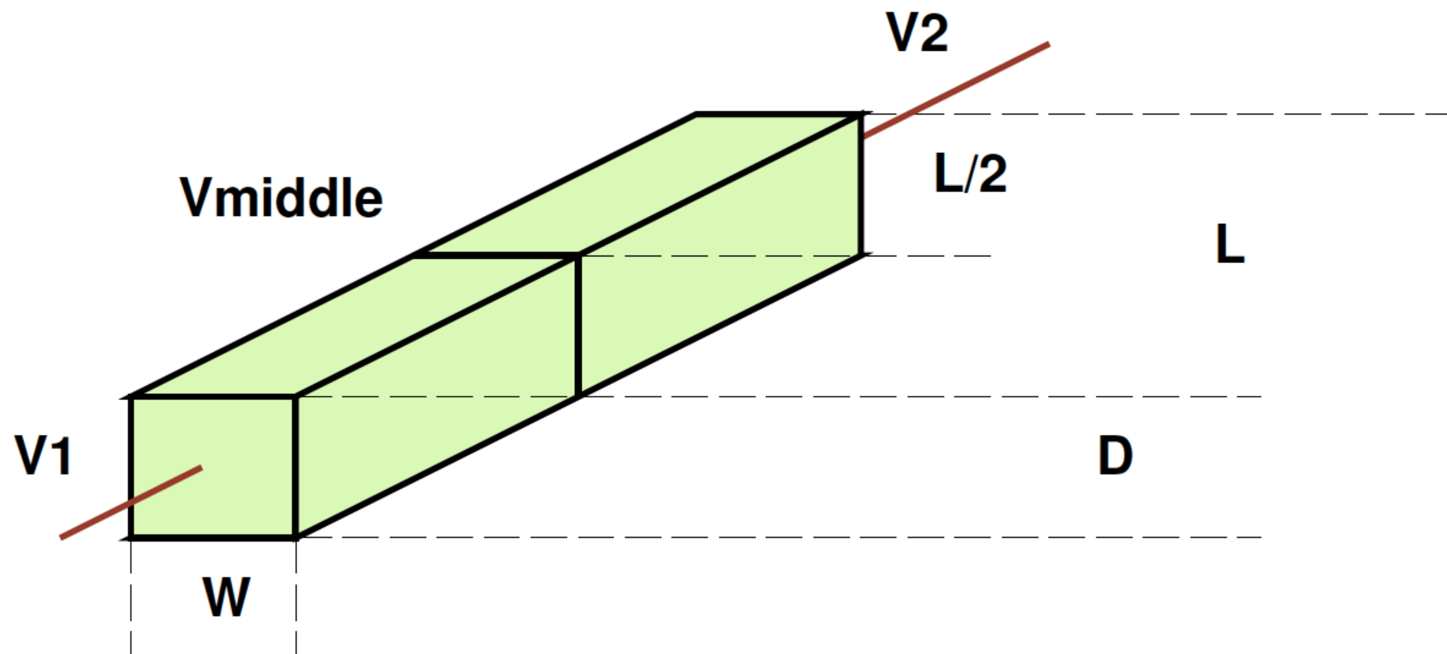
Channel Voltage

- Think of channel as resistor
- Voltage varies along channel



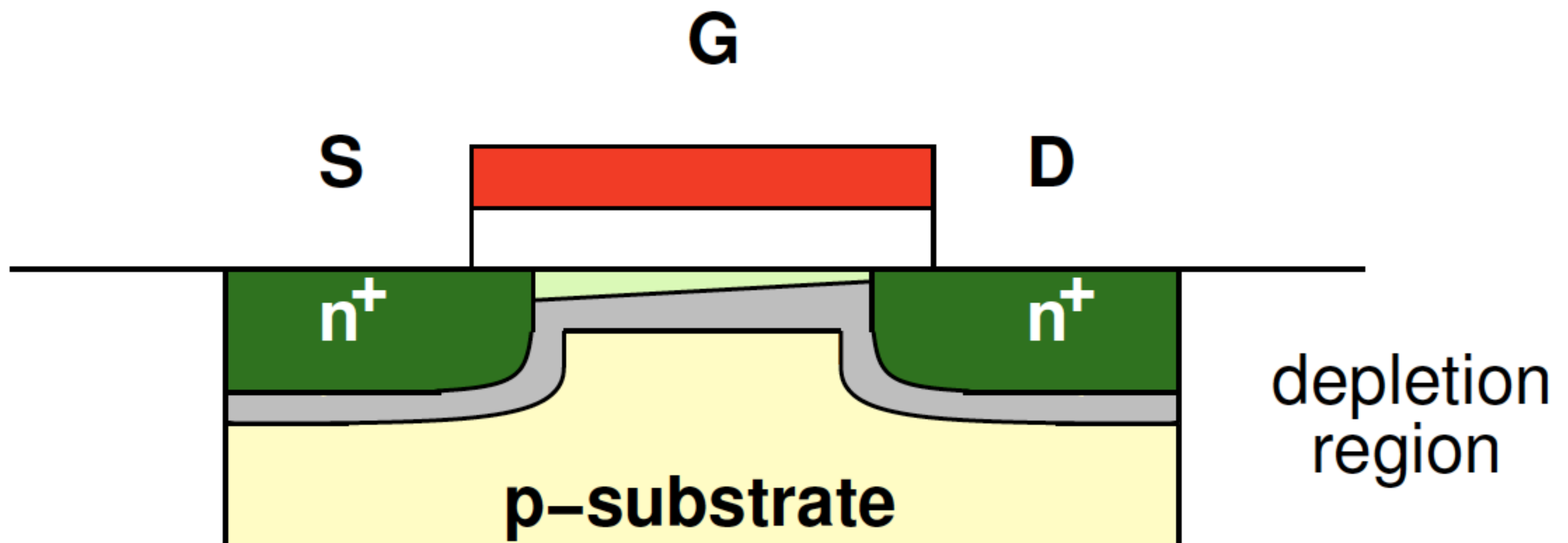
Preclass 3

- What is voltage in the middle of a resistive medium?
  - Relative to V1 and V2
  - halfway between terminals



Channel Voltage

- Think of channel as resistor
- Voltage varies along channel
  - Serves as a voltage divider between V_S and V_D



Voltage along Channel

- What does voltage along the channel look like?

Voltage along Channel

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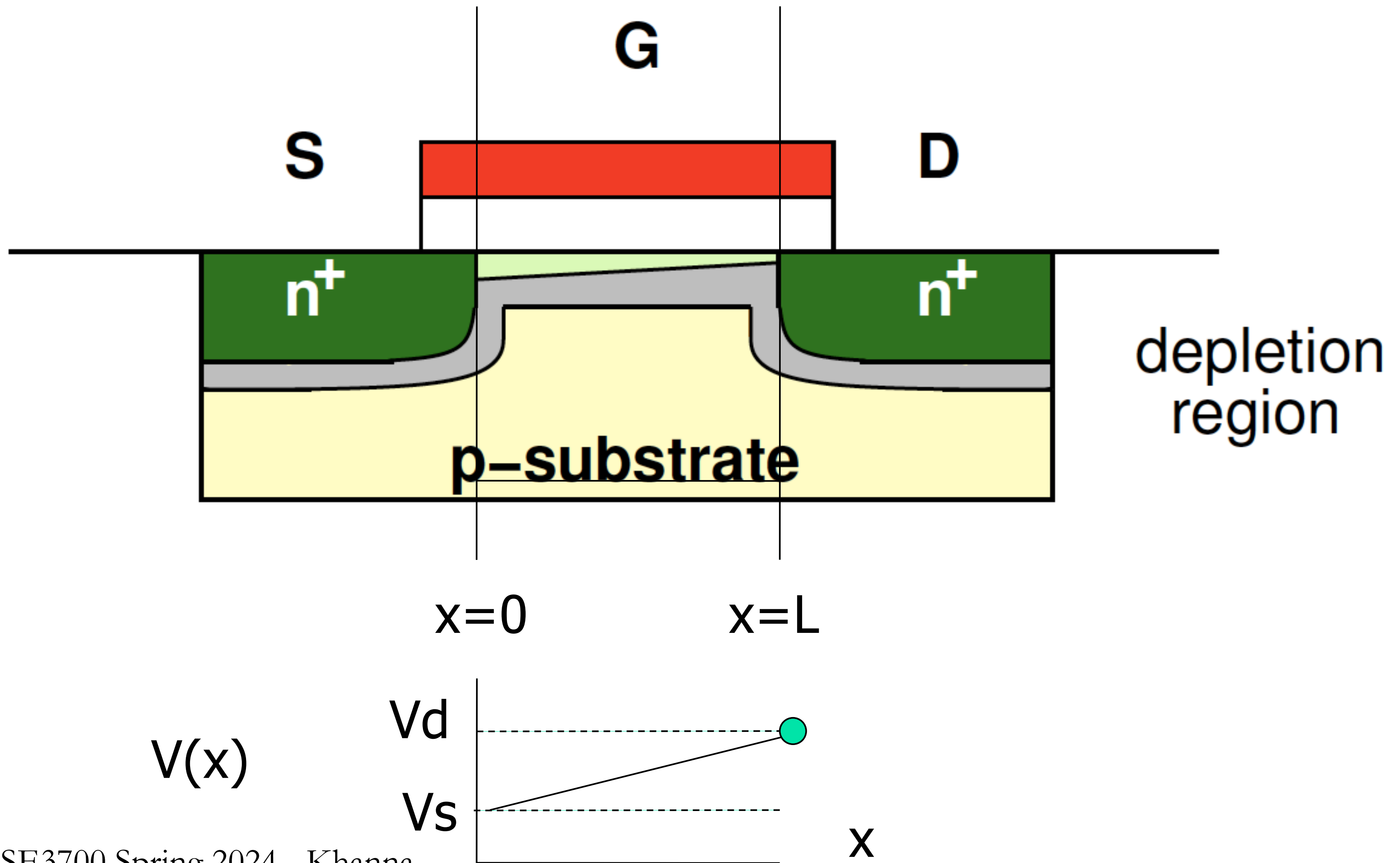
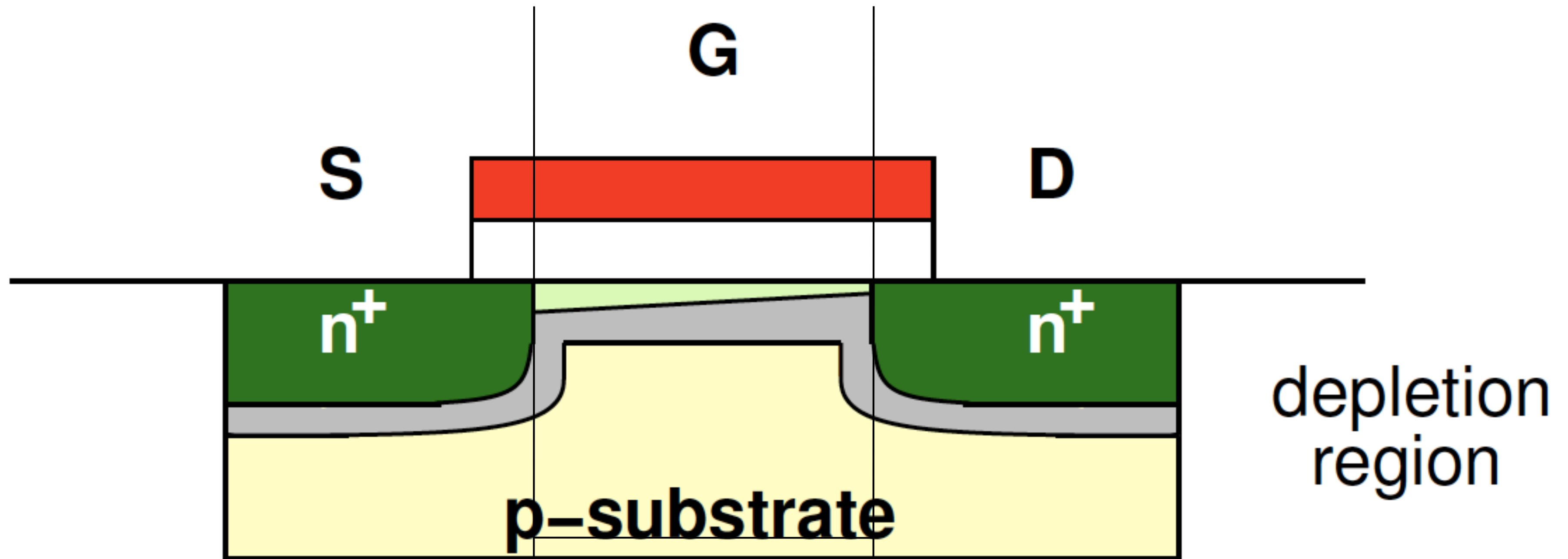
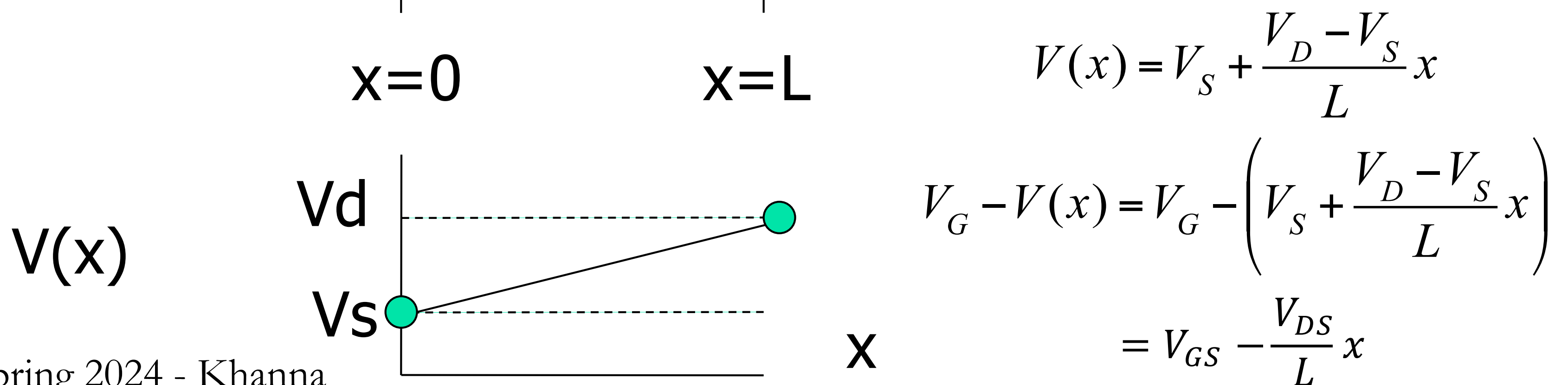


Voltage along Channel

- What does voltage along the channel look like?





$$V(x) = V_S + \frac{V_D - V_S}{L}x$$

$$V_G - V(x) = V_G - \left(V_S + \frac{V_D - V_S}{L}x\right)$$

$$= V_{GS} - \frac{V_{DS}}{L}x$$

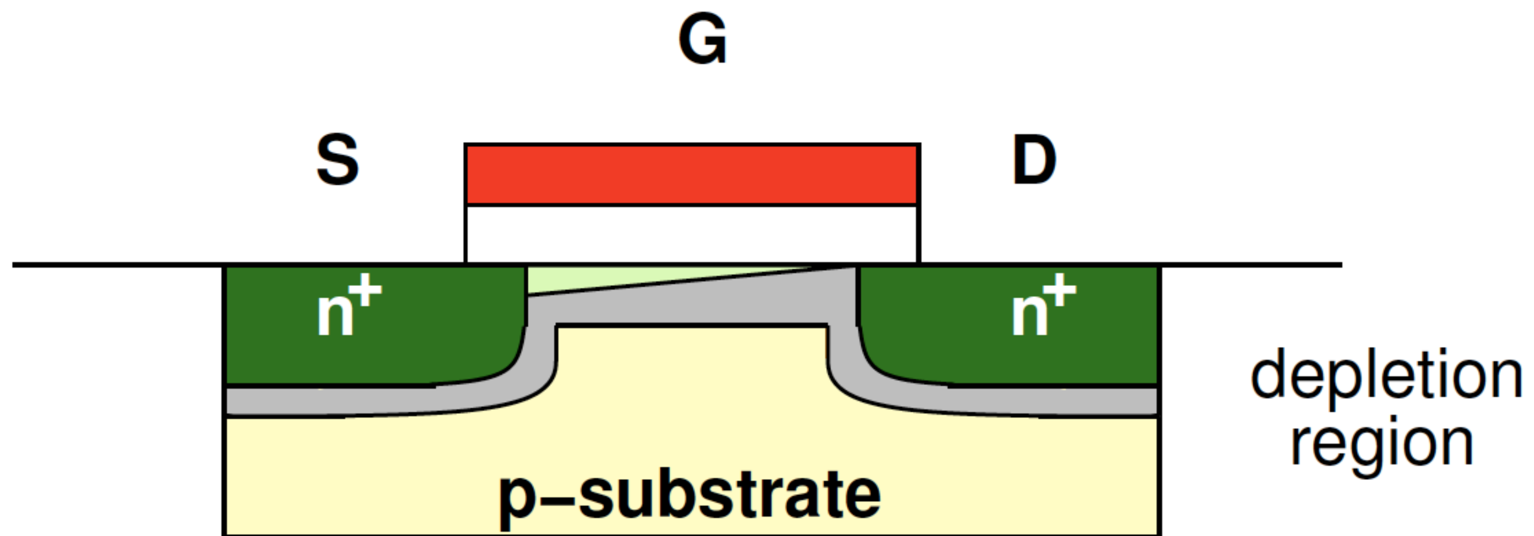
Channel Field

- When voltage gap V_G-V_x drops below V_{th}, drops out of inversion

G
S
D
V_x
n^+
n^+
depletion region
p–substrate

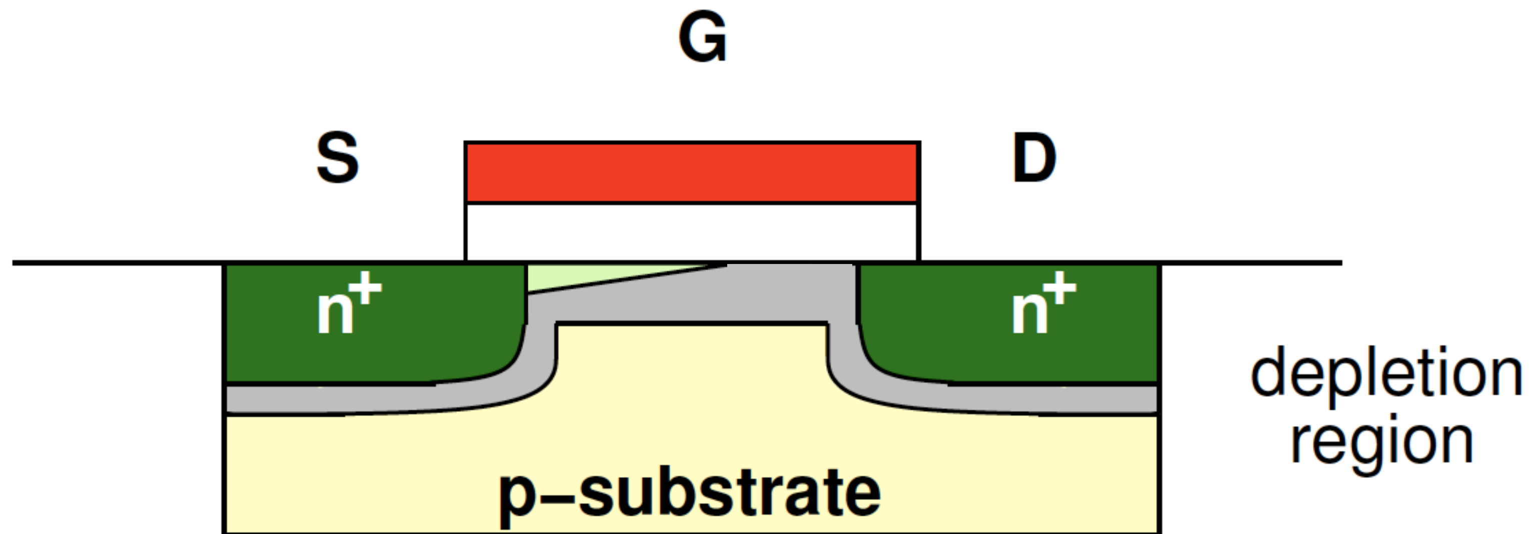
Channel Field

- When voltage gap V_G-V_x drops below V_{th}, drops out of inversion
  - Saturation Edge: $V_{DS} = V_{GS} - V_{th} \rightarrow V_G - V_X(@\ D) =$?



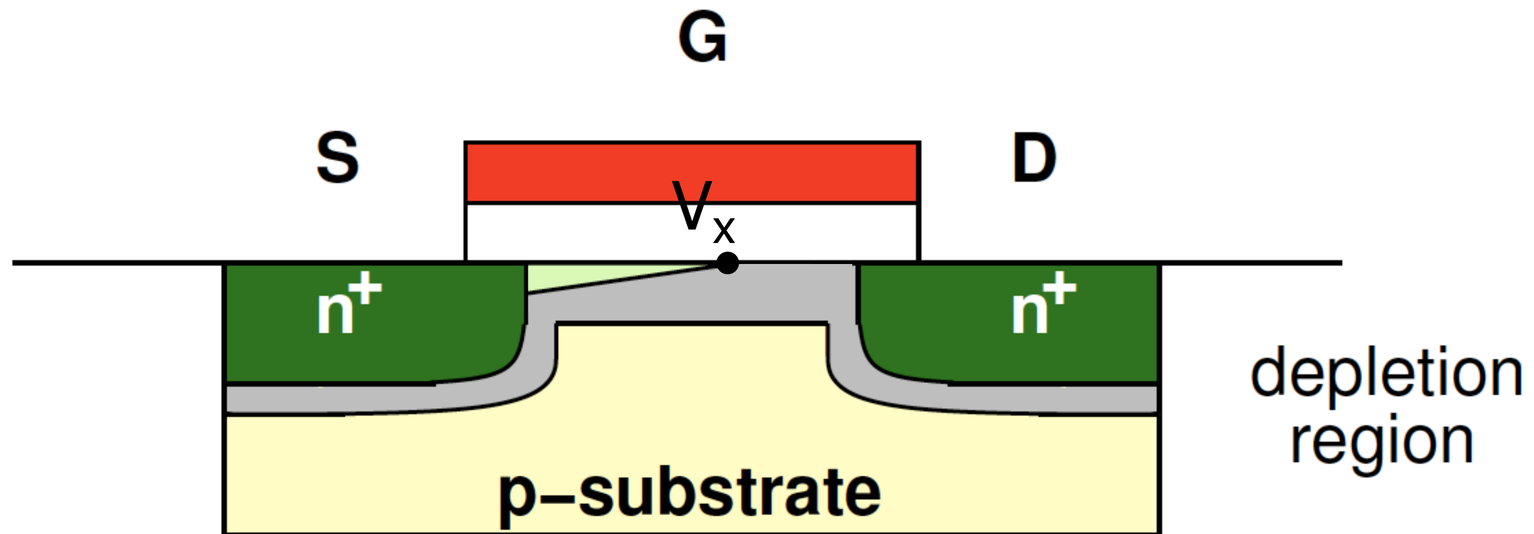
Channel Field

- When voltage gap V_G-V_x drops below V_{th}, drops out of inversion
  - Deep Saturation: $V_{DS} > V_{GS} - V_{th} \rightarrow V_G - V_X(@\ D) = ?$



Channel Field

- When voltage gap V_G-V_x drops below V_{th}, drops out of inversion
  - Deep Saturation: $V_{DS} > V_{GS} - V_{th} \rightarrow V_G - V_X(@\ D) < V_{th}$
    Upper limit on current, channel is "pinched off"



Channel Field

- When voltage gap V_G-V_x drops below V_{th}, drops out of inversion
  - What if $V_{DS} > V_{GS} - V_{th}$?
    - Upper limit on current, channel is "pinched off"
    - For what x, is V_G-$V(x)$=V_T?

G
S
D
V_x
n+
n+
depletion region
p–substrate

Channel Field

- When voltage gap V_G-V_x drops below V_{th}, drops out of inversion
  - What if $V_{DS} > V_{GS} – V_{th}$?
    - Upper limit on current, channel is "pinched off"
    - For what x, is V_G-$V(x)$=V_T?

$$V_G - V(x) = V_{GS} - \frac{V_{DS}}{L}x = V_T$$

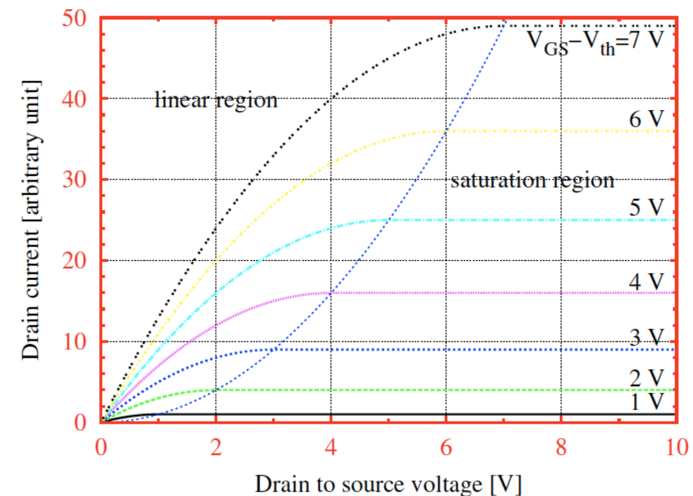
$$x = \frac{V_{GS} - V_T}{V_{DS}} L$$

G
S
D
V_x
n+
n+
depletion region
p–substrate

Pinch Off

- When voltage along the channel drops below V_{th}, the channel drops out of inversion
  - Occurs when: $V_G - V_X(@ D) < V_{th} \rightarrow V_{DS} > V_{GS} - V_{th}$

- **Conclusion:**
  - current cannot increase with V_{DS} once $V_{DS} > V_{GS}-V_T$
    - Not true! More later…



Saturation

- At edge of saturation, $V_{DS} = V_{GS} - V_T$

$$I_{DS} = \mu_n C_{OX}\left(\frac{W}{L}\right)\left[\left(V_{GS} - V_T\right)V_{DS} - \frac{V_{DS}^2}{2}\right]$$

- Becomes:

Saturation

- At edge of saturation, $V_{DS} = V_{GS} - V_T$

$$I_{DS} = \mu_n C_{OX}\left(\frac{W}{L}\right)\left[\left(V_{GS} - V_T\right)V_{DS} - \frac{V_{DS}^2}{2}\right]$$

- Becomes:

$$I_{DS} = \mu_n C_{OX}\left(\frac{W}{L}\right)\left[\left(V_{GS} - V_T\right)^2 - \frac{\left(V_{GS} - V_T\right)^2}{2}\right]$$

$$I_{DS} = \frac{\mu_n C_{OX}}{2}\left(\frac{W}{L}\right)\left[\left(V_{GS} - V_T\right)^2\right]$$

MOSFET – IV Characteristics

$$V_{DS} < V_{GS} - V_{TH}$$

linear region

saturation region

$$V_{DS} \geq V_{GS} - V_{TH}$$

$V_{GS}-V_{th}=7$ V

6 V

5 V

3 V

2 V

1 V

$V_{GS} - V_{th}$

I_{DS}

Drain current [arbitrary unit]

50
40
30
20
10
0

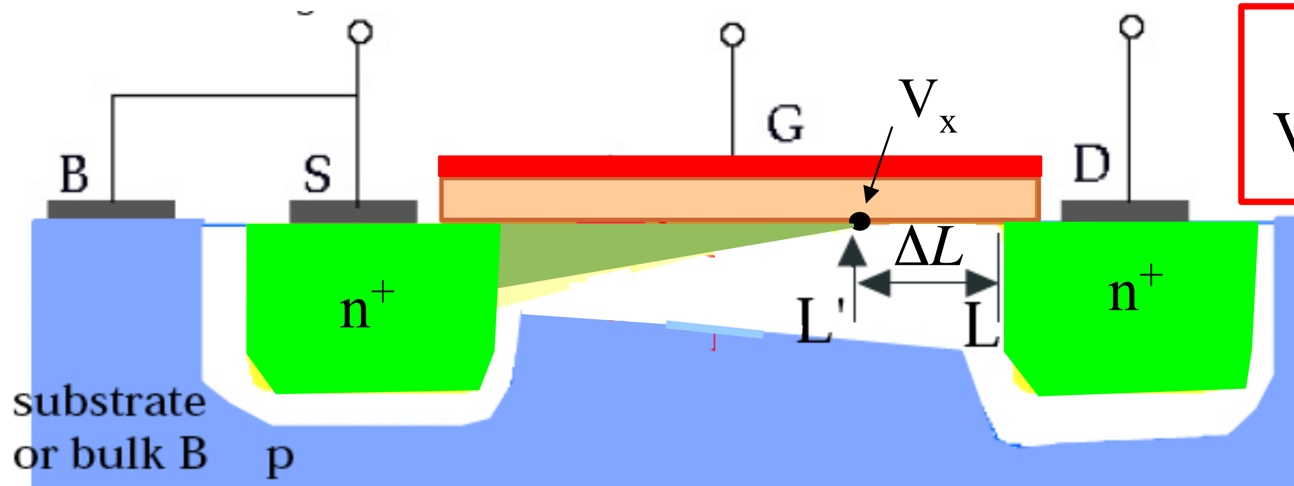
0 2 4 6 8 10

Drain to source voltage [V]

V_{DS}

Channel Length Modulation

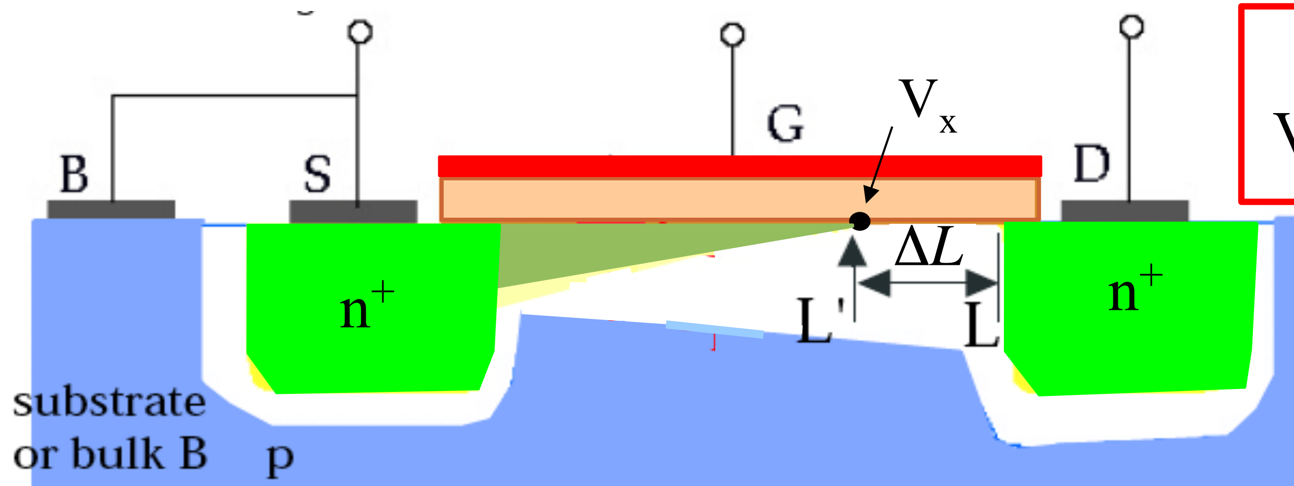
MOSFET IV Characteristics - Saturation



$V_{GS} > V_{T0}$
$V_{DS} > V_{GS} - V_{T0}$

$$I_{DS} = \frac{\mu_n \cdot C_{ox}}{2} \frac{W}{L'} \left(V_{GS} - V_{T0}\right)^2 = \frac{\mu_n \cdot C_{ox}}{2} \frac{W}{L - \Delta L} \left(V_{GS} - V_{T0}\right)^2$$

MOSFET IV Characteristics - Saturation



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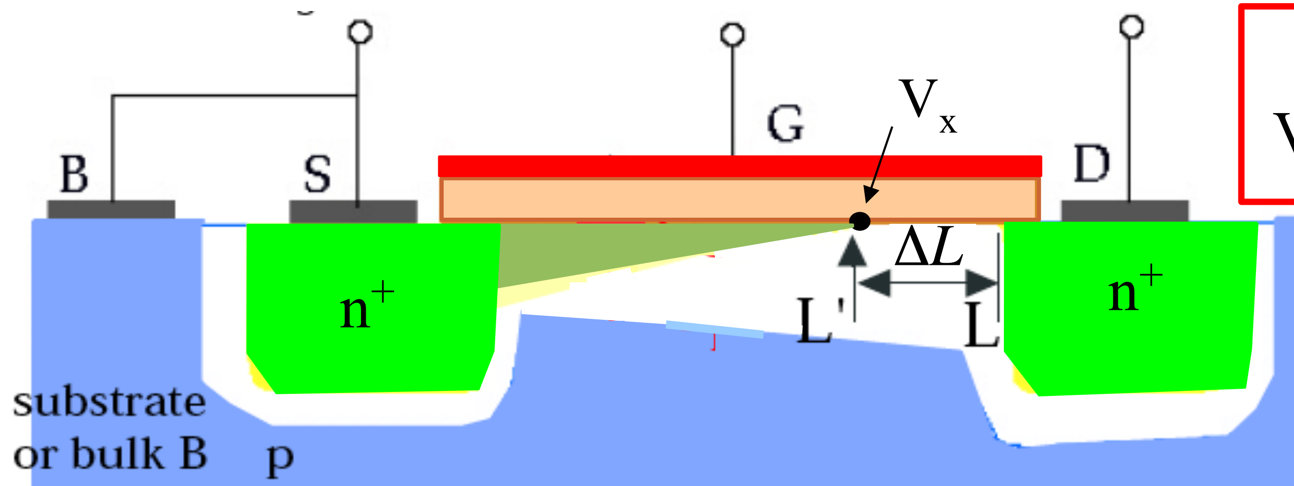
$$= \frac{\mu_n \cdot C_{ox}}{2} \frac{W}{L\left(1 - \frac{\Delta L}{L}\right)} \left(V_{GS} - V_{T0}\right)^2$$

$$= \frac{\mu_n \cdot C_{ox}}{2} \frac{W}{L} \left(V_{GS} - V_{T0}\right)^2 \frac{1}{\left(1 - \frac{\Delta L}{L}\right)}$$

MOSFET IV Characteristics - Saturation



$$V_{GS} > V_{T0}$$
$$V_{DS} > V_{GS} - V_{T0}$$

$$I_{DS} = \frac{\mu_n \cdot C_{ox}}{2} \frac{W}{L} \left(V_{GS} - V_{T0}\right)^2 \frac{1}{\left(1 - \frac{\Delta L}{L}\right)}$$

$$\Delta L \propto \sqrt{V_{DS} - (V_{GS} - V_{T0})} \xrightarrow{\text{empirically}} 1 - \frac{\Delta L}{L} \approx 1 - \lambda \cdot V_{DS}$$

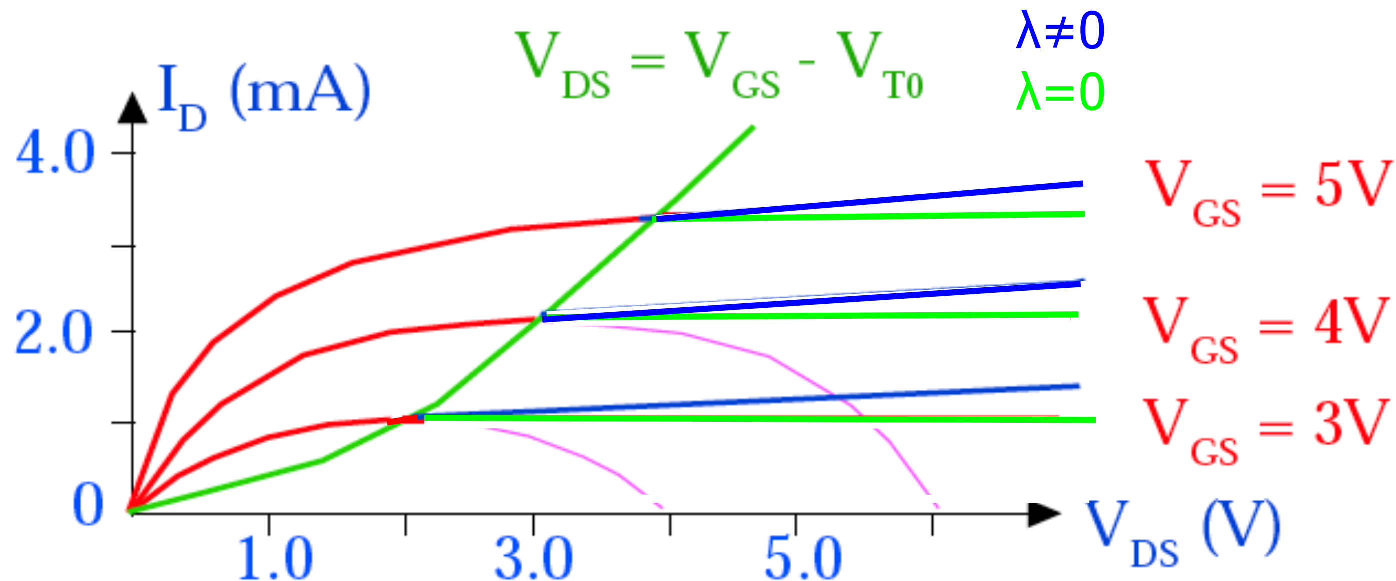
If $\lambda \cdot V_{DS} << 1$,

$$\left(1 - \frac{\Delta L}{L}\right)^{-1} \approx \boxed{1 + \lambda \cdot V_{DS}}$$

MOSFET IV Characteristics

Linear Region: $$I_D = \mu_n \cdot C_{ox} \frac{W}{L}\left((V_{GS} - V_{T0})V_{DS} - \frac{V_{DS}^2}{2}\right)$$

Saturation Region: $$I_D = \frac{\mu_n \cdot C_{ox}}{2} \frac{W}{L}\left(V_{GS} - V_{T0}\right)^2 (1 + \lambda \cdot V_{DS})$$



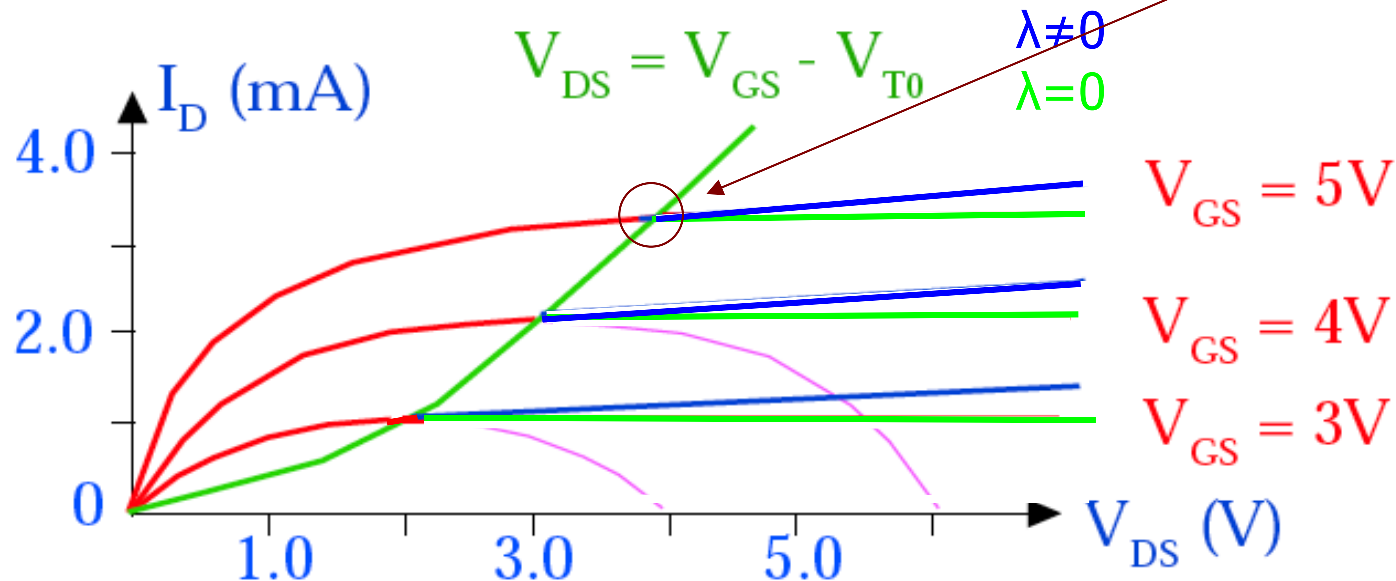
MOSFET IV Characteristics

Linear Region: $$I_D = \mu_n \cdot C_{ox} \frac{W}{L}\left((V_{GS} - V_{T0})V_{DS} - \frac{V_{DS}^2}{2}\right)$$

Saturation Region: $$I_D = \frac{\mu_n \cdot C_{ox}}{2} \frac{W}{L}\left(V_{GS} - V_{T0}\right)^2 (1 + \lambda \cdot V_{DS})$$

DISCONTINUOUS!

@ $V_{DS} = V_{GS} - V_T$



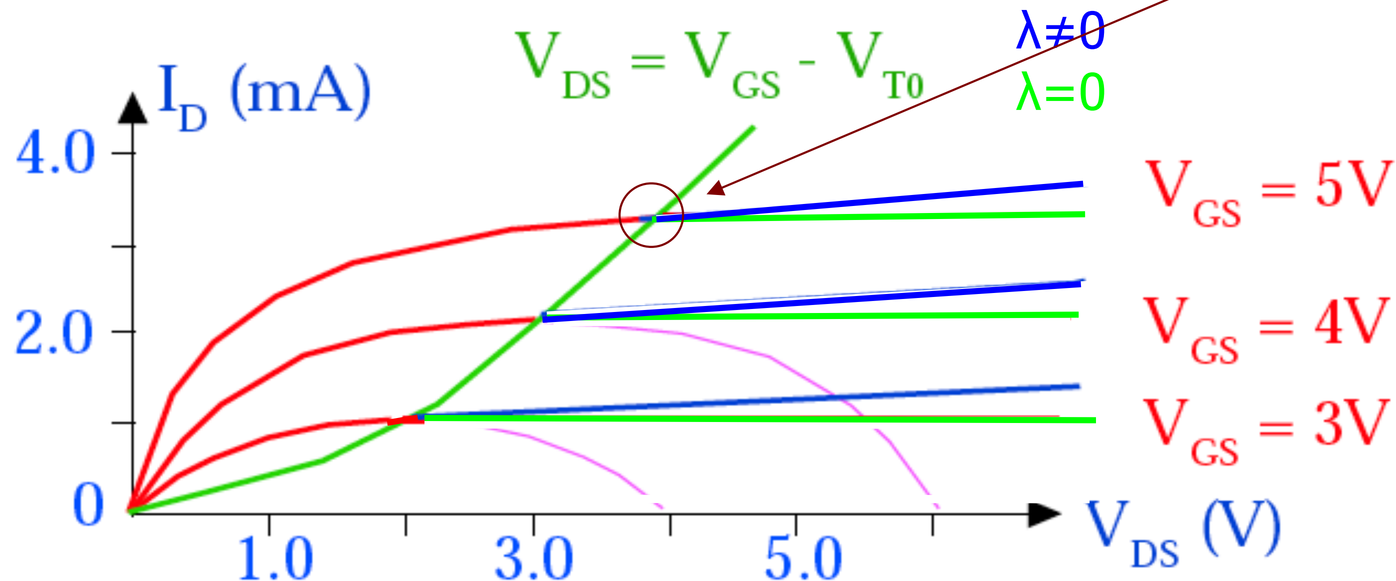
MOSFET IV Characteristics

Linear Region: $$I_D = \mu_n \cdot C_{ox} \frac{W}{L}\left((V_{GS} - V_{T0})V_{DS} - \frac{V_{DS}^2}{2}\right)(1 + \lambda \cdot V_{DS})$$

Saturation Region: $$I_D = \frac{\mu_n \cdot C_{ox}}{2} \frac{W}{L}\left(V_{GS} - V_{T0}\right)^2 (1 + \lambda \cdot V_{DS})$$

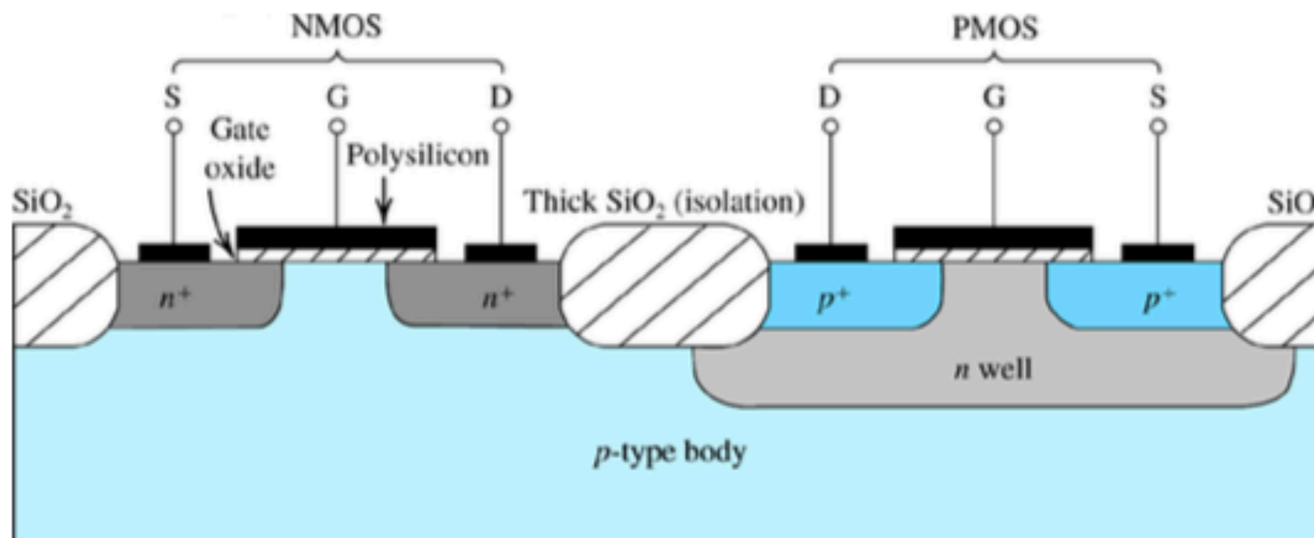
~~DIS~~CONTINUOUS!

@ $V_{DS} = V_{GS} - V_T$



pMOS Device

- Analogous phenomena to NMOS
- Opposite polarity
  - Negative V_{th}, λ
- Reason based on oppositely charged carriers

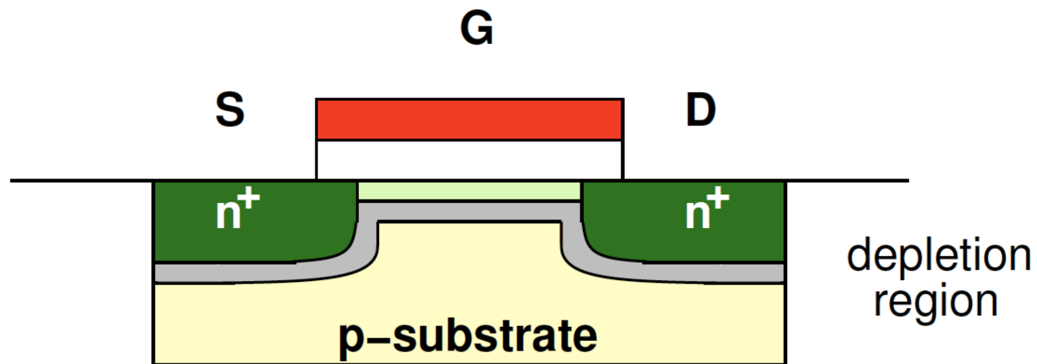


Above Threshold

Summary

Linear Region

- $V_{GS} > V_{th}$ and V_{DS} small



$$C_{OX} = \frac{\varepsilon_{OX}}{t_{OX}}$$

$$I_{DS} = \mu_n C_{OX} \left(\frac{W}{L}\right)\left[\left(V_{GS} - V_{th}\right)V_{DS} - \frac{V_{DS}^2}{2}\right]$$

Saturation

- In saturation, $V_{DS\text{-effective}} = V_x = V_{GS} - V_T$

$$I_{DS} = \mu_n C_{OX}\left(\frac{W}{L}\right)\left[\left(V_{GS} - V_T\right)V_{DS} - \frac{V_{DS}^2}{2}\right]$$

- Becomes:

$$I_{DS} = \mu_n C_{OX}\left(\frac{W}{L}\right)\left[\left(V_{GS} - V_T\right)^2 - \frac{\left(V_{GS} - V_T\right)^2}{2}\right]$$

$$I_{DS} = \frac{\mu_n C_{OX}}{2}\left(\frac{W}{L}\right)\left[\left(V_{GS} - V_T\right)^2\right]$$

MOSFET – IV Characteristics

$V_{DS} < V_{GS} - V_{TH}$

linear region

$V_{GS}-V_{th}$=7 V

6 V

saturation region

5 V

$V_{DS} \geq V_{GS} - V_{TH}$

3 V

2 V

1 V

50
40
30
20
10
0

0 2 4 6 8 10

Drain current [arbitrary unit]

Drain to source voltage [V]

I_{DS}

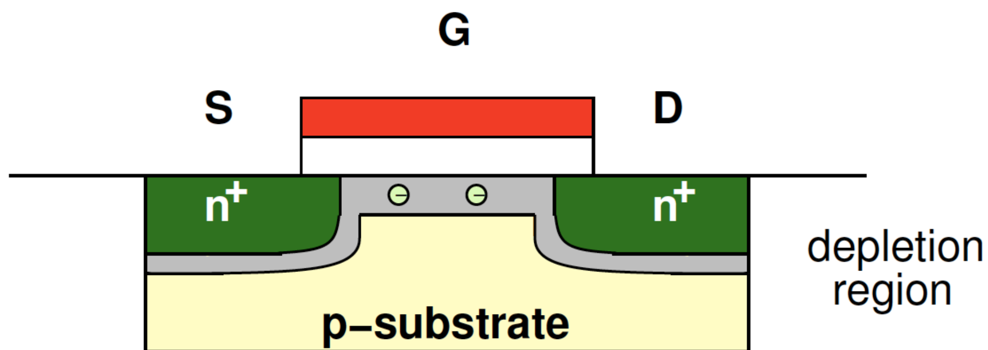
V_{DS}

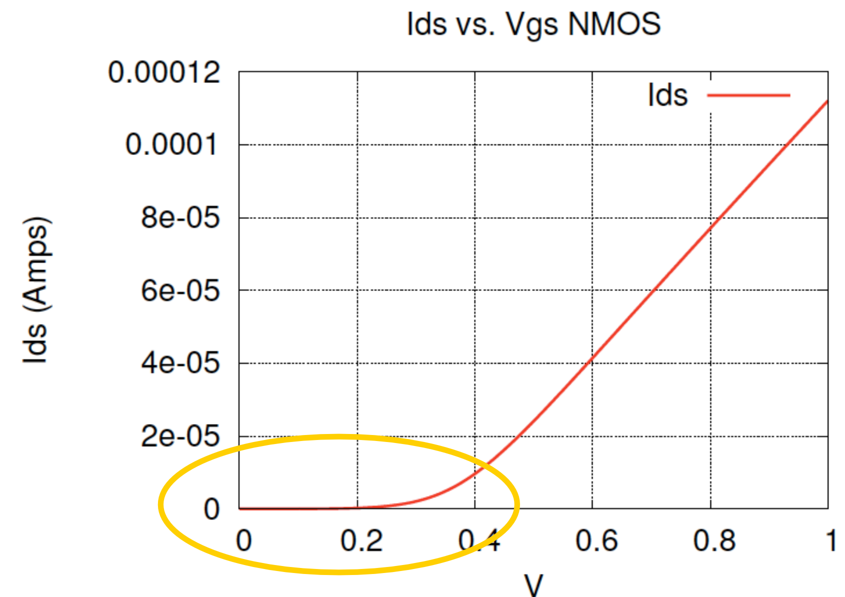
$V_{GS} - V_{th}$

Subthreshold

Below Threshold

- Transition from insulating to conducting is non-linear, but not abrupt
- Current does flow below threshold
  - But exponentially dependent on V_{GS}





Below Threshold

- Transition from insulating to conducting is non-linear, but not abrupt
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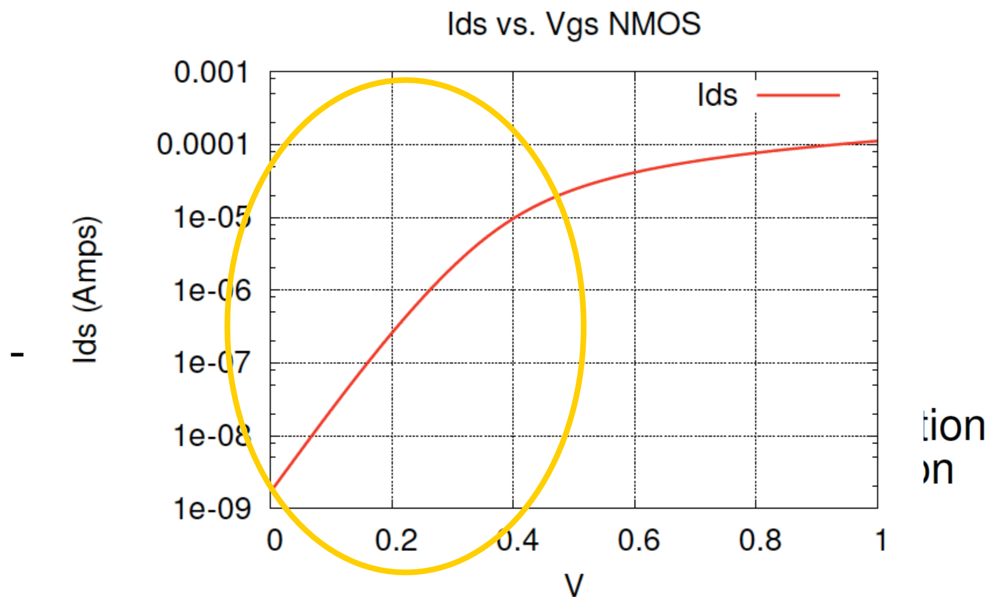
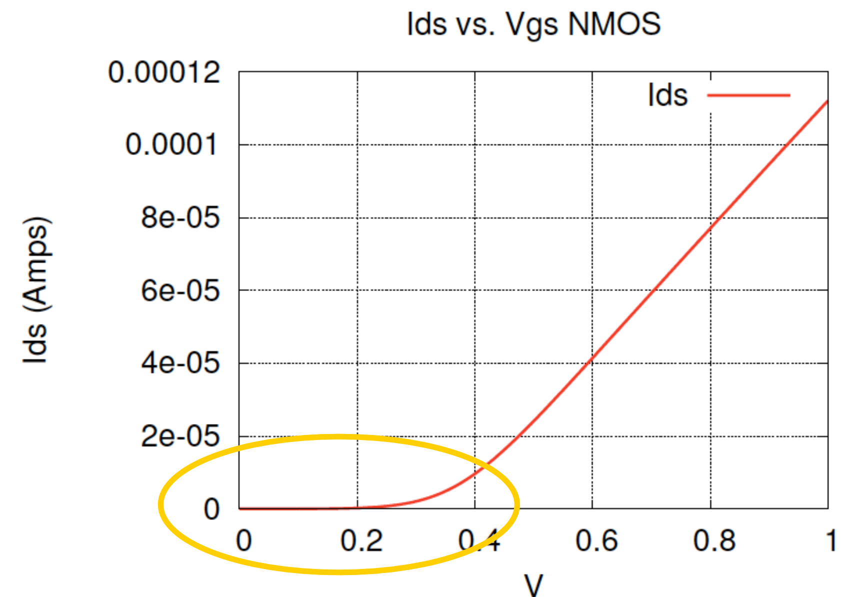
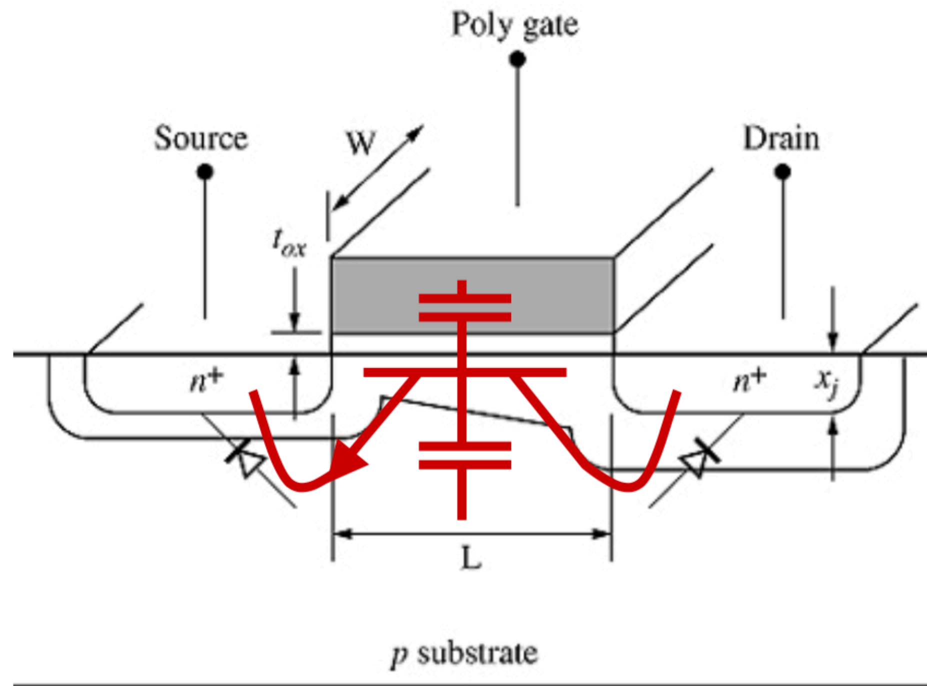




Parasitic NPN BJT

- We have an NPN sandwich, mobile minority carriers in the P region
- This is a BJT!
  - Except that the base potential is here controlled through a capacitive divider, and not directly an electrode



Subthreshold

$$\text{If} \quad V_{GS} < V_{th},$$

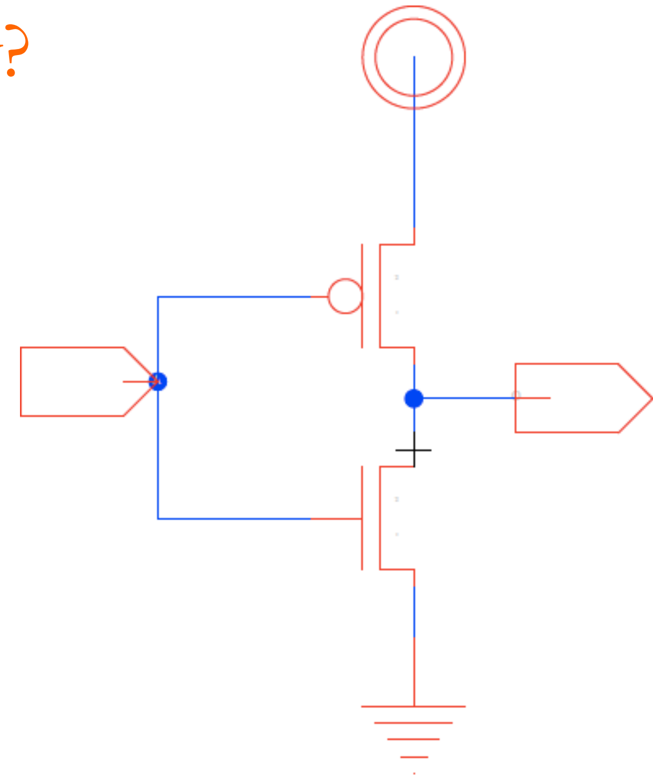
$$I_{DS} = I_S \left(\frac{W}{L}\right) e^{\left(\frac{V_{GS}-V_{th}}{nkT/q}\right)}$$

- Current is from the parasitic NPN BJT transistor when gate is below threshold and there is no conducting channel
  - n is the capacitive divider between parasitic capacitances
  - Typically 1 < n < 1.5

$$n = \frac{C_{js} + C_{ox}}{C_{ox}}$$

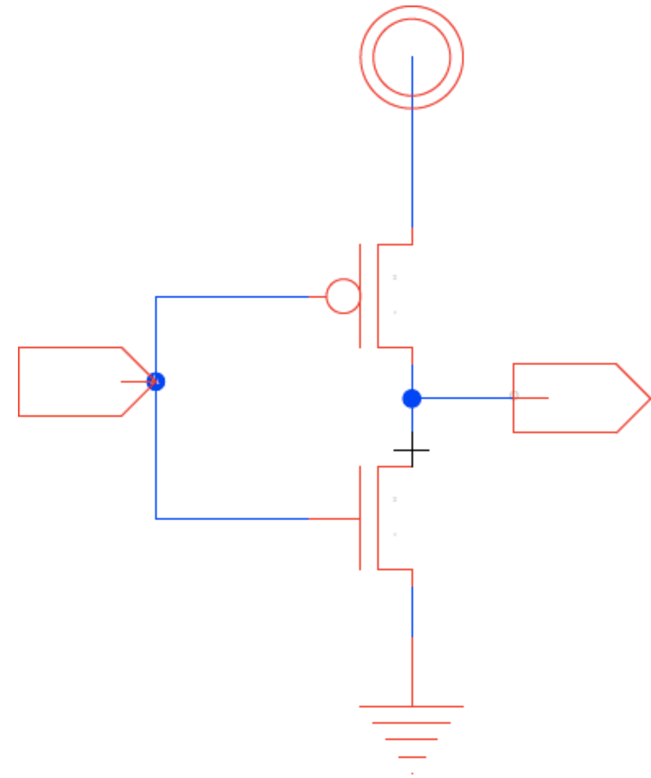
Steady State (Preclass 4)

- What current flows in steady state?
- What causes (and determines) the magnitude of current flow?
- Which device?



Leakage

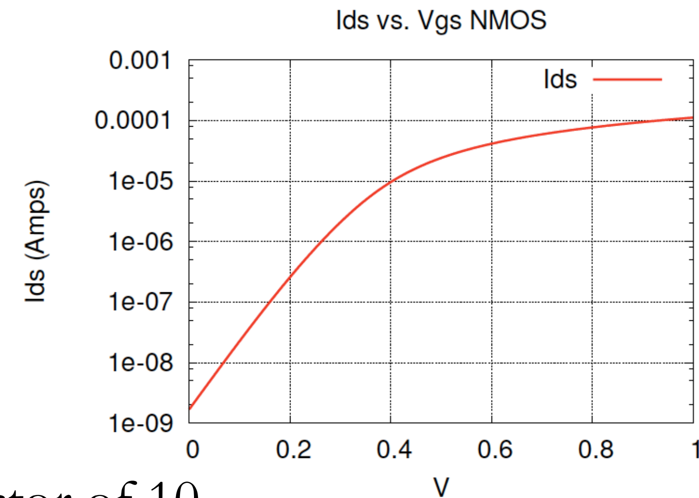
- Call this steady-state current flow leakage
  - $I_{ds,leakage}$



Subthreshold Slope Factor

- Exponent in V_{GS} determines how steep the turnon is

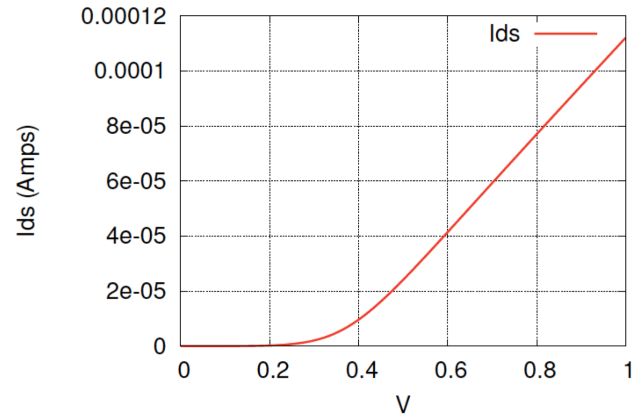
$$S = n\left(\frac{kT}{q}\right)\ln(10)$$



  - Units: V/decade
    - Every S Volts, I_{DS} is scaled by factor of 10

$$I_{DS} = I_S\left(\frac{W}{L}\right)e^{\left(\frac{V_{GS}-V_{th}}{nkT/q}\right)}$$

I_{DS} vs. V_{GS}



Ids vs. Vgs NMOS

Ids

Ids (Amps)

0.001
0.0001
1e-05
1e-06
1e-07
1e-08
1e-09

0 0.2 0.4 0.6 0.8 1

V

$$S = n\left(\frac{kT}{q}\right)\ln(10)$$

(Logscale)

Subthreshold Slope Factor

- Exponent in V_{GS} determines how steep the turnon is

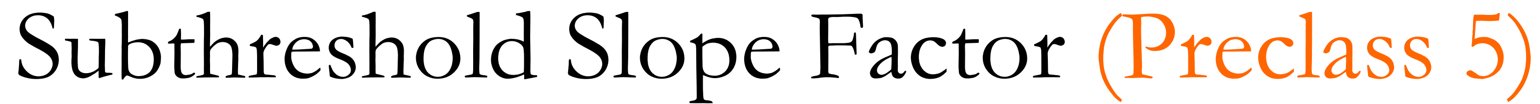
$$S = n\left(\frac{kT}{q}\right)\ln(10)$$

  - Units: V/dec
  - Every S Volts, I_{DS} is scaled by factor of 10

- n – depends on parasitic capacitance divider

$$n = \frac{C_{js} + C_{ox}}{C_{ox}}$$

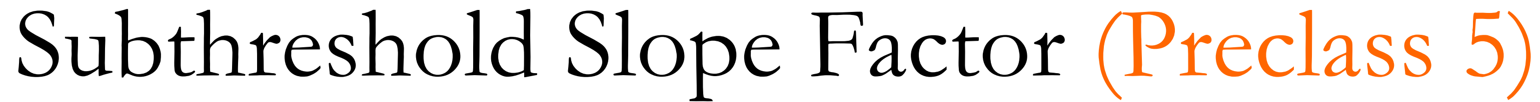
  - n=1 → S=60mV at Room Temp. (ideal)
  - n=1.5 → S=90mV
  - Single gate structure showing S=90-110mV



Subthreshold Slope Factor (Preclass 5)

- If S=100mV and V_{th}=300mV,
  what is Ids(Vgs=300mV)/Ids(Vgs=0V) ?

$$S = n\left(\frac{kT}{q}\right)\ln(10)$$



Subthreshold Slope Factor (Preclass 5)

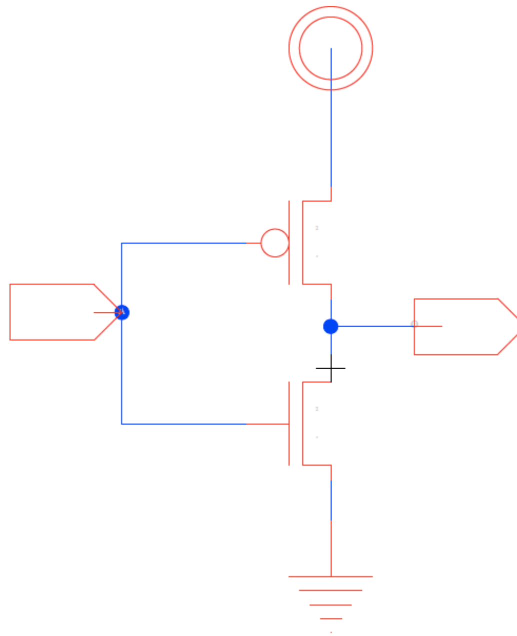
- If S=100mV and V_{th}=300mV, what is Ids(Vgs=300mV)/Ids(Vgs=0V) ?

- What if S=60mV?

$$S = n\left(\frac{kT}{q}\right)\ln(10)$$

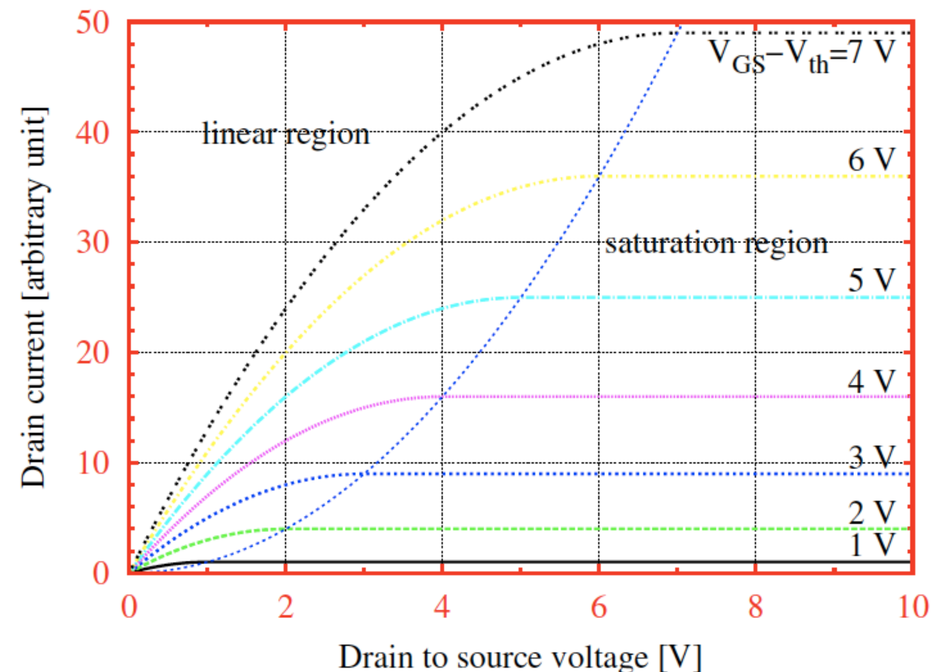
Approach

- Identify Region
- Understand governing equations
- Use region and equations to understand operation



Big Idea

- Semiconductor can act like metal or insulator
- Use electric field to modulate conduction state of semiconductor
- 3 Regions of operation for MOSFET
  - Linear
  - Saturation
    - With channel length modulation
  - Subthreshold



Admin

- HW 2 due 2/9 (Friday)
  - Make sure you label plots with node names (label nodes with relevant names, not just net0)
  - Reminder: OH every day of the week

- More Fabrication Videos:
  - From sand to silicon (intel) - https://www.youtube.com/watch?v=Q5paWn7bFg4
  - How microchips are made - https://www.youtube.com/watch?v=F2KcZGwntgg

Acknowledgement

- Prof. André DeHon (University of Pennsylvania)
- Prof. Jing Li (University of Pennsylvania)