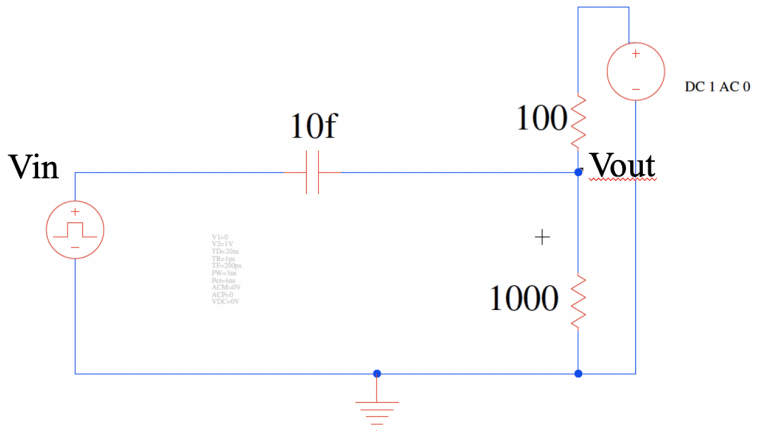
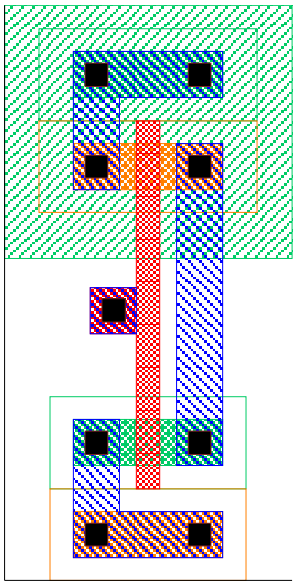
1. Assuming a step input from 0 to 1V by the pulse generator on the left, what does the voltage on $Vout$ as a function of time look like?



Hints: What is the initial voltage? What is the steady-state voltage as $t \to \infty$?

2. Consider the following layout for a CMOS inverter:



(a) The bar at the very top is V_{dd}, the one at the bottom is GND.

(b) Try to identify the PMOS and NMOS transistors. (Hint, the PMOS is on top and the NMOS is on bottom, like we draw schematics.)

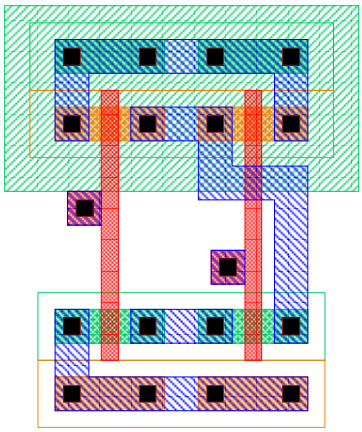
(c) Can you identify how the PMOS and NMOS transistors are connected?

(d) Where is the output?

(e) Where is the input?

This exercise is more "inclass" than "preclass". This is probably too foreign for you to do at the beginning of lecture (but maybe the questions about the structure on the previous page will help), but by the end of the lecture you should be able to do this.

3. Consider the following layout:



(a) How many PMOS transistors?

(b) How many NMOS transistors?

(c) How are the PMOS and NMOS transistors connected?

PMOS

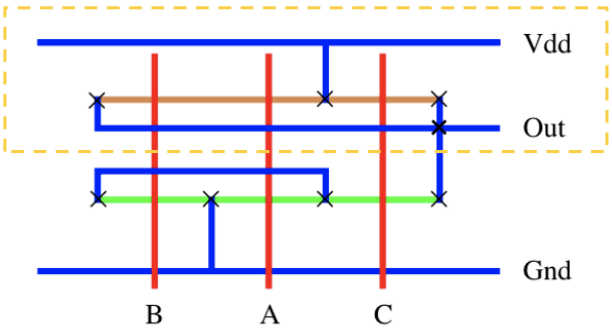
NMOS

(d) How is the output connected to the transistors?

(e) How are the inputs connected?

(f) What function does this circuit perform?

4. What is the gate function of the stick diagram below? Draw the corresponding schematic.



Ideal scaling:

L	1/S
W	1/S
t_{OX}	1/S
N_A	S
V	1/S

5. What is the scale factor, $1/S$, between a 32nm process and a 22nm process?

6. Under ideal scaling, how do the following characteristics scale?
(get started on what you can; we will complete together during lecture)

Area	
Capacitance, C_{ox}	
Capacitance, C_g	
Resistance	
V_{th}	1/S (given)
Current (I_{ds})	
Gate Delay (τ_{gd})	
Wire Delay	
Power [same freq]	
Power [scale freq $1/\tau_{td}$]	
Power Density (P/A) [same freq (f)]	
Power Density (P/A) [scale freq $1/\tau_{td}$]	

Note: Dynamic power in CMOS is capacitive charging: $P \propto CV^2 f$
(we will address on future lectures)