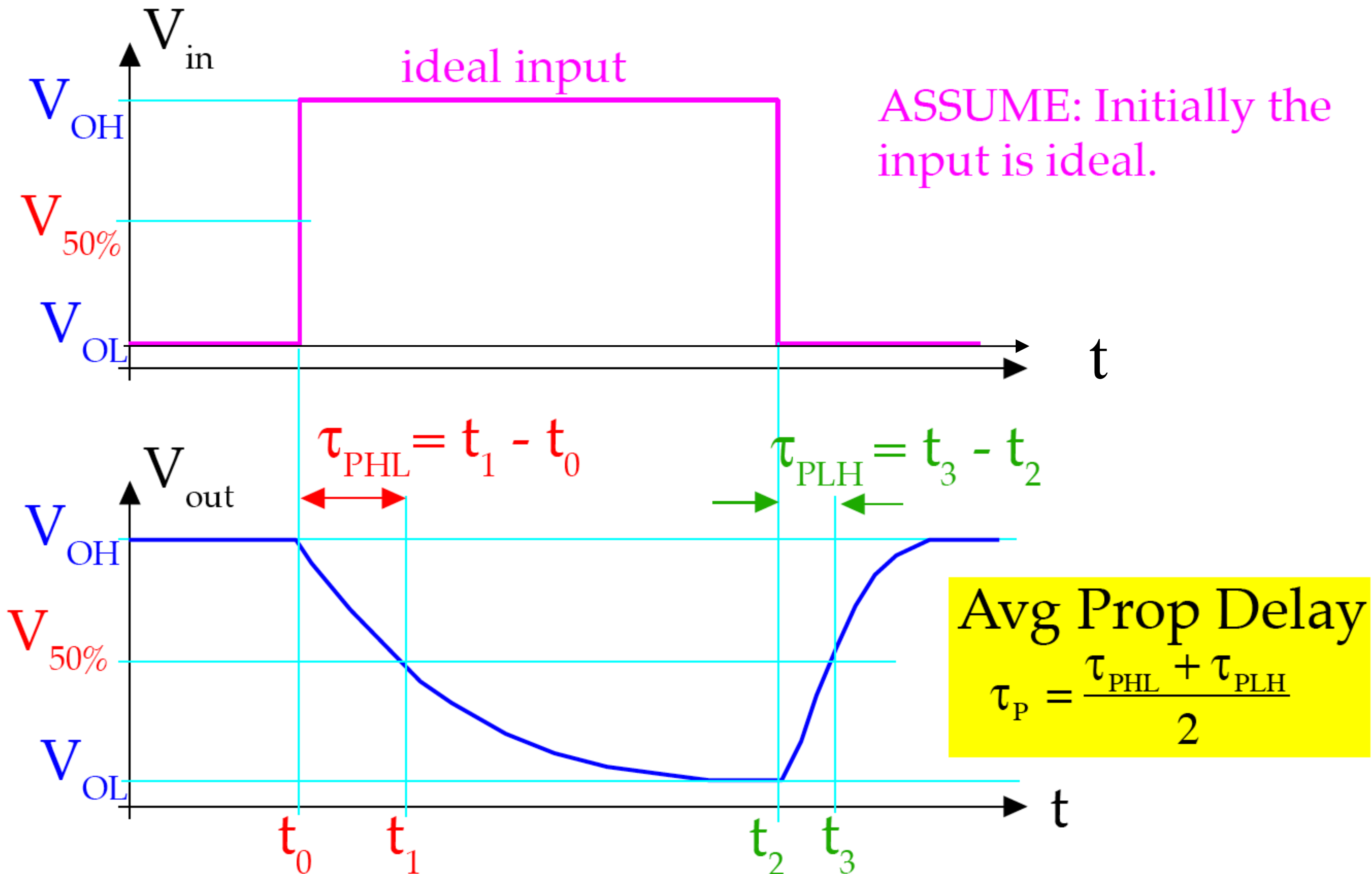
ESE3700: Circuit-Level Modeling, Design and Optimization for Digital Systems

Lec 8: February 19, 2024

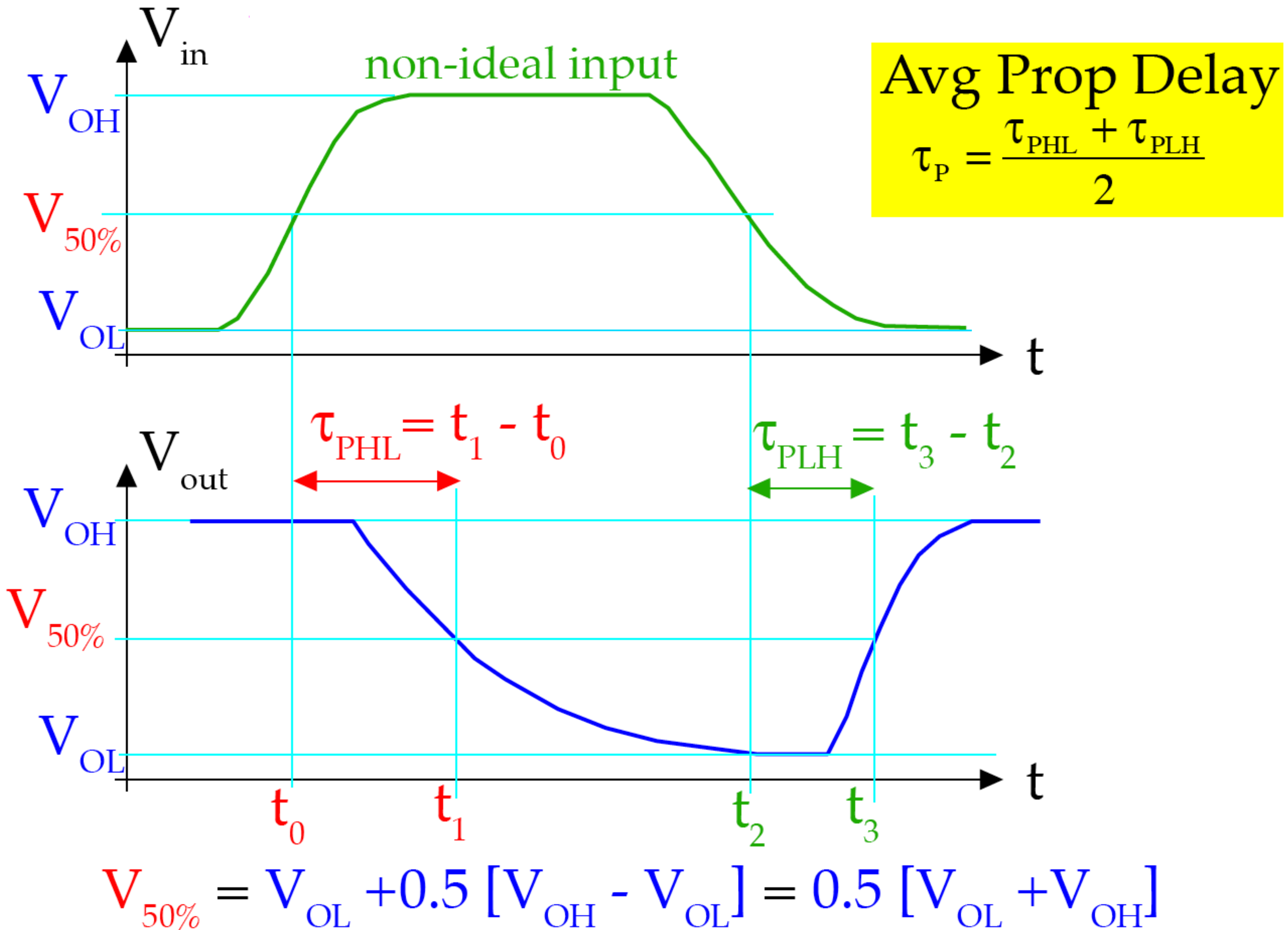
MOS Scaling (con't), MOS Variation

Penn

Propagation Delay Definitions

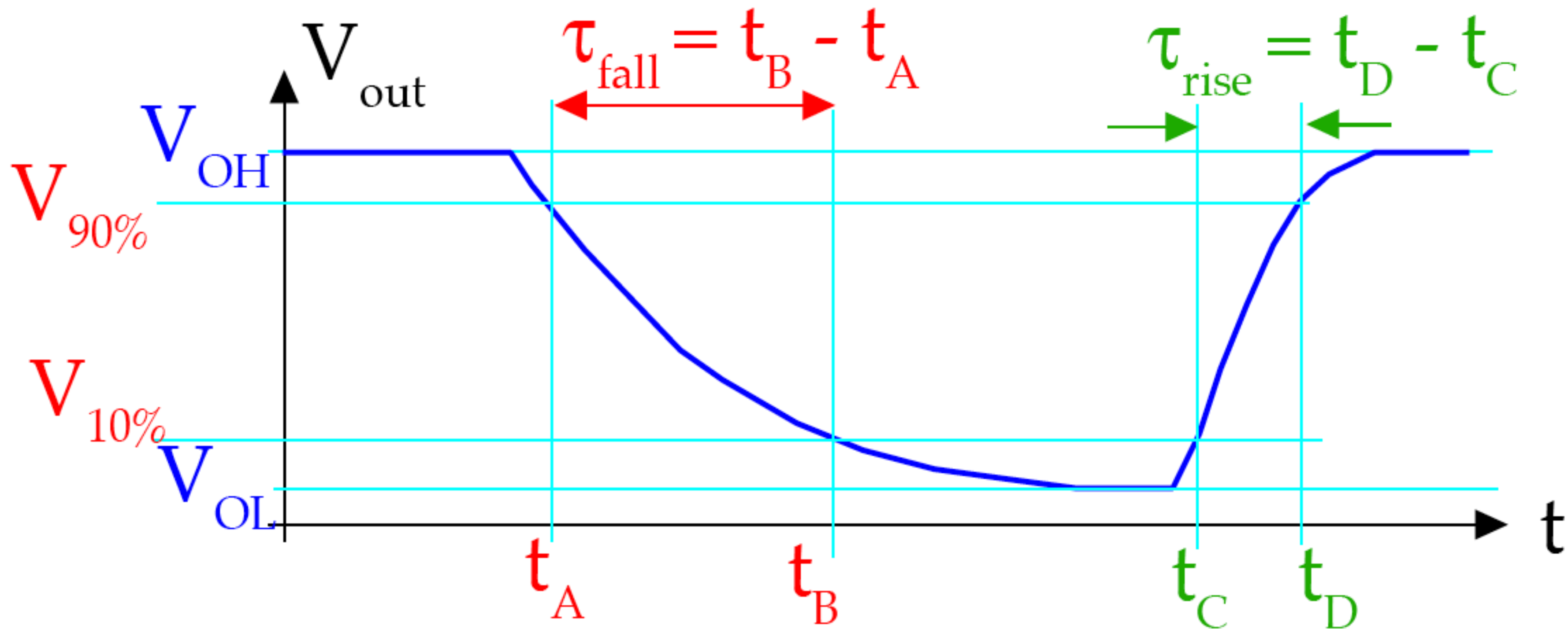


Propagation Delay Definitions



$$V_{50\%} = V_{OL} + 0.5\,[V_{OH} - V_{OL}] = 0.5\,[V_{OL} + V_{OH}]$$

Rise/Fall Times



$$V_{10\%} = V_{OL} + 0.1\,[V_{OH} - V_{OL}]$$

$$V_{90\%} = V_{OL} + 0.9\,[V_{OH} - V_{OL}]$$

MOS Scaling (con't)

Effects? (Preclass 1)

- Area $1/S^2$
- Capacitance (C_{ox}, C_g) S, $1/S$
- Wire Resistance S
- Threshold (V_{th}) $1/S$
- Current (I_d) $1/S$
- Gate Delay (τ_{gd}) $1/S$
- Wire Delay (τ_{wire}) 1
- Power $1/S^3$, $1/S^2$ (increased freq)
- Power Density $1/S$, 1 (increased freq)

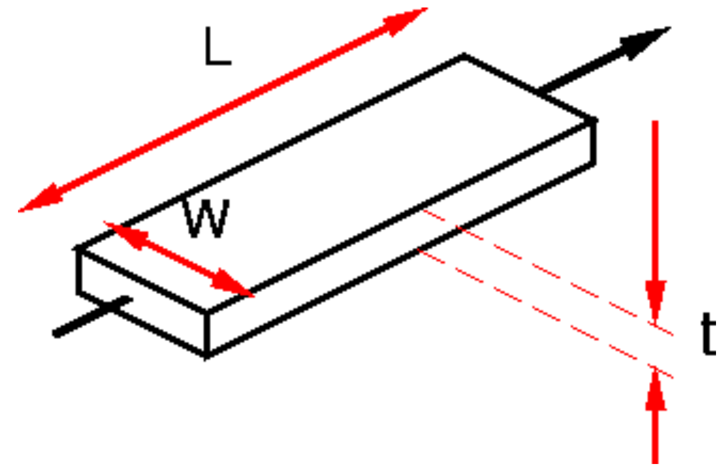
$1/S=0.7$

But…

- Don't like some of the implications
  - High resistance wires
  - Higher gate oxide capacitance with atomic-scale dimensions
    - …. Quantum tunneling
  - Need for more wiring
  - Not scale speed fast enough

Improving Resistance

- $R = \rho L / (W \times t)$
- W' → W/S
  - L, t similar
- R' → R×S



Improving Resistance

- $R = \rho L / (W \times t)$
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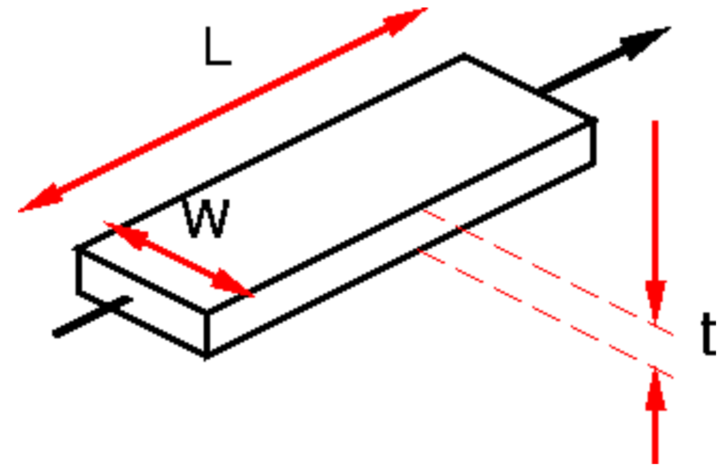
  - L, t similar
- $R' \rightarrow R \times S$



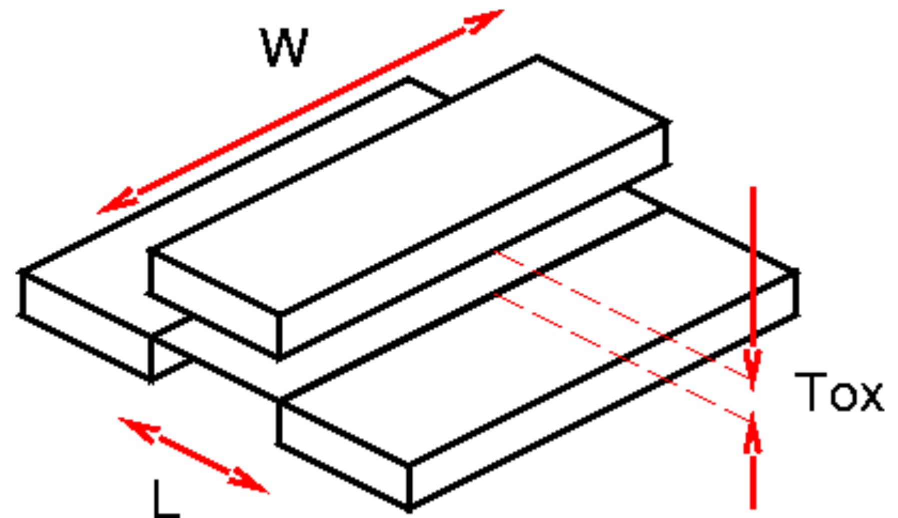
What might we do?

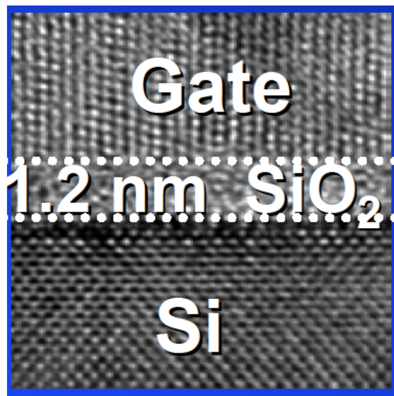
Decrease ρ (copper) – introduced 1997

http://www.ibm.com/ibm100/us/en/icons/copperchip/

Capacitance and Leakage

- Capacitance per unit area
  - $C_{ox} = \varepsilon_{SiO_2} / t_{ox}$
  - $t'_{ox} \rightarrow t_{ox}/S$
  - $C'_{ox} \rightarrow C_{ox} \times S$



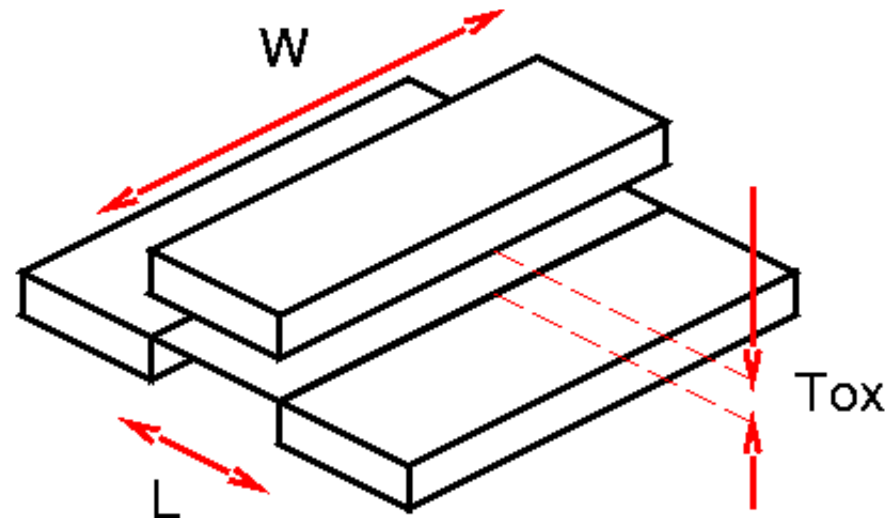


What's wrong with t_{ox} = 1.2nm?

source: Borkar/Micro 2004

Capacitance and Leakage

- Capacitance per unit area
  - $C_{ox} = \varepsilon_{SiO_2} / t_{ox}$
  - $t'_{ox} \rightarrow t_{ox}/S$
  - $C'_{ox} \rightarrow C_{ox} \times S$



What might we do?

Reduce dielectric constant, ε, and not scale thickness to mimic t_{ox} scaling.

High-K dielectric Survey

Table 2 Selected material and electrical properties of high-*k* gate dielectrics. Data compiled from Robertson [25], Gusev et al. [20], Hubbard and Schlom [19], and other sources.

Dielectric	*Dielectric constant (bulk)*	*Bandgap (eV)*	*Conduction band offset (eV)*	*Leakage current reduction w.r.t. SiO_2*	*Thermal stability w.r.t. silicon (MEIS data)*
Silicon dioxide (SiO_2)	3.9	9	3.5	N/A	>1050°C
Silicon nitride (Si_3N_4)	7	5.3	2.4		>1050°C
Aluminum oxide (Al_2O_3)	~10	8.8	2.8	10^2–10^3×	~1000°C, RTA
Tantulum pentoxide (Ta_2O_5)	25	4.4	0.36		Not thermodynamically stable with silicon
Lanthanum oxide (La_2O_3)	~21	6*	2.3		
Gadolinium oxide (Gd_2O_3)	~12				
Yttrium oxide (Y_2O_3)	~15	6	2.3	10^4–10^5×	Silicate formation
Hafnium oxide (HfO_2)	~20	6	1.5	10^4–10^5×	~950°C
Zirconium oxide (ZrO_2)	~23	5.8	1.4	10^4–10^5×	~900°C
Strontium titanate ($SrTiO_3$)		3.3	−0.1		
Zirconium silicate ($ZrSiO_4$)		6*	1.5		
Hafnium silicate ($HfSiO_4$)		6*	1.5		

*Estimated value.

Wong/IBM J. of R&D, V46N2/3P133—168, 2002

Wire Layers = More Wiring

Metal Levels

ITRS2005
ITRS2001
(unidentified)

Metal Levels

14
12
10
8
6
4
2

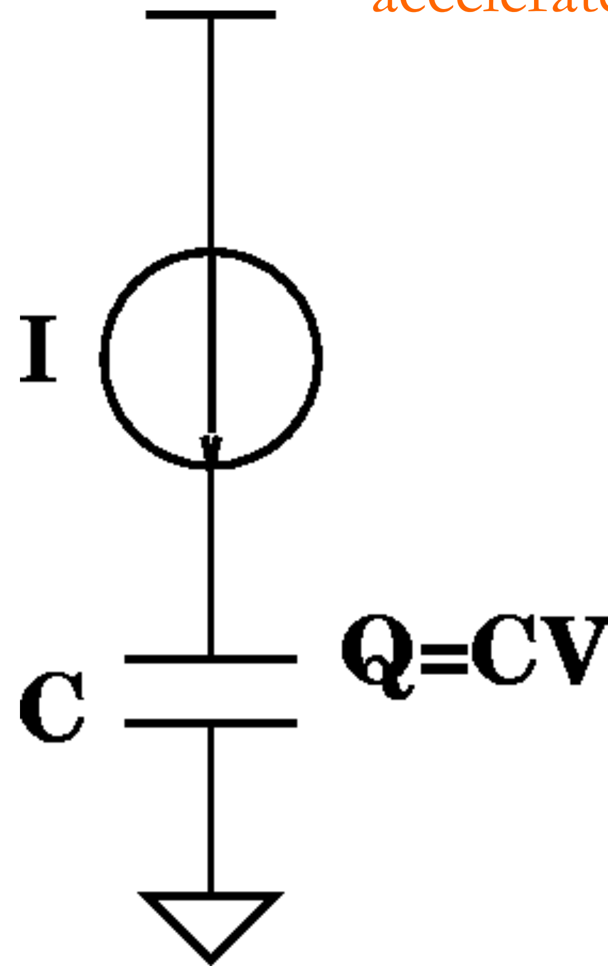
0.1 1 10 100 1000 10000

Millions of Transistors

Gate Delay

- $\tau_{gd}=Q/I=(CV)/I$
- $V' \rightarrow V/S$
- $I'_d \rightarrow I_d/S$
- $C_g' \rightarrow C_g/S$
- $\tau'_{gd} \rightarrow \tau_{gd}/S$

How might we accelerate speed up?

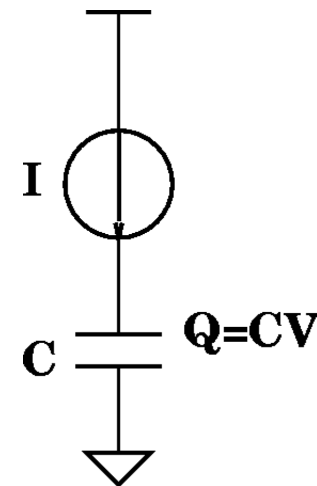


Gate Delay

- $\tau_{gd}=Q/I=(CV)/I$
- $V' \rightarrow V$
  - $I'_d=(\mu C_{OX}S/2)((W/S)/(L/S))(V_{gs}-V_{TH})^2$
- $I'_d \rightarrow I_d \times S$

How might we accelerate speed up?

Don't scale V!



Gate Delay

- τ_{gd}=Q/I=(CV)/I
- V'→ V
  - $I'_d=(\mu C_{OX}S/2)((W/S)/(L/S))(V_{gs}-V_{TH})^2$
- I'_d → I_d×S
- C_g' → C_g/S

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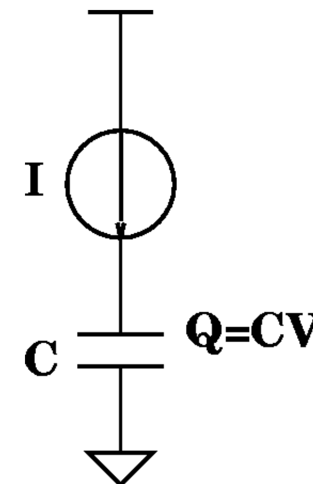

Gate Delay

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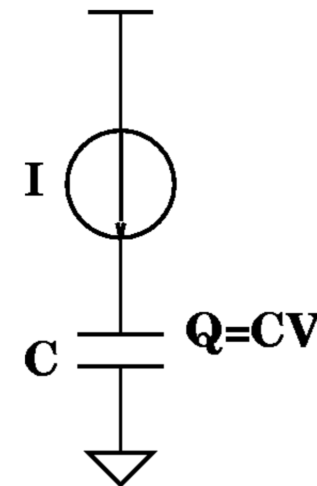
- $I'_d \rightarrow I_d \times S$
- $C_g' \rightarrow C_g/S$
- $\tau'_{gd} \rightarrow \tau_{gd}/S^2$
- $f' \rightarrow f \times S^2$

How might we accelerate speed up?

Don't scale V!



But… Power Dissipation (Dynamic)

- Capacitive (Dis)charging
  - $P=(1/2)CV^2f$
  - $V' \rightarrow V$
  - $C' \rightarrow C/S$
  - $P' \rightarrow P/S$

But… Power Dissipation (Dynamic)

- Capacitive (Dis)charging
  - $P=(1/2)CV^2f$
  - $V' \rightarrow V$
  - $C' \rightarrow C/S$
  - $P' \rightarrow P/S$
- Increase Frequency?
  - $\tau'_{gd} \rightarrow \tau_{gd}/S^2$
  - $f' \rightarrow f \times S^2$
  - $P' \rightarrow P \times S$

If don't scale V, power dissipation doesn't scale down!

…And Power Density

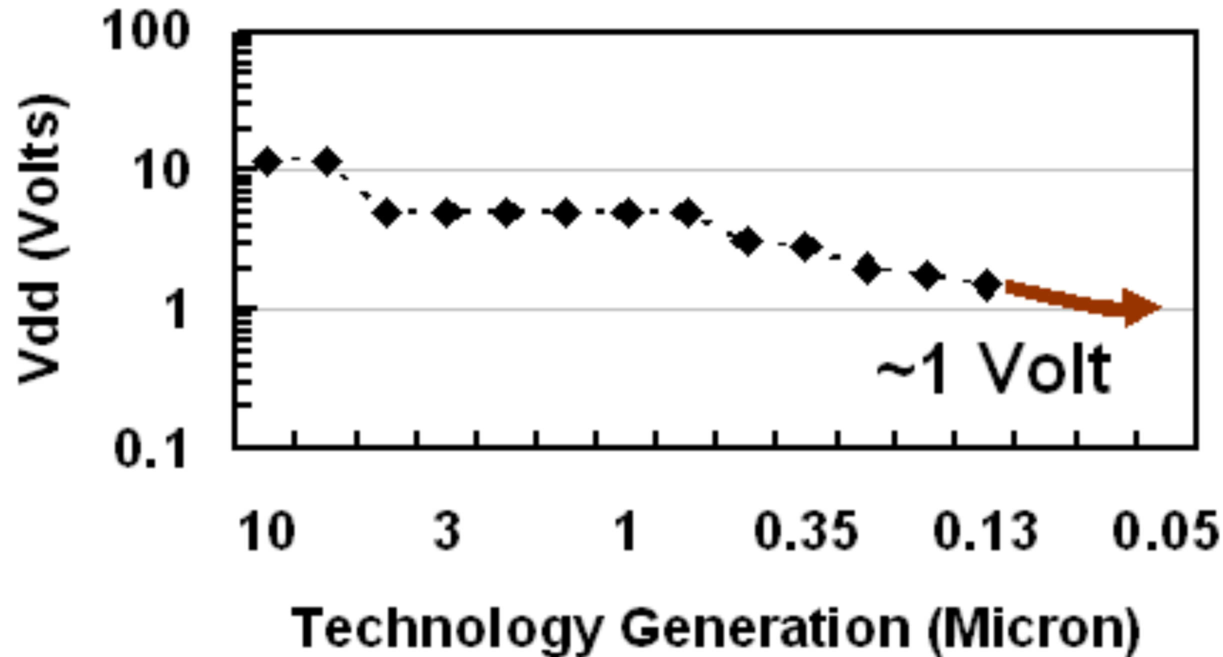
- P’ → P×S (increase frequency)
- A’ → A/S^2
- What happens to power density?

#

…And Power Density

- $P' \rightarrow P \times S$ (increase frequency)
- $A' \rightarrow A/S^2$
- What happens to power density?
- $P/A \rightarrow S^3 \times P$
- Power Density Increases!

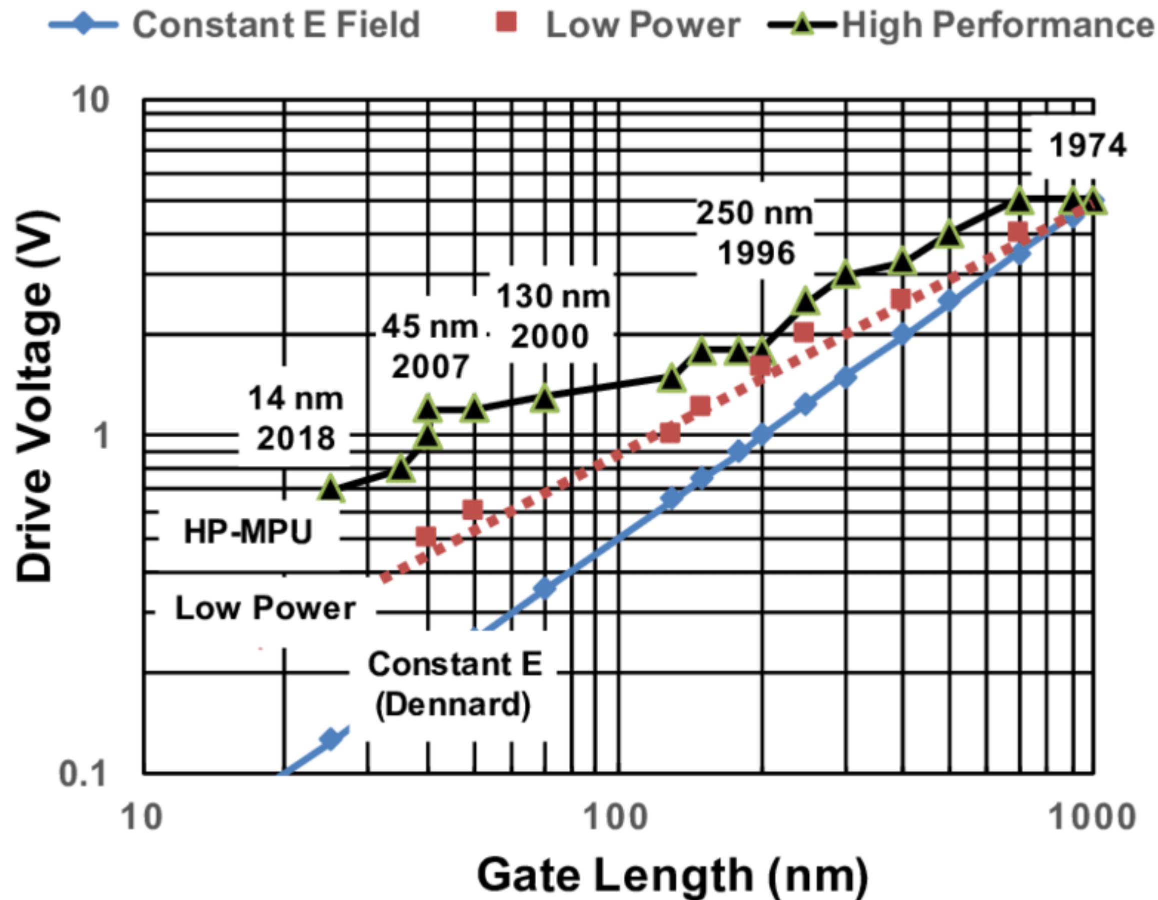
Historical Voltage Scaling



http://software.intel.com/en-us/articles/gigascale-integration-challenges-and-opportunities/

- Frequency impact?
- Power Density impact?

Historical Voltage Scaling

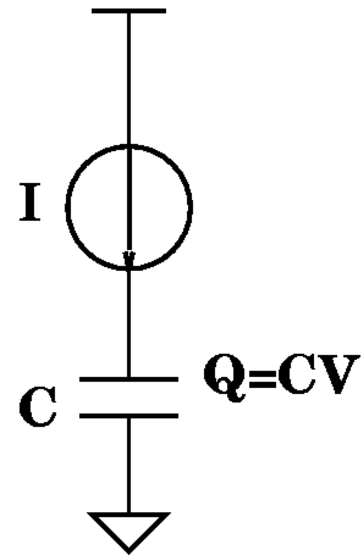


http://software ... -opportunities/

- Freq
- Pow

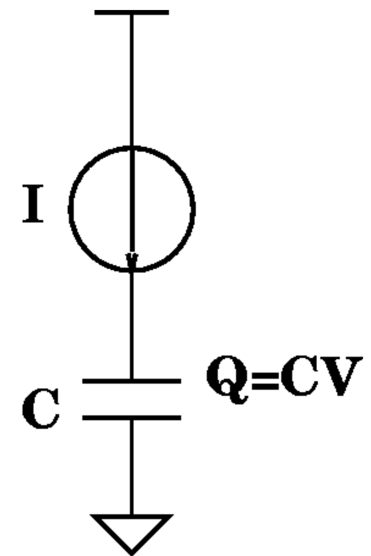
Scale V separately with Factor U, (U<S)

- $\tau_{gd}=Q/I=(CV)/I$
- $V' \rightarrow V/U$



Scale V separately with Factor U

- τ_{gd}=Q/I=(CV)/I
- V' → V/U
  - $I'_d = (\mu C_{OX} S/2)((W/S)/(L/S)(V_{gs}/U - V_{TH}/U)^2$
- $I'_d \rightarrow S/U^2 \times I_d$
- C' → C/S



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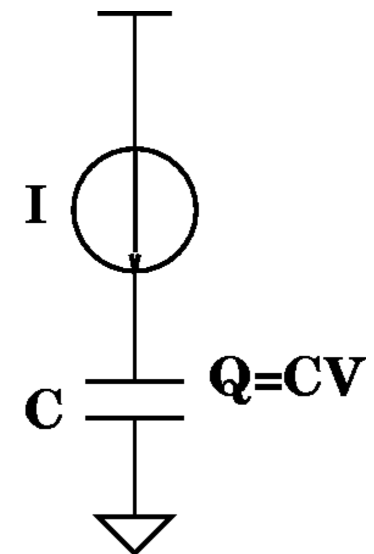
- $I'_d \rightarrow S/U^2 \times I_d$
- $C' \rightarrow C/S$
- $\tau'_{gd} \rightarrow ((1/(SU)) \ / \ (S/U^2) \ ) \times \tau_{gd}$
- $\tau'_{gd} \rightarrow (U/S^2) \times \tau_{gd}$



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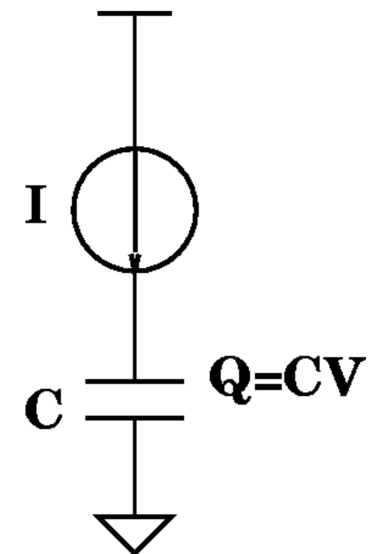
- $C' \rightarrow C/S$
- $\tau'_{gd} \rightarrow (\ (1/(SU))\ /\ (S/U^2)\ ) \times \tau_{gd}$
- $\tau'_{gd} \rightarrow (U/S^2) \times \tau_{gd}$
- $f' \rightarrow (S^2/U) \times f$



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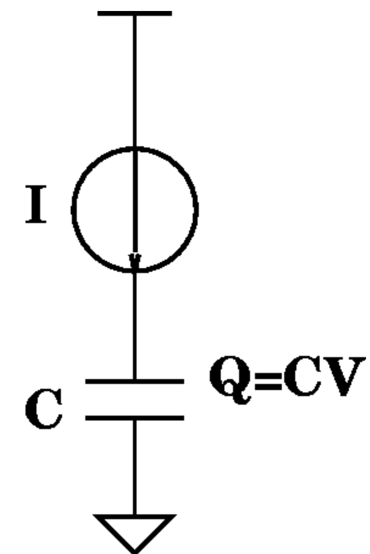
- $I'_d \rightarrow S/U^2 \times I_d$
- $C' \rightarrow C/S$
- $\tau'_{gd} \rightarrow ((1/(SU))\ /\ (S/U^2))\times\tau_{gd}$
- $\tau'_{gd} \rightarrow (U/S^2)\times\tau_{gd}$
- $f' \rightarrow (S^2/U)\times f$

Ideal scale factors:
S=100
U=100
τ=1/100
f_{ideal}=100



Preclass 2ab

- Assuming V_{dd}=10V in a 10μm process and V_{dd}=1V in a 100nm process, what are S and U? (assume everything else scales according to ideal scaling.)
  - S =
  - U =

Scale V separately with Factor U

- $\tau_{gd}=Q/I=(CV)/I$
- $V' \rightarrow V/U$
  - $I'_d=(\mu C_{OX}S/2)((W/S)/(L/S)(V_{gs}/U-V_{TH}/U)^2$
- $I'_d \rightarrow S/U^2 \times I_d$
- $C' \rightarrow C/S$
- $\tau'_{gd} \rightarrow ((1/(SU)) / (S/U^2)) \times \tau_{gd}$
- $\tau'_{gd} \rightarrow (U/S^2) \times \tau_{gd}$
- $f' \rightarrow (S^2/U) \times f$

Ideal scale factors:
S=100
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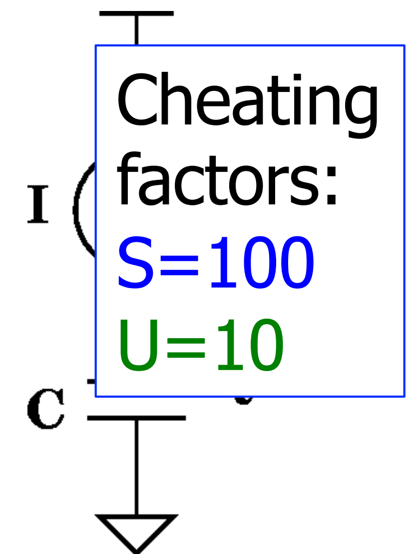

Cheating factors:
S=100
U=10

Preclass 2c:
How much faster are gates?

Scale V separately with Factor U

- $\tau_{gd}=Q/I=(CV)/I$
- $V' \rightarrow V/U$
  - $I'_d=(\mu C_{OX}S/2)((W/S)/(L/S)(V_{gs}/U-V_{TH}/U)^2$
- $I'_d \rightarrow S/U^2 \times I_d$
- $C' \rightarrow C/S$
- $\tau'_{gd} \rightarrow (\,(1/(SU))\,/\,(S/U^2)\,) \times \tau_{gd}$
- $\tau'_{gd} \rightarrow (U/S^2) \times \tau_{gd}$
- $f' \rightarrow (S^2/U) \times f$

Ideal scale factors:
S=100
U=100
τ=1/100
f_{ideal}=100

Cheating factors:
S=100
U=10
τ=1/1000
f_{new}=1000

How much faster are gates?

Scale V separately with Factor U

- $\tau_{gd}=Q/I=(CV)/I$
- $V' \rightarrow V/U$
  - $I'_d=(\mu C_{OX}S/2)((W/S)/(L/S)(V_{gs}/U-V_{TH}/U)^2$
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- $C' \rightarrow C/S$
- $\tau'_{gd} \rightarrow ((1/(SU)) \; / \; (S/U^2)) \times \tau_{gd}$
- $\tau'_{gd} \rightarrow (U/S^2) \times \tau_{gd}$
- $f' \rightarrow (S^2/U) \times f$

Ideal scale factors:
S=100
U=100
τ=1/100
f_{ideal}=100

Cheating factors:
S=100
U=10
τ=1/1000
f_{new}=1000

$f_{new}/f_{ideal}=10$

I

C

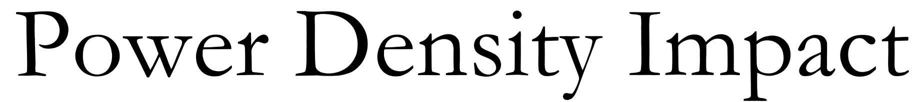
Power Density Impact (Preclass 2d)

- $P = (1/2)CV^2 f$
- $P \rightarrow (1/S)(1/U^2)(S^2/U) = S/U^3$
- $P/A \rightarrow (S/U^3) / (1/S^2) = S^3/U^3$

Power Density Impact

- $P = (1/2)CV^2 f$
- $P \rightarrow (1/S)\ (1/U^2)\ (S^2/U) = S/U^3$
- $P/A \rightarrow (S/U^3)\ /\ (1/S^2) = S^3/U^3$

- U=10 S=100
- $P/A \rightarrow 1000\ (P/A)$



Power Density Impact

- $P = (1/2)CV^2 f$
- $P \rightarrow (1/S)\ (1/U^2)\ (S^2/U) = S/U^3$
- $P/A \rightarrow (S/U^3)\ /\ (1/S^2) = S^3/U^3$

- U=10 S=100
- $P/A \rightarrow 1000\ (P/A)$

- Compare with previous:
- $P/A \rightarrow S^3 \times P$
- $P/A \rightarrow 1{,}000{,}000\ (P/A)$

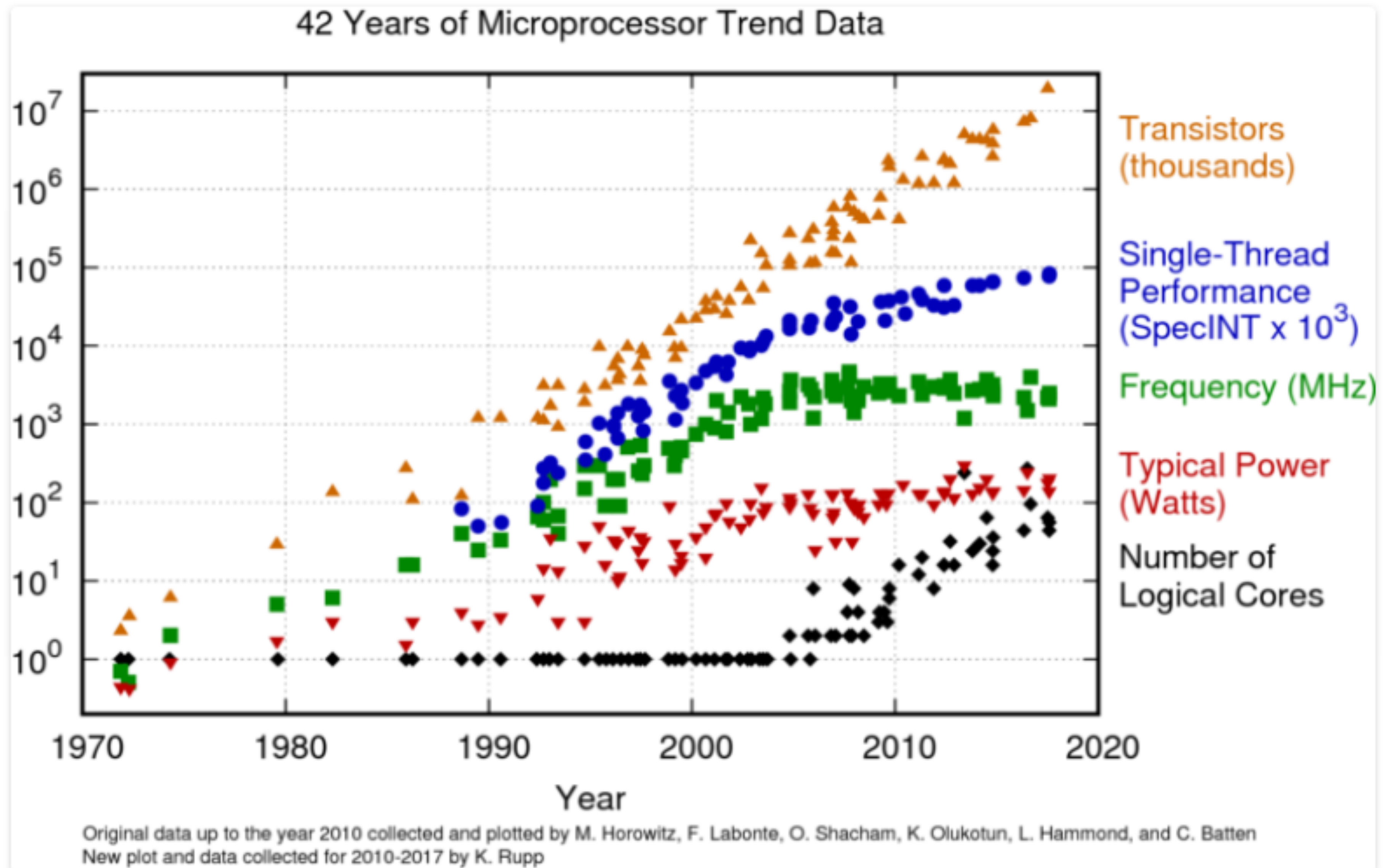
Scaling Methods

Table 3.8 Scaling scenarios for short-channel devices.

Parameter	Relation	Constant Field	General Scaling	Constant Voltage
W, L, t_{ox}		$1/S$	$1/S$	$1/S$
V_{DD}, V_T		$1/S$	$1/U$	1
N_{SUB}	$V/W_{depl}^{\ 2}$	S	S^2/U	S^2
$Area$/Device	WL	$1/S^2$	$1/S^2$	$1/S^2$
C_{ox}	$1/t_{ox}$	S	S	S
C_{gate}	$C_{ox}WL$	$1/S$	$1/S$	$1/S$
k_n, k_p	$C_{ox}W/L$	S	S	S

U<S

42 Years of uP Trend Data

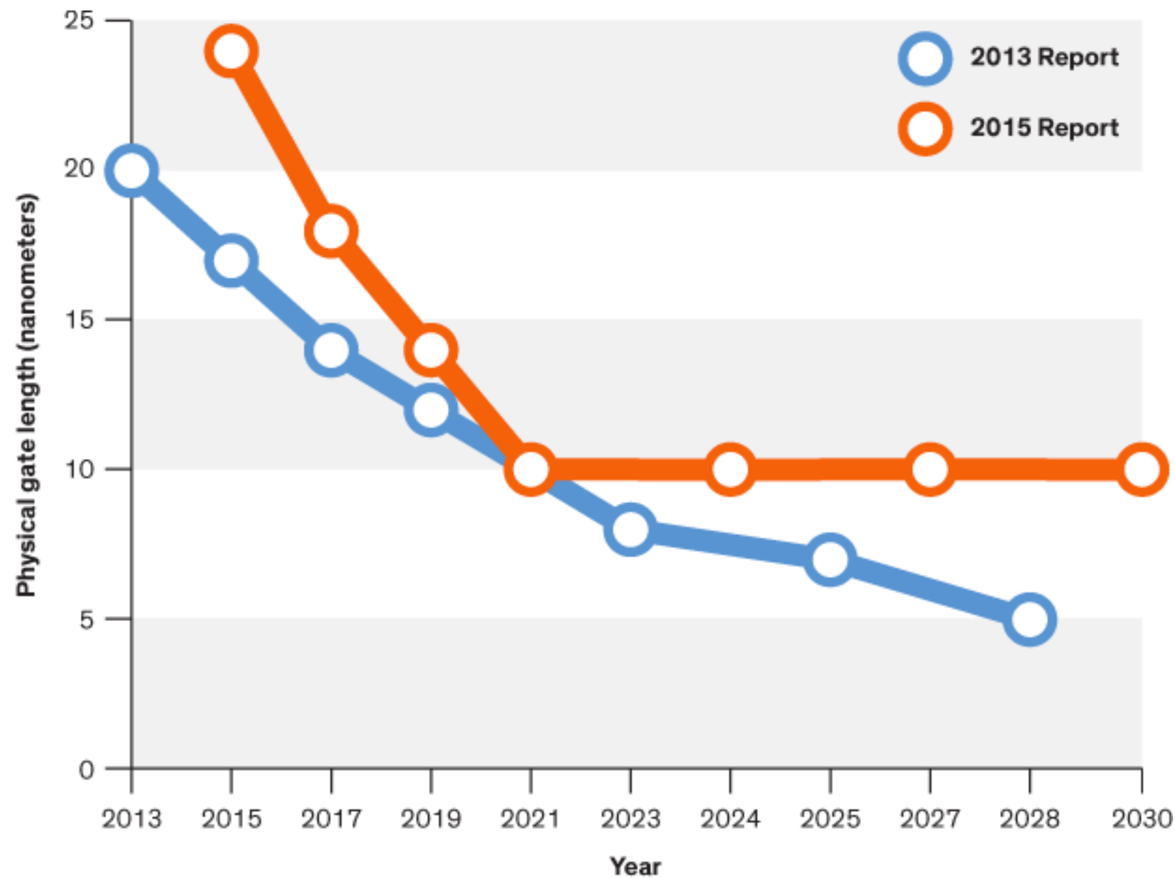


Conventional Scaling

- Ends in your lifetime
- Perhaps already:
  - "Basically, this is the end of scaling.”
    - May 2005, Bernard Meyerson, V.P. and chief technologist for IBM's systems and technology group

ITRS 2.0 Report 2015

- "After 2021, the report forecasts, it will no longer be economically desirable for companies to continue traditional transistor miniaturization in microprocessors."



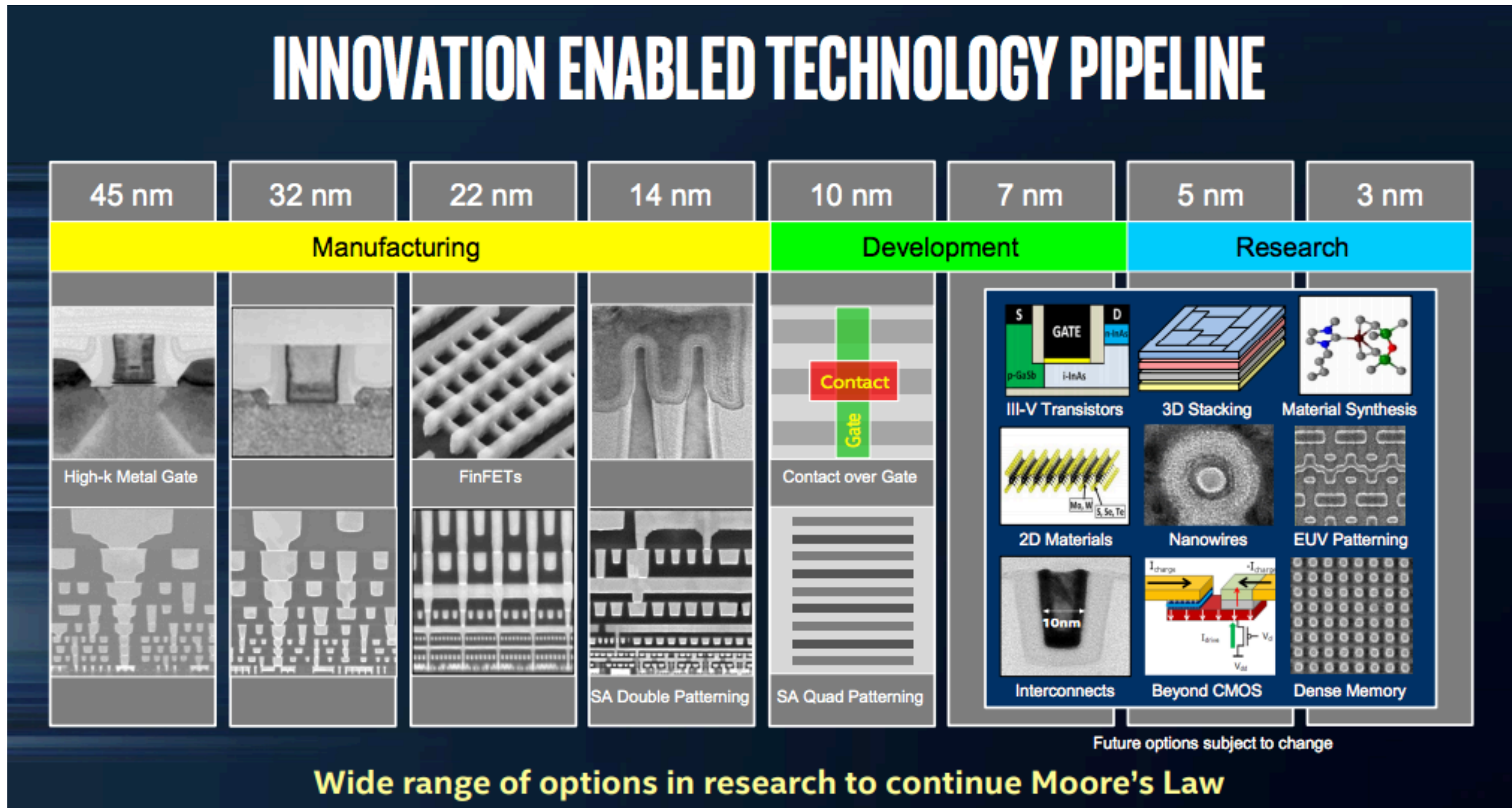
BUT…

INTEL INNOVATION LEADERSHIP

Intel	90nm Strained Silicon		65nm		45nm High-k Metal Gate		32nm Self Align Via		22nm FinFET Transistor		14nm Hyper Scaling				10nm Hyper Scaling			
Year	'03	'04	'05	'06	'07	'08	'09	'10	'11	'12	'13	'14	'15	'16	'17	'18	'19	'20
Others		90nm		65nm Strained Silicon >3 years later		40nm		28nm High-k Metal Gate >3 years later		20nm Self Align Via >3 years later		16nm FinFET Transistor >3 years later		10nm Hyper Scaling ~3 years later				Hyper Scaling ??

Source:https://newsroom.intel.com/newsroom/wp-content/uploads/sites/11/2017/09/mark-bohr-on-continuing-moores-law.pdf

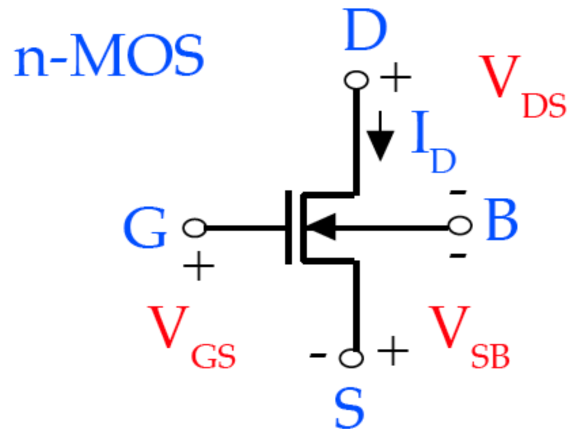
BUT…



Source:https://newsroom.intel.com/newsroom/wp-content/uploads/sites/11/2017/09/mark-bohr-on-continuing-moores-law.pdf

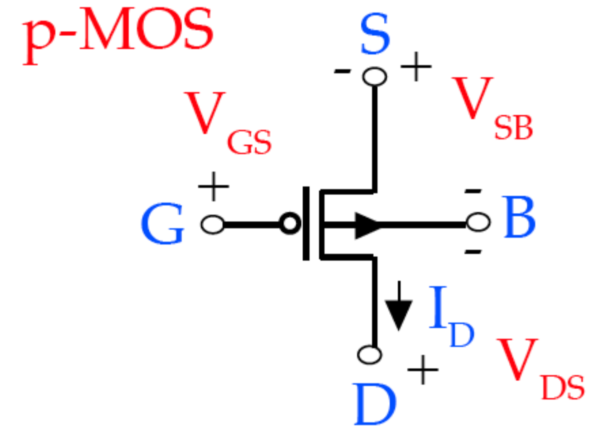
MOS Variation

Review: nMOS IV Model



$$I_D = \begin{cases} I_S\left(\frac{W}{L}\right)e^{\left(\frac{V_{GS}-V_{Tn}}{nkT/q}\right)} & V_{GS} \le V_{Tn} & \text{Subthreshold} \\ \frac{\mu_n \cdot C_{ox}}{2}\left(\frac{W}{L}\right)\left(2(V_{GS}-V_{Tn})V_{DS}-V_{DS}^2\right) & V_{GS} > V_{Tn}, V_{DS} < V_{GS}-V_{Tn} & \text{Linear} \\ \frac{\mu_n \cdot C_{ox}}{2}\left(\frac{W}{L}\right)(V_{GS}-V_{Tn})^2 & V_{GS} > V_{Tn}, V_{DS} \ge V_{GS}-V_{Tn} & \text{Saturation} \\ \approx v_{sat}C_{ox}W\left(V_{GS}-V_{Tn}-\frac{V_{dsat}}{2}\right) & E_y > E_{cn} & \text{Velocity Saturation} \end{cases}$$

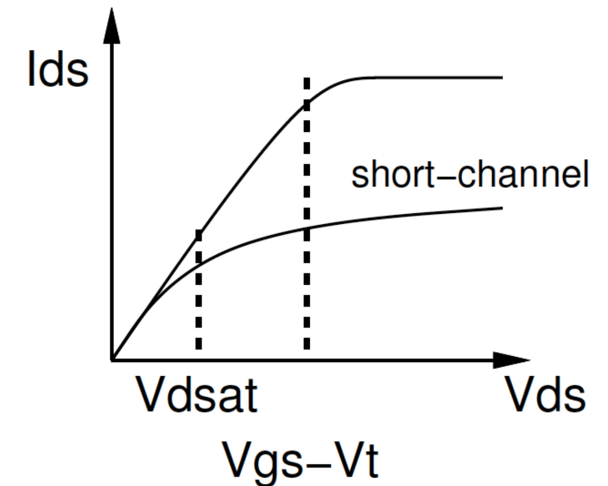
Review: pMOS IV Model

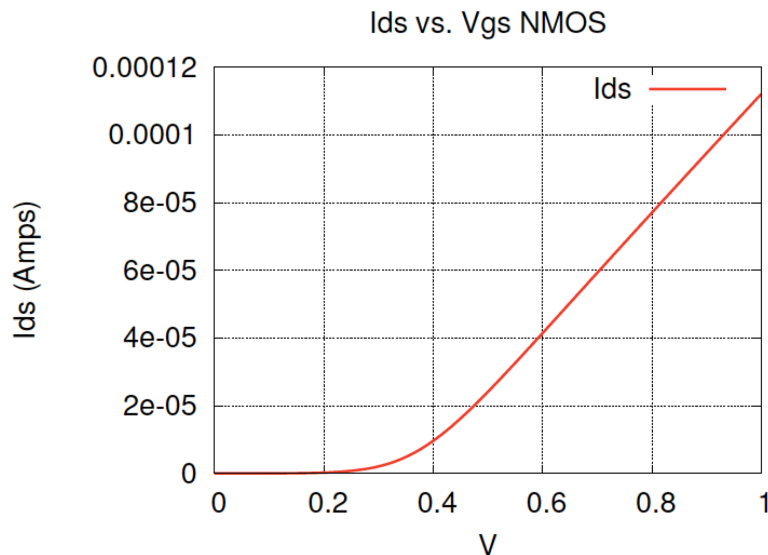


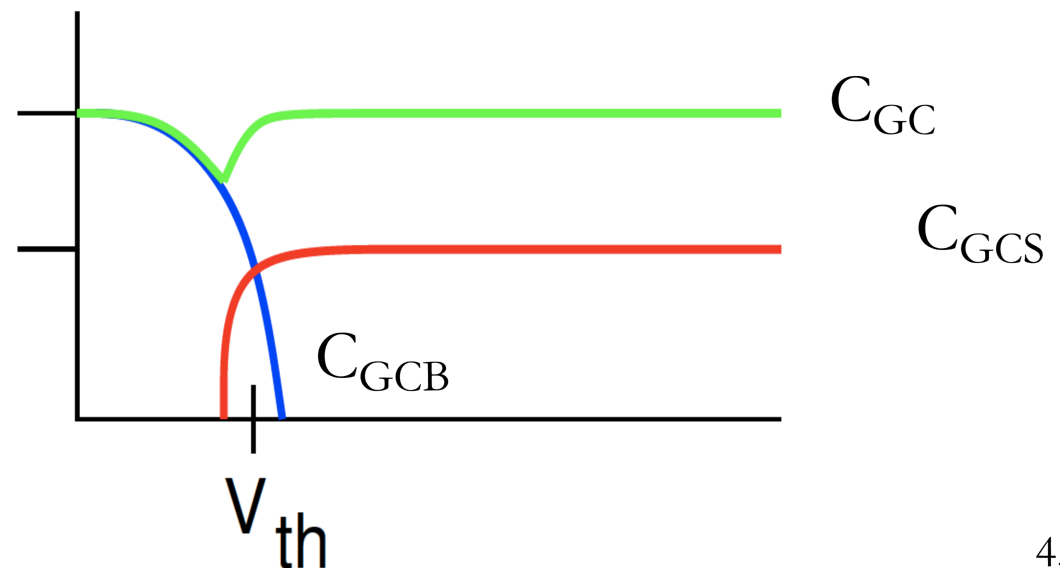
$$I_D = \begin{cases} I_S\left(\frac{W}{L}\right)e^{\left(\frac{V_{GS}-V_{Tp}}{nkT/q}\right)} & V_{GS} \geq V_{Tp} & \text{Subthreshold} \\ \frac{\mu_p \cdot C_{ox}}{2}\left(\frac{W}{L}\right)\left(2\left(V_{GS}-V_{Tp}\right)V_{DS}-V_{DS}^2\right) & V_{GS} < V_{Tp}, V_{DS} > V_{GS}-V_{Tp} & \text{Linear} \\ \frac{\mu_p \cdot C_{ox}}{2}\left(\frac{W}{L}\right)\left(V_{GS}-V_{Tp}\right)^2 & V_{GS} < V_{Tp}, V_{DS} \leq V_{GS}-V_{Tp} & \text{Saturation} \\ \approx v_{sat}C_{ox}W\left(V_{GS}-V_{Tp}-\frac{V_{dsat}}{2}\right) & E_y > E_{cp} & \text{Velocity Saturation} \end{cases}$$

Thus far…

- Understand how to model transistor behavior
- Given that we know its parameters
  - V_{dd}, V_{th}, C_{OX}, W, L, μ …







But…

- We don't know its parameters (perfectly)
  - Fabrication parameters have nominal values and error range
  - Impact on I_{ds}?

- Identically drawn devices differ because of fabrication techniques (e.g. process mismatch)
- Parameters change with environment (*e.g.* Temperature)
- Parameters change with time (aging)

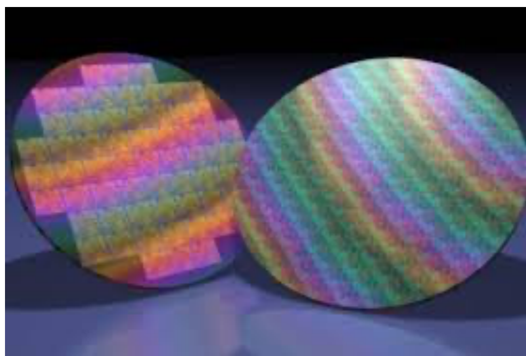
How to Design for Variation

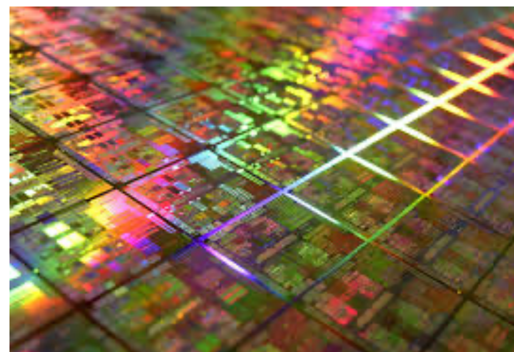
- Sources of Variation
  - Fabrication
  - Operation
  - Aging
- Designing to Account for Variation
  - Margin
  - Corner testing
  - Binning

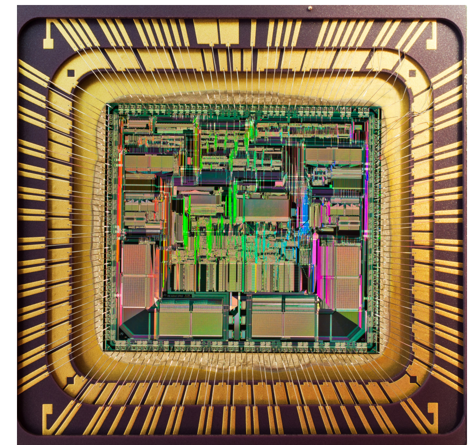
Fabrication

Variation Types

- Many reasons why variation occurs and shows up in different ways
- Scales of variation
  - Wafer-to-wafer, die-to-die, transistor-to-transistor
- Correlations of variation
  - Systematic, spatial, random (uncorrelated)

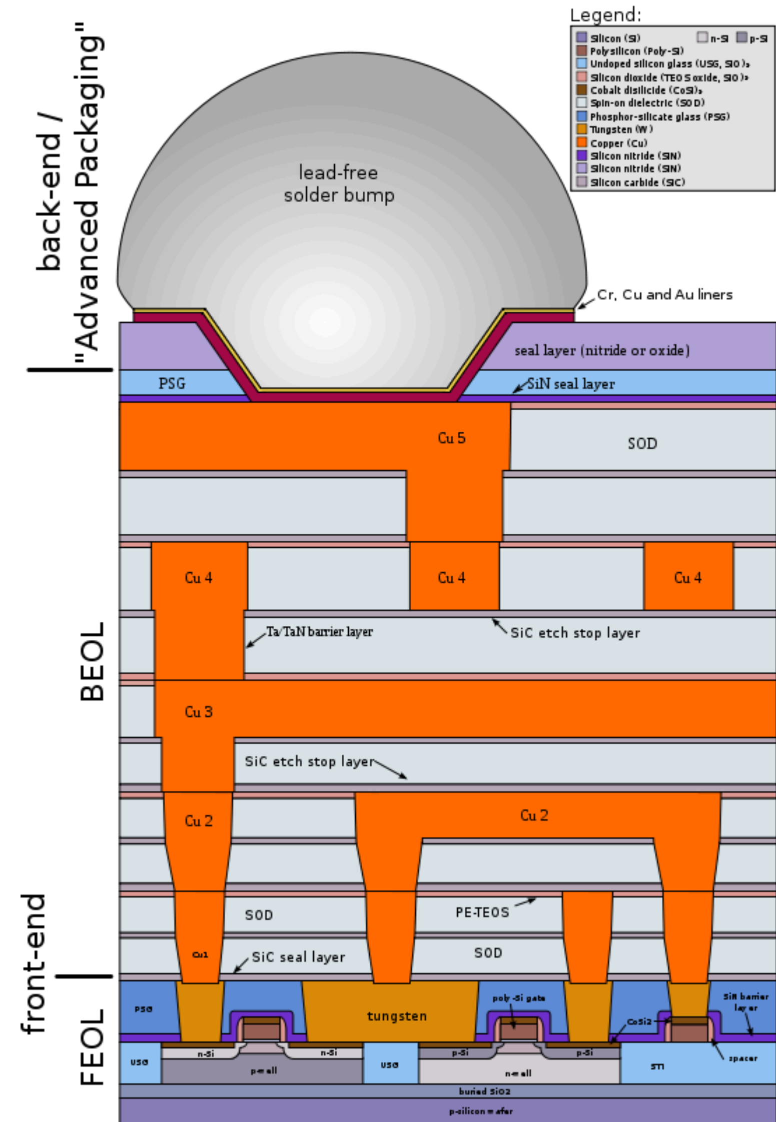






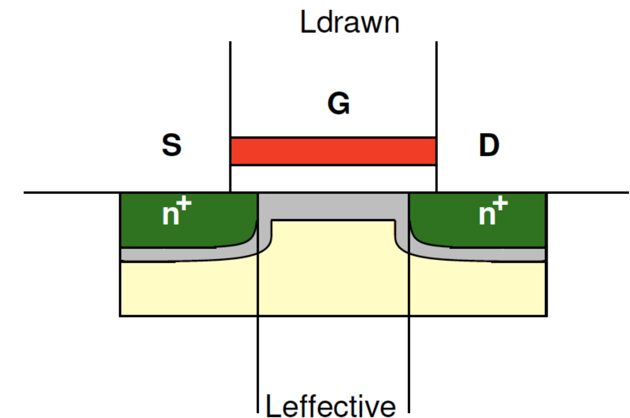
Basic Fabrication: Two Steps

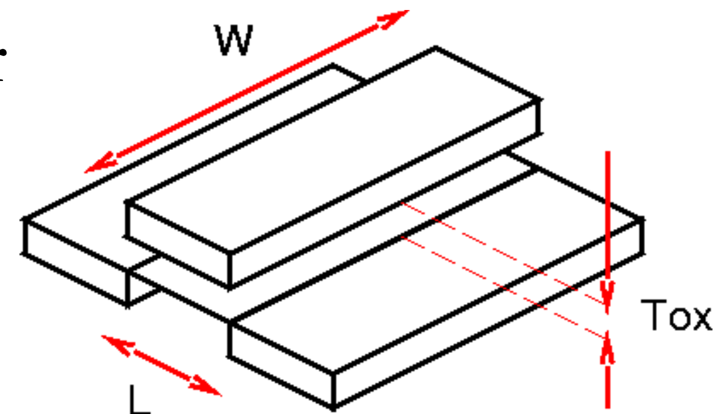
- (1) Transfer an image of the design to the wafer
- (2) Using that image (mask) as a guide, create the desired layers on silicon
  - Diffusion (add dopants to the silicon)
  - Oxide (create an insulating layer)
  - Metal (create a wire layer)



Wafer Scale: Process Shift

- Oxide thickness
- Doping level
- Layer alignment
- Growth and Etch rates and times
  - Depend on chemical concentrations
    - How precisely can we control those?
- Vary machine-to-machine, day-to-day
- Impact all transistors on wafer

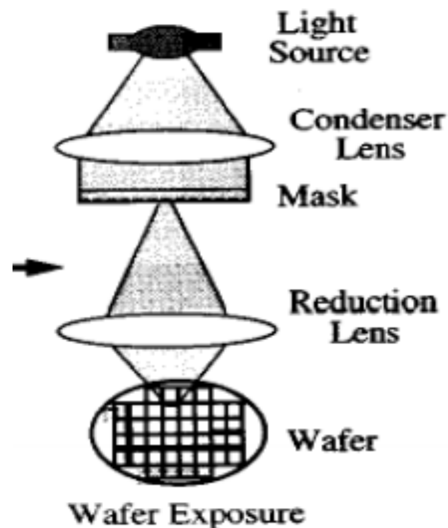


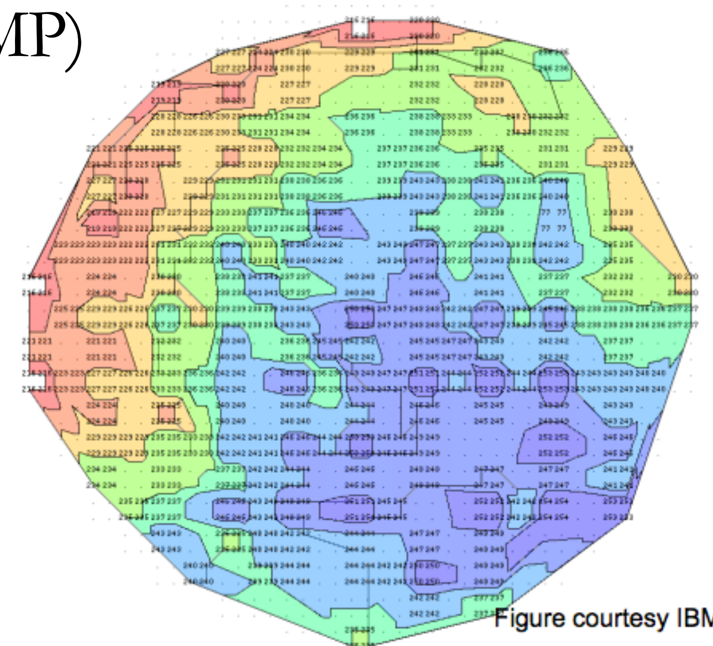


Systematic Spatial Variation

- Parameters change consistently across wafer or chip based on location

- Sources
  - Chemical-Mechanical Polishing (CMP)
    - Dishing
  - Lens distortion



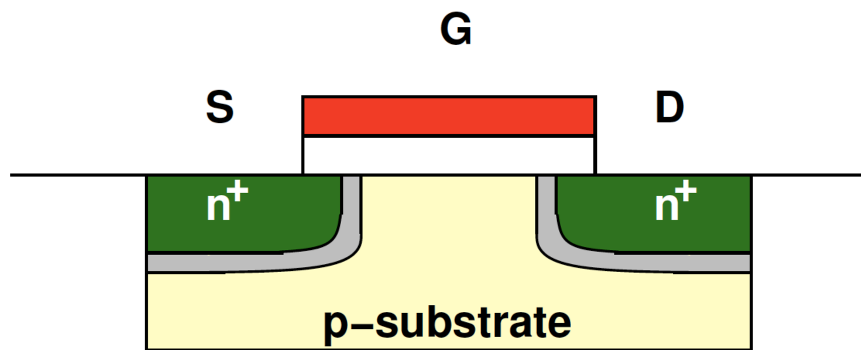


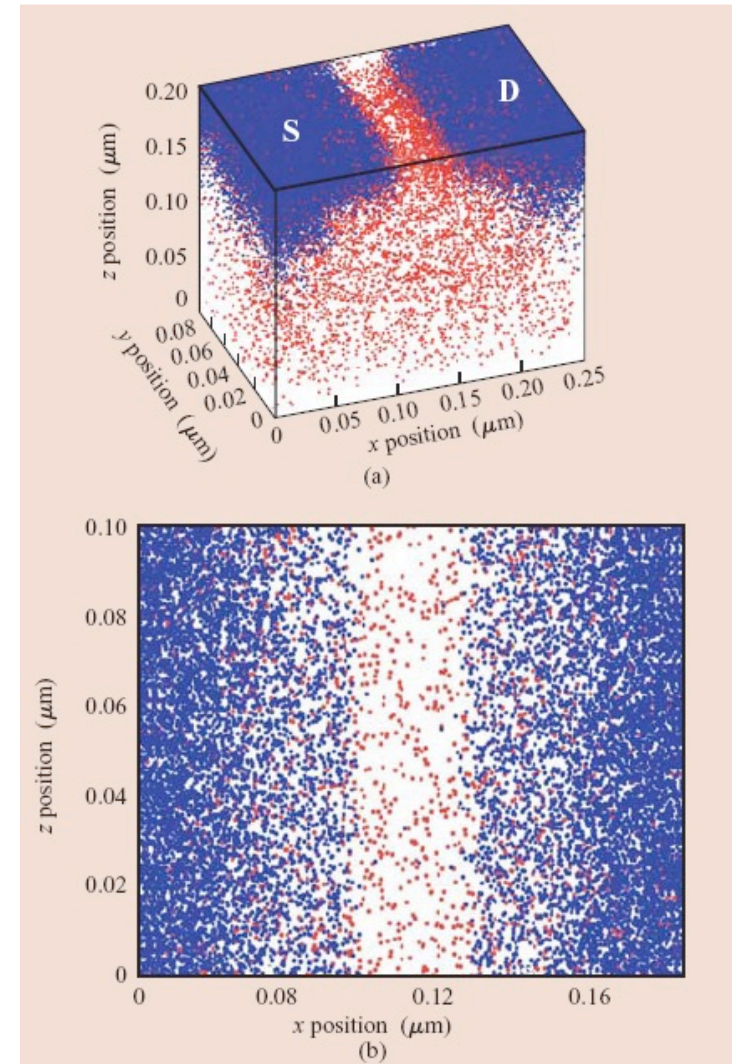
Random Transistor-to-Transistor

- Random dopant fluctuation
- Local oxide variation
- Line edge roughness
- Etch and growth rates

- Transistors differ from each other in random ways

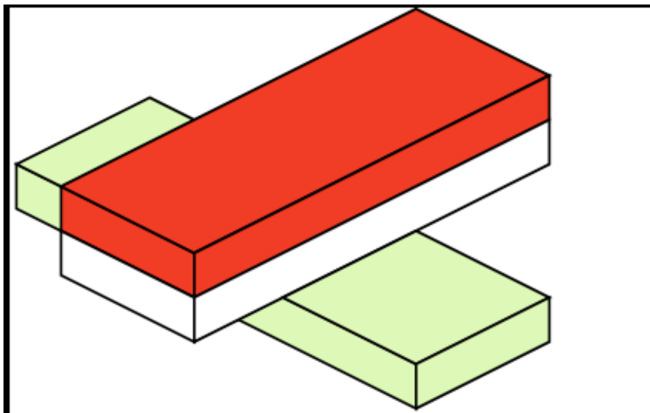
Statistical Dopant Placement

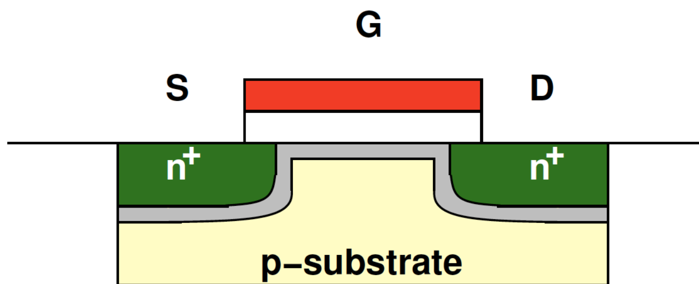




[Bernstein et al, IBM JRD 2006]

Oxide Thickness and Interface roughness





[Asenov et al. TRED 2002]

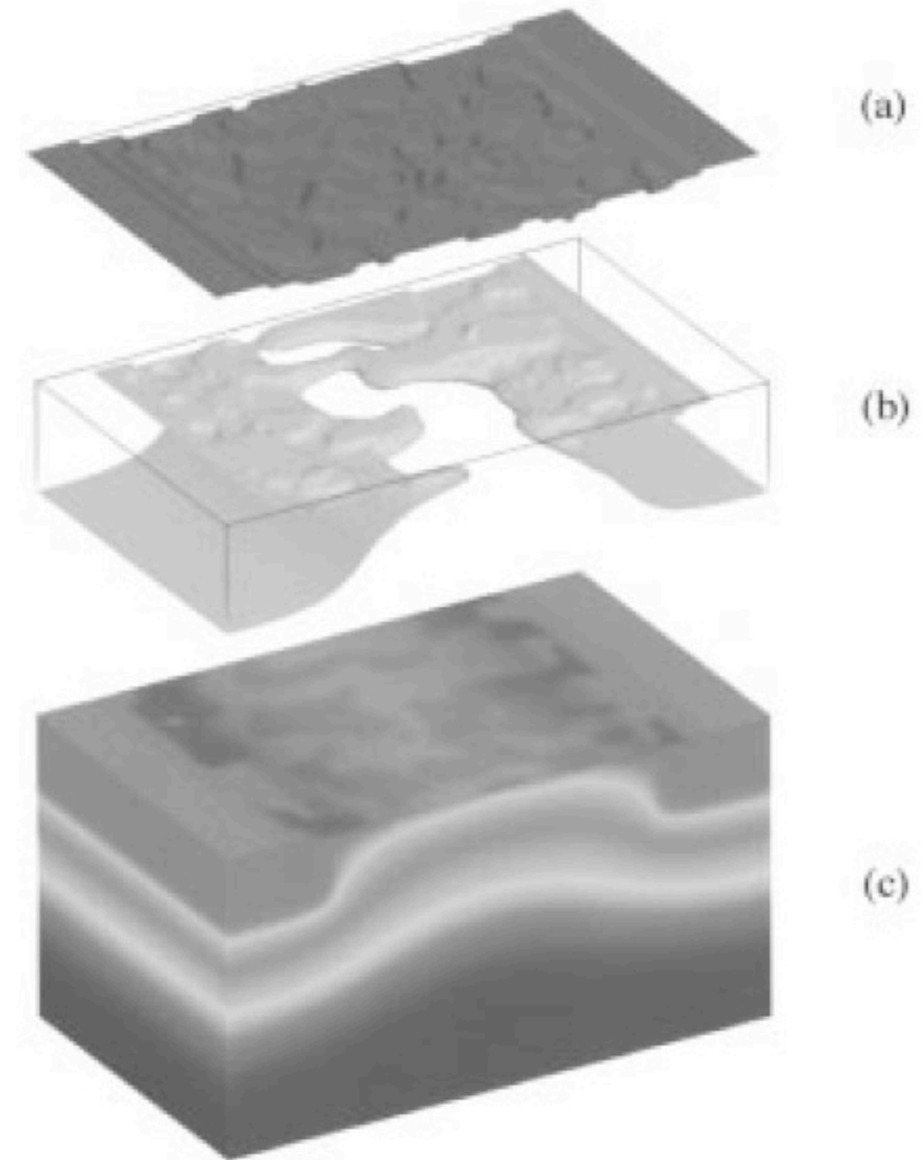
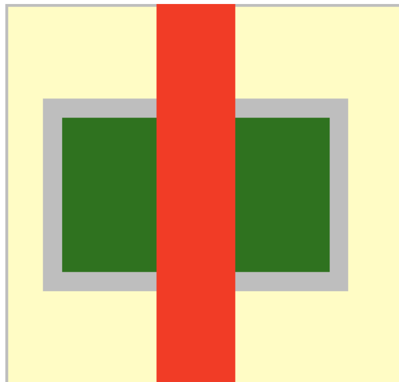
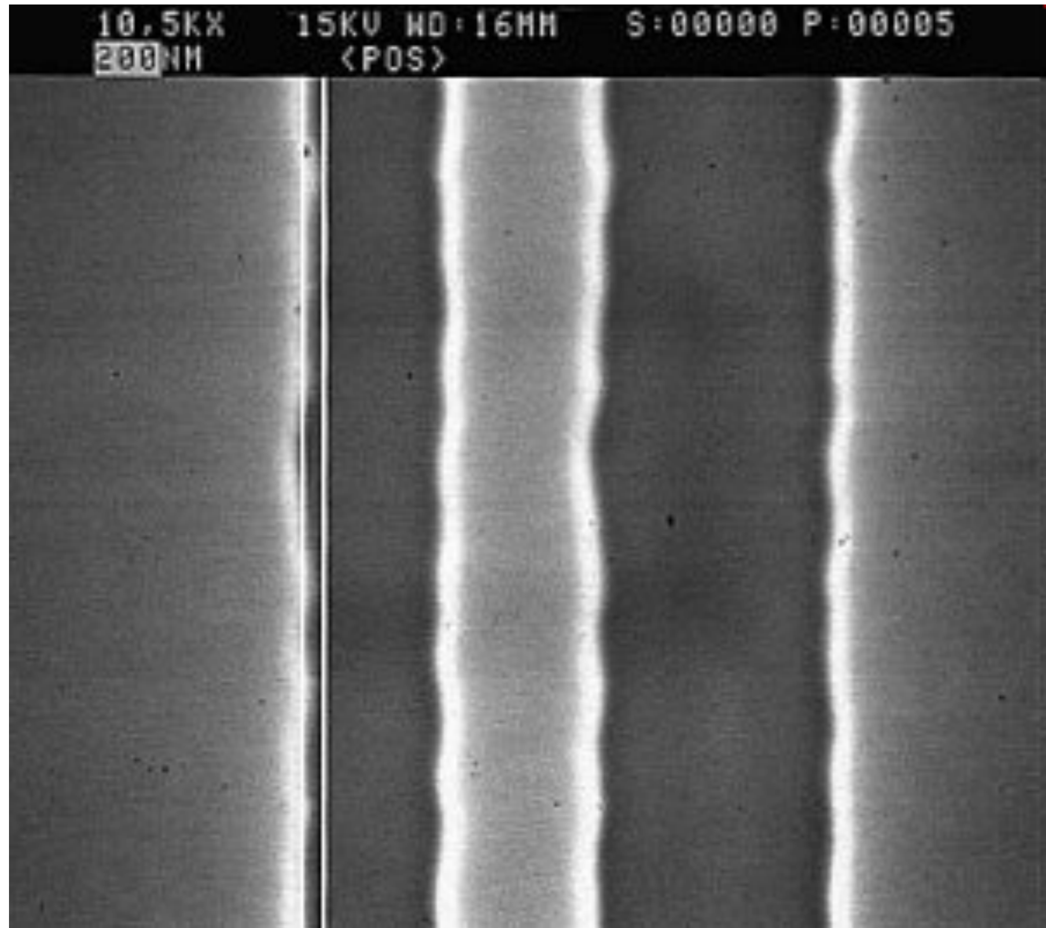


Fig. 1. (a) Typical profile of the random Si/SiO_2 interface in a $30 \times 30\ nm^2$ MOSFET, followed by (b) an equiconcentration contour obtained from DG simulations, and (c) the potential distribution.

Line Edge Roughness





From:
http://www.microtechweb.com/2d/lw_pict.htm

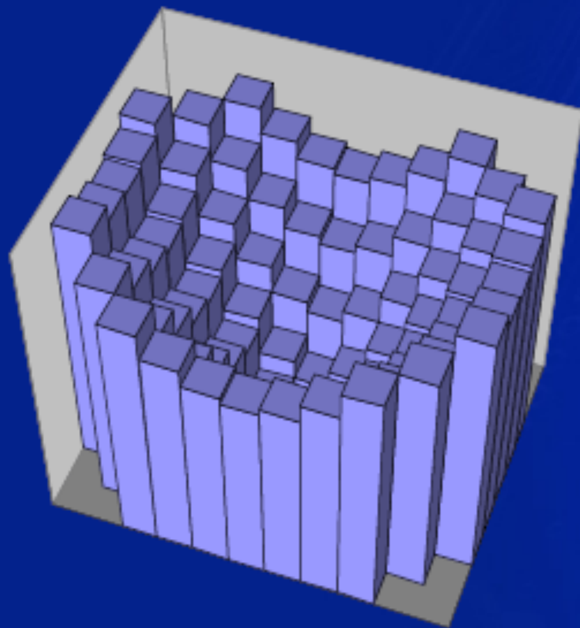
Scale of Variations

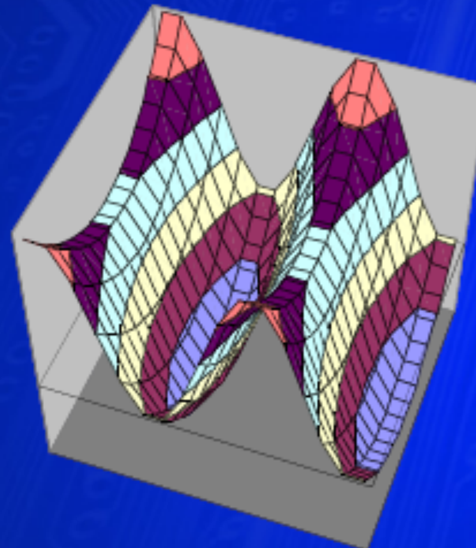
Die-to-Die (D2D) Variations

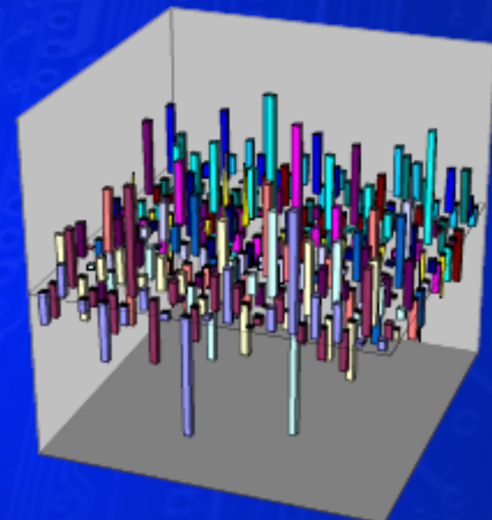
Within-Die (WID) Variations

Systematic

(Uncorrelated) Random







Wafer Scale | **Die Scale** | **Feature Scale**

Source: Noel Menezes, Intel ISPD2007

Impact on I_d (preclass 3)

- Changes parameters
  - W, L, t_{OX}, V_{th}, etc.
- Change transistor behavior
  - W increase?
  - L increase?
  - t_{OX} increase?
  - V_{th} increase?

$$I_{DS} \approx v_{sat} C_{OX} W \left(V_{GS} - V_T - \frac{V_{DSAT}}{2} \right)$$

$$I_{DS} = \mu_n C_{OX} \left(\frac{W}{L} \right) \left[\left(V_{GS} - V_T \right) V_{DS} - \frac{V_{DS}^2}{2} \right]$$

Example: V_{th}

- Many physical effects impact V_{th}
  - Doping, dimensions, roughness
- Behavior highly dependent on V_{th}

$$I_{DS} \approx v_{sat} C_{OX} W \left(V_{GS} - V_T - \frac{V_{DSAT}}{2} \right)$$

$$I_{DS} = I'_S \left(\frac{W}{L} \right) e^{\left(\frac{V_{GS} - V_T}{nkT/q} \right)}$$

V_{th} Variability @ 65nm

[Bernstein et al, IBM JRD 2006]

Impact of V_{th} Variation?

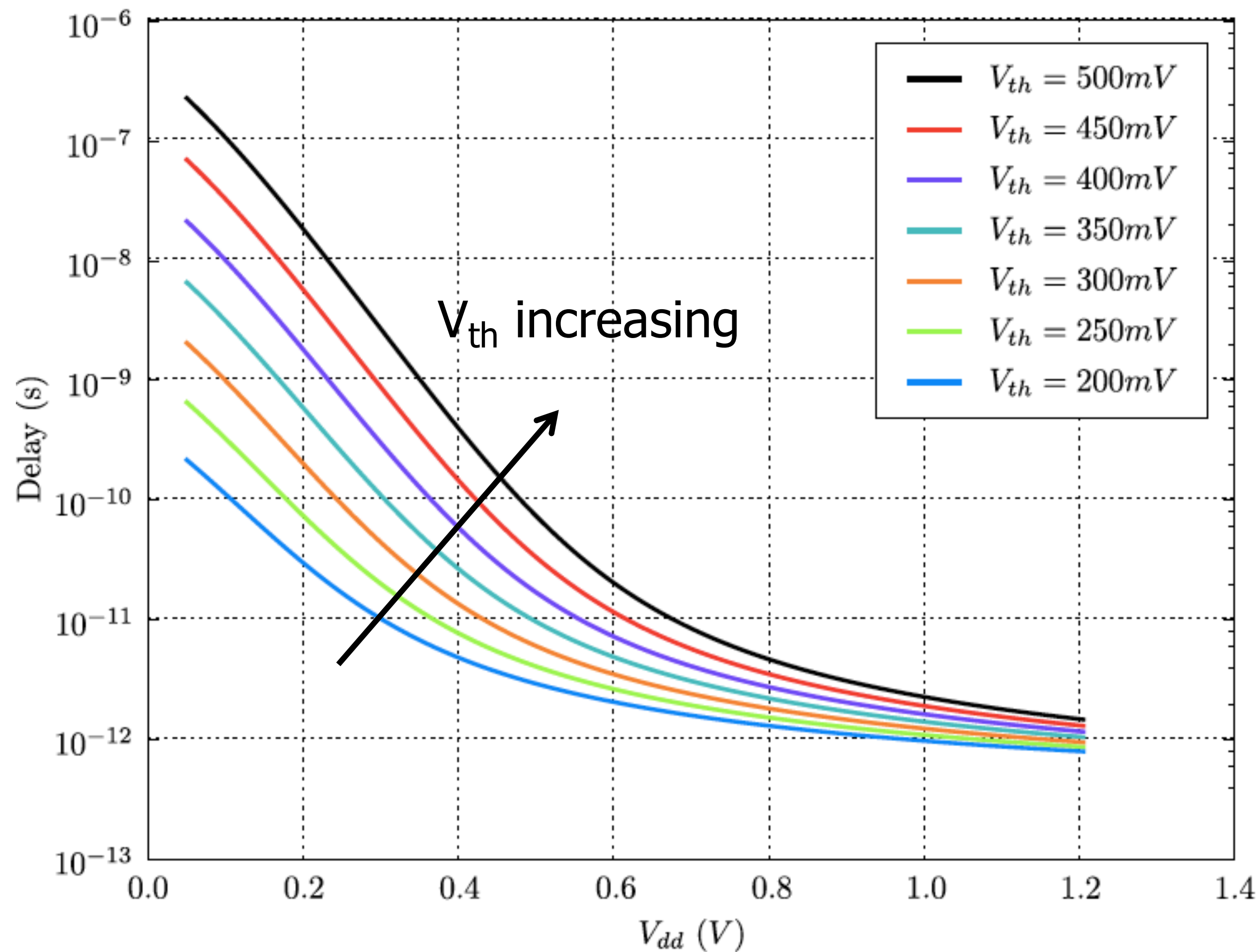
- Higher V_{th}?
  - Not drive as strongly
  - $I_{d,vsat} \propto (V_{gs}-V_{th})$
  - Performance?

Impact Performance

- Higher V_{th} → lower I_{ds} → Delay (R_{on} * C_{load})?

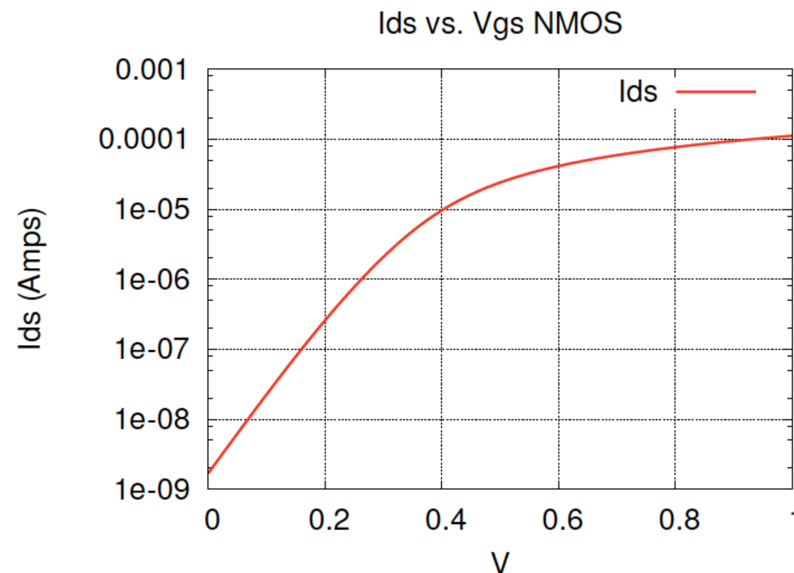
Impact Performance

- Higher V_{th} → lower I_{ds} → Delay (R_{on} * C_{load})?



Impact of V_{th} Variation?

- Lower V_{th}?
  - Not turn off as well → leaks more



$$I_{DS} = I_S'\left(\frac{W}{L}\right)e^{\left(\frac{V_{GS}-V_T}{nkT/q}\right)}$$

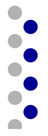
Operation

Temperature

Voltage

Temperature Changes

- Different ambient environments
  - January in Maine
  - July in Philly
  - Air conditioned machine room
- Self heat from activity of chip
- Quality of heat sink (attachment thereof)
  - E.g cooling fan



Thermal Profile for Processor

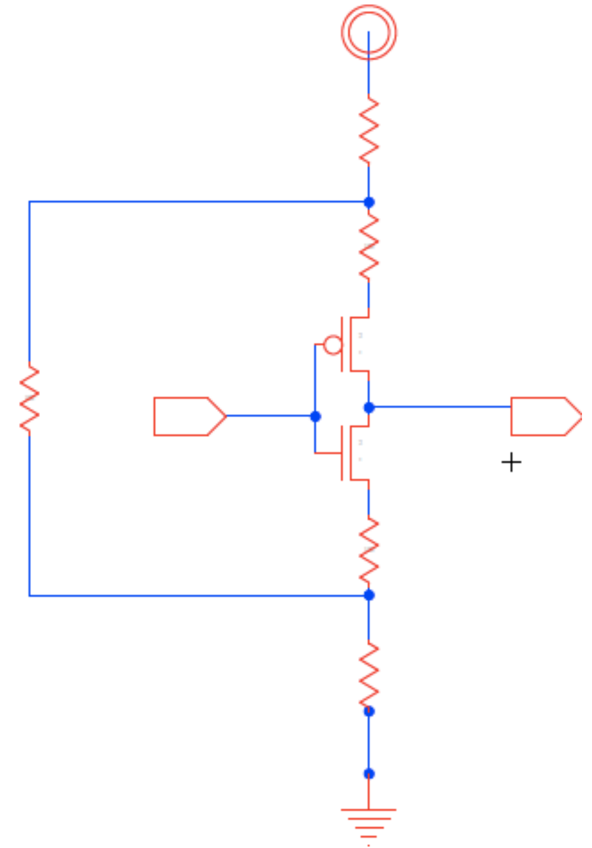
[Reda/IEEE Tr Emerging CAS v1n2 2011]

How does temperature impact on-current?

- High temperature
  - More free thermal energy
    - Easier to conduct
    - Lowers V_{th}
  - Increase rate of collision
    - Lower saturation velocity
    - Lower saturation voltage
    - Lower peak I_{ds} → slows down
- One reason don't want chips to run hot

Voltage

- Power supply isn't perfect
- Differs from design to design
  - Board to board?
  - How precise is regulator?
- IR-drop in distribution
- Bounce with current spikes



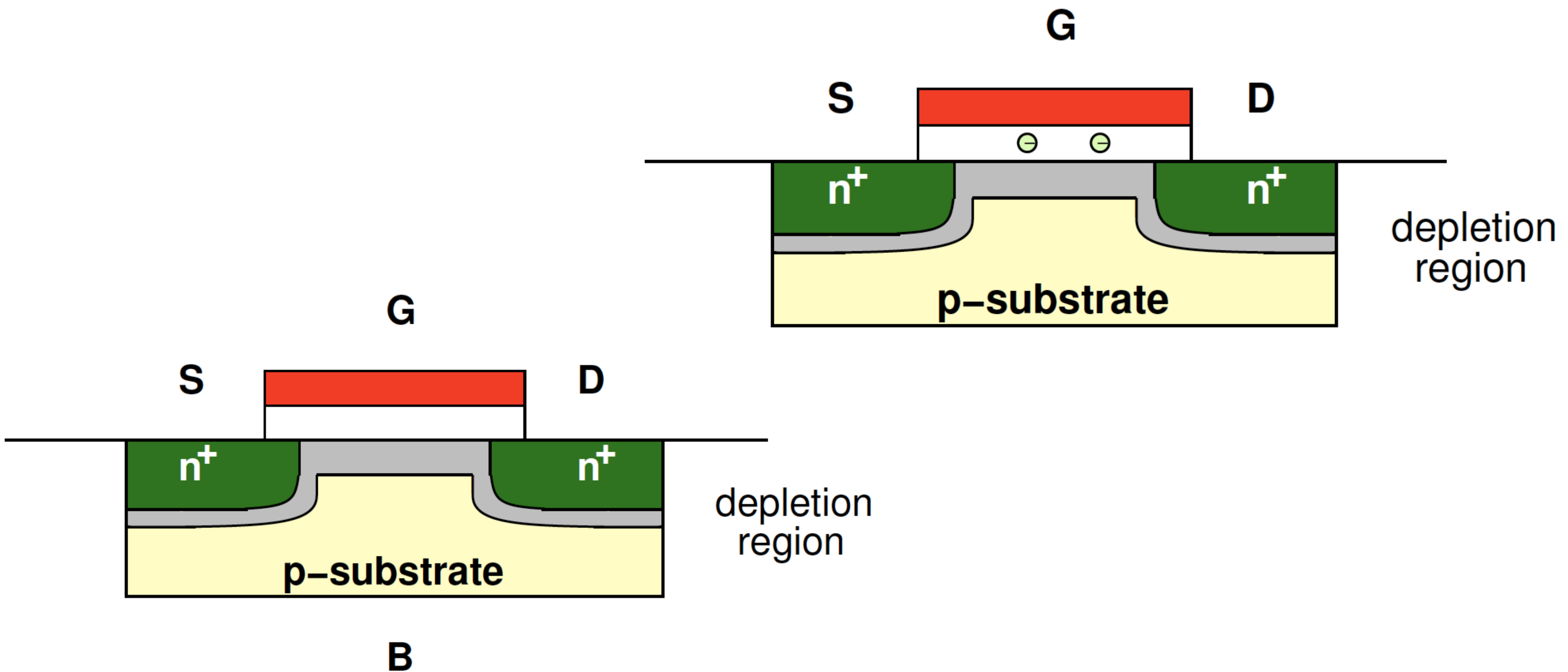
Aging

Hot Carrier Injection

Negative Bias Temperature Instability (NBTI)

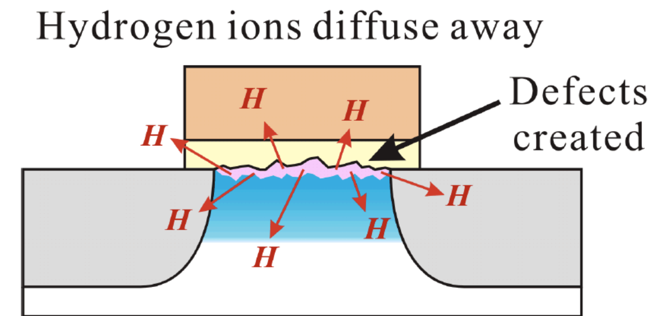
Hot Carrier Injection

- Trap electrons in oxide
  - increases V_{th}



NBTI

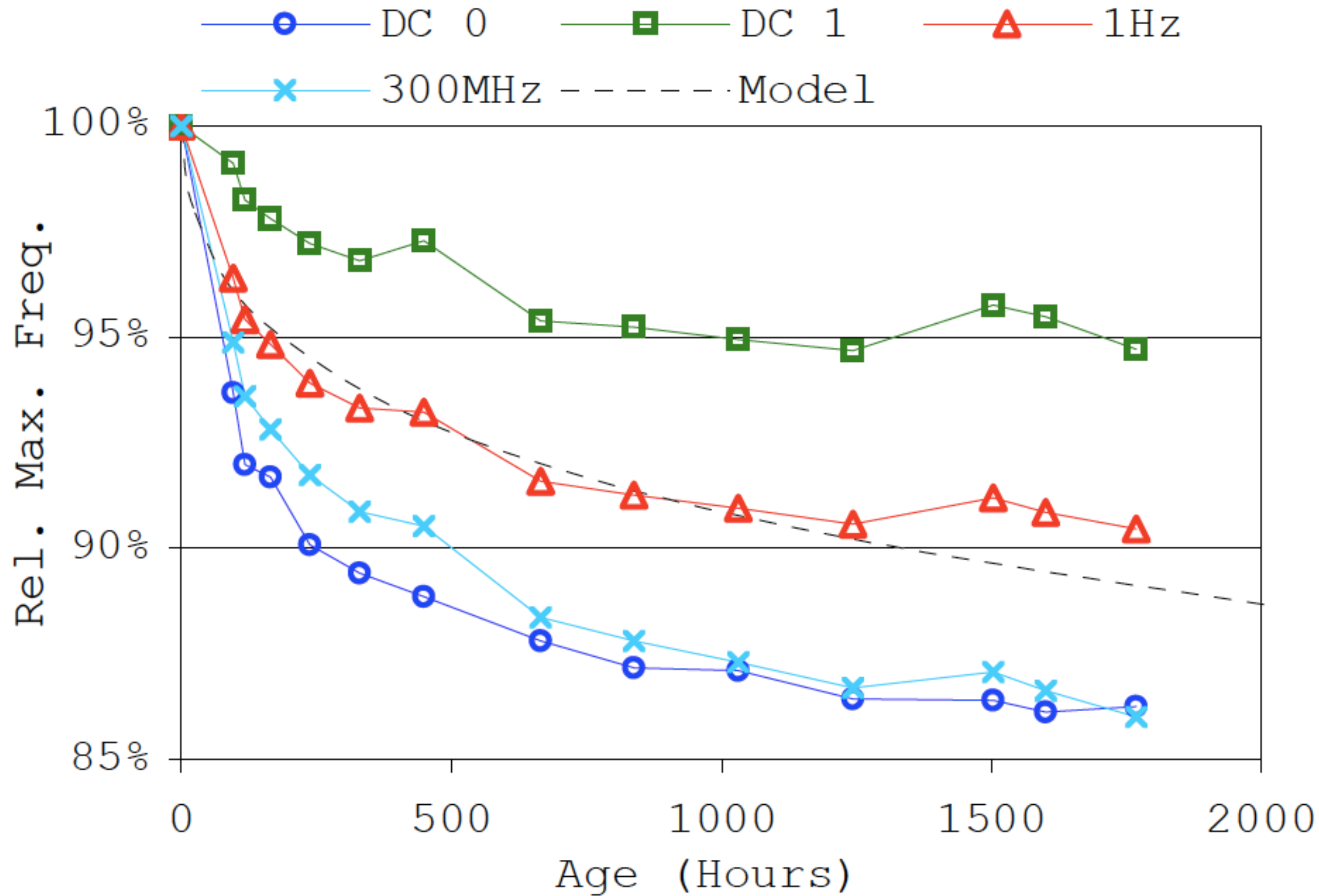
- Negative Bias Temperature Instability
  - Interface traps, Holes
- Long-term negative gate-source voltage
  - Affects PFET most
- Increase V_{th}
- Temperature dependent



[Stott, FPGA2010]

$$\Delta V_t(t) \propto \exp(-\beta V_G) \exp(-\frac{E_a}{\kappa T}) t^n$$

Measured Accelerated Aging (Cyclone III, 65nm FPGA)

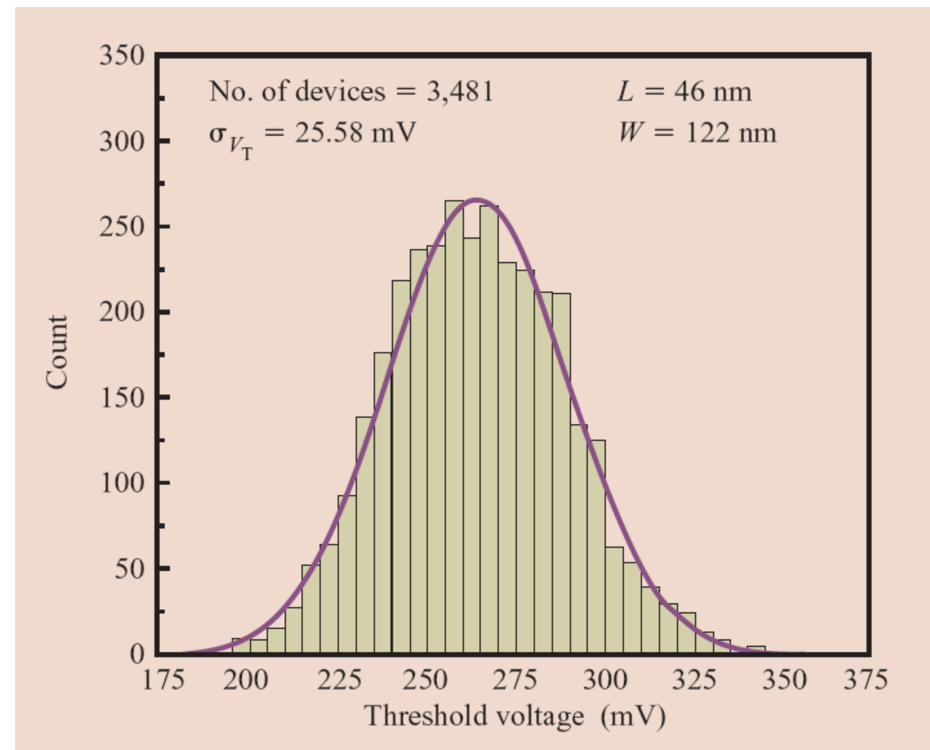


[Stott, FPGA2010]

Coping with Variation

Variation

- See a range of parameters
  - L: $L_{min} - L_{max}$
  - V_{th}: $V_{th,min} - V_{th,max}$



Impact of V_{th} Variation

- Higher V_{th}
  - Not drive as strongly
  - $I_{d,vsat} \propto (V_{gs} - V_{TH})$

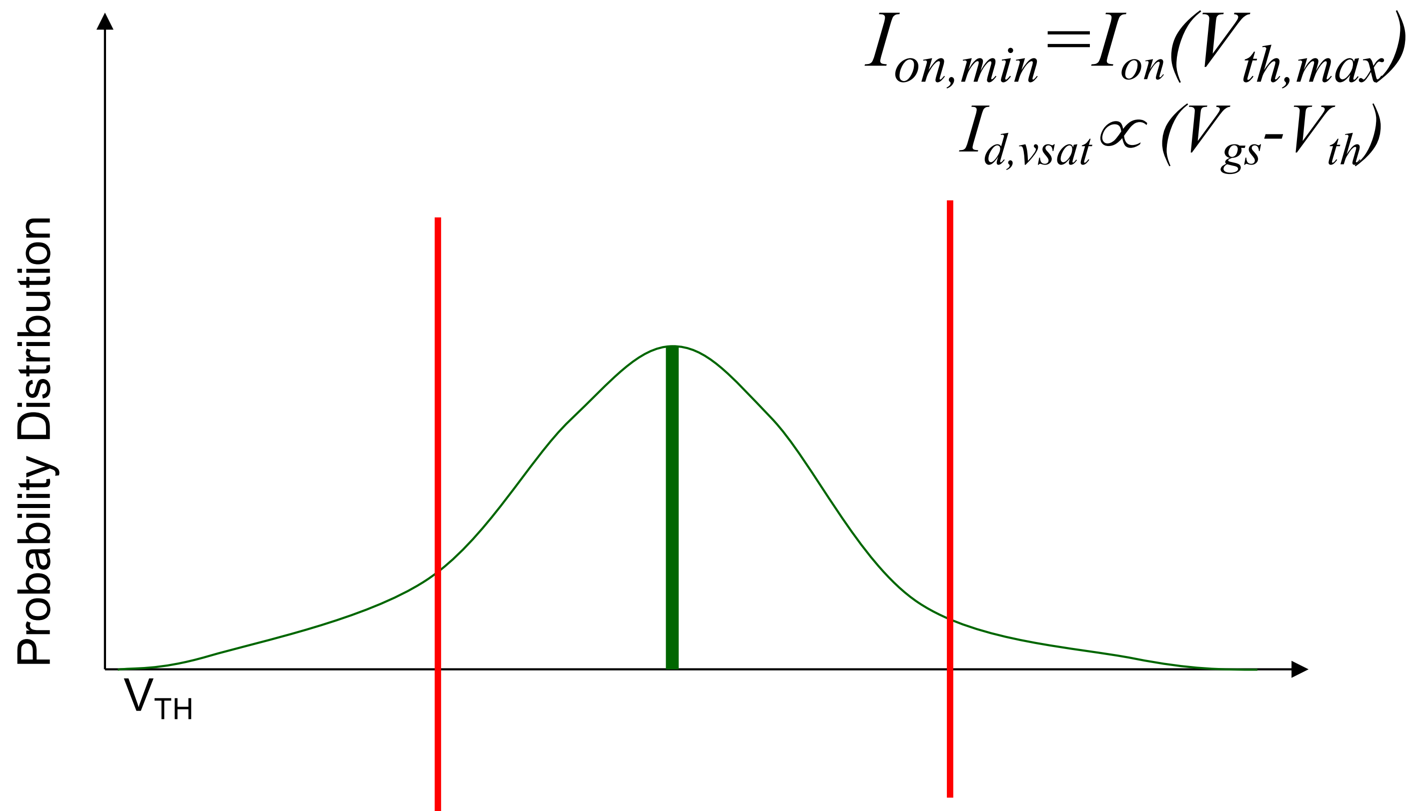
$$I_{DS} \approx v_{sat} C_{OX} W \left(V_{GS} - V_T - \frac{V_{DSAT}}{2} \right)$$

- Lower V_{th}
  - Not turn off as well → leaks more

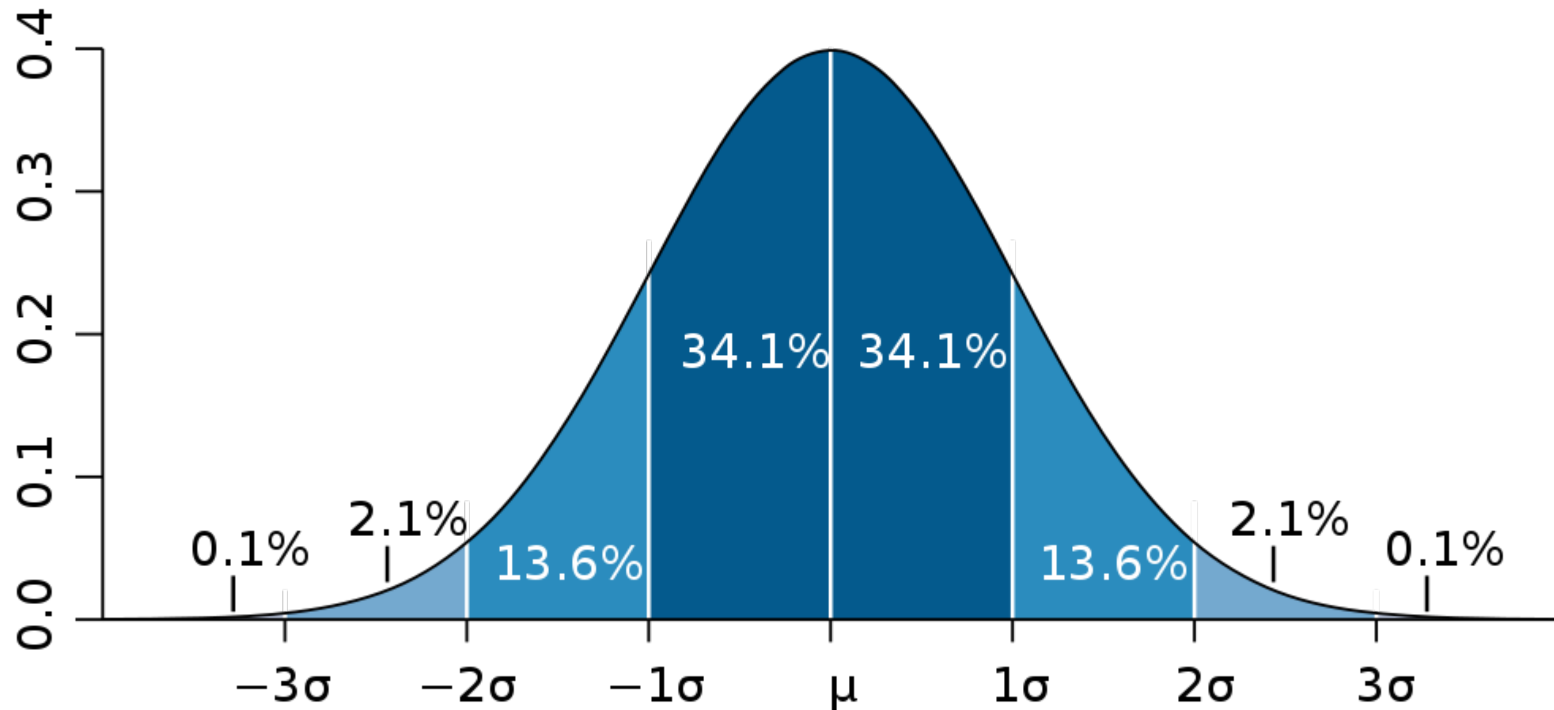
$$I_{DS} = I'_S \left(\frac{W}{L} \right) e^{\left(\frac{V_{GS} - V_T}{nkT/q} \right)}$$

Variation

- Margin for expected variation
- Must assume V_{th} can be any value in range
  - Speed → assume V_{th} slowest value



Gaussian Distribution



From: http://en.wikipedia.org/wiki/File:Standard_deviation_diagram.svg

Impact (Preclass 4)

- Given
  - $V_{th,nom} = 250mV$
  - Standard deviation: $\sigma = 25mV$
- Probability of 100 transistor circuit having all transistors with threshold in range $200mV < V_{th} < 300mV$
  - When each transistors has 96% prob of being in range?

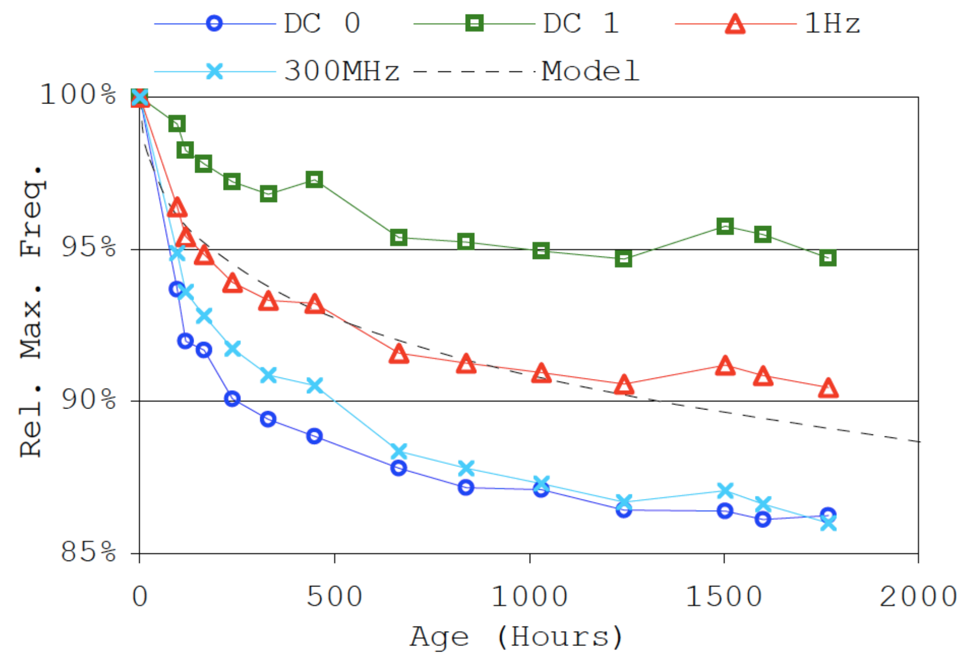
- Given
  - $V_{th,nom}$ = 250mV
  - Standard deviation: σ= 25mV
- Probability of 100 transistor circuit having all transistors with threshold in range $200mV < V_{th} < 300mV$
  - When each transistors has 96% prob of being in range?
  - When each has 99.8% probability?

Variation

- See a range of parameters
  - L: $L_{min} - L_{max}$
  - V_{th}: $V_{th,min} - V_{th,max}$
- Validate design at extremes
  - Work for both $V_{th,min}$ and $V_{th,max}$?
  - Design for worst-case scenario

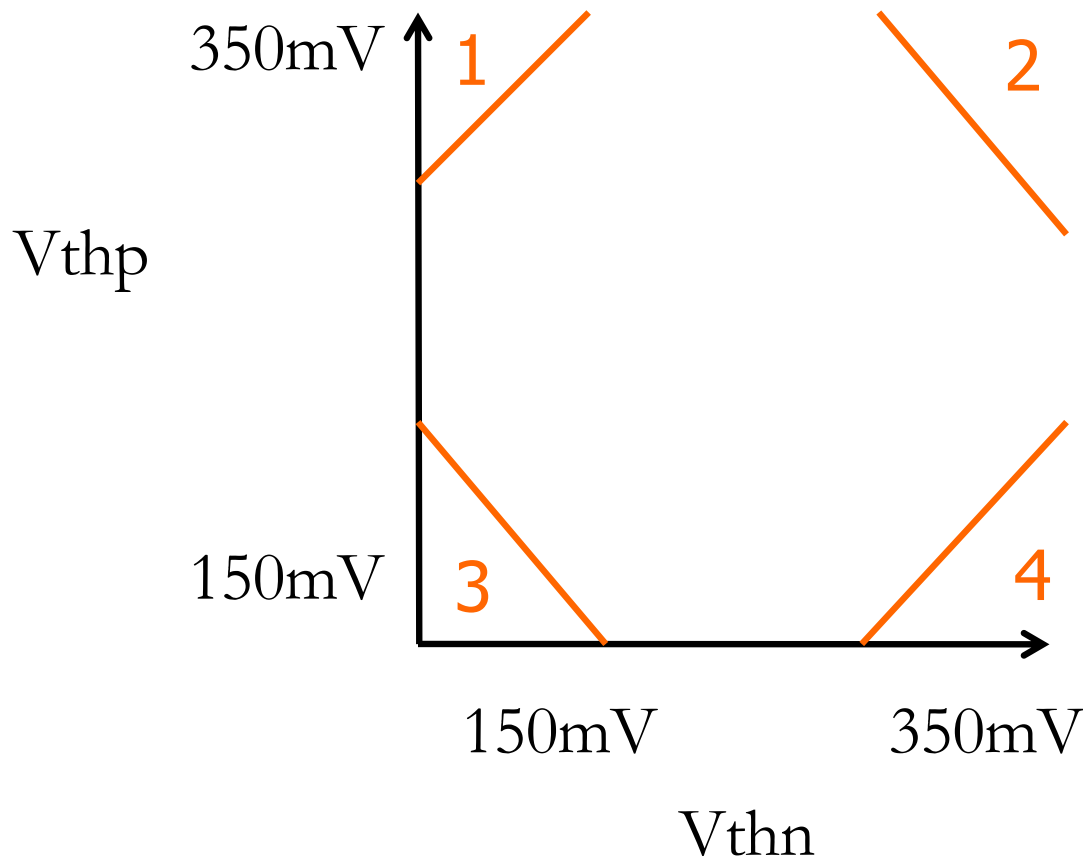
Margining

- Also margin for
  - Temperature
  - Voltage
  - Aging: end-of-life



- Many effects independent
- Many parameters
- With N parameters,
  - Look only at extreme ends (low, high)
  - How many cases?
- Try to identify the {worst,best} set of parameters
  - Slow corner of design space, fast corner
- Use corners to bracket behavior

Simple Corner Example



What happens at various corners?

Process Corners

- Many effects independent
- Many parameters
- Try to identify the {worst,best} set of parameters
  - E.g. Lump together things that make slow
    - Vtn, Vtp, temperature, Voltage
    - Try to reduce number of unique corners
  - Slow corner of design space
- Use corners to bracket behavior

Worst-case Corner Model

- corners for analog applications
  - For modeling worst-case speed
    - Slow NMOS and slow PMOS(SS) corner
  - For modeling worst-case power
    - Fast NMOS and fast PMOS(FF) corner
- corners for digital applications
  - For modeling worst-case 1
    - Fast NMOS and slow PMOS(FS) corner
  - For modeling worst-case 0
    - Slow NMOS and fast PMOS(SF) corner

Worst-case Corner Model

- Advantages
  - Worst case corner models give designers the capability to simulate the pass/fail results of a typical design and are usually pessimistic.

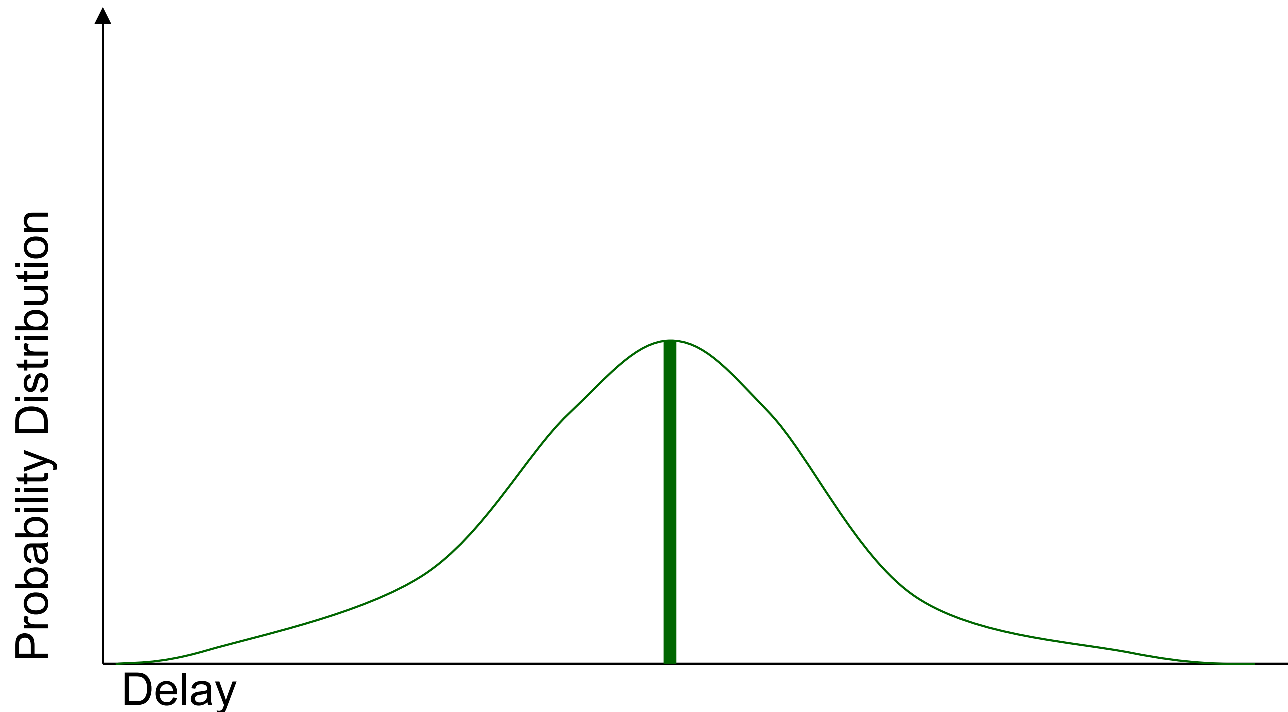
- Disadvantages
  - The fixed-corner method is too wide
  - Some valid designs can not be accepted in worst-case corner model
  - The correlations between the device parameters are ignored

Statistical Corner Model

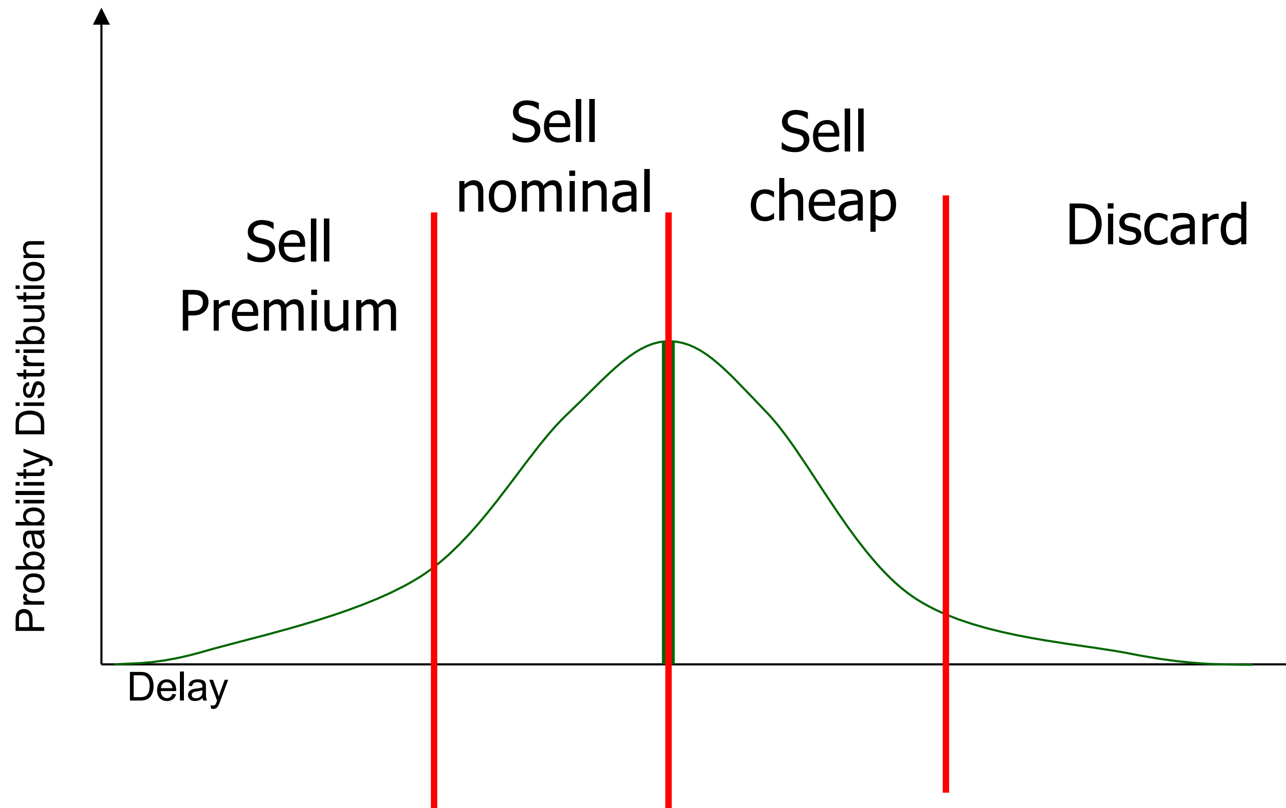
- For more realistic modeling for process variability than worst-case corner model.
  - Using data from different dies, wafers, and wafer lots collected over a long enough period of time to represents realistic process variability of the target technology
- The difference between statistical corner model and worst-case corner-model
  - Statistical corner model use the realistic PDF of the corresponding model parameter of its typical model
    - PDF is obtained from the distribution of a large set of production data
  - Statistical models can pass a valid design, which were rejected in worst-corner model

Range of Behavior

- Still get range of performances
- Any way to exploit the fact some are faster?

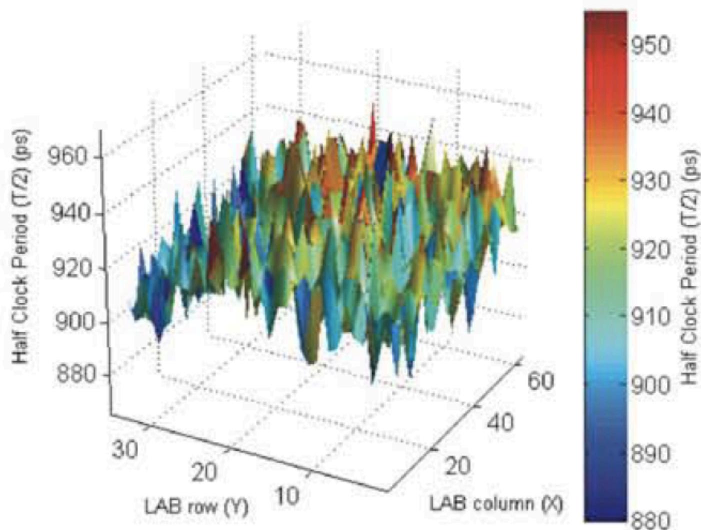


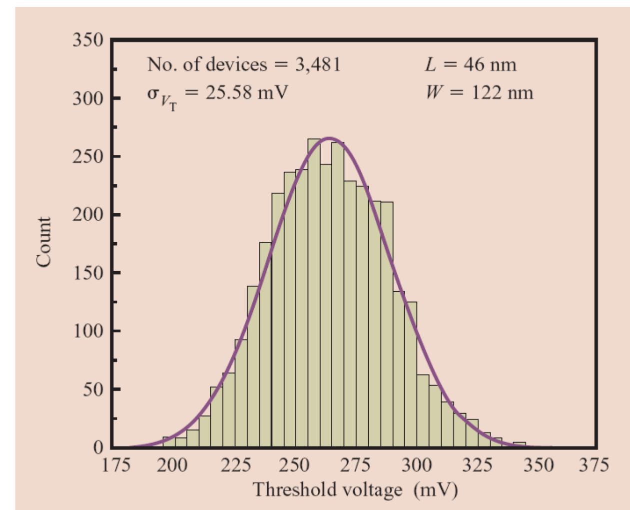
Speed Binning



Big Idea

- Parameters Approximate
- Differ
  - Chip-to-chip, transistor-to-transistor, over time
- Robust design accommodates
  - Tolerance and Margins
  - Doesn't depend on precise behavior





Admin

- Midterm 1 Wednesday 2/21
  - 1.5 hrs during class in Moore 216
  - Covers lecture 1-6
  - Old exams posted on previous years websites
    - Note old exams were for 2hrs
- HW 4 posted on 2/21

Acknowledgement

- Prof. André DeHon (University of Pennsylvania)
- Prof. Jing Li (University of Pennsylvania)