Ideal scaling:

L	1/S
W	1/S
t_{OX}	1/S
N_A	S
V	1/S

1. Under ideal scaling, how do the following characteristics scale?
(get started on what you can; we will complete together during lecture)

Area	
Capacitance, C_{ox}	
Capacitance, C_g	
Resistance	
V_{th}	1/S (given)
Current (I_{ds})	
Gate Delay (τ_{gd})	
Wire Delay	
Power [same freq]	
Power [scale freq $1/\tau_{td}$]	
Power Density (P/A) [same freq (f)]	
Power Density (P/A) [scale freq $1/\tau_{td}$]	

Note: Dynamic power in CMOS is capacitive charging: $P \propto CV^2f$
(we will address on future lectures)

2. Assuming V_{dd}=10V in a 10μm process and V_{dd}=1V in a 100nm process: (assume everything else scales according to ideal scaling.)

(a) What is the voltage scaled by (U)?

(b) What is the feature size scaled by (S)?

(c) How much faster are the gates than ideal scaling?

(d) Assuming you can exploit this gate speedup to increase frequency of operation, how does power density scale?

3. What is the variation impact on I_d:
   - W ?
   - L ?
   - t_{OX} ?
   - V_{th} ?
4. Assuming $V_{th,nom}$=250mV and $\sigma_{V_{th}}$=25mV, there is roughly a 96% probability that a given transistor has a V_{th} between 200mV and 300mV. What is the probability that **all** transistors in a 100 transistor circuit have a V_{th} between 200mV and 300mV?

5. Recompute the probability that **all** 100 transistors are in range when each transistor has a 99.8% probability of being in range.

6. If we need high and low brackets for N parameters, how many cases must we consider?

Resistive:

$$I_D = \mu_n C_{OX} \left(\frac{W}{L}\right) \left(\left(V_{GS} - V_{th}\right) V_{DS} - \frac{\left(V_{DS}\right)^2}{2} \right) \tag{1}$$

Saturated (Pinch Off):

$$I_D = \frac{1}{2} \mu_n C_{OX} \left(\frac{W}{L}\right) \left(V_{GS} - V_{th}\right)^2 \tag{2}$$

Velocity Saturated:

$$I_D = \nu_{sat} C_{OX} W \left(V_{GS} - V_{th} - \frac{V_{DSAT}}{2} \right) \tag{3}$$

Subthreshold:

$$I_D = I_S \left(\frac{W}{L}\right) e^{\frac{V_{GS} - V_{th}}{nkT/q}} \tag{4}$$