University of Pennsylvania
Department of Electrical and System Engineering
Circuit-Level Modeling, Design, and Optimization for Digital Systems

ESE3700, Spring 2024 Midterm 1 Wednesday, February 21

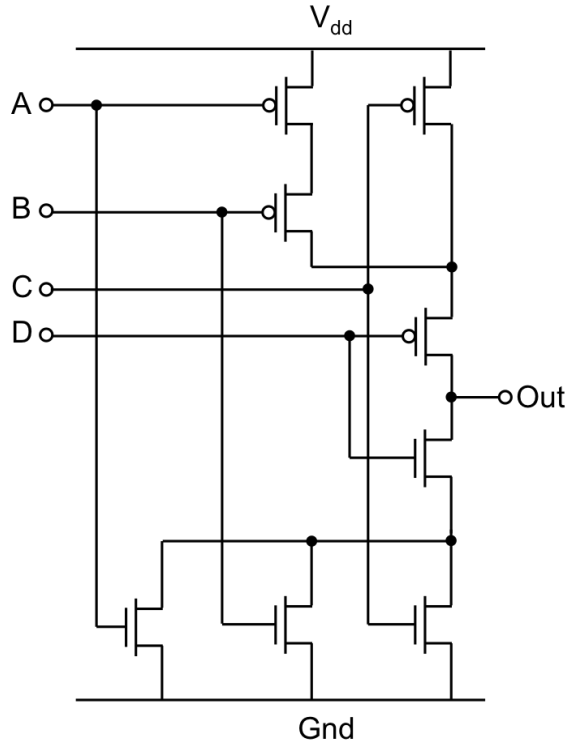
- 5 problems with weights indicated.
- Parts within a problem will not be weighted equally.
- Calculators allowed. (non-cellphone)
- Closed book = No text or notes allowed.

Name:

Grade:

Q1	
Q2	
Q3	
Q4	
Q5	
Total	

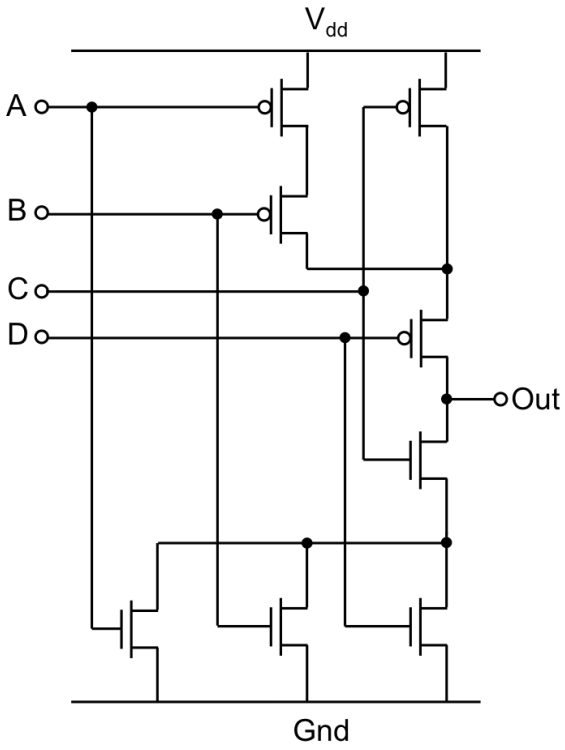
1. (27 points) Identify if the following circuits are CMOS, why or why not, and their functions. [Show your work for partial credit consideration.]



(a)

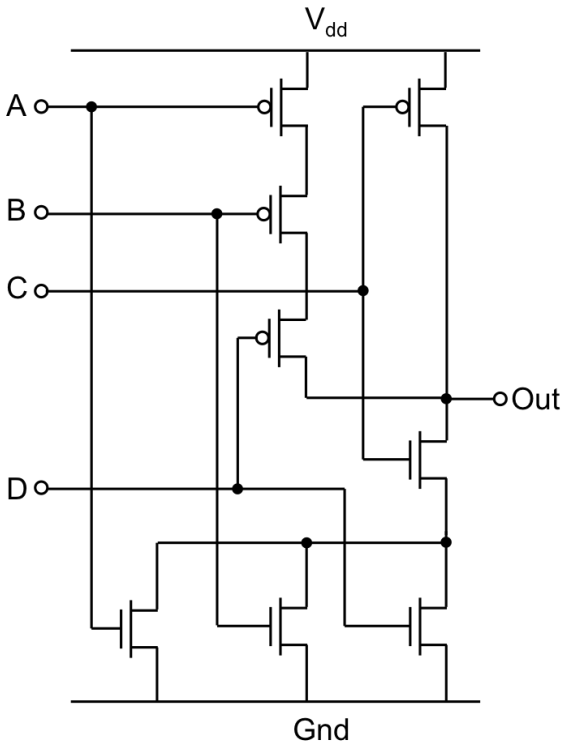
CMOS? (circle one)	Yes No
(if CMOS) Function (Out)	
(if not CMOS) Why not?	

(b)



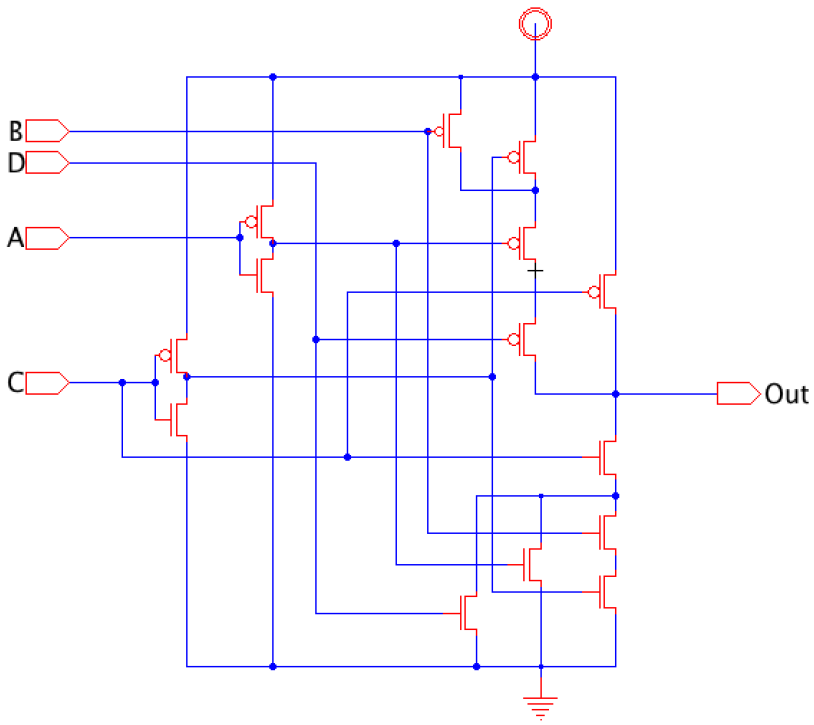
CMOS? (circle one)	Yes No
(if CMOS) Function (Out)	
(if not CMOS) Why not?	

(c)



CMOS? (circle one)	Yes No
(if CMOS) Function (Out)	
(if not CMOS) Why not?	

2. (26 points) Consider the following circuit:



Assume:

- all transistors are same size.
- all on transistors have resitance R_{on}.
- all transistors have total gate capacitance C_g.

(a) Identify the output function.

(b) Extra credit: Simplify the output function to the minimum sum of products. A K-map grid is provided here for your use.

AB \ CD	00	01	11	10
00				
01				
11				
10				

(c) Lowest resistance driving output?

Case: Resistance:

(d) Highest resistance driving output?

Case: Resistance:

(e) Lowest capacitance of an input?

Which: Capacitance:

(f) Highest capacitance of an input?

Which: Capacitance:

For parts (g)-(h), assume input inverters have 0 delay and all inputs are ideal. I.e. the input A and $\overline{A}$ have identical switching characteristics.

(g) Worst-case 10-90 rise time for one of these gates driving a C-input input of another of these gates?

Case:

Rise Time Expression:

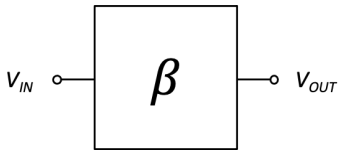
(h) Worst-case 10-90 fall time for one of these gates driving a D-input input of another of these gates?

Case:

Fall Time Expression:

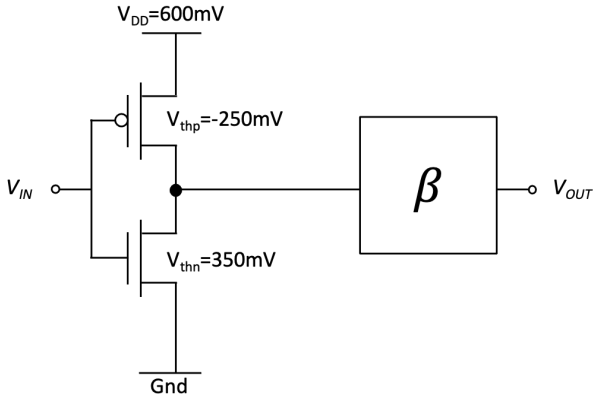
[Show calculation for partial credit consideration.]

3. (25 pts) For this problem we consider a new non-CMOS technology integrated with a CMOS technology. In addition, to the CMOS gates, we have a non-CMOS β-gate where:

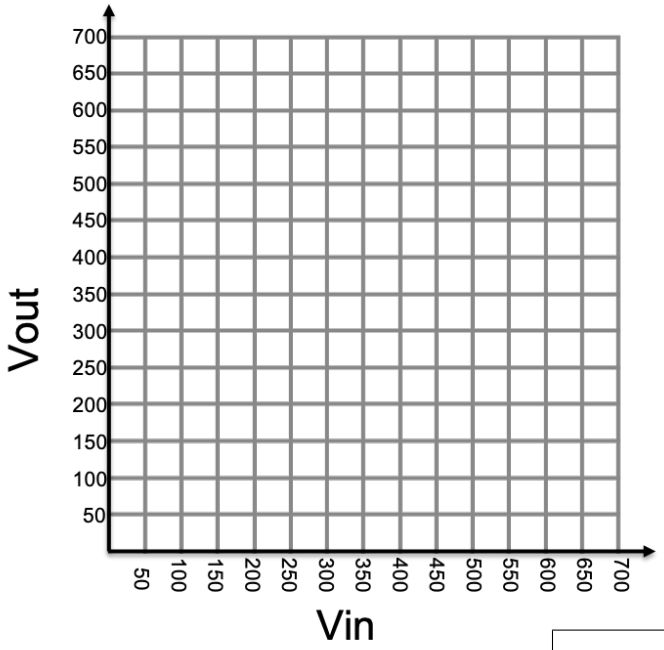


$$V_{out} = \begin{cases} 0.7 - 0.5V_{in} & V_{in} < 0.2 \\ 1 - 2V_{in} & 0.2 \leq V_{in} < 0.4 \\ 0.4 - 0.5V_{in} & 0.4 \leq V_{in} \end{cases}$$

Consider the following non-CMOS circuit of a CMOS inverter cascaded with the non-CMOS β-gate. The transistor thresholds are specified on the schematic.



(a) Draw the transfer function of the cascaded gate and identify noise margins that will provide restoration.



V_{OH}	
V_{IH}	
V_{IL}	
V_{OL}	
NM_L	
NM_H	

(b) What function does the circuit perform?

For reference:
NMOS:

V_{GS}	V_{DS}	Mode
$> V_{th}$	$< V_{GS} - V_{th}$	Resistive
	$> V_{GS} - V_{th}$	Saturation
$< V_{th}$		Subthreshold

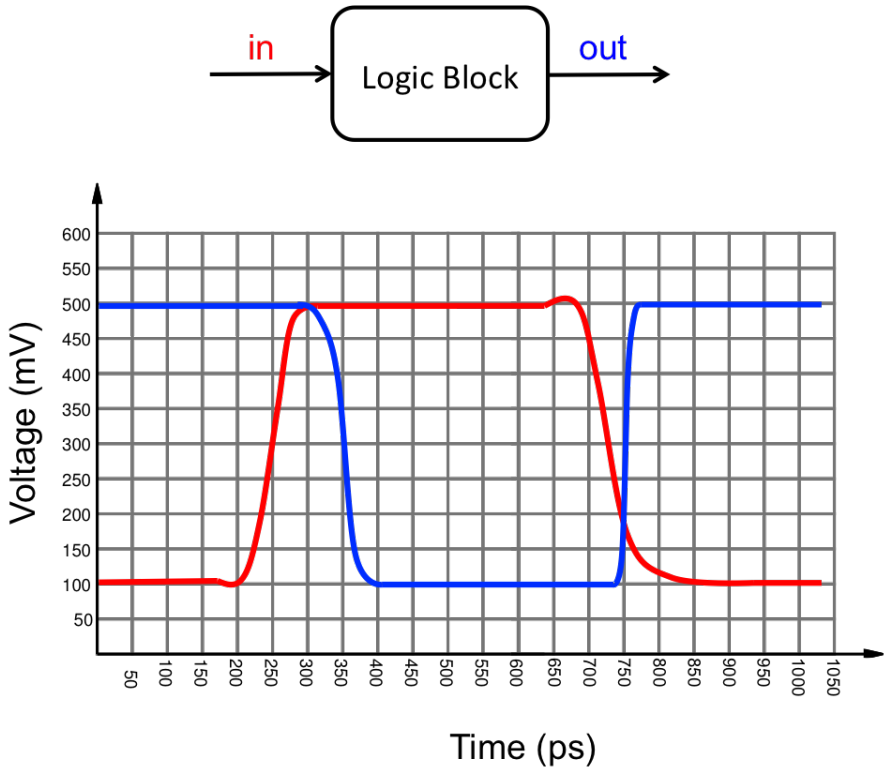
PMOS:

V_{GS}	V_{DS}	Mode
$< V_{th}$	$> V_{GS} - V_{th}$	Resistive
	$< V_{GS} - V_{th}$	Saturation
$> V_{th}$		Subthreshold

(You may work on this almost blank page for Problem 3.)

4. (10pts) For an NMOS device, draw the IV relationships between drain current and the drain-to-source voltage and gate-to-source voltage (I_d vs. V_{GS} and I_d vs. V_{DS}). Label all relevant features. Assume long channel behaviour.

5. (12pts) Below are transient waveforms for the input (red) and output (blue) to a logic block. Find the τ_{PLH}, τ_{PHL}, and τ_P of the logic block. Make sure to include the units.



τ_{PLH}: τ_{PHL}: τ_P: