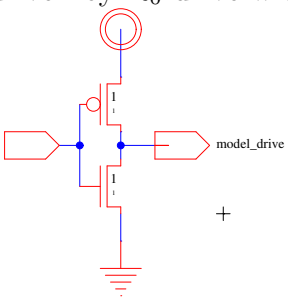
University of Pennsylvania
Department of Electrical and System Engineering
Circuit-Level Modeling, Design, and Optimization for Digital Systems

ESE3700, Spring 2024 — Midterm 2 — Wednesday, April 3

- Point values for each problem are denoted in exam. Point breakdown within problems varies.
- Calculators allowed. No smartphones.
- Closed book = No text or notes allowed.
- V_{dd}=1V, $V_{thn} = -V_{thp} = 250$mV, $\mu_n = \mu_p$, $R_{p0} = R_{n0} = R_0$, unless otherwise specified in problem.
- Unless otherwise noted, inputs driven by R_0 drive with self load $2\gamma C_0$.



A model for the input driver is:

Name: Answers

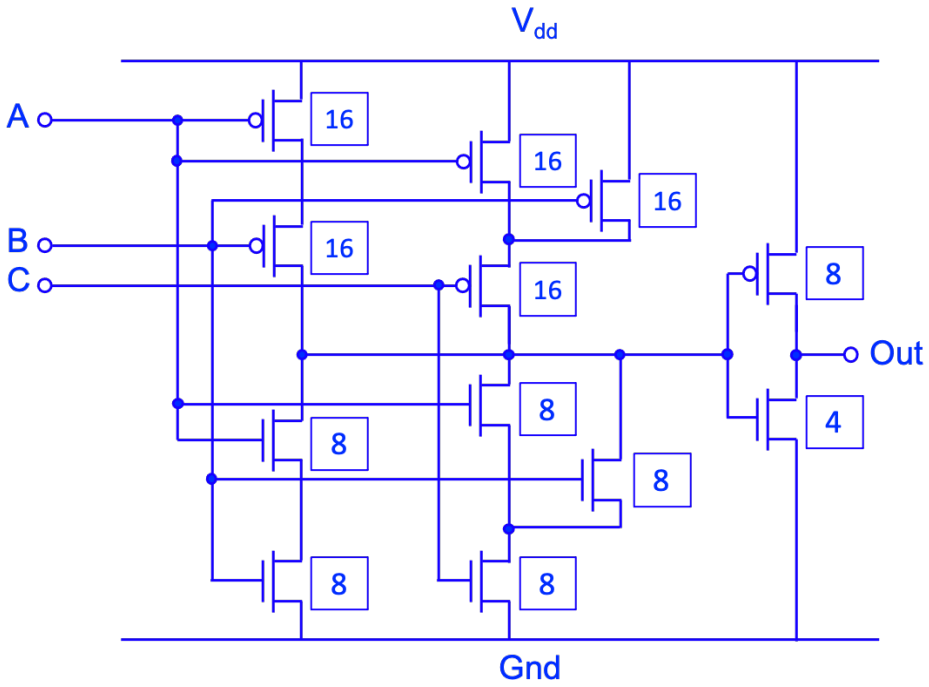
Grade:

Q1	
Q2	
Q3	
Q4	
Total	Mean: 85.7, Stdev: 13.2

1. (25 pts) Assume:

   - $|V_{T_p}| = |V_{T_n}|$
   - R_0=resistance of $W_n = 1$ NMOS transistor
   - μ_n=400 cm$^2/(V \cdot s)$, μ_p=200 cm$^2/(V \cdot s)$ (I.e. $R_{p0} = 2R_{n0}$)
   - C_0 = gate capacitance of $W_n = 1$ transistor
   - C_{diff}=0
   - The output is loaded with a $C_{Load} = 10C_0$
   - All inputs are driven by inverters with an output resistance of $R_0/4$

   Below is a CMOS circuit. Write the function of the design (no need to simplify) and size all devices for a worst-case output resistance of $R_0/4$ in each stage. Calculate the worst-case delay in units of τ including driving the inputs and worst case switching energy. Write all transistor sizes in the boxes next to each device.

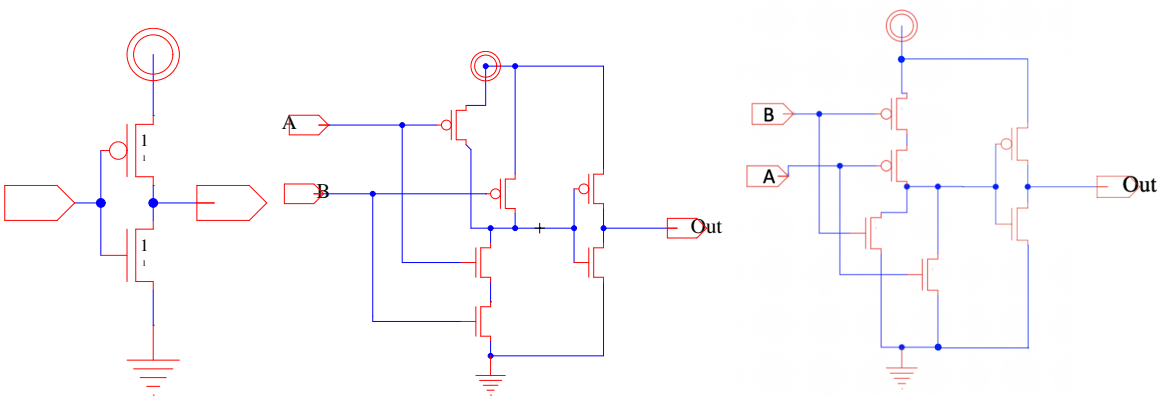


Function	$A \cdot B + A \cdot C + B \cdot C$
Delay	17.5τ
Dynamic Energy	$\frac{1}{2}(142C_0)V_{dd}^2 = 71C_0$

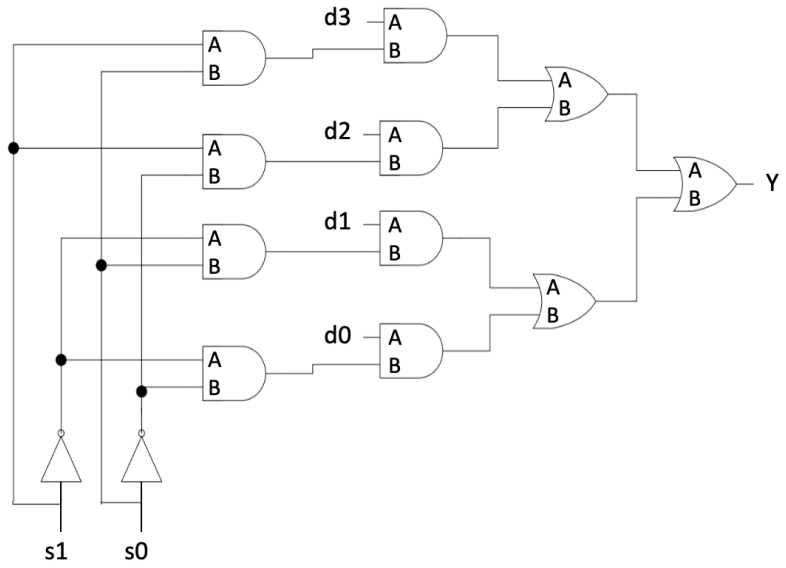
2. (30pts) Estimate Delay for the following two implementations of a 4-to-1 multiplexer (mux4) circuit with four data inputs, $d0$, $d1$, $d2$, and $d3$, two select inputs, $s0$ and $s1$, and a single output, y.

   For the rest of the problem assume:

   - Inverter, and2, and or2 schematics given below.
   - All transistors W=L=1.
   - Give answers in terms of τ and γ; $\gamma = C_{diff}/C_{gate}$.
   - Assume all inputs arrive at the same time and are driven by R_0 drive with $2\gamma C_0$ self load.
   - The load on the output is $8C_0$.



(a) Below is a CMOS implementation of the mux4:

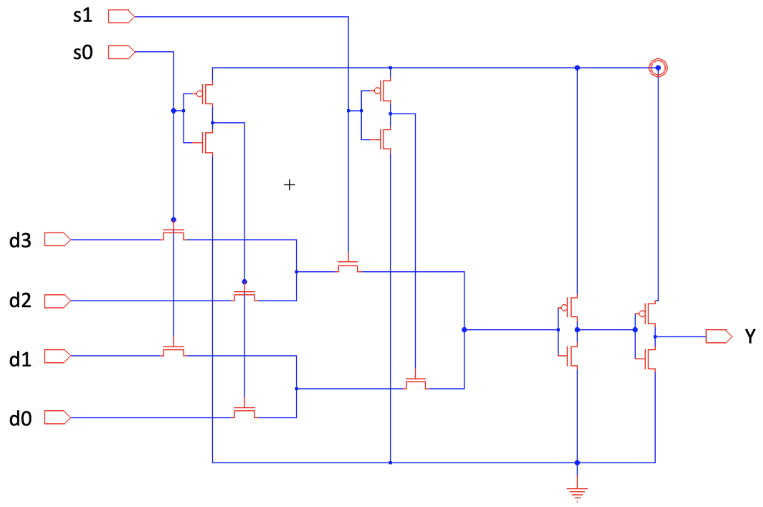


Report worst-case delay for the CMOS mux4 from the R_0 input driver driving the inputs through driving the $8C_0$ load on the output in units of τ. Show individual stage delays for partial credit.

Delay	$(44\gamma + 40)\tau$

Stage	Delay
Driving Input $s0$	$R_0(2\gamma + 6)C_0$
s0 Inv	$R_0(2\gamma + 4)C_0$
stg1 And	$R_0(5\gamma + 2)C_0 + R_0(3\gamma + 2)C_0 + R_0(2\gamma + 2)$
stg2 And	$R_0(5\gamma + 2)C_0 + R_0(3\gamma + 2)C_0 + R_0(2\gamma + 2)$
stg3 Or	$R_0(5\gamma + 2)C_0 + R_0(3\gamma + 2)C_0 + R_0(2\gamma + 2)$
stg4 Or	$R_0(5\gamma + 2)C_0 + R_0(3\gamma + 2)C_0 + R_0(2\gamma + 8)$
Sum	$(44\gamma + 40)\tau$

(b) Below is a pass transistor implementation of the mux4:

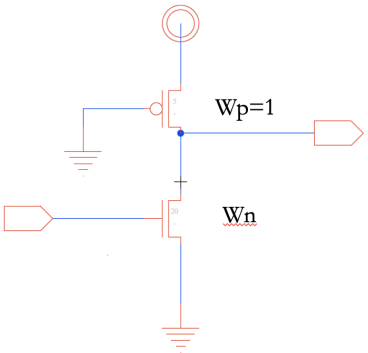


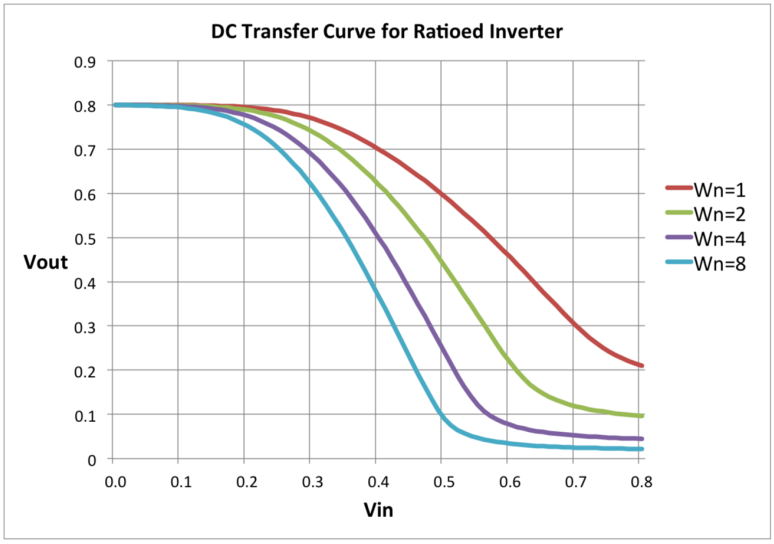
Report worst-case delay for the passT mux4 from the R_0 input driver driving the inputs through driving the $8C_0$ load on the output in units of τ. Assume the same inputs drivers. Show individual stage delays for partial credit.

Delay	$(20\gamma + 22)\tau$

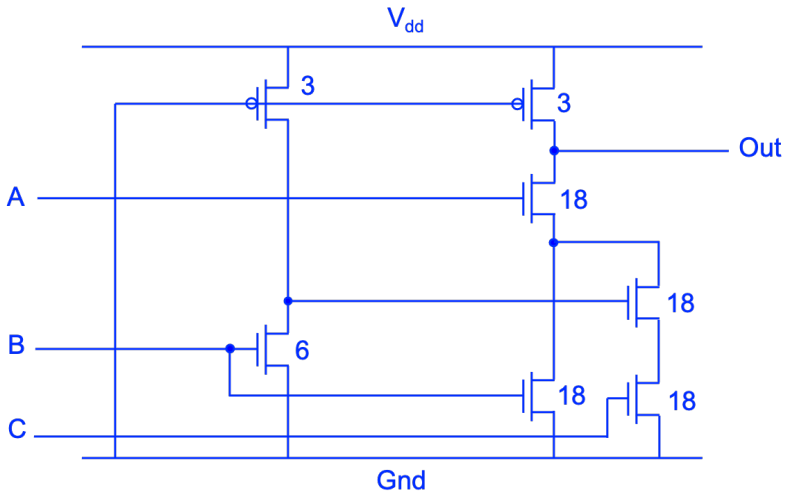
Stage	Delay
Driving Input $s0$	$R_0(2\gamma + 4)C_0$
s0 Inv	$R_0(2\gamma + 2)C_0$
pass tx path	$2R_0(5\gamma + 2)C_0 + R_0(2\gamma + 2)C_0$ (diffusion capacitance on data inputs already charged)
output inv stg1 And	$R_0(2\gamma + 2)$
output inv stg2 And	$R_0(2\gamma + 8)$
Sum	$(20\gamma + 22)\tau$

3. (25pts) Given below is a ratioed inverter with an input nMOS and pMOS load with its gate tied to ground. The voltage transfer characteristic is plotted for different sizes of Wn with $V_{DD} = 0.8V$. Design and size a circuit using only ratioed logic to implement the function $\overline{Out} = A \cdot (B + \overline{B} \cdot C)$. Your design should implement a drive of $\frac{R_0}{3}$ and minimize input capacitance, such that V_{OL} and V_{OH} are within 25% of the supply rails. Clearly label all sizes for every transistor in your design.





The IV curves indicate a $W_n \geq 2W_p$ for noise margins within 25% for $W_p = 1$. Therefore sizing every stage should with $\frac{R_0}{3}$ drive results in the following sizing.



4. (20 pts) Short Answer Questions: Answer the questions briefly. Include diagrams and equations as needed. Be clear in your explanation and handwriting.

A A 12mm long wire has a unit capacitance of 0.18pF per 1mm and unit resistance of 20kΩ per 1mm of wire. What is the delay of the wire using a distributed RC wire model?

$\frac{1}{2}N^2 R_{unit} C_{unit} = 259.2ns$

B How would you simulate and measure the worst case delay in an 8-bit ripple-carry adder? Be specific.

The worst case delay is when a carry is generated in the LSB stage and must be propagated to the final stage. This would occur for the input test case: input `A = 1111 1111` and `B` switches from `0000 0000 --> 0000 0001`. Using ideal voltage sources with input drivers equivalent to an adder output drive and loads equivalent to the input capacitance of the 8-bit adder, I would measure when the input is 50% of its switching to the final output to reach 50% of its swing.

C A CMOS inverter is designed with minimum sized devices. The threshold voltage of the nMOS and pMOS varies and both are larger in magnitude than the nominal value. What effect does this have on leakage energy of the inverter?

The increased threshold would decrease leakage current and thus decrease leakage energy.

D What is one advantage and one disadvantage of pass transistor logic?

Pass transistor logic is less complex to design and smaller in area, but it has a voltage threshold drop and can be slow with long cascades of pass gates.

E How is the delay of a gate affected by its fanout? Give a qualitative answer.

With larger fanout, the gate delay is larger because the load capacitance is larger.