University of Pennsylvania
Department of Electrical and System Engineering
Circuit-Level Modeling, Design, and Optimization for Digital Systems

ESE3700, Spring 2024 — Project 2: Memory Design — Wednesday, April 10

Milestone Due: Friday, April 19, 11:59PM
Due: Wednesday, May 1, 11:59PM

Project Pairs: You can work in groups of no more than 2 for this project. Each team must turn in one report with the clear contributions of each partner clearly delineated. Everyone is responsible for understanding the design and report in its entirety, and the instructor reserves the right to interview the students to verify this.

Extra Credit: The two reports with the lowest and second lowest reported FOM (see Design Metrics section), will receive 10 and 5 extra credit points respectively. You must correctly measure, calculate and report the metric to be eligible for the extra credit. Additionally one report will be awarded best writeup and will receive 5 extra credit points.

Design Problem: Design a 16x4 (16 words of 4 bits) SRAM memory

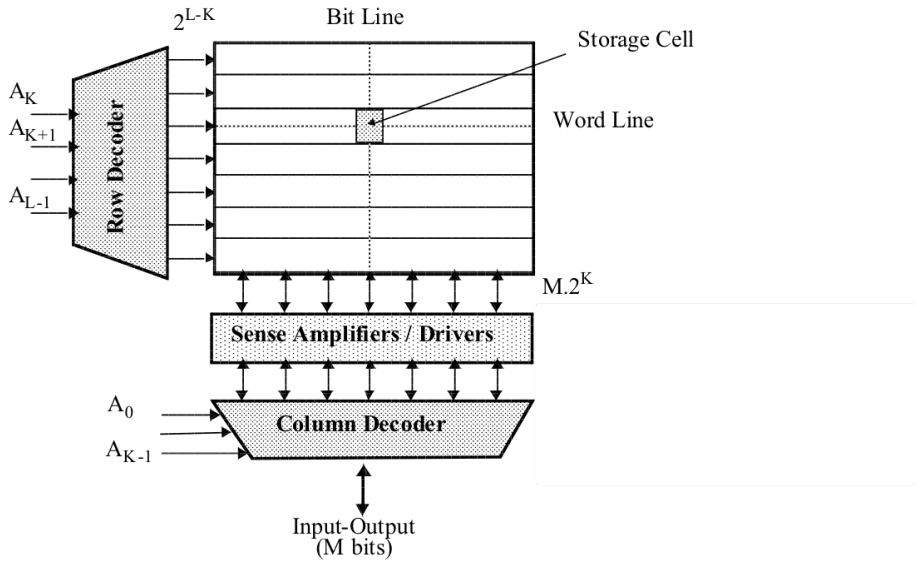
- The design will be characterized by a figure-of-merit (FOM) calculated as the area-power-delay product:

$$FOM = 60 * BitcellArea \cdot Power \cdot Delay^2$$

  The FOM should use the Power and Delay reported from the layout extracted schematic including parasitic effects.

- The design must have full word (4 bits) random access read and write capability and be SRAM, but the topology of the core cells and periphery circuits are open and available for optimization.

- Target technology is the High Performance 22nm process (`/home1/e/ese3700/ptm/22nm_HP.pm`)
- $V_{dd} \leq 1V$
- Design should be synchronous with the max CLK frequency (ie. min CLK period) based on your design's delay (ie. write access time and read access time). Your max frequency must be greater than 500 MHz (ie. your memory must be able to operate with at least a 500 MHz clock).



- We will concretely focus on an SRAM memory array with capacity of 16, holding 4b-wide data elements.
- Inputs: 4-bit address, active high write enable (WE=1 for write, WE=0 for read), 4-bit data bus, and a single clk signal for synchronization
- Outputs: 4-bit data bus
- A read or write operation must be completed within one clock period

Design Metrics:

- *memory cell area*: Sum the total transistor width for the repeated memory cell in the memory core.
- *delay*: Measure the worst-case write access time and read access time, and report the worst case delay (ie. maximum of read and write times)
- *power*: Measure the power consumed during writing the entire array with 0s, then writing the entire array with 1s. Repeat these two full array write operations 4 times each in sequence and measure the average current to calculate the power consumption. The CLK frequency for this measurement should be with the minimum CLK period that your SRAM will operate correctly based on your measured read/write delays.
- *FOM*: Report the $FOM = 60 * BitcellArea \cdot Power \cdot Delay^2$.

Recommendations:

- First thing you should do is create non-overlapping clocks from your single input CLK signal
- What should you add to ensure your inputs changing during a read/write cycle doesn't affect the read/write operation for that clock cycle?
- Even before you worry about optimizing the FOM, you need to assure that you can achieve correct operation.
- Pay careful attention to the timing of controls for writes. What do you need to guarantee to make sure you only write into the intended word cells on a write cycle?
- Use hierarchy in your schematics. You should have a single memory cell design that you instantiate. You should also organize cells into word rows. You may also want a separate organization into columns for reasons noted below.
- Use unit testing. Make sure your memory cell, decoder, buffers work in isolation before you integrate larger structures.
- Think about what sequence of inputs and multiple operations would test functionality of all possible read/write operations.
- To generate a sequence of logic values, you can use a VPWL (Piece-Wise Linear) source in electric. This produces a SPICE PWL. Please see HW6 and the ngspice manual for more information.
- We are not necessarily looking for innovation in the core memory cell circuit, but it will need to be sized for the technology and adapted for your usage.
- Cell sizing may be asymmetric to address the different needs of reads and writes.

Milestone (April 19): Turnin as a single PDF.

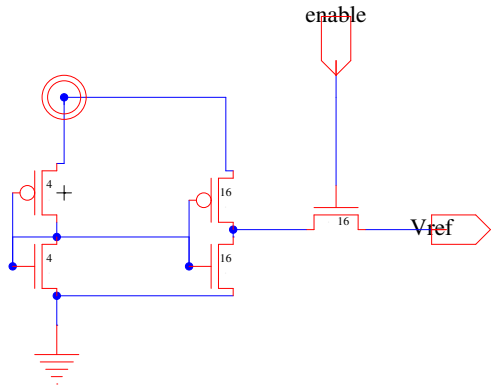
- Estimate bit line capacitance for target design point. Report and use in the simulations below to demonstrate cell operation.
- Include schematics for column driver and **sized** memory cell. You may use PWL controls and ideal voltage references for this phase of the design. PWL controls and ideal voltage references are temporary scaffolding; you will implement the controls and references in transistors for the final design.
- Identify the set of cases you should test in order to validate correct operation of your memory cell on both writes and reads.
- Demonstrate that you can write to the memory cell. Include schematics for setup and simulation waveforms as necessary.
- Demonstrate that you can read from the memory cell without losing the value. What test cases do you need to demonstrate this? Include schematics for setup and simulation waveforms as necessary.
- Identify the constraints on write timing in the full design (not just the cell) to guarantee correct operation, and identify how you will verify this (what test setup? what test cases?).

Final Report: Your report should be a single, stand-alone document and should include:

- Schematics for the design – make sure transistor sizing annotations are easily readable in the diagram you include in the report.
- For both the read and write operations show:
  - Waveform showing timing of key signals in the operation. Identify the delay of each component that makes up the critical path.
- Text description of the memory operation and design choices. Identify and describe the operation of each of the sub-components. Your description should make it easy for us to understand how and why your design works.
  - Explain the timing requirements of the memory for correct operation
  - Explain rationale for sizing of memory cell—why are the transistors sized as you did, and how did you arrive at this conclusion? Show simulations as necessary.
- Description of how you validated correctness of the design. This will include a description of your test cases.
- Summary of the design metrics and your calculated FOM. Include supporting evidence in the form of equations, simulation results, and figures.
- Include a table summarizing all design metrics.
- Please include a statement on your final submission:

> I, *your-name-here*, certify that I have complied with the University of Pennsylvania's Code of Academic Integrity in completing this project.

Voltage Midpoint Reference Generator



Here's a voltage reference generator that may be useful for your memory design. The inverter with input and output tied together settles to the midpoint of the transfer curve where the input and output are equal. The second inverter is driven to the same point. It serves to isolate the output from the reference generated by the first one. The pass gate allows you to connect or disconnect this reference voltage to a node.

You may need to resize the driving buffer and pass transistor. Sizes shown are just to give concrete examples.