University of Pennsylvania
Department of Electrical and System Engineering
Computer Organization

ESE680-002, Spring 2007 Assignment 6: Interconnect Design Monday, March 12

Due: Wednesday, March 21, 12:00PM

For this assignment, you will explore design parameters for mesh networks using Toronto's placement and routing tool `vpr`.

For the two designs given in `/home1/e/ese680s2/interconnect/nets/` (apex4, tseng): and associated placements in `/home1/e/ese680s2/interconnect/place/`:

1. Use `vpr` in route only mode to determine how the channel width and delay varies when the segment length is increased from 1 to the row width (36 for apex, 33 for tseng). Make a table and a plot of the results (channel width vs. segment length). You will have a delay and channel column and curve for each design.

   You don't have to run all 36 points—12 will probably do. Please zero in and provide per track increments around the actual minima (composite results below), but further from the minima, you may space samples further apart.

   Keep full population of connection boxes and switch boxes (`Frac_cb` and `Frac_sb` will be 1).

2. Calculate the number of switches per track per Logic Block for each of the cases. Make a table and a plot of the results (switches per track per Logic Block vs. segment length).

   Pay attention to the Logic Block to channel IO population as described in the architecture file. The Mesh-of-Trees paper shows a picture of this connection (Figure 10).

   I believe `vpr` assumes there is a single switch which allows you to make a corner turn between horizontal and vertical segments which do not end in a particular switchbox. Consequently, each track which does not end at a switchbox contributes 1 switch, while a track that does end contributes 6. (We did not count this extra switch in the equations in the Mesh-of-Trees paper.)

3. Use the previous two results to compute switches per logic block as a function of segment length for each of the designs. Make a table and a plot of the results.

4. Identify the segment lengths which minimize switch requirements for each design.

5. Characterize the track-length-induced area-delay tradeoff for the two designs. From this data can you pick a single, preferred track length for the FPGA?

vpr notes:

- You can find a copy of the `vpr` executable on the CETS computing systems:
  `/project/ese/ic/usr/vpr/vpr`
- You can find the manual for vpr:
  `/project/ese/ic/usr/vpr/manual430.pdf`
- To perform this experiment, you will need to create a separate architecture file for each segment length. The architecture file is described in Section 6.2.3 of the vpr manual (around pp. 17–20). For this problem you will especially be interested in Figure 7 and the example on the top of that page that goes with it.
- A base, segment length 1, architecture file is provided in:
  `/home1/e/ese680s2/interconnect/arch/seg1.txt`
- A typical command for invoking vpr will look like:
  `vpr apex4.net seg1.txt apex4.placed apex4.seg1.route -nodisp -route_only -router_algorithm breadth_first`
  Where:
  - `apex4.net` is the design (the netlist)
  - `seg1.txt` is the architecture file
  - `apex4.placed` is a placement for the design
  - `apex4.seg1.route` is the file in which to store the route for the design
  - `-nodisp` tells it not to bring up the interactive X display
  - `-route_only` tells it not to perform placement (use the given placement)
  - `-route_algorithm breadth_first` tells it to use a channel minimizing router
- If you drop the `-nodisp` option, you can interact with vpr and it will show you pictures of the design. See the vpr manual for further detail on this and other vpr options.