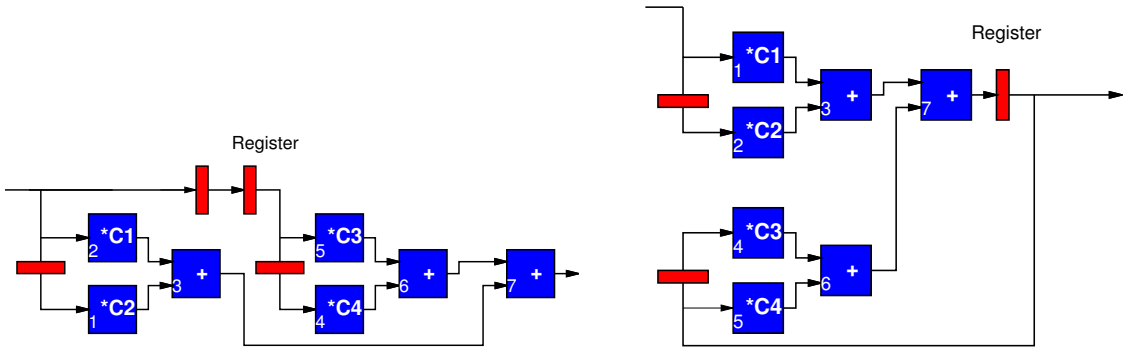
University of Pennsylvania
Department of Electrical and System Engineering
Computer Organization

ESE680-002, Spring 2007 — Assignment 8: Scheduling — Wednesday, March 28

Due: Wednesday, April 4, 12:00PM

Consider the two computational graphs shown here:



These are the same as on the previous assignment, however we've numbered the functional units to assist your writeup.

This time we will time-multiplex the datapath and explore multi-cycle solutions scheduled on the datapath.

1. Starting with the datapath on page 3 (a slight modification of the one from the previous assignment) identify the *pinst* for the basic cell.

   (a) what are the logical fields?

   (b) how many bits in each field?
   (state assumptions necessary to reduce field lengths to absolute numbers)

2. Map each of the reference graphs above to a time-multiplexed, 4-cell design. Each cell has two instructions which execute in round-robin fashion. Target producing a single result every second cycle. For each graph:

   (a) what is the minimum channel widths (Left→Right and Right→Left)?

   (b) what is the maximum depth required for input retiming registers?

   (c) what is the minimum C for the design?

   (d) show the schedule/programming for the mapped design in a table of the form shown below:

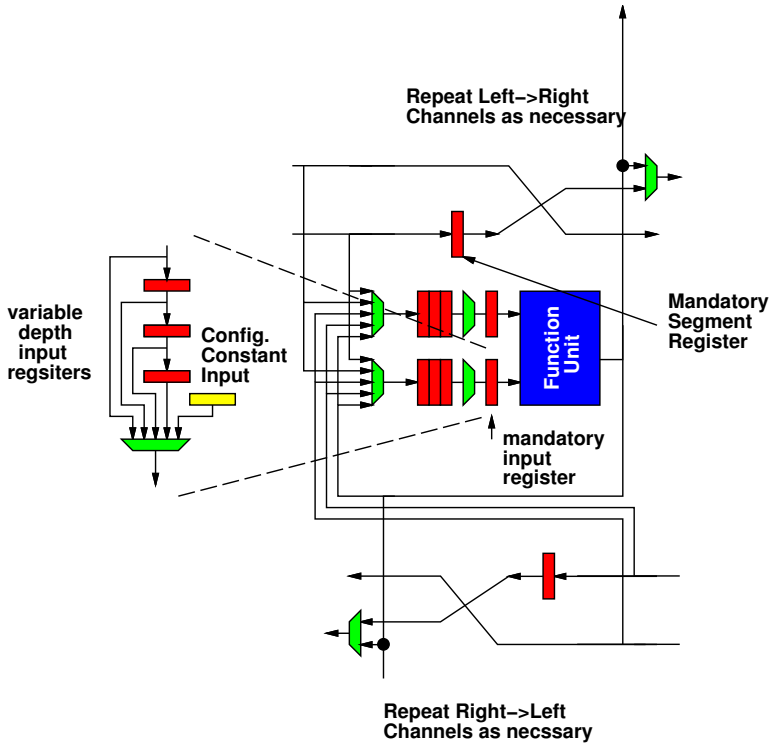
Cycle	Cell 0					Cell 1					Cell 2					Cell 3				
	Graph Node (#)	Pinst field 0	1	2	3	Graph Node (#)	Pinst field 0	1	2	3	Graph Node (#)	Pinst field 0	1	2	3	Graph Node (#)	Pinst field 0	1	2	3
1																				
2																				

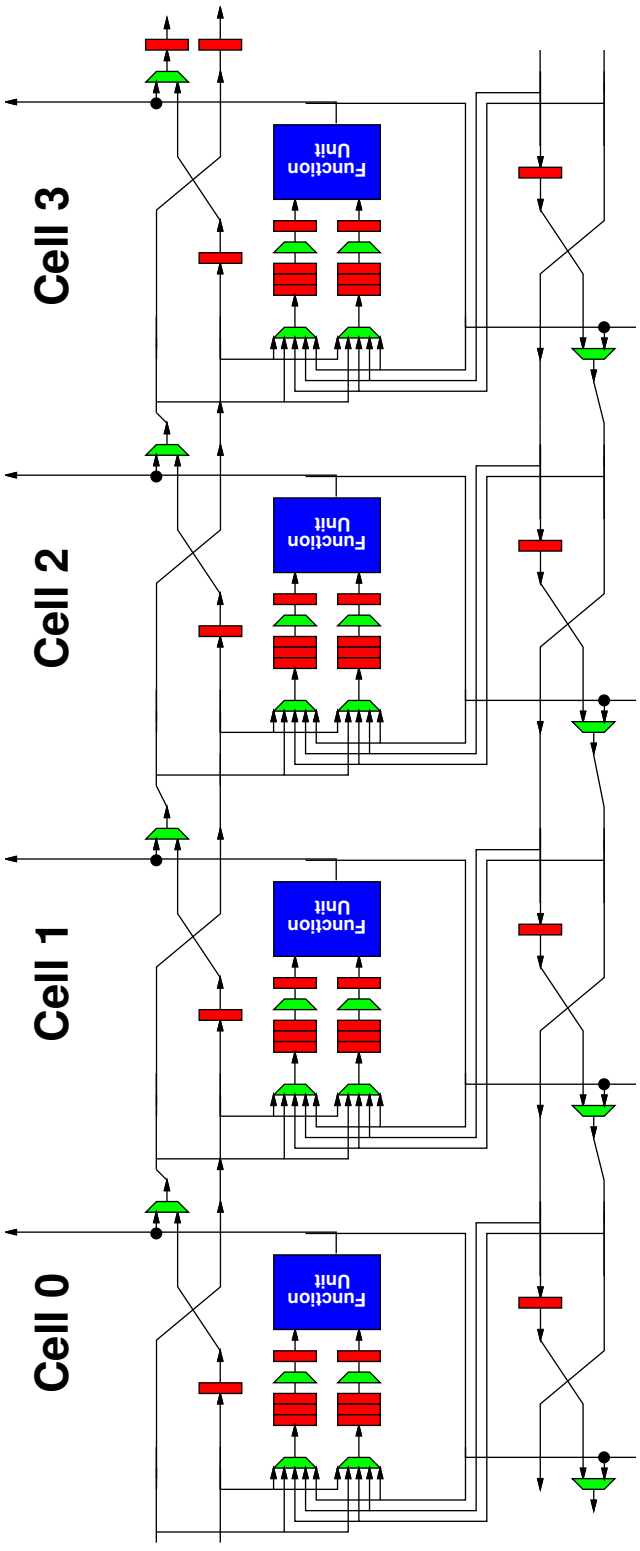
   [Shown with 4 fields for illustration only; use as many as you identified above, and give them meaningful semantic names rather than "field 0".]

3. Schedule the right graph only onto a 1-cell design. The cell has seven instructions which execute in round-robin fashion. Target producing a single result every seventh cycle. Provide the same information as above.

Shown below is a single slice of the one-dimensional datapath architecture. A 4 slice instance of the architecture is shown on the following page.

- This is largerly the same datapath from the previous assignment.
- Interconnect is shown as muxes instead of individual switches to ease *pinst* identification and description; for this simplification, there is one capability removed on this design (the output can no longer enter the middle of a length 2 segment).
- The output of a cell can now feedback to itself.
- The input muxes are shown with inputs from only one left→right and one right→left track pair for simplicity. These input muxes should expand with the track width so that all tracks are available as possible inputs.




Cell 3
Function Unit
Cell 2
Function Unit
Cell 1
Function Unit
Cell 0
Function Unit