

ESE680-002 (ESE534): Computer Organization

Day 1: January 8, 2007
Introduction and Overview

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Today

- Matter Computes
- Architecture Matters
- This Course (short)
- Unique Nature of This Course
- Change
- More on this course

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Review: Two Universality Facts

- NAND gate Universality
 - We can implement any computation by interconnecting a sufficiently large network of NAND gates
- Turing Machine is Universal
 - We can implement any *computable* function with a TM
 - We can build a single TM which can be programmed to implement any computable function

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On Prerequisites

- Suggested:
 - ESE200/201 or CSE240/370/371....(some exposure to boolean logic, basic logic circuits)
 - CS262 (compute models, universality)

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Review: Matter Computes

- We can build NAND gates out of:
 - transistors (semiconductor devices)
 - physical laws of electron conduction
 - mechanical switches
 - basic physical mechanics
 - protein binding / promotion / inhibition
 - Basic biochemical reactions
 - ...many other things

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Starting Point

- Given sufficient raw materials:
 - can implement any computable function
- Our goal in computer architecture
 - is **not** to figure out how to compute new things
 - rather, it is an **engineering** problem

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Engineering Problem

- Implement a computation:
 - with least resources (in fixed resources)
 - with least cost
 - in least time (in fixed time)
 - with least energy
- Optimization problem
 - how do we do it best?

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Quote

- “An Engineer can do for a dime what everyone else can do for a dollar.”

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Architecture Matters?

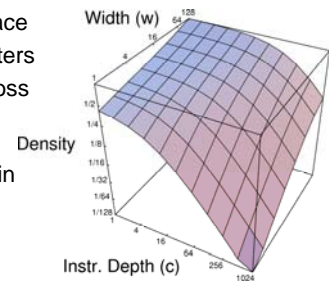
- How much difference is there between architectures?
- How badly can I be wrong in implementing/picking the wrong architecture?
- How efficient is the IA-32, IA-64?
 - Is there much room to do better?
- Is architecture done?
 - A solved problem?

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Peak Computational Densities from Model

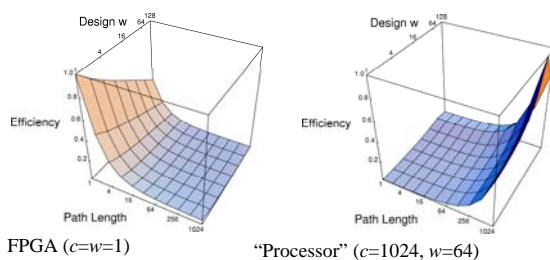
- Small slice of space
 - only 2 parameters
- 100× density across
- Large difference in peak densities
 - large design space!



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Yielded Efficiency



FPGA ($c=w=1$) "Processor" ($c=1024, w=64$)

- Large variation in **yielded** density
 - large design space!

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Architecture **Not** Done

- Many ways, not fully understood
 - design space
 - requirements of computation
 - limits on requirements, density...
- ...and the *costs* are changing
 - optimal solutions change
 - creating new challenges and opportunities

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Personal Goal?

- Develop systematic design
- Parameterize design space
 - adapt to costs
- Understand/capture req. of computing
- Efficiency metrics
 - (similar to information theory?)
- ...we'll see a start at these this term

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Architecture **Not** Done

- Not here to just teach you the forms which are already understood
 - (though, will do that and give you a strong understanding of their strengths and weaknesses)
- **Goal:** enable you to design and synthesize new and better architectures

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This Course (short)

- How to organize computations
- Requirements
- Design space
- Characteristics of computations
- Building blocks
 - compute, interconnect, retiming, instructions, control
- Comparisons, limits, tradeoffs

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This Course

- Sort out:
 - Custom, RISC, SIMD, Vector, VLIW, Multithreaded, Superscalar, EPIC, MIMD, FPGA
- Basis for design and analysis
- Techniques
- [more detail at end]

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Graduate Class

- Assume you are here to learn
 - Motivated
 - Mature
 - Not just doing minimal to get by and get a grade
- Problems
 - May not be fully, tightly specified

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Uniqueness of Class

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Not a Traditional Arch. Class

- Traditional class (240, 370, 501)
 - focus RISC Processor
 - history
 - undergraduate class on μ P internals
 - then graduate class on details
- This class
 - much broader in scope
 - develop design space
 - see RISC processors in context of alternatives

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Authority/History

- "Science is the belief in the ignorance of experts." -- **Richard Feynman**
- Traditional Architecture has been too much about history and authority
- Should be more about engineering evaluation
 - **physical world** is "final authority"
- **Goal:** Teach you to think critically and independently about computer design.

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Next Few Lectures

- Quick run through logic/arithmetic basics
 - make sure everyone remembers
 - (some see for first time?)
 - get us ready to start with observations about the key components of computing devices
- Trivial/old hat for many
 - But will be some observations couldn't make in ESE200/CIS370
- May be fast if seeing for first time
- Background quiz intended to help me tune

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Themes

- Design Space
 - Parameterization
 - Costs
 - Change
 - Structure in Computations
- FUTURE:**
Except for the last one,
These felt redundant,
Already covered on slide 14,16

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Focus

- Focus on raw computing organization
- **Not** worry about nice abstractions, models
 - 501, 370, 240 provide a few good models
 - ...but probably not all you should know...

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Change

- A key feature of the computer industry has been **rapid and continual change**.
- We must be prepared to adapt.

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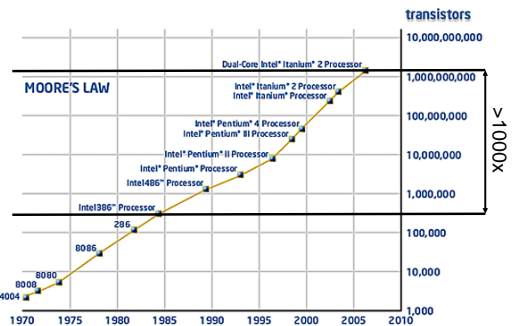
What has changed?

- [Discuss]
- Capacity
 - Total
 - Per die
- Size
- Applications
 - Number
 - Size/complexity of each
 - Types/variety
- Use Environment
 - Embedded
 - Mission critical
- Speed
 - Ratio of fast memory to dense memory
 - Wire delay vs. Gate delay
 - Onchip vs. inter-chip
- Joules/op
- Mfg cost
 - Per transistor
 - Per wafer

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Intel's Moore's Law



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1983 (early VLSI)

- Early RISC processors
 - RISC-II, $15M\lambda^2$, 40K transistors
 - MIPS, $20M\lambda^2$, 24K transistors
 - ~10MHz clock cycle
- Xilinx XC2064
 - 64 4-LUTs

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Today

- CPUs
 - Multi-issue, 64b processors
 - GHz clock cycles
 - MByte caches
 - Multicore
- FPGAs
 - >100,000 bit processing elements
 - Mbits of on-chip RAM

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More chip capacity?

- Should a 2007 single-chip multiprocessor look like a 1983 multiprocessor systems?
 - Processor→processor latency?
 - Inter-processor bandwidth costs?
 - Cost of customization?

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Memory Levels

- Why do we have 5+ levels of memory today?
 - Apple II, IBM PC had 2
 - MIPS-X had 3

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Class Components

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Class Components

- Lecture
- Reading [~1 required paper/lecture]
 - No text
- 8 assignments
 - (roughly every 3 lectures)
- Final design/analysis exercise
 - (2 weeks)
- Note syllabus, course admin online
 - See URL bottom of logic assignments

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Feedback

- Will have anonymous feedback sheets for each lecture
 - Clarity?
 - Speed?
 - Vocabulary?
 - General comments

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Fountainhead Quote

Howard Roark's Critique of the Parthenon
-- Ayn Rand

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Fountainhead Parthenon Quote

"Look," said Roark. "The famous flutings on the famous columns---what are they there for? To hide the joints in wood---when columns were made of wood, only these aren't, they're marble. The triglyphs, what are they? Wood. Wooden beams, the way they had to be laid when people began to build wooden shacks. Your Greeks took marble and they made copies of their wooden structures out of it, because others had done it that way. Then your masters of the Renaissance came along and made copies in plaster of copies in marble of copies in wood. Now here we are making copies in steel and concrete of copies in plaster of copies in marble of copies in wood. Why?"

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Computer Architecture Parallel

- Are we making:
 - copies in submicron CMOS
 - of copies in early NMOS
 - of copies in discrete TTL
 - of vacuum tube computers?

Big Ideas

- Matter Computes
- Efficiency of architectures varies widely
- Computation design is an engineering discipline
- Costs change \Rightarrow Best solutions (architectures) change
- Learn to cut through hype
 - analyze, think, critique, synthesize