ESE680-002 (ESE534): Computer Organization

Day 4: January 22, 2007
Memories

Last Time

- Arithmetic: addition, subtraction
- Reuse:
  - pipelining
  - bit-serial (vectorization)
  - shared datapath elements
- FSMDs
- Area/Time Tradeoffs
- Latency and Throughput

Today

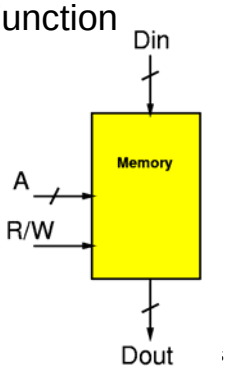
- Memory
  - features
  - design
  - technology

Memory

- What's a memory?
- What's special about a memory?

Memory Function

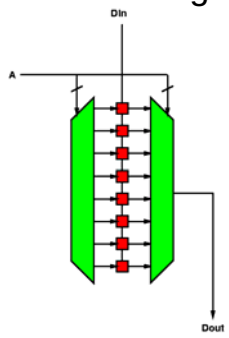
- Typical:
  - Data Input Bus
  - Data Output Bus
  - Address
    - (location or name)
  - read/write control



Memory

- Block for storing data for later retrieval
- State element
- What's different between a memory and a collection of registers like we've been discussing?

Collection of Registers

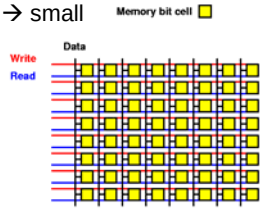


Memory Uniqueness

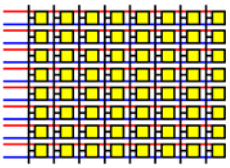
- Cost
- Compact state element
- Packs data very tightly
- At the expense of sequentializing access
- Example of Area-Time tradeoff
  - and a key enabler

Memory Organization

- **Key idea**: sharing
  - factor out common components among state elements
  - can have big elements if amortize costs
  - state element unique → small



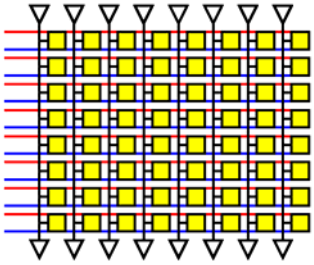
Memory Organization



- Share: Interconnect
  - Input bus
  - Output bus
  - Control routing
- **very** topology/wire cost aware design
- Note: local, abuttment wiring

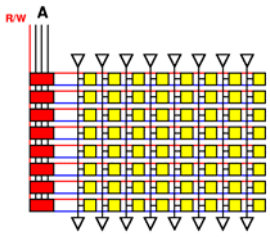
Share Interconnect

- Input Sharing
  - wiring
  - drivers
- Output Sharing
  - wiring
  - sensing
  - driving

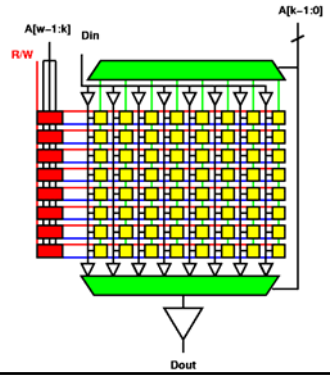


Address/Control

- Addressing and Control
  - an overhead
  - paid to allow this sharing

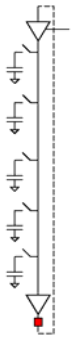


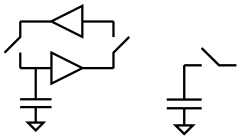
Memory Organization



Dynamic RAM

- Goes a step further
- Share refresh/restoration logic as well
- Minimal storage is a capacitor
- "Feature" DRAM process is ability to make capacitors efficiently

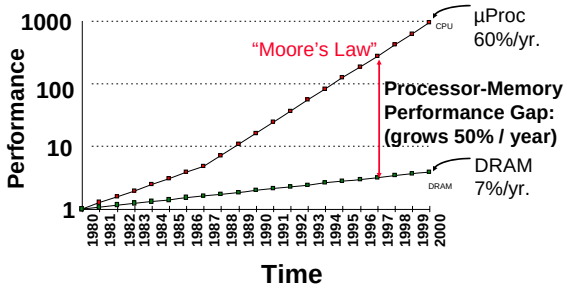




Some Numbers (memory)

- Unit of area = λ^2
  - [more next time]
- Register as stand-alone element ≈ $4K\lambda^2$
  - *e.g.* as needed/used last two lectures
- Static RAM cell ≈ $1K\lambda^2$
  - SRAM Memory (single ported)
- Dynamic RAM cell (DRAM process) ≈ $100\lambda^2$
- Dynamic RAM cell (SRAM process) ≈ $300\lambda^2$

DRAM Latency



[From Patterson et al., IRAM: **http://iram.cs.berkeley.edu/]**

Contemporary DRAM

- 1GB DDR3 SDRAM from Micron
  - http://www.micron.com/products/dram/ddr3/
  - 96 pin pakage
  - 16b datapath IO
  - Operate at 500+MHz
  - 37.5ns random access latency

Table 1: Key Timing Parameters

Speed Grade	Data Rate (Mb/s)	Target RCD/RP/CL	t_{RCD} (ns)	t_{RP} (ns)	CL (ns)
-25E	800	5-5-5	12.5	12.5	12.5
-25	800	6-6-6	15	15	15
-187E	1,066	7-7-7	13.1	13.1	13.1
-187	1,066	8-8-8	15	15	15
-15E	1,333	9-9-9	13.5	13.5	13.5
-15	1,333	10-10-10	15	15	15

Options **Marking**

- Configuration
  - 64 Meg x 16 (8 Meg x 16 x 8 banks) 64M16
  - 128 Meg x 8 (16 Meg x 8 x 8 banks) 128M8
  - 256 Meg x 4 (32 Meg x 4 x 8 banks) 256M4
- FBGA package (lead-free)
  - x4, x8; 86-ball FBGA (9mm x 15.5mm) BY
  - x16; 96-ball FBGA (9mm x 15.5mm) LA
- Timing – cycle time
  - 2.5ns @ CL = 6 (DDR3-800) -25
  - 2.5ns @ CL = 5 (DDR3-800) -25E
  - 1.87ns @ CL = 8 (DDR3-1066) -187
  - 1.87ns @ CL = 7 (DDR3-1066) -187E
  - 1.5ns @ CL = 10 (DDR3-1333) -15
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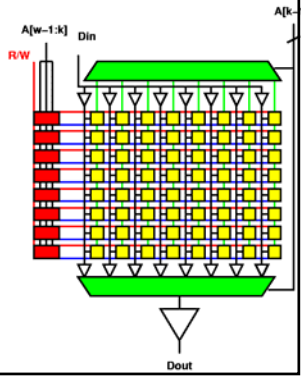
Memory Access Timing

- RAS/CAS access
- Optimization for access within a row



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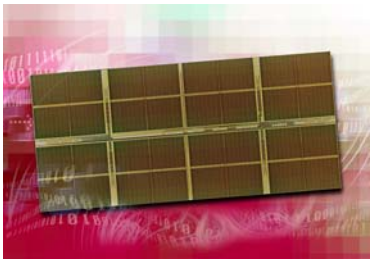
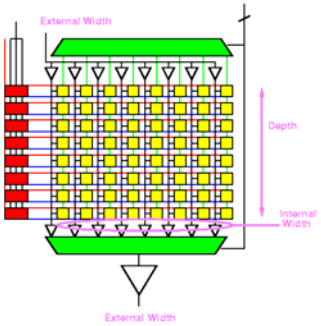
1 Gigabit DDR2 SDRAM



[Source: http://www.elpida.com/en/news/2004/11-18.html]

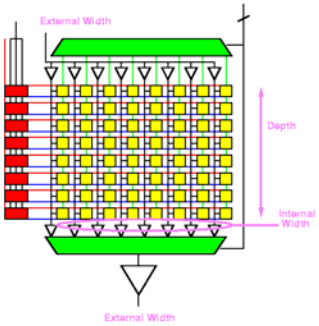
Basic Memory Design Space

- Width
- Depth
- Internal vs. External Width
- *Banking*
  - *To come*



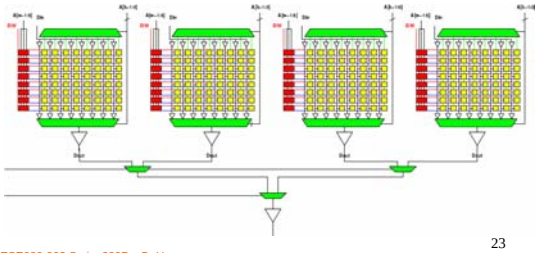
Depth

- What happens as make deeper?

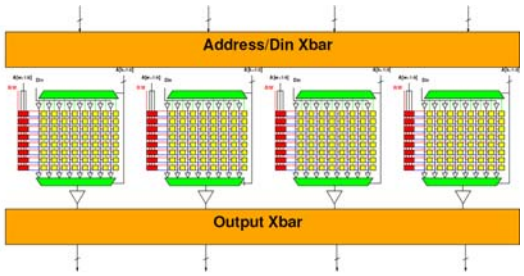


Banking

- Tile Banks/memory blocks



Independent Bank Access



Memory

- **Key Idea**
  - Memories hold state compactly
  - Do so by minimizing key state storage and amortizing rest of structure across large array

System Memory Design

- Have a memory capacity to provide
- What are choices?

System Memory Design

- One monolithic memory?
  - Internal vs. external width
  - internal banking
- External width
- Separate memory banks (address ports)

Yesterday vs. Today (Memory Technology)

- What's changed?

Yesterday vs. Today (Memory Technology)

- What's changed?
  - Capacity
    - single chip
  - Integration
    - memory and logic
    - dram and logic
    - embedded memories
  - Room on chip for big memories
    - And many memories…
  - Don't have to make a chip crossing to get to memory

Important Technology Cost

- IO between chips << IO on chip
  - pad spacing
  - area vs. perimeter ($4s$ vs. s^2)
  - wiring technology
- **BIG** factor in multi-chip system designs
- Memories nice
  - very efficient with IO cost vs. internal area

On-Chip vs. Off-Chip BW

- Use Micron 1Gb DRAM as example

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On Chip BW:
assume 8 1024b banks?
assume 8×16 1024b banks?
assume 1024×1024b banks?

Costs Change

- Design space changes when whole system goes on single chip
- Can afford
  - wider busses
  - more banks
  - memory tailored to application/architecture
- Beware of old (stale) answers
  - their cost model was different

What is Importance of Memory?

- Radical Hypothesis:
  - Memory is simply a very efficient organization which allows us to store data compactly
    - (at least, in the technologies we've seen to date)
  - A great engineering trick to optimize resources
- Alternative:
  - memory is a **primary**

Admin

- André still in Moore 305 for now
- Reading for next Monday on web
  - Classic paper on MOS scaling

Big Ideas [MSB Ideas]

- Memory: efficient way to hold state
- Resource sharing: key trick to reduce area
- Memories are a great example of resource sharing

Big Ideas [MSB-1 Ideas]

- Tradeoffs in memory organization
- Changing cost of memory organization as we go to on-chip, embedded memories